

Document Title

128K x8 bit Super Low Power and Low Voltage Full CMOS Static RAM

Revision History

<u>Revision No.</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
0.0	Initial draft	March 15, 1996	Advance
0.1	Revise - Erase 100ns from KM68FS1000 Family - Add 150ns for KM68FS1000 Family - Add 32-sTSP1 new package - Add high power version $I_{SB1}=5.0\mu A(\text{Max})$ - Change $V_{DR}(\text{Min})$ 1.0 to 1.5V	July 7, 1996	Preliminary
1.0	Finalize - Concept change high power version to low low power version $I_{SB1}=5.0\mu A(\text{Max})$ - Change super low power version with special handling $I_{SB1}=1.0\mu A(\text{Max})$ - I_{CC} & $I_{CC1}(\text{Read})$ decrease 10 to 5mA	December 1, 1996	Final
2.0	Revise - Change datasheet format - Remove reverse type package from product - Remove reserved speed bin(100ns)	February 26, 1998	Final
3.0	Revise - Add CSP type packaged product. - Improved I_{CC2}	July 29, 1998	Final

The attached datasheets are provided by SAMSUNG Electronics. SAMSUNG Electronics CO., LTD. reserves the right to change the specifications and products. SAMSUNG Electronics will answer to your questions about device. If you have any questions, please contact the SAMSUNG branch offices.

128K x8 bit Super Low Power and Low Voltage Full CMOS Static RAM

FEATURES

- Process Technology : Full CMOS
- Organization : 128K x8 bit
- Power Supply Voltage
 - KM68FV1000 Family : 3.0V ~ 3.6V
 - KM68FS1000 Family : 2.3V ~ 3.3V
 - KM68FR1000 Family : 1.8V ~ 2.7V
- Low Data Retention Voltage : 1.5V(Min)
- Three state output and TTL Compatible
- Package Type : 32-SOP-525, 32-TSOP1-0820F, 32-TSOP1-0813.4F, 48-CSP

GENERAL DESCRIPTION

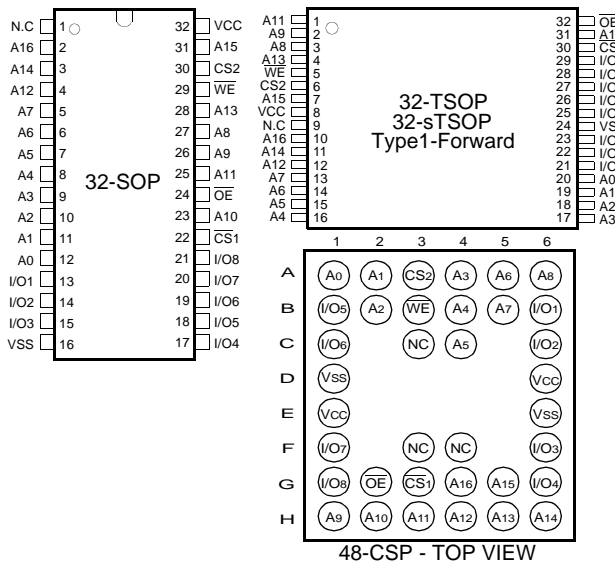
The KM68FV1000, KM68FS1000 and KM68FR1000 families are fabricated by SAMSUNG's advanced Full CMOS process technology. The families support various operating temperature range and have various package types for user flexibility of system design. The families also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

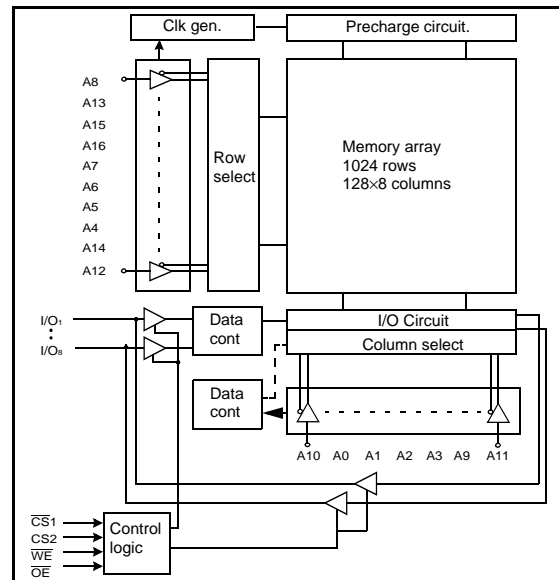
Product Family	Operating Temperature	Vcc Range	Speed(ns)	Power Dissipation		PKG Type
				Standby (I _{SB1} , Max)	Operating (I _{CC2} , Max)	
KM68FV1000	Commercial(0~70°C)	3.0~3.6V	70 ¹⁾ /85@V _{CC} =3.3±0.3V	5μA ²⁾	40mA	32-SOP
KM68FS1000		2.3~3.3V	70 ¹⁾ /85@V _{CC} =3.0±0.3V 120 ¹⁾ /150@V _{CC} =2.5±0.2V		35mA	
KM68FR1000		1.8~2.7V	300 ¹⁾ @V _{CC} =2.0±0.2V		15mA	
KM68FV1000I	Industrial(-40~85°C)	3.0~3.6V	70 ¹⁾ /85@V _{CC} =3.3±0.3V		40mA	32-sTSOP1 Forward
KM68FS1000I		2.3~3.3V	70 ¹⁾ /85/100@V _{CC} =3.0±0.3V 120 ¹⁾ /150@V _{CC} =2.5±0.2V		35mA	
KM68FR1000I		1.8~2.7V	300 ¹⁾ @V _{CC} =2.0±0.2V		15mA	

1. The parameter is measured with 30pF test load.
2. 1μA for super low power version with special handling.

PIN DESCRIPTION



FUNCTIONAL BLOCK DIAGRAM



Name	Function	Name	Function	Name	Function	Name	Function
CS ₁ , CS ₂	Chip Select Input	OE	Output Enable Input	Vcc	Power	I/O ₁ -I/O ₈	Data Inputs/Outputs
N.C.	No Connection	WE	Write Enable Input	Vss	Ground	A ₀ -A ₁₆	Address Inputs

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PRODUCT LIST

Commercial Temperature Products(0~70°C)		Industrial Temperature Products(-40~85°C)	
Part Name	Function	Part Name	Function
KM68FV1000G-7	32-SOP, 70ns, 3.3V	KM68FV1000GI-7	32-SOP, 70ns, 3.3V
KM68FV1000G-8	32-SOP, 85ns, 3.3V	KM68FV1000GI-8	32-SOP, 85ns, 3.3V
KM68FV1000T-7	32-TSOP1 F, 70ns, 3.3V	KM68FV1000TI-7	32-TSOP1 F, 70ns, 3.3V
KM68FV1000T-8	32-TSOP1 F, 85ns, 3.3V	KM68FV1000TI-8	32-TSOP1 F, 85ns, 3.3V
KM68FS1000G-12	32-SOP, 120/70ns, 2.5/3.0V	KM68FS1000GI-12	32-SOP, 120/70ns, 2.5/3.0V
KM68FS1000G-15	32-SOP, 150/85ns, 2.5/3.0V	KM68FS1000GI-15	32-SOP, 150/85ns, 2.5/3.0V
KM68FS1000T-12	32-TSOP1 F, 120/70ns, 2.5/3.0V	KM68FS1000TI-12	32-TSOP1 F, 120/70ns, 2.5/3.0V
KM68FS1000T-15	32-TSOP1 F, 150/85ns, 2.5/3.0V	KM68FS1000TI-15	32-TSOP1 F, 150/85ns, 2.5/3.0V
KM68FS1000TG-12	32-sTSOP1 F, 120/70ns, 2.5/3.0V	KM68FS1000TGI-12	32-sTSOP1 F, 120/70ns, 2.5/3.0V
KM68FS1000TG-15	32-sTSOP1 F, 150/85ns, 2.5/3.0V	KM68FS1000TGI-15	32-sTSOP1 F, 150/85ns, 2.5/3.0V
KM68FR1000G-30	32-SOP, 300ns, 2.0/2.5V	KM68FR1000GI-30	32-SOP, 300ns, 2.0/2.5V
KM68FR1000T-30	32-TSOP1 F, 300ns, 2.0/2.5V	KM68FR1000TI-30	32-TSOP1 F, 300ns, 2.0/2.5V
KM68FR1000TG-30	32-sTSOP1 F, 300ns, 2.0/2.5V	KM68FR1000TGI-30	32-sTSOP1 F, 300ns, 2.0/2.5V
		KM68FR1000ZI-30	48-CSP, 300ns, 2.0/2.5V

FUNCTIONAL DESCRIPTION

CS ₁	CS ₂	OE	WE	I/O	Mode	Power
H	X ¹⁾	X ¹⁾	X ¹⁾	High-Z	Deselected	Standby
X ¹⁾	L	X ¹⁾	X ¹⁾	High-Z	Deselected	Standby
L	H	H	H	High-Z	Output Disabled	Active
L	H	L	H	Dout	Read	Active
L	H	X ¹⁾	L	Din	Write	Active

1. X means don't care. (Must be high or low states)

ABSOLUTE MAXIMUM RATINGS¹⁾

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to V _{SS}	V _{IN} , V _{OUT}	-0.2 to 3.6V ²⁾	V	-
Voltage on V _{CC} supply relative to V _{SS}	V _{CC}	-0.2 to 4.0V ³⁾	V	-
Power Dissipation	P _D	1.0	W	-
Storage temperature	T _{STG}	-55 to 150	°C	-
Operating Temperature	T _A	0 to 70	°C	KM68FV1000, KM68FS1000, KM68FR1000
		-40 to 85	°C	KM68FV1000I, KM68FS1000I, KM68FR1000I
Soldering temperature and time	T _{SOLDER}	260°C, 5sec (Lead Only)	-	-

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. V_{IN}/V_{OUT}=-0.2 to 3.9V for KM68FV1000 Family.

3. Maximum V_{CC}=-0.2 to 4.6V for KM68FV1000 Family.

RECOMMENDED DC OPERATING CONDITIONS¹⁾

Item	Symbol	Product	Min	Typ	Max	Unit	
Supply voltage	V _{CC}	KM68FV1000 Family	3.0	3.3	3.6	V	
		KM68FS1000 Family	2.3	2.5/3.0	3.3		
		KM68FR1000 Family	1.8	2.0/2.5	2.7		
Ground	V _{SS}	All Family	0	0	0	V	
Input high voltage	V _{IH}	KM68FV1000 Family	V _{CC} =3.3±0.3V	2.2	-	V _{CC} +0.2 ²⁾	V
		KM68FS1000 Family	V _{CC} =3.0±0.3V	2.2			
			V _{CC} =2.5±0.2V	2.0			
		KM68FR1000 Family	V _{CC} =2.5±0.2V	2.0			
V _{CC} =2.0±0.2V	1.6						
Input low voltage	V _{IL}	All Family	-0.2 ³⁾	-	0.4	V	

Note

- Commercial Product : T_A=0 to 70°C, unless otherwise specified
Industrial Product : T_A=-40 to 85°C, unless otherwise specified
- Overshoot : V_{CC} + 1.0V in case of pulse width ≤20ns
- Undershoot : -1.0V in case of pulse width ≤20ns
- Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE¹⁾ (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C _{IN}	V _{IN} =0V	-	8	pF
Input/Output capacitance	C _{IO}	V _{IO} =0V	-	10	pF

- Capacitance is sampled, not 100% tested

DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions	Min	Typ	Max	Unit			
Input leakage current	I _{LI}	V _{IN} =V _{SS} to V _{CC}	-1	-	1	μA			
Output leakage current	I _{LO}	$\overline{CS}_1=V_{IH}$ or $CS_2=V_{IL}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$, V _{IO} =V _{SS} to V _{CC}	-1	-	1	μA			
Operating power supply current	I _{CC}	I _{IO} =0mA, $\overline{CS}_1=V_{IL}$, CS ₂ =V _{IH} , V _{IN} =V _{IL} or V _{IH} , Read	-	-	2	mA			
Average operating current	I _{CC1}	Cycle time=1μs, 100% duty, I _{IO} =0mA, $\overline{CS}_1 \leq 0.2V$, CS ₂ ≥V _{CC} -0.2V, V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	Read	-	-	3	mA		
			Write	-	10	15			
	I _{CC2}	Cycle time=Min, 100% duty, I _{IO} =0mA, $\overline{CS}_1=V_{IL}$, CS ₂ =V _{IH} , V _{IN} =V _{IL} or V _{IH}	V _{CC} =3.3V @ 70ns	-	-	35 ¹⁾	mA		
			V _{CC} =2.7V @ 120ns	-	-	30			
V _{CC} =2.2V @ 300ns	-	-	15						
Output low voltage	V _{OL}	I _{OL}	2.1mA at V _{CC} =3.0/3.3V 0.5mA at V _{CC} =2.5V 0.33mA at V _{CC} =2.0V			-	-	0.4	V
Output high voltage	V _{OH}	I _{OH}	-1.0mA at V _{CC} =3.0/3.3V			2.4	-	-	V
			-0.5mA at V _{CC} =2.5V			2.0	-	-	
			-0.44mA at V _{CC} =2.0V			1.6	-	-	
Standby Current(TTL)	I _{SB}	$\overline{CS}_1=V_{IH}$ or CS ₂ =V _{IL} , Other inputs=V _{IL} or V _{IH}	-	-	0.3	mA			
Standby Current(CMOS)	I _{SB1}	$\overline{CS}_1 \geq V_{CC}-0.2V$, CS ₂ ≥V _{CC} -0.2V or CS ₂ ≤0.2V, Other inputs=0-V _{CC}	-	-	5 ¹⁾	μA			

- KM68FV1000 Family = 40mA
- Super low power product = 1μA with special handling.

AC OPERATING CONDITIONS

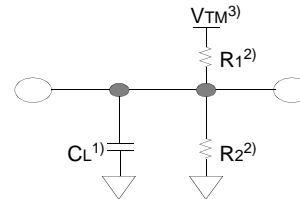
TEST CONDITIONS (Test Load and Test Input/Output Reference)

Input pulse level : 0.4 to 2.2V for Vcc=3.3V, 3.0V, 2.5V
0.4 to 1.8V for Vcc=2.0V

Input rising and falling time : 5ns

Input and output reference voltage : 1.5V for Vcc=3.3V, 3.0V
1.1V for Vcc=2.5V
0.9V for Vcc=2.0V

Output load (See right) : CL=100pF+1TTL
CL=30pF+1TTL



1. Including scope and jig capacitance
2. R1=3070Ω, R2=3150Ω
3. VTM=2.8V for Vcc=3.0/3.3V
2.3V for Vcc=2.5V
1.8V for Vcc=2.0V

AC CHARACTERISTICS

(Commercial product : TA=0 to 70°C, Industrial product : TA=-40 to 85°C
KM68FV1000 Family : Vcc=3.0~3.6V, KM68FS1000 Family : Vcc=2.3~3.3V,
KM68FR1000 Family : Vcc=1.8~2.7V)

Parameter List		Symbol	Speed Bins												Units
			70ns		85ns		100ns		120ns		150ns		300ns		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read	Read cycle time	tRC	70	-	85	-	100	-	120	-	150	-	300	-	ns
	Address access time	tAA	-	70	-	85	-	100	-	120	-	150	-	300	ns
	Chip select to output	tCO1, tCO2	-	70	-	85	-	100	-	120	-	150	-	300	ns
	Output enable to valid output	tOE	-	35	-	45	-	50	-	60	-	75	-	150	ns
	Chip select to low-Z output	tLZ1, tLZ2	10	-	10	-	10	-	10	-	20	-	50	-	ns
	Output enable to low-Z output	tOLZ	5	-	5	-	5	-	5	-	10	-	30	-	ns
	Chip disable to high-Z output	tHZ1, tHZ2	0	25	0	25	0	30	0	35	0	40	0	60	ns
	Output disable to high-Z output	tOHZ	0	25	0	25	0	30	0	35	0	40	0	60	ns
	Output hold from address change	tOH	10	-	15	-	15	-	15	-	15	-	30	-	ns
Write	Write cycle time	tWC	70	-	85	-	100	-	120	-	150	-	300	-	ns
	Chip select to end of write	tCW	65	-	70	-	80	-	100	-	120	-	300	-	ns
	Address set-up time	tAS	0	-	0	-	0	-	0	-	0	-	0	-	ns
	Address valid to end of write	tAW	65	-	70	-	80	-	100	-	120	-	300	-	ns
	Write pulse width	tWP	55	-	60	-	70	-	80	-	100	-	200	-	ns
	Write recovery time	tWR	0	-	0	-	0	-	0	-	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	25	0	25	0	30	0	35	0	40	0	60	ns
	Data to write time overlap	tDW	30	-	35	-	40	-	50	-	60	-	120	-	ns
	Data hold from write time	tDH	0	-	0	-	0	-	0	-	0	-	0	-	ns
End write to output low-Z	tOW	5	-	5	-	5	-	5	-	5	-	20	-	ns	

DATA RETENTION CHARACTERISTICS

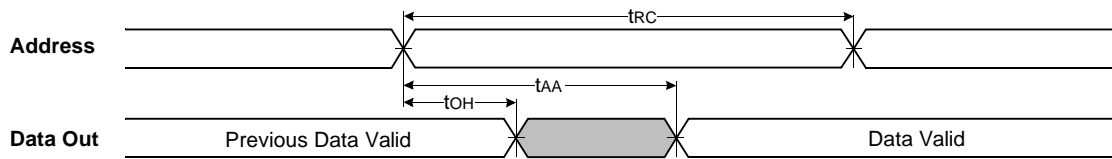
Item	Symbol	Test Condition	Min	Typ	Max	Unit
Vcc for data retention	VDR	$\overline{CS}_1 \geq V_{cc} - 0.2V^{(1)}$	1.5	-	3.6	V
Data retention current	IDR	Vcc=3.0V, $\overline{CS}_1 \geq V_{cc} - 0.2V^{(1)}$	-	-	5.0 ⁽²⁾	μA
Data retention set-up time	tSDR	See data retention waveform	0	-	-	ns
Recovery time	tRDR		tRC	-	-	

1. $\overline{CS}_1 \geq V_{cc} - 0.2V$, $\overline{CS}_2 \geq V_{cc} - 0.2V$ (\overline{CS}_1 controlled) or $\overline{CS}_2 \leq 0.2V$ (\overline{CS}_2 controlled)

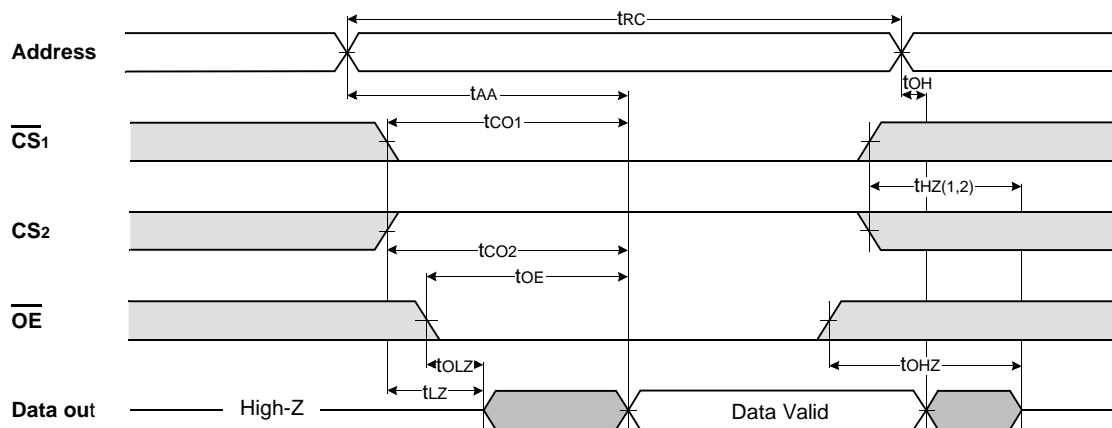
2. Super low power product = 1μA with special handling.

TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS1}=\overline{OE}=V_{IL}$, $\overline{WE}=V_{IH}$)



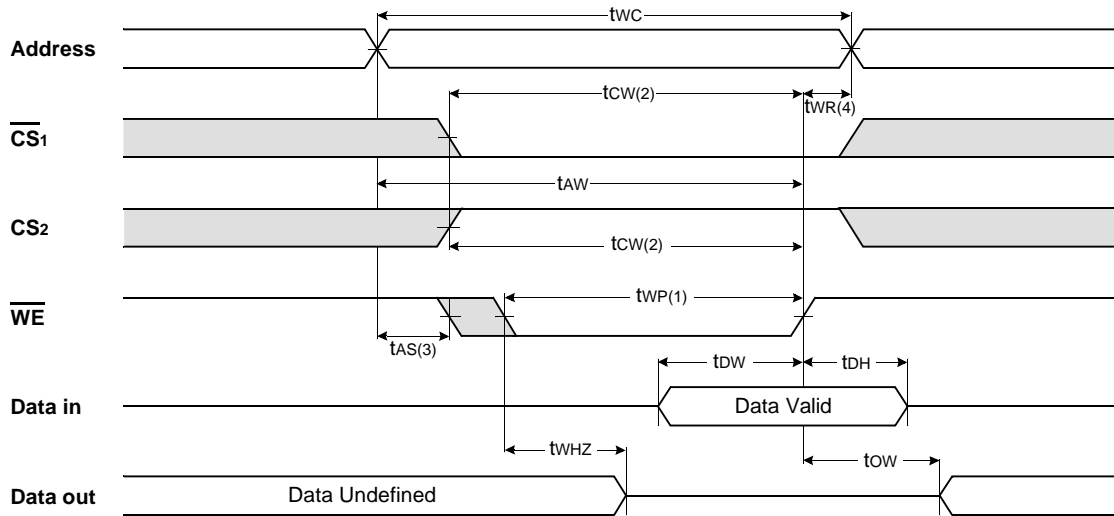
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}=V_{IH}$)



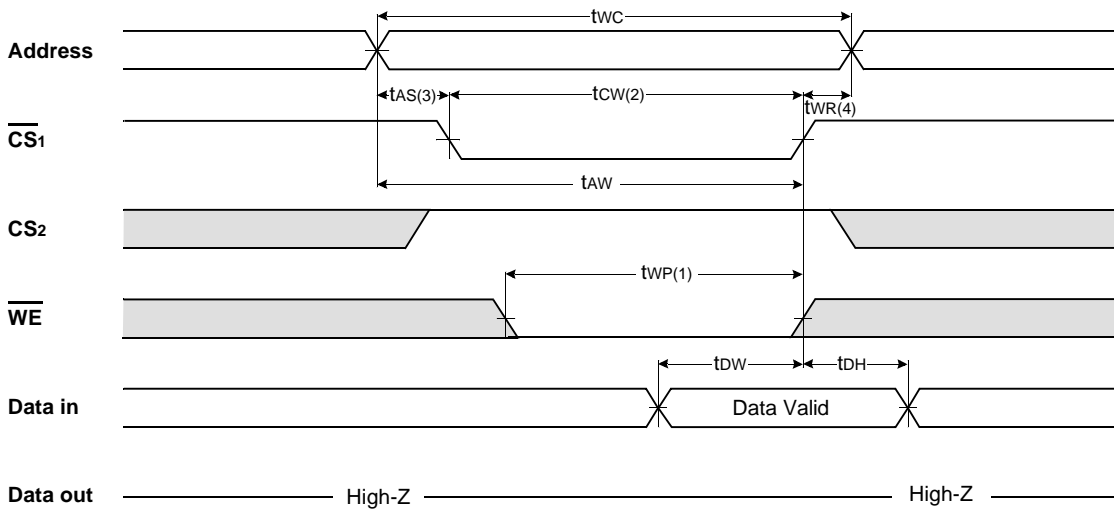
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device interconnection.

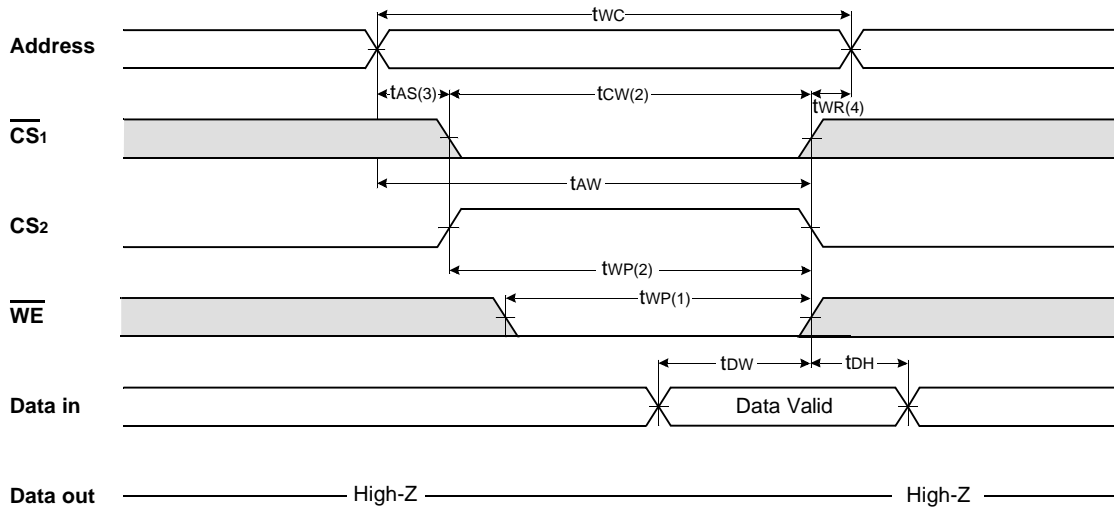
TIMING WAVEFORM OF WRITE CYCLE(1) (\overline{WE} Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS1}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) (\overline{CS}_1 Controlled)

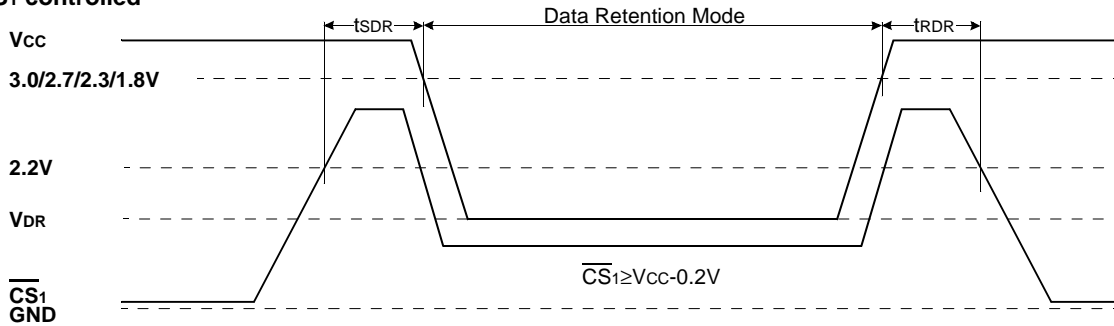


NOTES (WRITE CYCLE)

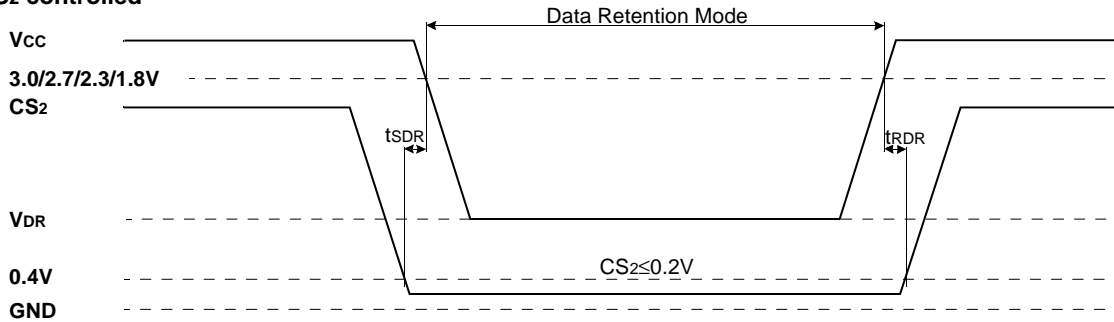
1. A write occurs during the overlap of a low \overline{CS}_1 , a high CS_2 and a low \overline{WE} . A write begins at the latest transition among \overline{CS}_1 goes low, CS_2 going high and \overline{WE} going low: A write ends at the earliest transition among \overline{CS}_1 going high, CS_2 going low and \overline{WE} going high, t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the \overline{CS}_1 going low or CS_2 going high to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. $t_{WR(1)}$ applied in case a write ends as \overline{CS}_1 or \overline{WE} going high $t_{WR(2)}$ applied in case a write ends as CS_2 going to low.

DATA RETENTION WAVE FORM

\overline{CS}_1 controlled



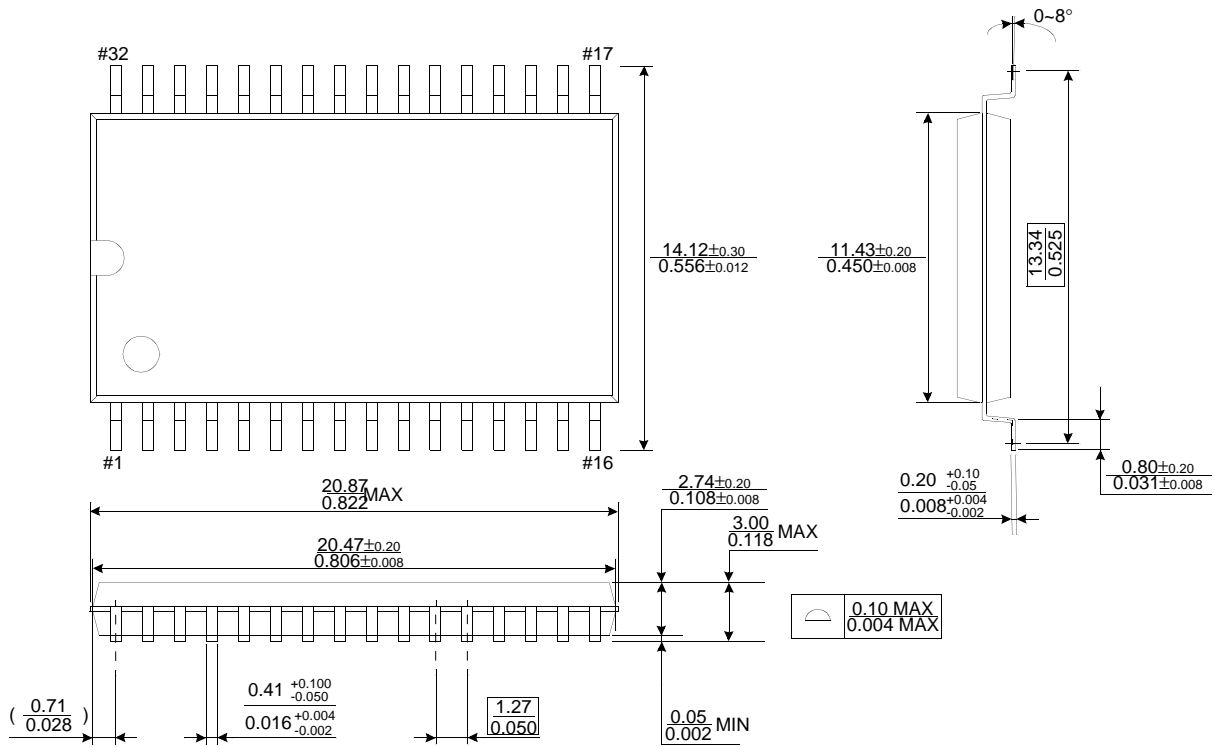
CS_2 controlled



PACKAGE DIMENSIONS

Units: millimeter(inch)

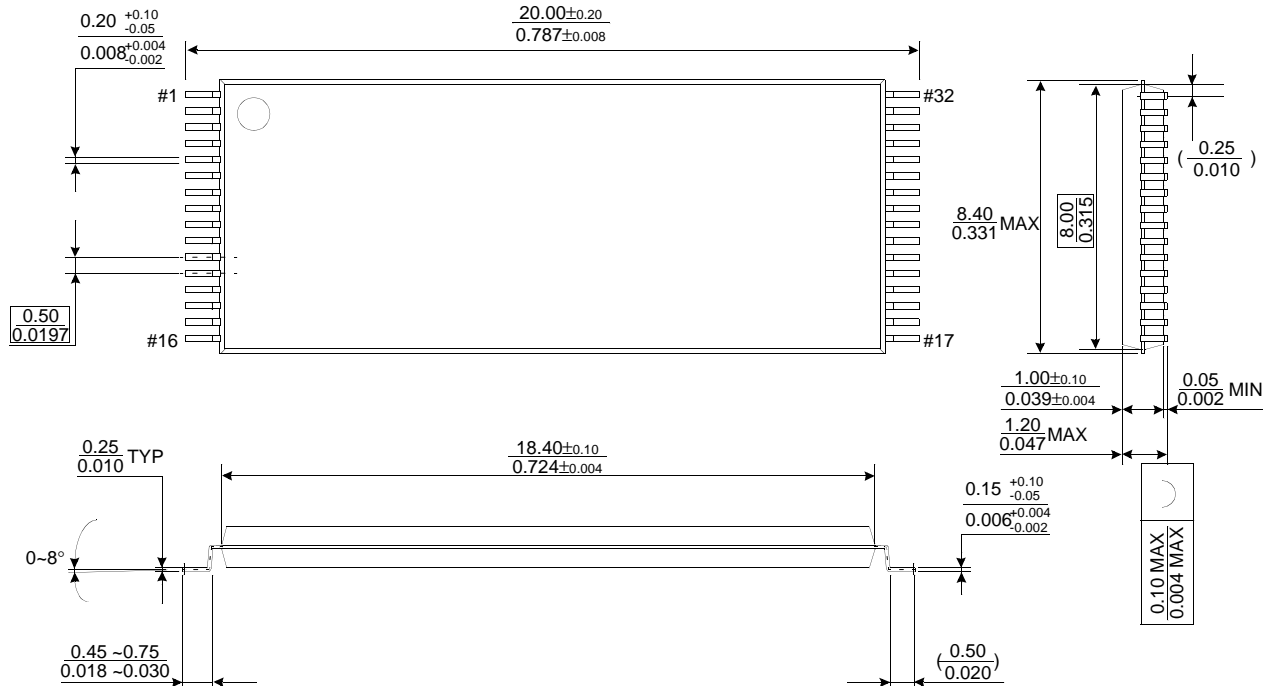
32 PLASTIC SMALL OUTLINE PACKAGE (525mil)



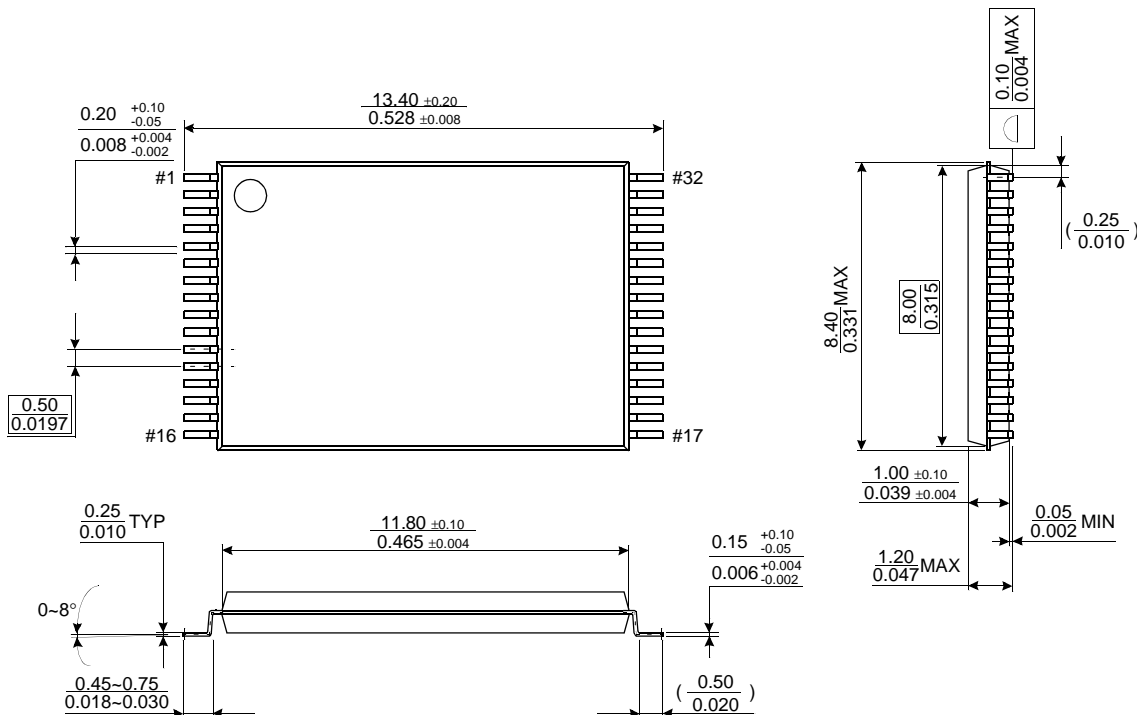
PACKAGE DIMENSIONS

Units: millimeter(inch)

32 PIN THIN SMALL OUTLINE PACKAGE TYPE I (0820F)



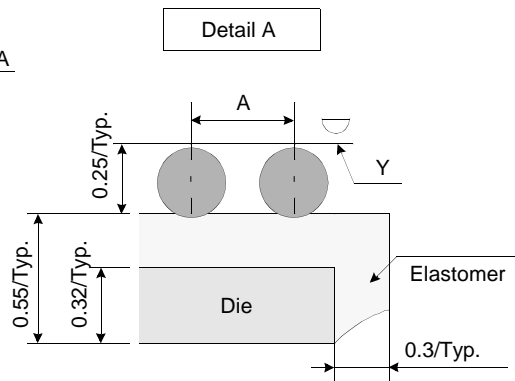
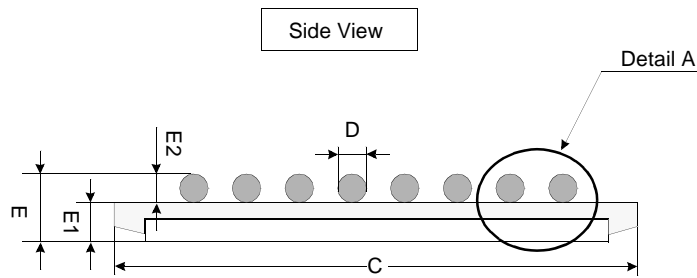
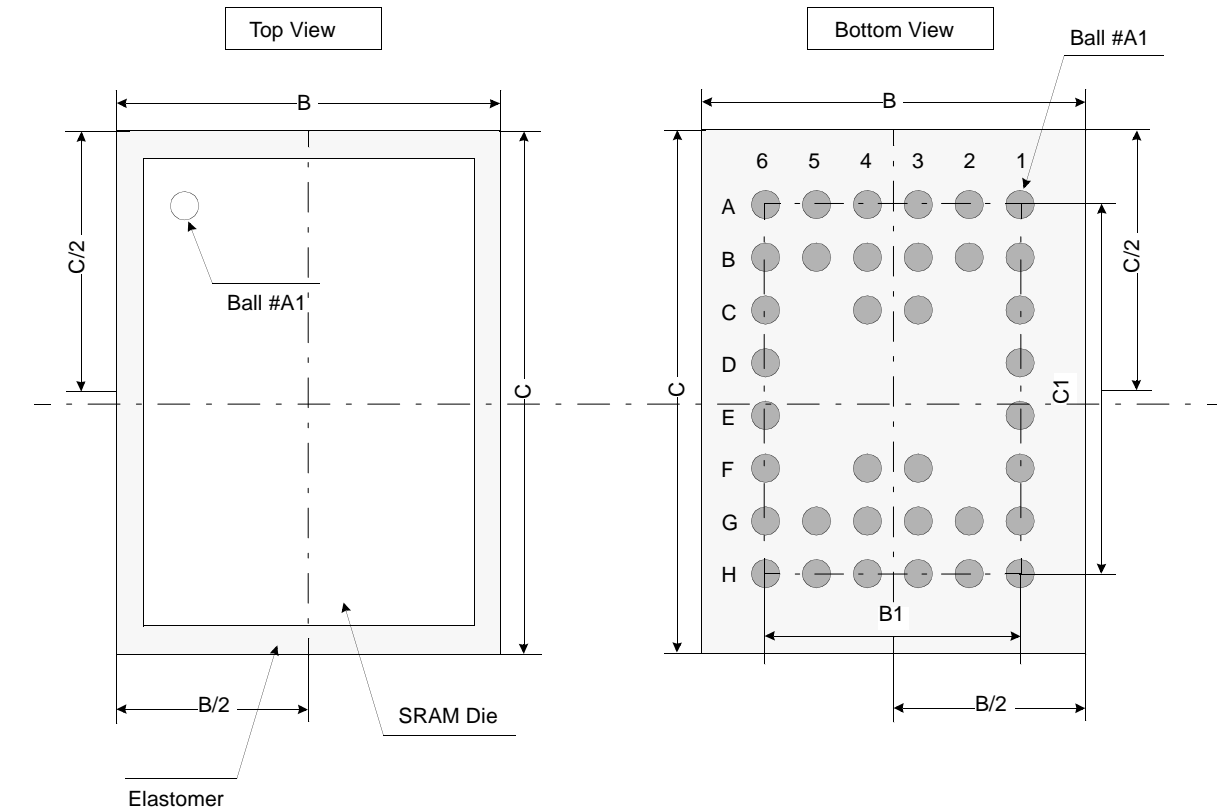
32 PIN THIN SMALL OUTLINE PACKAGE TYPE I (0813.4F)



PACKAGE DIMENSIONS

Units: millimeter(inch)

32 PIN THIN SMALL OUTLINE PACKAGE TYPE I (0820F)



	Min	Typ	Max
A	-	0.75	-
B	5.90	6.00	6.10
B1	-	3.75	-
C	7.90	8.00	8.10
C1	-	5.25	-
D	0.30	0.35	0.40
E	-	0.80	0.81
E1	-	0.55	-
E2	-	0.25	-
Y	-	-	0.08

- Notes.**
1. Bump counts : 48(8row x 6column)
 2. Bump pitch : (x,y)=(0.75 x 0.75)(typ.)
 3. All tolerance are +/-0.050 unless otherwise specified.
 4. Typ : Typical
 5. Y is coplanarity: 0.08(Max)