Digitally Programmable Delay Lines

SERIES: PDU-2600 (DIP)
PDU-2600S (SMD)

High Accuracy¹ Frequency Compensated¹ ¹See Application Notes 1 & 2

Test Conditions (for F_{ϕ} , $F_1 = \text{Logic } \phi$)



Features:

- Guaranteed delay increments throughout range.
- Guaranteed programmed delay throughout range.
- Up to 3 separate frequencies compensated (customer specified).
- 6-Bit programmable delay.
- Fast-TTL interfaced.
- 40 pins DIP & SMD package.

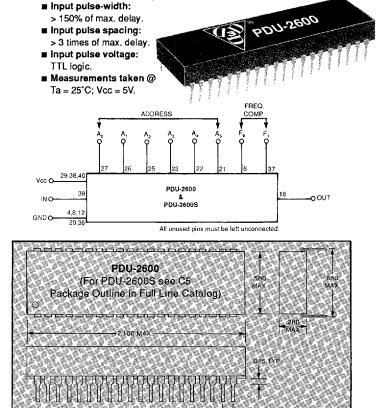
Specifications:

- Delay variation: Monotonic
- Programmed delay tolerance: See Table 1.
- Increment delay tolerance: See Table 1.
- Propagation delay:
 - Address to output $(T_{SUA}) = 7$ ns typ.
- Supply voltage: 5 Vdc ± 5%.
- Supply current:

ICCH = 65 ma.ICCL = 128 ma.

- Operating temperature: 0-70°C (-55° to +125°C on request).
- Temperature coefficient: 100 PPM/*C.
- DC parameter: See TTL-Fast Schottky Logic Table on Page 6.
- Minimum input pulse-width: 10% of total delay.

TABLE 1



P/N DIP	Delay Increments (ns)	Total Programmed Delay (ns)	Operating Frequency (F _p , F ₁ = Logic ¢)	Customer Specified Max. Frequency
PDU-26005	.5±-4	315± 5	DC △10 MHZ	50 MHZ
PDU-2600-1	1 ± .4	63 ± .5	DC 5 MHZ	40 MHZ
PDU-2600-2	2 ± 5	126 ± .5	DC- 2.5 MHZ	35 MHZ
PDU-2600-3	3 ±1	189 ±1	DO - 1.7 MHZ	25 MHZ
PDU-2600-4	4.11	252 ±1	DC - 1.2 MHZ	20 MHZ
PDU-2600-5	5.4	315 ±2	DC - 1.0 MHZ	15 MHZ
PDU-2600-6	6 ±1.5	378 ±2	DC88 MHZ	13 MHZ
PDU-2600-7	7 ±15	441 ±2	DC75 MHZ	11 MHZ
PDU-2600-8	8 ±2	504 ±2	DC70 MHZ	10 MHZ
PDU-2600-9	9 ±3	567 ±3	DG = 1.58 MHZ	9 MHZ
PDU-2600-10	10 ±3	630 ±3	DC - 1.53 MHZ	8 MHZ

- A. Any frequency between "Customer Specified Max. Frequency" & "Operating Frequency" can be programmed with compensation to guarantee the delay tolerances. A maximum of 3 separate frequencies can be programmed in each unit.
- B. Other increments available. Contact Engineering.
- C. Customer programmed frequencies can be specified by completing the P/N as follows:

PDU-2600(S)	_xxxx_	Z XXXX	
SERIES	STEP DELAY	HOUSE ASSIGNED	
		PER TABLE 2	

TABLE 2

Customer Specified Frequency	Logic F _{\$}	Level F ₁
[1 [2 [3	0	1 0 1

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