

# SIEMENS



## ICs for Consumer Electronics

COMPACTTEXT

SDA 5273-3C

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	29	New command Previous Page
5 Appl. Notes	59	Value of column 0 has been changed
25	34	New input parameter TWIST2(4:0) and TWIST2C(14:12)
	54	New dataport for binary access via I <sup>2</sup> C Bus. <sup>1)</sup>
24	39	New input parameter bit P26_C8.
25	39	New input parameter WSS_CNT(7:0).
25	39	New input parameter NU_VALID_HEADER(7:0).
	63	Language support for thai.
	49 - 52	Text detection and WSS reception improvement (refer chapters 1.8 and 1.9).
	52 - 53	Additional information about the CVBS signal quality.
	53	Firmware refresh for the external DRAM up to 16 Mbit.
4 Appl. Notes	57	Bits 47...40 must be defined new
		The layout of the document has been completely updated.

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<b>Table of Contents</b>		<b>Page</b>
<b>1</b>	<b>Delta Specification</b> .....	<b>7</b>
1.1	General Information .....	7
1.1.1	Page Request Priority Table .....	8
1.1.2	Memory Configuration .....	9
1.1.3	Additional Features in COMPACTTEXT compared to MEGATEXT® .....	10
1.2	Differences to the MEGATEXT® Volume 1 Documentation .....	10
1.2.1	General Differences .....	10
1.2.2	Firmware Overview .....	10
1.2.3	ACQ Reference .....	10
1.2.4	Command Interface .....	10
1.2.5	M3L-Bus Register .....	11
1.3	Command Directory .....	13
1.3.1	How to Use an MCI Command .....	13
1.3.2	Command Handshake .....	13
1.3.3	Error Code .....	14
1.3.4	MCI Command Table .....	14
1.3.5	Command Description .....	16
1.3.5.1	Call Subroutine (No. 34) .....	16
1.3.5.2	Clock (No. 12) .....	16
1.3.5.3	Cursor Down (No. 19) .....	16
1.3.5.4	Cursor Up (No. 18) .....	17
1.3.5.5	Cyan (No. 17) .....	17
1.3.5.6	Digit 0 (No. 23) .....	18
1.3.5.7	Digit 1 (No. 24) .....	18
1.3.5.8	Digit 2 (No. 25) .....	18
1.3.5.9	Digit 3 (No. 26) .....	18
1.3.5.10	Digit 4 (No. 27) .....	18
1.3.5.11	Digit 5 (No. 28) .....	18
1.3.5.12	Digit 6 (No. 29) .....	18
1.3.5.13	Digit 7 (No. 30) .....	19
1.3.5.14	Digit 8 (No. 31) .....	19
1.3.5.15	Digit 9 (No. 32) .....	19
1.3.5.16	Green (No. 15) .....	19
1.3.5.17	Hold (No. 10) .....	19
1.3.5.18	Index Page (No. 07) .....	20
1.3.5.19	Inhibit Update S/P-C (No. 35) .....	20
1.3.5.20	Last Seen Page (No. 38) .....	22
1.3.5.21	List Mode (No. 06) .....	22
1.3.5.22	List Page (No. 13) .....	23
1.3.5.23	Mix Mode (No. 04) .....	24
1.3.5.24	Move Memory Seg (No. 33) .....	25
1.3.5.25	Next Page (No. 01) .....	28

<b>Table of Contents</b>		<b>Page</b>
1.3.5.26	Page Catching Off (No. 36) .....	28
1.3.5.27	Picture Mode (No. 02) .....	28
1.3.5.28	Previous Page (No. 05) .....	29
1.3.5.29	Red (No. 14) .....	29
1.3.5.30	Reset Acq (No. 00) .....	29
1.3.5.31	Reset Intq (No. 20) .....	30
1.3.5.32	Reveal (No. 11) .....	30
1.3.5.33	Search Page (No. 37) .....	30
1.3.5.34	Size (No. 09) .....	31
1.3.5.35	Size Off (No. 21) .....	31
1.3.5.36	Start New Request (No. 39) .....	32
1.3.5.37	Store OK (No. 22) .....	32
1.3.5.38	Subpage Mode (No. 08) .....	32
1.3.5.39	Text Mode (No. 03) .....	33
1.3.5.40	Yellow (No. 16) .....	33
1.4	Setup Parameters .....	34
1.5	User Defined Characters (UDC) .....	40
1.6	Return Parameters .....	41
1.7	Description of the Stored Data Formats .....	45
1.7.1	Stored Format of 1-Byte Hamming Protected Data .....	45
1.7.2	Stored Format of Page .....	45
1.7.3	Stored Format of Packet 8/30 (000x) Format 1 .....	46
1.7.4	Stored Format of Packet 8/30 (001x) Format 2 (PDC) .....	47
1.7.5	Format of TOP Title .....	48
1.7.6	Format of Stored BTT .....	48
1.8	Wide Screen Signaling (WSS), Video Program System (VPS) .....	49
1.8.1	Wide Screen Signaling (WSS) .....	49
1.8.2	Video Program System (VPS) .....	50
1.9	Teletext Identification .....	51
1.9.1	Teletext Identification in Line 16 .....	51
1.10	Signal Quality Status Bits .....	52
1.11	Firmware Refresh for the External DRAM .....	53
1.12	Binary Address Port .....	54
<b>2</b>	<b>Application Notes</b> .....	<b>55</b>
2.1	Version Code Overview .....	55
2.2	Example for COMPACTTEXT Initialization .....	56
2.3	How to Initialize COMPACTTEXT for Russian Market .....	61
2.4	How to Initialize COMPACTTEXT for Thai Language .....	63
2.5	Pages to be Requested .....	64
2.6	Digit Input .....	65
<b>3</b>	<b>Abbreviations</b> .....	<b>66</b>

---

Table of Contents	Page
4      References .....	67

## 1 Delta Specification

### 1.1 General Information

The **SDA 5273-3C** is a powerful one-chip videotext decoder with all the display features of his “big brother” SDA 5273 but with a very simple command interface for reduced external software.

The whole documentation of the **MEGATEXT® SDA 5273** is also valid for **COMPACTTEXT SDA 5273-3C** except for the differences which are described in **chapter 1.2 “Differences to the MEGATEXT® Volume 1 Documentation” on page 10.**

After power-on of the system, the setup parameters for CTX must be initialized by the external controller. These setup parameters are read every time when necessary by the **SDA 5273-3C**. The complete page management is done on chip. TOP and FLOF detection is done automatically, as well as the acquisition of packet 8/30/1, 8/30/2 or VPS and WSS data. The initial teletext page is taken from packet 8/30 (if present) or from the setup parameter or from the 5th FLOF link (if present).

The user has several choices to enter a page request. One way is entering a page number for a new display page with the “DIGIT” commands. It is also possible to enter a page request by a “page catching” or with the colour keys RED, GREEN, YELLOW, and CYAN. These keys have different meanings depending on the current request mode (simple, TOP, FLOF). In all cases only the new display page has to be entered and all following page requests are automatically done by the firmware depending on the current mode.

Some additional status information is also available (i.e. TOP, FLOF, page found...) for generating individual messages like “page xxx not broadcasted” by the external controller (return parameter).

For page acquisition a maximum of 10 pages (+ 2 chapters for x/26) is available. After reset, the **SDA 5273-3C** is in the “simple mode”, that means the initial page (page 100) and the following 9 pages are requested. The processor will start with the picture mode. **SDA 5273-3C** automatically changes to the page trace mode as soon as the page trace is stable.

The user has the possibility to block up to 4 of the 10 available pages (with the list page command) for so-called favourite or list pages. These pages are favourite page numbers of the user, programmed for each program individually, and stored for example in the NVM of the TV. These pages can not be removed by the automatic TOP or FLOF requests. In the list mode, a special menu in row 24 can be generated for easy page selection by use of the remote control’s colour keys.

In TOP mode, the BTT and a given number of AITs are immediately requested. Then the memory is filled with the next block page, group page and so on (see below). A standard





### 1.1.2 Memory Configuration

The following table shows the internal memory allocation of the **SDA 5273-3C**.

In all memory configurations, up to 10 pages are available for page acquisition. If block 1 is used for graphics or block 3 for outer screen display, byte 4 and byte 3 of block 2 can be used for page acquisition.

**Table 2**

	Byte 5	Byte 4	Byte 3	Byte 2	Byte 1	Byte 0
Block 0	Reserved for PU work space + DRCS definition + Packet 8/30/1 + Packet 8/30/2 + VPS + WSS					
Block 1	BTT + X/26 -Memory	ACQ (Chapter 4)	ACQ (Chapter 3)	ACQ (Chapter 2)	ACQ (Chapter 1)	ACQ (Chapter 0)
Block 2	Packet- Buffer + page trace	DISPLAY or ACQ	DISPLAY or ACQ	DISPLAY	DISPLAY	DISPLAY
Block 3	Inhibit- Update- Table + X/26 -Memory	ACQ (Chapter 9)	ACQ (Chapter 8)	ACQ (Chapter 7)	ACQ (Chapter 6)	ACQ (Chapter 5)

Related register: **Memory Allocation Register IAT(2:0)**, refer to **chapter 1.2.5**

### 1.1.3 Additional Features in COMPACTTEXT compared to MEGATEXT®

- Multiple window function for OSD in TV/TXT-mode
- Twist mode
- Non-latin based language support (cyrillic, arabic, greek, hebrew)
- Simple command interface to the external controller
- List mode (user pages)
- More internal page memory (up to 10 pages)
- Page catching
- Automatic detection and processing of text in Line 16
- Automatic detection and storing of VPS in line 16
- Reception and decoding of Wide Screen Signaling (WSS) in Line 23
- Reception and decoding of Video Program Service (VPS) in line 16
- Reception and decoding of Program Delivery Control (PDC) data via packet 8/30
- TOP and FLOF support

## 1.2 Differences to the MEGATEXT® Volume 1 Documentation

### 1.2.1 General Differences

The firmware initializes the display mask register OSMR, ISMR0, ISMR1, BOXMR0 and BOXMR1 to 00 00 00 00 00 00<sub>H</sub>. Therefore, the display generator uses all 6 attribute bytes of the character display words in block 2 and 3.

To prevent the interpretation of byte position 5 attributes of a character display word, the user software has to initialize the above mentioned display mask registers to FF 00 00 00 00 00<sub>H</sub> and the related control registers OSDW, ISDW0, ISDW1, BOXDW0 and BOXDW1 must be 00 xx xx xx xx xx<sub>H</sub> (xx means customer-specific values that depend on the application).

An example for **COMPACTTEXT** initialization is given in this document. Refer to **chapter 2.2 “Example for COMPACTTEXT Initialization” on page 56.**

### 1.2.2 Firmware Overview

This respective part of the MTX document is completely replaced by this document, the **COMPACTTEXT Delta Specification.**

### 1.2.3 ACQ Reference

This respective part of the MTX document is completely replaced by this document, the **COMPACTTEXT Delta Specification** and **Application Notes for COMPACTTEXT.**

### 1.2.4 Command Interface

This respective part of the MTX document is completely replaced by the **COMPACTTEXT** command interface description which is part of **COMPACTTEXT Delta Specification.**

## 1.2.5 M3L-Bus Register

The registers R 2 - R 5 have to be initialized as follows:

### R2 / PB\_LENGTH

0	0	0	1	0	0	0	1
---	---	---	---	---	---	---	---

### R3 / PB\_ADR\_2

0	1	0	1	1	0	0	0
---	---	---	---	---	---	---	---

### R4 / PB\_ADR\_1

0	0	0	1	0	0	1	0
---	---	---	---	---	---	---	---

### R5 / PB\_ADR\_0

0	0	0	0	0	0	0	0
---	---	---	---	---	---	---	---

The following registers are not defined in **COMPACTTEXT**:

- FREE CHAP CHAIN control register** : R40, R41, R42, R43, R44, R45
- FREE P80 CHAIN control register** : R64, R65, R66, R67, R68, R69
- FREE P40 CHAIN control register** : R72, R73, R74, R75, R76, R77
- MEMORY ALLOCATION register** : R91, R92, R93
- ACQUISITION control register** : R105, R106
- TOP COM BAS register** : R120, R121, R122
- PAGE TRACE register** : R123, R124, R125

**Delta Specification**

The following register group (Memory Allocation Register IAT\_2-IAT0) has a different meaning in **COMPACTTEXT** than in **MEGATEXT**<sup>®</sup>. Be careful not to copy the respective MTX code.

**R88 / IAT\_2**

0	blk3_by4	blk3_by3	blk3_by2	blk3_by1	blk3_by0	0	blk2_by4
---	----------	----------	----------	----------	----------	---	----------

**R89 / IAT\_1**

blk2_by3	0	0	0	0	blk1_by4	blk1_by3	blk1_by2
----------	---	---	---	---	----------	----------	----------

**R90 / IAT\_0**

blk1_by1	blk1_by0	0	0	0	0	0	0
----------	----------	---	---	---	---	---	---

Each bit of the memory allocation register IAT(2:0) enables 1Kbyte of the internal memory for page acquisition.

- 1: Chapter is enabled for page acquisition
- 0: Chapter is disabled for page acquisition

**1.3 Command Directory**

This chapter contains a list of commands from the **COMPACTTEXT** command interface MCI in alphabetical order. The documentation for each command contains a statement about the command’s purpose, a description of its input parameters with used parameter registers, and a description of its return values with used parameter registers. The documentation contains additional important comments for some functions that a designer needs in order to properly use the command.

**1.3.1 How to Use an MCI Command**

Set all MCI input parameters as described.

Set the CMD RUN bit in MCI input parameter register “MCI3\_1” bit position MCI3\_1\_0 to activate MCI handshake.

Transmit the MCI command to subaddress MCI COMMAND (see **MEGATEXT**® documentation volume 1, chapter “M3L-Bus Registers Programmers Reference”).

As long as the MCI command is in execution, the CMD RUN bit will be in the 1 condition.

Use a polling technique to detect whether the CMD RUN bit has changed into the 0 condition.

If the CMD RUN bit is in the 0 condition, the MCI is ready to receive a new command.

Always evaluate the return parameters, especially the error code.

**1.3.2 Command Handshake**

An MCI command can be given only if the previous command is finished. The CMD RUN bit shows the command status. As long as it is in the 1 condition, a command is in execution. The external controller must check this bit before giving a new command. The user is responsible for setting the CMD RUN bit before giving the MCI command. The CMD RUN bit is reset to 0 by the internal firmware after the command is executed.

**MCI3\_1 / COMMAND STATUS**

0	0	0	0	0	0	0	CMD_RUN
---	---	---	---	---	---	---	---------

**CMD\_RUN:** MCI command running flag  
 1: MCI command is in execution.  
 0: MCI command is finished.

### 1.3.3 Error Code

Some commands return an error code to acknowledge the command result. It looks as follows:

#### MCI3\_2 / ERROR CODE

ERR_7	ERR_6	ERR_5	ERR_4	ERR_3	ERR_2	ERR_1	ERR_0
-------	-------	-------	-------	-------	-------	-------	-------

**ERR(7:0)** Error-code bits are explained in the command description. Unless stated otherwise, MCI3\_2 is used for the error-code register.

### 1.3.4 MCI Command Table

The following table shows the command name/command number assignment:

**Table 3**

Command Name	Command Number (Decimal)
CALL SUBROUTINE	34
CLOCK	12
CURSOR DOWN	19
CURSOR UP	18
CYAN	17
DIGIT 0	23
DIGIT 1	24
DIGIT 2	25
DIGIT 3	26
DIGIT 4	27
DIGIT 5	28
DIGIT 6	29
DIGIT 7	30
DIGIT 8	31
DIGIT 9	32
GREEN	15
HOLD	10
INDEX PAGE	07
INHIBIT UPDATE S/P-C	35
LAST SEEN PAGE	38

## Delta Specification

**Table 3 (cont'd)**

<b>Command Name</b>	<b>Command Number (Decimal)</b>
LIST MODE	06
LIST PAGE	13
MIX MODE	04
MOVE MEMORY SEGMENT	33
NEXT PAGE	01
PAGE CATCHING OFF	36
PICTURE MODE	02
PREVIOUS PAGE	05
RED	14
RESET ACQ	00
RESET INTQ	20
REVEAL	11
SEARCH PAGE	37
SIZE	09
SIZE OFF	21
START NEW REQUEST	39
STORE OK	22
SUBPAGE MODE	08
TEXT MODE	03
YELLOW	16

## 1.3.5 Command Description

### 1.3.5.1 Call Subroutine (No. 34)

Calls the subroutine given by its call address. This command is only relevant for customers using downloadable RAM-modules.

**Input Parameters:** Subroutine call address. The subroutine call address is the binary IRAM address given in the setup parameters.

**Return Values:** Depends on the called subroutine.

#### Error Code

Table 4

ERR (7:0)	Description
0	Command execution was successful.
1 – 255	Not defined

**Comment:** The subroutine call address bits must be written over M3L-Bus data port 0 or 1.

### 1.3.5.2 Clock (No. 12)

In picture mode, this command shows the current time on the TV screen from the last 8 characters of each TTX page header. If the command is given again or if text mode is chosen, the clock display is switched off.

**Input parameters:** None.

**Return values:** None.

**Comments:** For position and attributes of the clock, refer to the setup parameters.

### 1.3.5.3 Cursor Down (No. 19)

In text or mix mode (TOP, FLOF, simple or list) the **PAGE CATCHING** feature is activated. This command searches the next page number beginning from row 1 / column 0 of the display page downward (three digits from 0...9 immediately following each other with a leading blank) and highlights it. If any page number is already highlighted search is started from that position. After reaching row 23 / column 37 of the display chapter, search is started again at the top of the page.

**Input parameters:** None.

**Return values:** None.

**Comments:** The page catching function is quit by any other page selection method.



#### 1.3.5.4 Cursor Up (No. 18)

In text or mix mode (TOP, FLOF, simple or list) the **PAGE CATCHING** feature is activated. This command searches beginning from row 23 / column 37 of the display page the next page number upward (three digits from 0...9 immediately following each other with a leading blank) and highlights it. If any page number is already highlighted search is started from that position. After reaching row 1 / column 0 of the display chapter search is started again in row 23 / column 37.

**Input parameters:** None.

**Return values:** None.

**Comments:** The page catching function is quit by any other page selection method.

#### 1.3.5.5 Cyan (No. 17)

Depending on the current mode, the display chapter is changed to the page number indicated by the cyan button.

- In TOP mode, this is the next available block page marked in the BTT.
- In FLOF mode, it is the fourth link of packet x/27 of the current display page.
- In list mode, it is the list#4 page.
- In simple mode, it is the next available page in the next hundred group.
- In subpage mode, this button is not defined.

After changing the display chapter, the new page requests are automatically done.

**Input parameters:** None.

**Return values:** None.

**Comments:** Setting any other page selecting method quits this one. If a new page request is done, the current page number will be written in row 0 of the display chapter.

### 1.3.5.6 Digit 0 (No. 23)

The digit 0 is added to the page number and written to the actual column position of row 0 of the display memory. This command is used for numeric selection of a page. 3 digits (4 in subpage mode) must be given one after another to select a new page. After entering the third digit for the page number (the fourth in subpage mode) the display chapter will change and the page request of the complete page number will be executed. Depending on the current mode (TOP, FLOF, simple or list), all other page requests are automatically done in the background.

**Input parameters:** None.

**Return values:** None.

**Comments:** Setting any other page selecting method quits this one. Incomplete page numbers in the first 8 columns of the header are replaced by "-". The first digit of the page number must be  $> 0$  and  $\leq 8$ . For format of the first 8 characters in row 0 of the display memory refer to the user defined characters UDC.

### 1.3.5.7 Digit 1 (No. 24)

This command has the same meaning as "DIGIT 0" except that the digit 1 is added to the page number.

### 1.3.5.8 Digit 2 (No. 25)

This command has the same meaning as "DIGIT 0" except that the digit 2 is added to the page number.

### 1.3.5.9 Digit 3 (No. 26)

This command has the same meaning as "DIGIT 0" except that the digit 3 is added to the page number.

### 1.3.5.10 Digit 4 (No. 27)

This command has the same meaning as "DIGIT 0" except that the digit 4 is added to the page number.

### 1.3.5.11 Digit 5 (No. 28)

This command has the same meaning as "DIGIT 0" except that the digit 5 is added to the page number.

### 1.3.5.12 Digit 6 (No. 29)

This command has the same meaning as "DIGIT 0" except that the digit 6 is added to the page number.

### 1.3.5.13 Digit 7 (No. 30)

This command has the same meaning as “DIGIT 0” except that the digit 7 is added to the page number.

### 1.3.5.14 Digit 8 (No. 31)

This command has the same meaning as “DIGIT 0” except that the digit 8 is added to the page number.

### 1.3.5.15 Digit 9 (No. 32)

This command has the same meaning as “DIGIT 0” except that the digit 9 is added to the page number.

### 1.3.5.16 Green (No. 15)

Depending on the current mode, the display chapter is changed to the page number indicated by the green button.

- In TOP mode, this is the next available page marked in the BTT.
- In FLOF mode, it is the second link of packet x/27 of the current display page.
- In list mode, it is the list#2 page.
- In simple mode, it is the next available page in binary order.
- IN subpage mode, it is the subpage with next higher subpage number.

After changing the display chapter, the new page requests are automatically done.

**Input parameters:** None.

**Return values:** None.

**Comments:** Setting any other page selecting method quits this one. If a new page request is done, the current page number will be written in row 0 of the display chapter.

### 1.3.5.17 Hold (No. 10)

This command stops the acquisition of the current display chapter. If the hold command is given again, the current page appears (corresponding return parameters STOP\_DIS).

**Input parameters:** None.

**Return values:** None.

**Comments:** None.

### 1.3.5.18 Index Page (No. 07)

This command switches the display page

- in FLOF mode to the 5th link (index page).
- if there is no FLOF mode to the initial page of packet 8/30.
- if there is no packet 8/30 to the initial page given in the setup parameters (IP\_M, IP\_PT, IP\_PU).

**Input parameters:** None.

**Return values:** None.

**Comments:** None.

### 1.3.5.19 Inhibit Update S/P-C (No. 35)

This command defines display memory parts which are forbidden to be overwritten by the S/P-C. Any number of inhibit update windows can be defined. In between these windows bytes 0 - 4 of the CDW are always blocked for the S/P-C. The window can be closed again by using the bits ALL and UPDATE. See **table 5** below for an explanation of all combinations ALL / UPDATE.

#### Input Parameters

#### MCI0\_0 / MODE\_1

0	0	0	0	0	0	ALL	UPDATE
---	---	---	---	---	---	-----	--------

**UPDATE:** This bit forces the S/P-C to update the specified window again with teletext data.

- 1: The specified inhibit update window is cancelled.
- 0: The specified window is not updated anymore by the S/P-C.

**ALL:**

- 1: The total memory of block 2 is influenced by this command.
- 0: Only the window defined by the COORDINATE registers is influenced by this command

**Table 5**

ALL	UPDATE	
0	0	No update of the defined window.
0	1	Update of the defined window.
1	0	No part of the display memory will be updated.
1	1	The total display memory (block 2) will be updated.

**Delta Specification**

**MCI0\_4 / COORDINATE\_ROW\_START**

0	0	0	S_ROW_4	S_ROW_3	S_ROW_2	S_ROW_1	S_ROW_0
---	---	---	---------	---------	---------	---------	---------

**MCI0\_3 / COORDINATE\_COLUMN\_START**

0	0	S_COL_5	S_COL_4	S_COL_3	S_COL_2	S_COL_1	S_COL_0
---	---	---------	---------	---------	---------	---------	---------

**MCI0\_2 / COORDINATE\_ROW\_END**

0	0	0	E_ROW_4	E_ROW_3	E_ROW_2	E_ROW_1	E_ROW_0
---	---	---	---------	---------	---------	---------	---------

**MCI0\_1 / COORDINATE\_COLUMN\_END**

0	0	E_COL_5	E_COL_4	E_COL_3	E_COL_2	E_COL_1	E_COL_0
---	---	---------	---------	---------	---------	---------	---------

The COORDINATE registers define the start and end, row and column addresses of the inhibit update windows. The end address must always be higher than the start address.

**Return Values:**               None.

**Table 6  
Error Code**

<b>ERR (7:0)</b>	<b>Description</b>
0	Command execution was successful.
1 – 255	Not defined

**Comments:**                    Activate and deactivate of the defined inhibit update windows can be done with the bit ENA\_INHIBIT\_UPDATE in the setup parameter.

### 1.3.5.20 Last Seen Page (No. 38)

This command changes the display page one displayed before the current one.

**Input parameters:** None.

**Return values:** None.

**Comments:** None.

### 1.3.5.21 List Mode (No. 06)

This command switches on the list mode and offers a single line menu similar to the FLOF menu. This line contains the stored list page numbers which can be selected by the appropriate colour buttons. If there are less than 4 list pages stored, a “???” will appear in some buttons. If the list page is a subpage (subcode unequal 0000h or 3F7Fh) the subpage number will also appear. If this command is executed again, **COMPACTTEXT** will return to the last chosen text mode (TOP, FLOF or simple).

**Input parameters:** None.

**Return values:** None.

**Comments:** If the list mode is switched on, **SDA 5273-3C** will generate a status line in the display memory. Each field of this line will get a different background colour (red, green, yellow, cyan) and black as a foreground colour. If the field contains a subpage number, the page number and the subpage number will be separated by a slash (“/”). The complete page number is preceded by 2 leading blanks. If the list page is only a basic page in subpage don't care mode, this page number is surrounded by 4 leading and 3 filling blanks.

**Table 7**

Column Position	0 - 9	10 - 19	20 - 29	30 - 39
<b>LIST-PAGE #</b>	<b>0</b>	<b>1</b>	<b>2</b>	<b>3</b>
<b>Example</b>	<b>301</b>	<b>???</b>	<b>422/0004</b>	<b>409/0004</b>
<b>Colour</b>	<b>red</b>	<b>green</b>	<b>yellow</b>	<b>cyan</b>

### 1.3.5.22 List Page (No. 13)

This command adds / removes a list page (a favourite page) to / from the page memory. If the list page to be added is already requested, only the status of the page is changed. List pages can only be removed by the list command or after reset. If the memory is full, the page with the lowest priority is automatically removed.

#### Input parameters

#### MCI1\_5 / PRQ\_RECORD\_4

0	0	0	0	0	M2	M1	M0
---	---	---	---	---	----	----	----

#### MCI1\_4 / PRQ\_RECORD\_3

PT3	PT2	PT1	PT0	PU3	PU2	PU1	PU0
-----	-----	-----	-----	-----	-----	-----	-----

#### MCI1\_3 / PRQ\_RECORD\_2

0	MT2	MT1	MT0	MU3	MU2	MU1	MU0
---	-----	-----	-----	-----	-----	-----	-----

#### MCI1\_2 / PRQ\_RECORD\_1

0	0	HT1	HT2	HU3	HU2	HU1	HU0
---	---	-----	-----	-----	-----	-----	-----

All above listed request bits have the same meaning as defined in the WST.

#### MCI1\_1 / RESERVED

0	0	0	0	0	0	0	0
---	---	---	---	---	---	---	---

#### MCI1\_0 / LIST\_MODE

0	0	0	LC_1	LC_0	SDC	ADD/REM	0
---	---	---	------	------	-----	---------	---

#### SDC:

Subpage don't care mode:

1: The list page is a running-through subpage.

0: The list page is a subpage.

#### ADD/REM:

Add or remove a list page:

1: The list page is added to the page memory.

0: The list page of the given list colour is removed from the page memory.

#### LC\_1...0:

List colour:

0: The list page is assigned to the red colour button.

1: The list page is assigned to the green colour button.

2: The list page is assigned to the yellow colour button.

3: The list page is assigned to the cyan colour button.

---

**Delta Specification**

**Return values:** None.

**Comments:** The command list mode offers a menu line that shows the stored list pages.

**Table 8**  
**Error Code**

<b>ERR (7:0)</b>	<b>Description</b>
<b>0</b>	Command execution was successful.
<b>1</b>	The given list colour is already used
<b>2</b>	No memory space available to add this page
<b>3</b>	The given page is already a list page
<b>4</b>	The given list colour is not used (remove)
<b>5 – 255</b>	Not defined

**1.3.5.23 Mix Mode (No. 04)**

This command toggles between background colour and transparent background colour (text mode - mix mode) or between foreground colour and transparent foreground colour (picture mode - mix mode).

**Input parameters:** None.

**Return values:** None.

**Comments:** None.



### 1.3.5.24 Move Memory Seg (No. 33)

This command moves any internal source memory byte segment to an internal destination memory byte segment. Substitution capabilities are supported.

Input Parameters are Source Segment Start Address, Source Segment End Address, Destination Segment Start Address and the Substitution Parameters.

#### Source Segment Start Address

##### MCI0\_5 / MOVE\_SOURCE\_SEG\_START\_2

0	0	0	0	BYT_5	BYT_4	BYT_3	BYT_2
---	---	---	---	-------	-------	-------	-------

##### MCI0\_4 / MOVE\_SOURCE\_SEG\_START\_1

BYT_1	BYT_0	BLK_2	BLK_1	BLK_0	ROW_4	ROW_3	ROW_2
-------	-------	-------	-------	-------	-------	-------	-------

##### MCI0\_3 / MOVE\_SOURCE\_SEG\_START\_0

ROW_1	ROW_0	COL_5	COL_4	COL_3	COL_2	COL_1	COL_0
-------	-------	-------	-------	-------	-------	-------	-------

**BYT\_5 – BYT\_0:** Byte position of the internal memory doubleword.  
Only one BYT bit must be selected.

**BLK\_2 – BLK\_0:** Block of internal memory.  
 $0 \leq \text{block address} \leq 3$ .

**ROW\_4 – ROW\_0:** Internal memory row address.  
 $0 \leq \text{row address} \leq 25$ .

**COL\_5 – COL\_0:** Internal memory column address.  
For row address = 0 - 24  $\rightarrow 0 \leq \text{column address} \leq 39$ .  
For row address = 25  $\rightarrow 0 \leq \text{column address} \leq 23$ .

## Delta Specification

### Source Segment End Address

#### MCI0\_2 / MOVE\_SOURCE\_SEG\_END\_2

0	0	0	0	0	0	0	0
---	---	---	---	---	---	---	---

#### MCI0\_1 / MOVE\_SOURCE\_SEG\_END\_1

0	0	0	0	0	ROW_4	ROW_3	ROW_2
---	---	---	---	---	-------	-------	-------

#### MCI0\_0 / MOVE\_SOURCE\_SEG\_END\_0

ROW_1	ROW_0	COL_5	COL_4	COL_3	COL_2	COL_1	COL_0
-------	-------	-------	-------	-------	-------	-------	-------

**ROW\_4 – ROW\_0:** Row address for the end of memory source segment  
 $0 \leq \text{row address} \leq 25$ .

**COL\_5 – COL\_0:** Column address for the end of memory source segment  
 For row address = 0 - 24  $\rightarrow 0 \leq \text{column address} \leq 39$ .  
 For row address = 25  $\rightarrow 0 \leq \text{column address} \leq 23$ .

### Destination Segment Start Address

#### MCI1\_5 / MOVE\_DESTINATION\_SEG\_START\_2

0	0	0	0	BYT_5	BYT_4	BYT_3	BYT_2
---	---	---	---	-------	-------	-------	-------

#### MCI1\_4 / MOVE\_DESTINATION\_SEG\_START\_1

BYT_1	BYT_0	BLK_2	BLK_1	BLK_0	ROW_4	ROW_3	ROW_2
-------	-------	-------	-------	-------	-------	-------	-------

#### MCI1\_3 / MOVE\_DESTINATION\_SEG\_START\_0

ROW_1	ROW_0	COL_5	COL_4	COL_3	COL_2	COL_1	COL_0
-------	-------	-------	-------	-------	-------	-------	-------

**BYT\_5 – BYT\_0:** Byte position of the internal memory doubleword.  
 Only one BYT bit must be selected.

**BLK\_2 – BLK\_0:** Block of internal memory.  
 $0 \leq \text{block address} \leq 3$ .

**ROW\_4 – ROW\_0:** Internal memory row address.  
 $0 \leq \text{row address} \leq 25$ .

**COL\_5 – COL\_0:** Internal memory column address.  
 For row address = 0 - 24  $\rightarrow 0 \leq \text{column address} \leq 39$ .  
 For row address = 25  $\rightarrow 0 \leq \text{column address} \leq 23$ .

**Substitution Parameters**

**MCI1\_1 / SUBSTITUTION\_PATTERN\_DISABLE**

SUBSDIS_7	SUBSDIS_6	SUBSDIS_5	SUBSDIS_4	SUBSDIS_3	SUBSDIS_2	SUBSDIS_1	SUBSDIS_0
-----------	-----------	-----------	-----------	-----------	-----------	-----------	-----------

**MCI1\_0 / SUBSTITUTION\_PATTERN**

SUBS_7	SUBS_6	SUBS_5	SUBS_4	SUBS_3	SUBS_2	SUBS_1	SUBS_0
--------	--------	--------	--------	--------	--------	--------	--------

**SUBSDIS(7:0):** Substitution pattern disables/enables the associated substitution pattern bit for substitution. So a selection of bits to be substituted by the given substitution pattern is possible.  
 0: Substitution is enabled.  
 1: Substitution is disabled.

**SUBS(7:0):** Substitution value. Only bits which are enabled by the associated substitution pattern disable bit will be substituted.

**MCI3\_3 / MOVE\_CONTROL**

WINDOWS	BINARY	0	MOV_DIS	SUB_EN	0	0	0
---------	--------	---	---------	--------	---	---	---

**SUB\_EN:** Substitution enable  
 1: All bytes of the selected memory segment are substituted with the reference value of the substitute pattern.  
 0: Substitution is disabled.

**MOV\_DIS:** Move disable  
 1: Moving any byte of the selected byte segment is disabled.  
 0: Each byte is moved to the destination address.

**BINARY:**  
 1: The binary address scheme is assumed. Row 4 - row 0 and col 5 - col 1 of move source reg start and end are interpreted as binary address bits. Col 0 has don't care value.  
 0: The row/col address scheme is assumed.

**WINDOWS:**  
 1: The address given in move source seg start is interpreted as the top left corner of a window and the address in move source seg end the bottom right corner. The column and row address in move source seg end must be bigger than move source seg start.  
 0: Continuous row/col address scheme is assumed.

**Return Values:** Address of actual destination: mov destination seg start.

## Comments

- A byte segment can be 1 to 1024 bytes and must be inside a chapter.
- Source segment size must fit into the destination chapter.
- Following segments can be selected:  
 Selection of 1 byte segment by the BYT\_5 to BYT\_0 bits is possible. The segment length is determined by the move source seg start and move source seg end parameters. The destination byte segment can be at any byte position of a doubleword.
- Minimum source segment start address of a chapter is row/column = 0/0.  
 Maximum source segment start address of a chapter is row/column = 25/23.  
 Minimum source segment end address of a chapter is row/column = 0/0.  
 Maximum source segment end address of a chapter is row/column = 25/23.  
 Minimum destination segment start address of a chapter is row/column = 0/0.  
 Maximum destination segment start address of a chapter is row/column = 25/23.

### 1.3.5.25 Next Page (No. 01)

This command changes the display page to the next page:

- Binary mode: Next page = display page + 1
- Page trace mode: Next page = next available page in the page trace in ascending order.

**Input parameters:** None.

**Return values:** None.

**Comments:** None.

### 1.3.5.26 Page Catching Off (No. 36)

Switches off the page catching feature.

**Input parameters:** None.

**Return values:** None.

**Comments:** None.

### 1.3.5.27 Picture Mode (No. 02)

Switches from any text mode to TV mode. The switch is done by stopping the S/P-C and setting the foreground and background transparent bits in the character display word to 1 (transparent). All acquisition tasks are continued in the background.

**Input parameters:** None.

**Return values:** None.

**Comments:** None.

### 1.3.5.28 Previous Page (No. 05)

This command changes the display page to the previous page:

- Binary mode: Previous page = display page - 1
- Page trace mode: Previous page = next available page in the page trace in descending order

**Input parameters:** None.

**Return values:** None.

**Comments:** None.

### 1.3.5.29 Red (No. 14)

Depending on the current mode, the display chapter is changed to the page number indicated by the red button.

- In TOP mode, this is the previous available page marked in the BTT.
- In FLOF mode, this is the first link of packet x/27 of the current display page.
- In list mode, this is the list#1 page.
- In simple mode, this is the previous available page in binary order.
- In subpage mode, this is the subpage with next lower subpage number.

After changing the display chapter, the new page requests are automatically done.

**Input parameters:** None.

**Return values:** None.

**Comments:** Setting any other page selecting method quits this one. If a new page request is done, the current page number will be written in row 0 of the display chapter.

### 1.3.5.30 Reset Acq (No. 00)

This command initializes COMPACTTEXT for teletext reception and should be given after power up and each channel change. Before invoking this command, all setup parameters must be defined.

**Input parameters:** Setup parameters.

**Return values:** None.

**Comments:** None.

**1.3.5.31 Reset Intq (No. 20)**

This command resets the pin INTQ, reads out the interrupt request source bits and resets the interrupt request source bits.

**Input parameters:** None.

**Return values**

**MCI3\_5 / IRQS**

0	REC_WSS	TEXT_INT	0	0	REC_VPS	0	0
---	---------	----------	---	---	---------	---	---

**Comments:** For a description of the bits please refer to the **chapter 1.6**.

**1.3.5.32 Reveal (No. 11)**

All hidden characters are revealed. Giving this command again, hides these characters again.

**Input parameters:** None.

**Return values:** None.

**Comments:** None.

**1.3.5.33 Search Page (No. 37)**

This command returns the chapter address of the given page number.

**Input parameters**

**MCI1\_5 / Magazine number**

0	0	0	0	0	MAG_2	MAG_1	MAG_0
---	---	---	---	---	-------	-------	-------

**MCI1\_4 / Page number**

PT_3	PT_2	PT_1	PT_0	PU_3	PU_2	PU_1	PU_0
------	------	------	------	------	------	------	------

**Return values**

**MCI1\_2 / Destination\_Address\_2**

0	0	0	0	By_5	By_4	By_3	By_2
---	---	---	---	------	------	------	------

**MCI1\_1 / Destination\_Address\_1**

By_1	By_0	BI_2	BI_1	BI_0	0	0	0
------	------	------	------	------	---	---	---

**MCI1\_0 / Destination\_Address\_0**

0	0	0	0	0	0	0	0
---	---	---	---	---	---	---	---

**Table 9  
Error Code**

<b>ERR (7:0)</b>	<b>Description</b>
0	Page found
1	Page not found
2 – 255	Not defined

**Comments:** None.

**1.3.5.34 Size (No. 09)**

This command toggles between the three possible display sizes in the following order:

- Normal size: Row 0 - 24 are shown in normal height.
- Double size upper half: Row 0 - 11 are shown in double height, row 24 in normal height.
- Double size lower half: Row 12 - 23 are shown in double height, row 24 in normal height.

**Input parameters:** None.

**Return values:** None.

**Comments:** None.

**1.3.5.35 Size Off (No. 21)**

Switches directly back to normal height if **COMPACTTEXT** has been in double height mode by giving the command size.

**Input parameters:** None.

**Return values:** None.

**Comments:** None.

### 1.3.5.36 Start New Request (No. 39)

This command generates a new page request starting from the given display page and changes the current display page.

#### Input parameters

#### MCI1\_5 / Magazine number

0	0	0	0	0	MAG_2	MAG_1	MAG_0
---	---	---	---	---	-------	-------	-------

#### MCI1\_4 / Page number

PT_3	PT_2	PT_1	PT_0	PU_3	PU_2	PU_1	PU_0
------	------	------	------	------	------	------	------

**Return values:** None.

**Comments:** None.

### 1.3.5.37 Store OK (No. 22)

If page catching mode is activated by the commands cursor up/down, **COMPACTTEXT** will change to the highlighted page number. All new page requests are automatically done depending on the current text mode (TOP, FLOF, list, simple).

**Input parameters:** None.

**Return values:** None.

**Comments:** None.

### 1.3.5.38 Subpage Mode (No. 08)

If this command is given, the subpage mode is activated. That means that any subpage of the current basic display chapter can be requested. In that mode 4 digits must be given to specify a subpage. The subpage mode is terminated if this command is given again, or if any other page select method (i.e. page catching) is used. With the colour keys, the next and the previous subcode can be selected.

**Input parameters:** None.

**Return values:** None.

**Comments:** None.



Table 10

Column Position	0 - 4	5 - 9	10 - 39
Example	-	+	100/0004
Colour	red	green	white

### 1.3.5.39 Text Mode (No. 03)

Switches from TV mode to text mode. The switch is done by resetting all transparent background and foreground bits in the CDW. Further on, any special text modes (i.e. double height, hold, reveal) are cleared.

**Input parameters:** None.

**Return values:** None.

**Comments:** None.

### 1.3.5.40 Yellow (No. 16)

Depending on the current mode the display chapter is changed to the page number indicated by the yellow button.

- In TOP mode, this is the next available group or block page marked in the BTT.
- In FLOF mode, this is the third link of packet x/27 of the current display page.
- In list mode, this is the list#3 page.
- In simple mode, this is the next available page in the next tens group.
- In subpage mode this button is not defined.

After changing the display chapter the new page requests are automatically done.

**Input parameters:** None.

**Return values:** None.

**Comments:** Setting any other page selecting method quits this one. If a new page request is done, the current page number will be written in row 0 of the display chapter.

### 1.4 Setup Parameters

The following table gives an overview of all possible setup parameters. These parameters are stored in block 0 / row 5 / column 0- 39 / byte 4 of the internal DRAM.

**Table 11**

**Address = Block 0 / Row 5 / Byte 4**

Col.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	ENA_TOP	ENA_FLOF	0	0	0	ENA_LINE 16/23	ENA_B1_B3_ACQ	ENA_VBI
1	ENA_PAGE_TRACE	ENA_INHIBIT_UPDATE	ENA_X26	ENA_INTQ	ENA_INI_PAGE_8/30	TIM_ROW_4	TIM_ROW_3	TIM_ROW_2
2	TIM_ROW_1	TIM_ROW_0	TIM_COL_5	TIM_COL_4	TIM_COL_3	TIM_COL_2	TIM_COL_1	TIM_COL_0
3	TA_23	TA22	TA_21	TA_20	TA_19	TA_18	TA_17	TA_16
4	TA_15	TA_14	TA_13	TA_12	TA_11	0	TA_9	0
5	0	0	0	0	DISABLE_ROW_24	0	CLOCK_OFF	HEAD_OFF
6	G0_S_7	G0_S_6	G0_S_5	G0_S_4	G0_S_3	G0_S_2	G0_S_1	G0_S_0
7	G0_E_7	G0_E_6	G0_E_5	G0_E_4	G0_E_3	G0_E_2	G0_E_1	G0_E_0
8	G2_S_7	G2_S_6	G2_S_5	G2_S_4	G2_S_3	G2_S_2	G2_S_1	G2_S_0
9	G2_E_7	G2_E_6	G2_E_5	G2_E_4	G2_E_3	G2_E_2	G2_E_1	G2_E_0
10	0	CHSNR_6	CHSNR_5	CHSNR_4	CHSNR_3	CHSNR_2	CHSNR_1	CHSNR_0
11	TWIST1C14	TWIST1C13	TWIST1C12	TWIST1_4	TWIST1_3	TWIST1_2	TWIST1_1	TWIST1_0
12	NU_TE_FR_7	NU_TE_FR_6	NU_TE_FR_5	NU_TE_FR_4	NU_TE_FR_3	NU_TE_FR_2	NU_TE_FR_1	NU_TE_FR_0
13	0	1	0	1	1	1	1	1
14	1	1	BLK2	BLK1	BLK0	ROW_4	ROW_3	ROW_2
15	ROW_1	ROW_0	COL_5	COL_4	COL_3	COL_2	COL_1	COL_0
16	0	0	0	0	0	NU_AIT_2	NU_AIT_1	NU_AIT_0
17-24	User Set Table							
25	0	0	0	D_HAM1_ERR	0	0	0	P26_C8
26	TWIST2C14	TWIST2C13	TWIST2C12	TWIST2_4	TWIST2_3	TWIST2_2	TWIST2_1	TWIST2_0
27	0	0	0	0	0	0	0	0
28	0	0	0	0	0	0	0	0
29	WSS_CNT7	WSS_CNT6	WSS_CNT5	WSS_CNT4	WSS_CNT3	WSS_CNT2	WSS_CNT1	WSS_CNT0
30	NU_VALID_HEAD7	NU_VALID_HEAD6	NU_VALID_HEAD5	NU_VALID_HEAD4	NU_VALID_HEAD3	NU_VALID_HEAD2	NU_VALID_HEAD1	NU_VALID_HEAD0
31	0	0	0	0	0	IP_M2	IP_M1	IP_M0

Table 11

Address = Block 0 / Row 5 / Byte 4 (cont'd)

Col.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
32	IP_PT3	IP_PT2	IP_PT1	IP_PT0	IP_PU3	IP_PU2	IP_PU1	IP_PU0
33	VPS_WAIT_ 7	VPS_WAIT_ 6	VPS_WAIT_ 5	VPS_WAIT_ 4	VPS_WAIT_ 3	VPS_WAIT_ 2	VPS_WAIT_ 1	VPS_WAIT_ 0

- ENA\_VBI:** 1: The VBI Buffer is enabled.  
0: The VBI Buffer is disabled.
- ENA\_B1\_B3\_ACQ:** 1: Block 1 and block 3 are enabled for acquisition.  
0: Both blocks are disabled for acquisition.
- ENA\_LINE16/23:** 1: Automatic handling of the single data lines 16 and 23 is activated. VPS, WSS and text in line 16 are processed automatically by internal PU. After the command reset acq, the **COMPACTTEXT** sets the single data line register to line 16. If VPS is detected in the given time period (VPS\_WAIT in setup parameters). **COMPACTTEXT** toggles the single data line register between line 16 and line 23 to receive VPS and WSS in one field. If no VPS is detected, **COMPACTTEXT** sets the single data line register to line 23. In this case, line 16 is enabled for text reception.  
0: Automatic handling of the single data lines 16 and 23 is disabled.
- ENA\_FLOF:** 1: The automatic reception of linked FLOF pages is enabled.  
0: The automatic acquisition of linked FLOF pages is disabled.
- ENA\_TOP:** 1: The automatic reception of TOP pages (including block pages, group pages and so on) is enabled.  
0: The automatic acquisition of TOP pages is disabled.
- ENA\_INI\_PAGE\_8/30:** 0: Automatic change of the initial page via 8/30 is disabled.  
1: Automatic change of the initial page via 8/30 is enabled.
- ENA\_INTQ:** 1: If WSS or VPS is detected, the INTQ pin is set to high.  
0: Setting INTQ pin is disabled.
- ENA\_X26:** 1: Request of packet 26 is enabled.  
0: Request of packet 26 is disabled.
- ENA\_INHIBIT\_UPDATE:** 1: The inhibit update window is enabled.  
0: The inhibit update window is disabled.

## Delta Specification

<b>ENA_PAGE_TRACE:</b>	1: The page trace is enabled for page request. 0: The page trace is disabled for page request.
<b>TIM_ROW_(4:0):</b>	Defines the display row address of the clock in picture mode.
<b>TIM_COL_(5:0):</b>	Defines the display column address of the clock in picture mode.
<b>TA_(23:9):</b>	Defines the parallel attributes of the clock (format is the same as in the CDW).
<b>HEAD_OFF:</b>	1: During the rolling header mode row0 / col8 - col31 are not overwritten. 0: During the rolling header mode these positions are overwritten by the S/P-C with all incoming headers.
<b>CLOCK_OFF:</b>	1: During the rolling header mode row0 / col32 - col39 are not overwritten. 0: During the rolling header mode these positions are overwritten by the S/P-C with the time information of all incoming headers.
<b>DISABLE_ROW_24:</b>	0: Menuline in row24 is updated. 1: Menuline in row24 of BDM will not be updated.
<b>G0_S_(7:0):</b>	Define the lowest address of the G0 set to be substituted by PCS characters. This value must be bigger/equal than 20 <sub>H</sub> .
<b>G0_E_(7:0):</b>	Define the highest address of the G0 set to be substituted by PCS characters. This value must be smaller/equal than 7F <sub>H</sub> .
<b>G2_S_(7:0):</b>	Define the lowest address of the G2 set to be substituted by PCS characters. This value must be bigger/equal than 20 <sub>H</sub> .
<b>G2_E_(7:0):</b>	Define the highest address of the G2 set to be substituted by PCS characters. This value must be smaller/equal than 7F <sub>H</sub> .
<b>CHSNR_(6:0):</b>	Define the character set number which should be used for the G0-set. In the <b>SDA 5273-3C</b> , character sets 6, 38, 55 are integrated. If the user wants to define a new character set, the CHSNR(6:0) has to be set to 63 <sub>d</sub> . In this case, the language will be calculated accordingly to the USER SET TABLE which must be defined by the user. The USER SET TABLE (see below) must be initialized by the controller.
<b>TWIST1(4:0):</b>	Defines the second "twisted" language after an ESCAPE Character. Any combinations of languages as defined in the language table are possible. The TWIST1(4:0) defines the twist language, if the language, defined by the header control bits C14...C12, is a latin based language.

## Delta Specification

- TWIST1C(14:12):** Defines the language header control-bit combination of the “twisted” language.
- TWIST2(4:0):** Defines the second “twisted” language after an ESCAPE Character. Any combinations of languages as defined in the language table are possible. The TWIST2(4:0) defines the twist language, if the language, defined by the header control bits C14...C12, is a non-latin based language.
- TWIST2C(14:12):** Defines the language header control-bit combination of the “twisted” language.
- NU\_TE\_FR\_(7:0):** These bits define the number of frames which have to pass without text reception, before the flag TEXT\_INT is set.
- BLK(2:0), ROW(4:0), COL(5:0):** These bits define the start address of the subroutine to be called by the command call subroutine. The format of the address must be a valid address format.
- NU\_AIT\_(2:0):** Define the maximum number of AITs which are automatically requested by the ACQ (max 4).

**Table 12**  
**User Set Table**

Column-Address	C12, C13, C14	Char. Set 63 (User Set)
17	000	language number
18	100	language number
19	010	language number
20	110	language number
21	001	language number
22	101	language number
23	011	language number
24	111	language number

The following tables explain the assignment of the language numbers to the possible integrated languages and the numbers of user definable languages.

## Delta Specification

**Table 13**

<b>C12, C13, C14</b>	<b>Char. Set 6</b>	<b>Char. Set 38</b>	<b>Char. Set 55</b>	<b>Char. Set 63</b>
000	English	Polish	English	language number
001	German	German	German	language number
010	Swedish	Swedish	Swedish	language number
011	Italian	Italian	Italian	language number
100	French	French	French	language number
101	Portuguese	Serbocroat	Portuguese	language number
110	Czechoslovakian	Czechoslovakian	Turkish	language number
111	English	Rumanian	English	language number

**Table 14**  
**Language Table**

<b>Language Number</b>	<b>Language</b>
0	Polish
1	English
2	Turkish
3	German
4	Rumanian
5	Swedish
6	Czechoslovakian
7	Italian
8	Estonian
9	French
10	Serbocroat
11	Portuguese
12	non-latin languages (russian, arabic, hebrew, greek)
13	Ukrainian
14	Not defined
15	Lettish/Lithuanian
16 - 127	Not defined

---

**Delta Specification**

- D\_HAM1\_ERR:** 0: Packets with 1-bit hamming errors in the magazine or packet byte will be accepted.  
1: Packets with 1-bit hamming errors in the magazine or packet byte will be rejected.
- P26\_C8:** 0: X/26 information which is already stored for a page will not be removed if the header control bit C8 is not set in packet 0 of this page.  
1: X/26 information which is already stored for a page will be removed with the incoming header if the header control bit C8 is set (erase X/26).
- WSS\_CNT(7:0):** WSS repetition counter. This is an input parameter for the internal WSS module. It controls the setting of the bit REC\_WSS in the return parameters. This parameter defines how often the WSS data have to be received without any errors in sequence before the bit REC\_WSS will be set by the internal firmware.
- NU\_VALID\_HEAD(7:0):** Number of valid headers. This parameter is used together with NU\_TE\_FR\_(7:0) to define a criterion for the text indication module. With the NU\_TE\_FR\_(7:0) you define the number of frames with text information and with NU\_VALID\_HEAD(7:0) you define the number of headers within this frames. All hamming coded bytes of the detected headers must be free of errors.
- IP\_PT(3:0):** Page number tens of the initial page.
- IP\_PU(3:0):** Page number units of the initial page.
- IP\_M(2:0):** Magazine number of the initial page.
- VPS\_WAIT(7:0):** Defines the number of fields which have to be passed without VPS in line 16 before **COMPACTTEXT** switches to text in line 16.

**1.5 User Defined Characters (UDC)**

The UDC are the first 8 bytes of the display memory and used to display the page number of the current display page.

**UDC\_ATTR\_2**

DPA_23	DPA_22	DPA_21	DPA_20	DPA_19	DPA_18	DPA_17	DPA_16
--------	--------	--------	--------	--------	--------	--------	--------

**UDC\_ATTR\_1**

DPA_15	DPA_14	DPA_13	DPA_12	DPA_11	DPA_10	DPA_9	DPA_8
--------	--------	--------	--------	--------	--------	-------	-------

**UDC\_ATTR\_0**

DPA_7	DPA_6	DPA_5	DPA_4	DPA_3	DPA_2	DPA_1	DPA_0
-------	-------	-------	-------	-------	-------	-------	-------

**DPA(23:0):** These bits define the attributes for the UDC (same format as the CDW).

The firmware overwrites only the character bits DPA(7:0) of the UDC 2, 3, 4 in the display memory. The rest of the attributes inclusive the UDC characters 0, 1, 5, 6,7 must be defined by the user.

**Table 15  
MEMORY LOCATION**

<b>Corresponding Display Address</b>	<b>UDC Address</b>
BL_2/By2-0/Ro_0/Col_0	BI_0/By2-0/Ro_2/Col_27
BL_2/By2-0/Ro_0/Col_1	BI_0/By5-3/Ro_2/Col_27
BL_2/By2-0/Ro_0/Col_2	BI_0/By2-0/Ro_2/Col_28
BL_2/By2-0/Ro_0/Col_3	BI_0/By5-3/Ro_2/Col_28
BL_2/By2-0/Ro_0/Col_4	BI_0/By2-0/Ro_2/Col_29
BL_2/By2-0/Ro_0/Col_5	BI_0/By5-3/Ro_2/Col_29
BL_2/By2-0/Ro_0/Col_6	BI_0/By2-0/Ro_2/Col_30
BL_2/By2-0/Ro_0/Col_7	BI_0/By5-3/Ro_2/Col_30



## Delta Specification

### 1.6 Return Parameters

The following table gives an overview of all possible return parameters. These parameters are stored in block 0 / row 5 / column 0 - 39 / byte 3 of the internal DRAM and can be read every time.

**Table 16**  
**Address = Block 0 / Row 5 / Byte 3**

Col.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	x	PG_TRACE_MODE	0	PG_CATCH_MODE	LIST_MODE	FLOF_MODE	TOP_MODE	SIMPLE_MODE
1	PG_NOT_IN_CYCLE	0	TEXT_INT	0	CLOCK_MODE	PICTURE	MIX	TEXT
2	SUBPAGE_MODE	REC_WSS	LINE16_VPS	0	0	REC_VPS	REC_8_30_2	REC_8_30_1
3	0	0	0	0	0	M2	M1	M0
4	PT3	PT2	PT1	PT0	PU3	PU2	PU1	PU0
5	0	MT2	MT1	MT0	MU3	MU2	MU1	MU0
6	0	0	HT1	HT0	HU3	HU2	HU1	HU0
7	DIS_X27_FOUND	STOP_DIS	SUBTITLE	0	0	PAGE_FOUND	NEWS	0
8	VPS_5_7	VPS_5_6	VPS_5_5	VPS_5_4	VPS_5_3	VPS_5_2	VPS_5_1	VPS_5_0
9	VPS_11_7	VPS_11_6	VPS_11_5	VPS_11_4	VPS_11_3	VPS_11_2	VPS_11_1	VPS_11_0
10	VPS_12_7	VPS_12_6	VPS_12_5	VPS_12_4	VPS_12_3	VPS_12_2	VPS_12_1	VPS_12_0
11	VPS_13_7	VPS_13_6	VPS_13_5	VPS_13_4	VPS_13_3	VPS_13_2	VPS_13_1	VPS_13_0
12	VPS_14_7	VPS_14_6	VPS_14_5	VPS_14_4	VPS_14_3	VPS_14_2	VPS_14_1	VPS_14_0
13	WSS_7	WSS_6	WSS_5	WSS_4	WSS_3	WSS_2	WSS_1	WSS_0
14	0	0	WSS_13	WSS_12	WSS_11	WSS_10	WSS_9	WSS_8
15	0	0	0	0	D_AD_19	D_AD_18	D_AD_17	D_AD_16
16	D_AD_15	D_AD_14	D_AD_13	D_AD_12	D_AD_11	0	0	0
17	0	0	0	0	0	0	0	0
18	0	0	0	0	0	0	0	0
19	0	0	0	0	0	0	0	0
20	0	0	0	0	0	0	0	0
21	0	0	0	0	0	0	0	0
22	0	0	0	0	0	0	0	0
23	0	0	0	0	0	0	0	0
24	0	0	0	0	0	0	0	0

**Delta Specification**

**Table 16**  
**Address = Block 0 / Row 5 / Byte 3 (cont'd)**

Col.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
25	0	0	0	0	0	0	0	DIS_NOT_CHANGE
26	0	0	0	0	0	0	COI	ACQ_EN
27	0	0	0	0	0	0	0	0
28	0	0	0	0	D_AIT1_19	D_AIT1_18	D_AIT1_17	D_AIT1_16
29	D_AIT1_15	D_AIT1_14	D_AIT1_13	D_AIT1_12	D_AIT1_11	0	0	NIL
30	0	0	0	0	D_AIT2_19	D_AIT2_18	D_AIT2_17	D_AIT2_16
31	D_AIT2_15	D_AIT2_14	D_AIT2_13	D_AIT2_12	D_AIT2_11	0	0	NIL
32	0	0	0	0	D_AIT3_19	D_AIT3_18	D_AIT3_17	D_AIT3_16
33	D_AIT3_15	D_AIT3_14	D_AIT3_13	D_AIT3_12	D_AIT3_11	0	0	NIL
34	0	0	0	0	D_AIT4_19	D_AIT4_18	D_AIT4_17	D_AIT4_16
35	D_AIT4_15	D_AIT4_14	D_AIT4_13	D_AIT4_12	D_AIT4_11	0	0	NIL
36								
37								ASOF
38								
39								

**Table 17**  
**Address = Block 0 / Row 5 / Byte 2**

Col.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	NU	0	0	0	0	AIT1_MG2	AIT1_MG1	AIT1_MG0
1	AIT1_PT3	AIT1_PT2	AIT1_PT1	AIT1_PT0	AIT1_PU3	AIT1_PU2	AIT1_PU1	AIT1_PU0
2	NU	0	0	0	0	AIT2_MG2	AIT2_MG1	AIT2_MG0
3	AIT2_PT3	AIT2_PT2	AIT2_PT1	AIT2_PT0	AIT2_PU3	AIT2_PU2	AIT2_PU1	AIT2_PU0
4	NU	0	0	0	0	AIT3_MG2	AIT3_MG1	AIT3_MG0
5	AIT3_PT3	AIT3_PT2	AIT3_PT1	AIT3_PT0	AIT3_PU3	AIT3_PU2	AIT3_PU1	AIT3_PU0
6	NU	0	0	0	0	AIT4_MG2	AIT4_MG1	AIT4_MG0
7	AIT4_PT3	AIT4_PT2	AIT4_PT1	AIT4_PT0	AIT4_PU3	AIT4_PU2	AIT4_PU1	AIT4_PU0
8								
9								
10								
11								
12								

<b>SIMPLE_MODE:</b>	<b>COMPACTTEXT</b> is in simple mode.
<b>TOP_MODE:</b>	<b>COMPACTTEXT</b> is in TOP mode.
<b>FLOF_MODE:</b>	<b>COMPACTTEXT</b> is in FLOF mode.
<b>LIST_MODE:</b>	<b>COMPACTTEXT</b> is in list mode.
<b>PG_CATCH_MODE:</b>	<b>COMPACTTEXT</b> is in page catching mode.
<b>PG_TRACE_MODE:</b>	<b>COMPACTTEXT</b> is in page trace mode.
<b>TEXT:</b>	<b>COMPACTTEXT</b> is in text mode.
<b>MIX:</b>	<b>COMPACTTEXT</b> is in mix mode.
<b>PICTURE:</b>	<b>COMPACTTEXT</b> is in picture mode.
<b>CLOCK_MODE:</b>	The clock command is active.
<b>TEXT_INT:</b>	This bit indicates that it was not possible to receive teletext within the last few frames. The number of frames can be programmed by the setup parameter NU_TE_FR_(7:0). This bit can be used as an indicator whether a channel transmits teletext or not. It is reset by the command reset acq.
<b>PG_NOT_IN_CYCLE:</b>	This bit indicates whether the current display page is in the transmission cycle or not.
<b>REC_8_30_1:</b>	Packet 8/30/format1 is received.
<b>REC_8_30_2:</b>	Packet 8/30/format2 is received.
<b>REC_VPS:</b>	VPS data is received.
<b>LINE16_VPS:</b>	If this bit is set to 1, a VPS signal is detected in line 16. No VPS signal is detected when this bit is 0 and the setup parameter VPS_WAIT_COUNTER is also 0.
<b>REC_WSS:</b>	WSS data is received.
<b>SUBPAGE_MODE:</b>	<b>COMPACTTEXT</b> is in subpage mode.
<b>M(2:0):</b>	Magazine number of the current display page.
<b>PT(3:0), PU(3:0):</b>	Page number of the current display page.
<b>MT(2:0), MU(3:0):</b>	Subpage units of the current display page number.
<b>HT(1:0), HU(3:0):</b>	Subpage tens of the current display page number.
<b>NEWS:</b>	The display page is a newsflash page.
<b>PAGE_FOUND:</b>	The display page is received.
<b>SUBTITLE:</b>	The display page is a subtitle page.
<b>STOP_DIS:</b>	If this bit is set to 1 the display page is in "hold" condition. If it is 0 the display page shows always the current subpage.
<b>DIS_X27_FOUND:</b>	X27 for Display page found (for internal use only).

## Delta Specification

<b>VPS<sub>i</sub><sub>j</sub>:</b>	VPS data is error checked and written to a buffer in the internal DRAM. Their values can be read anytime. The received data is biphasic decoded and only updated if all 5 relevant bytes are received without any errors. The VPS received flag (REC_VPS) indicates that after a channel change the data in the buffer (VPS <sub>i</sub> <sub>j</sub> ) has been updated and is valid again (i = byte number, j = bit number).
<b>WSS<sub>i</sub><sub>j</sub>:</b>	WSS data is error checked and written to a buffer in the internal DRAM. Their values can be read anytime. The received data is biphasic decoded and only updated if the 2 relevant bytes are received without any errors. The WSS received flag (REC_WSS) indicates that after a channel change the data in the buffer (WSS <sub>j</sub> ) has been updated and is valid again (i = byte number, j = bit number).
<b>D_AD_(19:0):</b>	Address of current display chapter. D_AD_(19:14) are the byte position bits and D_AD_(13:11) are the block bits.
<b>DIS_NOT_CHANGE:</b>	For internal use only 1: Display page has not been changed by the user yet. 0: Display page has been changed by the user.
<b>ACQ_EN:</b>	Acquisition sync signal reference 1: HPLL lock condition is very good. 0: HPLL lock condition is bad.
<b>COI:</b>	Coincidence Indicator 1: HPLL phase difference is less than 4% of line period. 0: HPLL is not locked.
<b>D_AIT1_(19:0):</b>	Destination address of the additional information table1 (format is the same as D_AD_(19:0)).
<b>D_AIT2_(19:0):</b>	Destination address of the additional information table2 (format is the same as D_AD_(19:0)).
<b>D_AIT3_(19:0):</b>	Destination address of the additional information table3 (format is the same as D_AD_(19:0)).
<b>D_AIT4_(19:0):</b>	Destination address of the additional information table4 (format is the same as D_AD_(19:0)).
<b>UP_TITLE:</b>	This bit will be set if the end of page of the BTT is detected.
<b>ASOF:</b>	Field indicator will be set at each field.
<b>AIT<sub>i</sub>_MG(2:0):</b>	Magazine number of the additional information table i.
<b>AIT<sub>i</sub>_PU(3:0):</b>	Page units of the additional information table i.
<b>AIT<sub>i</sub>_PT(3:0):</b>	Page tens of the additional information table i. (i = 1 to 4)
<b>NU:</b>	Not used.

### 1.7 Description of the Stored Data Formats

#### 1.7.1 Stored Format of 1-Byte Hamming Protected Data

The 1-byte hamming check of data bytes transmitted in TOP tables is done on-line before storing the data byte. The data bits are compressed to the four LSBs. If there is a non correctable hamming error, the code 0<sub>h</sub> will be stored.

0	0	0	0	D3 <sub>j</sub>	D2 <sub>j</sub>	D1 <sub>j</sub>	D0 <sub>j</sub>
---	---	---	---	-----------------	-----------------	-----------------	-----------------

#### 1.7.2 Stored Format of Page

The bits in column 3 – 7 of row 0 have the same meaning as defined in the world system teletext specification. They represent the “header bits” of received packet 0.

All bytes in column 8 – 39 of row 0 and all bytes in row 1 - 24 are either parity or hamming checked (corresponding to the world system teletext specification).

The bit PAG\_ER indicates that the appropriate FLOF link is received correctly and can be used for further page acquisition.

**Table 18**

Row	Column	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R0	C0-2	Reserved for internal use							
R0	C3	0	0	0	0	0	M2	M1	M0
R0	C4	PT3	PT2	PT1	PT0	PU3	PU2	PU1	PU0
R0	C5	C4	MT2	MT1	MT0	MU3	MU2	MU1	MU0
R0	C6	C6	C5	HT1	HT0	HU3	HU2	HU1	HU0
R0	C7	C14	C13	C12	C11	C10	C9	C8	C7
R0	C8 – C39	P	D6	D5	D4	D3	D2	D1	D0
R1 – R24	C0 – C39	P	D6	D5	D4	D3	D2	D1	D0
R25	C0 – C19	X/27/0000 Flof links 1-4 and index link (the format of the record is the same as the format of the index page in packet 8/30). The header control bits C4, C5, C6 are already converted to the magazine number and set to 0.							
R25	C20 - C23	reserved for internal use							

## 1.7.3 Stored Format of Packet 8/30 (000x) Format 1

Table 19

Address = Block 0 / Row 5 / Byte 0

Column	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
C0	0	0	PAG_ER	0	0	M2	M1	M0
C1	PT3	PT2	PT1	PT0	PU3	PU2	PU1	PU0
C2	0	MT2	MT1	MT0	MU3	MU2	MU1	MU0
C3	0	0	HT1	HT0	HU3	HU2	HU1	HU0
C4	Network Identification (see byte 13 WST)							
C5	Network Identification (see byte 14 WST)							
C6	Time Offset Code (see byte 15 WST)							
C7	Modified Julian Date 1. Byte (see byte 16 WST)							
C8	Modified Julian Date 2. Byte (see byte 17 WST)							
C9	Modified Julian Date 3. Byte (see byte 18 WST)							
C10	Universal Time Coordinated 1. Byte (see byte 19 WST)							
C11	Universal Time Coordinated 2. Byte (see byte 20 WST)							
C12	Universal Time Coordinated 3. Byte (see byte 21 WST)							
C13	Short Program Label 1. Byte (see byte 22 WST)							
C14	Short Program Label 2. Byte (see byte 23 WST)							
C15	Short Program Label 3. Byte (see byte 24 WST)							
C16	Short Program Label 4. Byte (see byte 25 WST)							
C17 - C36	20 Bytes parity coded for "Status Display"							

**PAG\_ER:** 1: The initial teletext page number is not completely received.  
0: The initial teletext page number was received without any errors.

**M(i), PT(i), PU(i), MT(i), MU(i), HT(i), HU(i):**

The bits in column 0 - 3 contain the **absolute** magazine number, the page number and the page subcode of the initial teletext page.

1.7.4 Stored Format of Packet 8/30 (001x) Format 2 (PDC)

Table 20

Address = Block 0 / Row 5 / Byte 1

Column	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
C0	0	0	PAG_ER	0	0	M2	M1	M0
C1	PT3	PT2	PT1	PT0	PU3	PU2	PU1	PU0
C2	0	MT2	MT1	MT0	MU3	MU2	MU1	MU0
C3	0	0	HT1	HT0	HU3	HU2	HU1	HU0
C4	Reserved				Byte 13 of Format 2			
C5					Byte 14 of Format 2			
C6					Byte 15 of Format 2			
C7					Byte 16 of Format 2			
C8					Byte 17 of Format 2			
C9					Byte 18 of Format 2			
C10					Byte 19 of Format 2			
C11					Byte 20 of Format 2			
C12					Byte 21 of Format 2			
C13					Byte 22 of Format 2			
C14					Byte 23 of Format 2			
C15					Byte 24 of Format 2			
C16					Byte 25 of Format 2			
C17 - C36	20 Bytes parity coded for "Status Display" (see WST)							

**PAG\_ER:** 1: The initial teletext page number is not completely received.  
 0: The initial teletext page number was received without any errors.

**M(i), PT(i), PU(i), MT(i), MU(i), HT(i), HU(i):**

The bits in column 0 - 3 contain the **absolute** magazine number, the page number and the page subcode of the initial teletext page.

### 1.7.5 Format of TOP Title

As soon as the TOP mode is recognized by the **SDA 5273-3C**, the firmware will create a TOP title in row 24 of the current display chapter. The TOP title will be updated each time after the BTT is received. Pages which are not included in the AIT will be represented by their digit page number.

**Table 21**

Column Position	0 - 4	5 - 9	10 - 24	25 - 39
Description	Previous Page	Next Page	Next Block/Group	Next Block
Example	-	+	News	111
Colour	red	green	yellow	cyan

### 1.7.6 Format of Stored BTT

The BTT is hamming checked and compressed before storing so that it is only necessary to store 400 Bytes. Because the AITs are automatically requested, there is no need to store the page linking table and the basic TOP table list. The BTT is stored at a fixed position starting at block 1 / byte 5 / row 15/ col 5. Two pages are stored in one byte. The code of the lower page number is stored in the higher nibble, the next page in the least significant nibble. So in one row the codes of 80 pages are stored. Because of less storage capability for the possible AITs in parallel mode, TOP is not supported in parallel magazine mode.

#### Storage of 2 BTT Codes in One Byte

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BTT-code (page n)				BTT-code (page n + 1)			

#### Block 1 / Byte 5 / Row 25

Col	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
5	0	0	0	0	0	0	0	PBR
6	0	0	0	0	0	MAG2	MAG1	MAG0
7	PT3	PT2	PT1	PT0	PU3	PU2	PU1	PU0
8	C4	MT2	MT1	MT0	MU3	MU2	MU1	MU0
9	C6	C5	HT1	HT0	HU3	HU2	HU1	HU0
10	C14	C13	C12	C11	C10	C9	C8	C7



**1.8 Wide Screen Signaling (WSS), Video Program System (VPS)**

The **SDA 5273-3C** has an integrated single data line module for real-time WSS and VPS processing. If this module is enabled, the internal PU takes over the control of the M3I-Bus Register 98 SINGLE\_DATA\_LINE. The single data line module switches automatically between line 16 (VPS) and line 23 (WSS) in one field. The WSS data are error checked and written to a buffer in the internal memory. Their actual values can be read at any time. The received data are biphase decoded and only written if the whole WSS line is received without any errors. Clock-run-in and framing-code are not stored. The threshold when the data should be indicated as valid can be controlled by the setup parameter WSS\_CNT(7:0). This input parameter sets the threshold how often the WSS data have to be received without any errors in sequence before the data will be stored and the REC\_WSS bit will be set in the return parameters. To enable the WSS/VPS module set the bit ENA\_LINE16/23 in the setup parameters before giving the command *RESET\_ACQ*. Initialize the M3I-Register EXTRA FRAMINGCODE WINDOW to B4<sub>H</sub>.

**1.8.1 Wide Screen Signaling (WSS)**

**Return Parameter Block 0 / Byte 3 / Row 5 / Col 13**

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
WSS_7	WSS_6	WSS_5	WSS_4	WSS_3	WSS_2	WSS_1	WSS_0

**Return Parameter Block 0 / Byte 3 / Row 5 / Col 14**

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0	0	WSS_13	WSS_12	WSS_11	WSS_10	WSS_9	WSS_8

**WSS(13:0)** Data bits of the transmitted WSS information. Refer to the WSS specification [4].

- WSS(3:0) → aspect ratio
- WSS(7:4) → enhanced service
- WSS(10:8) → subtitles
- WSS(13:11) → reserved

**Return Parameter Block 0 / Byte 3 / Row 5 / Col 2**

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
SUBPAGE_MODE	REC_WSS	LINE16_VPS	0	0	REC_VPS	REC_8_30_2	REC_8_30_1

The REC\_WSS status bit is an indicator for the reception of a valid WSS packet. Before reading WSS data, set the REC\_WSS status bit to 0. Use a polling technique until the REC\_WSS status bit is 1 again.

**1.8.2 Video Program System (VPS)**

**Table 22**  
**Return Parameter Block 0 / Byte 3 / Row 5 / Col 8 - 12**

Column Position	VPS Word	VPS Data Word
8	5	sound data special identification
9	11	VPS extra information
10	12	VPS extra information
11	13	VPS extra information
12	14	VPS extra information

**Bit-Resolution for the VPS Data Words**

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0	0	0	0	VPS_3	VPS_2	VPS_1	VPS_0

The VPS data are error checked and written to a buffer in the internal memory. Their current values can be read anytime. The received data are biphasic decoded and only written if the whole VPS line is received without error. Clock-run-in and framing-code are not stored. For further information about VPS refer to the VPS Specification [5].

**Return Parameter Block 0 / Byte 3 / Row 5 / Col 2**

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
SUBPAGE_MODE	REC_WSS	LINE16_VPS	0	0	<b>REC_VPS</b>	REC_8_30_2	REC_8_30_1

The VPS status bit is an indicator for the reception of a valid VPS packet. Before reading VPS data, set the VPS status bit to 0. Use a polling technique until the VPS status bit is 1 again.

## 1.9 Teletext Identification

The **COMPACTTEXT** provides an internal module to recognize whether the current TV channel transmits teletext or not.

This module delivers a bit (TEXT\_INT) in the return parameters which indicates this information. To activate this function, the following input parameters must be set:

### Setup Parameter NU\_TE\_FR\_(7:0)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0	0	1	1	0	0	1	0

These bits define the number of frames which have to be pass without text reception.

### Setup Parameter NU\_VALID\_HEAD(7:0)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0	0	0	0	0	1	0	1

Number of valid headers. This parameter is used together with NU\_TE\_FR\_(7:0) to define a criterion for the text identification modul. With the NU\_TE\_FR\_(7:0) you define the number of frames with text information and with NU\_VALID\_HEAD(7:0) you define the number of headers within these frames. All hamming coded bytes of the detected headers must be free of errors before a header will be interpreted as valid. This monitoring of the text identification is active all the time.

### 1.9.1 Teletext Identification in Line 16

The **COMPACTTEXT** hardware has two paths for data reception. One path is for the teletext reception and the other one for the reception of the single data line services. For both data paths a separate framingcode is defined. The switch between the two branches will be done via the M3I-Bus register 98 SINGLE\_DATA\_LINE.

Example: The M3I-Bus register 98 is set to line 16. An incoming line 16 will only be processed in the single data line path, not in the teletext path. Be careful that with this setting, if teletext information is transmitted in line 16, this data will never be recognized by the text decoder.

To overcome this situation an extra function is implemented in **COMPACTTEXT** to check first if this channel provides VPS information or not.

With a channel change (command *RESET\_ACQ* must be given), the single data line will be set to line 16 for a given time span. After this time, a decision will be made depending on the return parameter bit LINE16\_VPS. If this bit is set to 1 the single data line will further be used to receive VPS info in line 16. If this bit is still 0 the single data line will not be loaded with the value 16<sub>d</sub> anymore because of possible teletext transmission in this line.

Delta Specification

This function needs the setup parameter VPS\_WAIT(7:0) to define the wait time and can be activated by the setup parameter bit ENA\_LINE16/23. Both parameters must be set before sending the command *RESET\_ACQ*.

**Setup Parameter VPS\_WAIT(7:0)**

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0	1	1	0	1	1	1	1

**1.10 Signal Quality Status Bits**

The **COMPACTTEXT** provides some signal quality bits which can be read any time from the internal memory. These bits will be updated by the internal firmware several times per field.

**Signal Quality Status Bits\_0 / Block 0 / Byte 0 / Row 3 / Col 34**

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
S525	V_FINE	SYNC_ERR_3	SYNC_ERR_2	SYNC_ERR_1	SYNC_ERR_0	COI	ACQ_EN

**Signal Quality Status Bits\_1 / Block 0 / Byte 1 / Row 3 / Col 34**

bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
nu	nu	nu	nu	nu	nu	nu	PDF_OK

**ACQ\_EN:** Acquisition sync signal quality reference.  
 1: HPLL is locked very excellent. Switching on the acquisition by the PU or external controller is useful.  
 0: HPLL lock condition is bad. Switching on the acquisition by the PU or external controller is not recommended.

**COI:** Coincidence indicator.  
 1: HPLL phase difference is less then 4% of line period. Line period does not need to be a TV line standard.  
 0: HPLL is not locked. Pull in range is  $\pm 7\%$  of 15625 Hz line frequency.

**SYNC\_ERR(3:0):** Horizontal sync distortion measurement. The measurement is done by counting the ripple during H-sync pulse.  
 very good signal  $1 < \text{SYNC\_ERR} \leq 15$  bad signal

Delta Specification

- V\_FINE:** V-sync detection quality fine.  
 1: Detected V-sync is inside the A(D)VFW\_WDTH window.  
 0: Detected V-sync is outside the A(D)VFW\_WDTH window.  
 The following table shows the interpretation of the 625/525 line detection; bits S525 and V\_FINE.  
 (A(D)VFW\_WDTH refer to M3I-Bus register [2])
- S525:** 525 line sync signal. This bit indicates 625 or 525 line CVBS signal. It is set by the timing logic.  
 1: The timing logic has detected a CVBS signal closer to 525 lines.  
 0: The timing logic has detected a CVBS signal closer to 625 lines.  
 Referenced bit V\_FINE
- PDF\_OK:** Display PLL locked.  
 1: Display PLL is locked.  
 0: Display PLL is not locked.

Table 23

V_FINE	S525	Interpretation
0	0	> 287 lines; 50 Hz unsure
0	1	≤ 287 lines; 60 Hz unsure
1	0	625 lines standard; 50 Hz sure
1	1	525 lines standard; 60 Hz sure

1.11 Firmware Refresh for the External DRAM

The **COMPACTTEXT** now supports a firmware refresh for an external DRAM. By setting the following input parameters the external refresh can be switched on respectively off. External DRAMs up to 16 Mbit will be supported.

Block 0 / Byte 0 / Row 3 / Col 33

REFRESH_7	REFRESH_6	REFRESH_5	REFRESH_4	REFRESH_3	REFRESH_2	REFRESH_1	REFRESH_0
-----------	-----------	-----------	-----------	-----------	-----------	-----------	-----------

- REFRESH(7:0):** 00<sub>H</sub>: refresh off  
 35<sub>H</sub>: refresh on

**NB:** If no external DRAM is connected to the COMPACTTEXT, it is recommended to switch off the firmware refresh.

### 1.12 Binary Address Port

In addition to the existing M3I/I2C-Bus dataports\_0/1, **COMPACTTEXT** has a new dataport\_2. This dataport uses only the binary addressing for the internal or external DRAM. This port can be used with the full speed of 1 MHz SCL frequency for the M3I-Bus. The dataport\_2 is used together with the address\_pointer\_1 (refer to M3I-Bus register description [2]).

#### ADDRESS\_POINTER\_1\_2 / R56

EXT_MEM=0	0	0	1	BYT_5	BYT_4	BYT_3	BYT_2
EXT_MEM=1	0	CHP_10	CHP_9	CHP_8	CHP_7	CHP_6	CHP_5

#### ADDRESS\_POINTER\_1\_1 / R57

BYT_1	BYT_0	BLK_2	BLK_1	BLK_0	ROW_4	ROW_3	ROW_2
CHP_4	CHP_3	CHP_2	CHP_1	CHP_0			

#### ADDRESS\_POINTER\_1\_0 / R58

ROW_1	ROW_0	COL_5	COL_4	COL_3	COL_2	COL_1	COL_0
-------	-------	-------	-------	-------	-------	-------	-------

(for bit level description refer to M3I-Bus register description [2])

#### DATAPORT\_2 / R67

DATA_P_27	DATA_P_26	DATA_P_25	DATA_P_24v	DATA_P_23	DATA_P_22	DATA_P_21	DATA_P_20
-----------	-----------	-----------	------------	-----------	-----------	-----------	-----------

#### DATA\_P\_(27:20):

These bits are the data to transfer to or from the selected memory address. Any write or read to or from dataport\_2 activates the binary autoincrement function in the address pointer 1.

## 2 Application Notes

### 2.1 Version Code Overview

Version code overview for

- Megatext SDA 5273 / -2
- MEGATEXT PLUS SDA 5275 / -2 / -3
- Compacttext SDA 5273C / -2C / -3C

In the internal memory one location is reserved for the version code. This version code can be used to distinguish the above mentioned ICs.

#### IC Differentiation

Memory Address	SDA 5273/-2	SDA 5275/-2/-3	SDA 5273C/-2C/-3C
Block_0 Byte_4 Row_7 Column_23	00 <sub>H</sub>	01 <sub>H</sub>	02 <sub>H</sub>

#### Version Differentiation

Memory Address	SDA5275/-2/-3		SDA 5273C/-2C/-3C	
	Version	Version Code	Version	Version Code
Block_0	A23	22 <sub>H</sub>	C29	11 <sub>H</sub>
Byte_3	B11	22 <sub>H</sub>	C129	12 <sub>H</sub>
Row_7	B12	22 <sub>H</sub>	C229	12 <sub>H</sub>
Column_23	C01-11	23 <sub>H</sub>	B50-13	14 <sub>H</sub>
	C01-12	23 <sub>H</sub>	C50-11	14 <sub>H</sub>
	C02-22	24 <sub>H</sub>	C50-12	14 <sub>H</sub>
			C55-12	15 <sub>H</sub>
			C55-22	15 <sub>H</sub>
			B51-13	16 <sub>H</sub>

#### Version Differentiation

Version	SDA 5273/-2					
	Memory Address					
	mci0_5	mci0_4	mci0_3	mci0_2	mci0_1	mci0_0
C22	32 <sub>H</sub>	35 <sub>H</sub>	30 <sub>H</sub>	38 <sub>H</sub>	39 <sub>H</sub>	33 <sub>H</sub>
C24	31 <sub>H</sub>	34 <sub>H</sub>	30 <sub>H</sub>	33 <sub>H</sub>	39 <sub>H</sub>	34 <sub>H</sub>

**Version Differentiation**

Version	SDA 5273/-2					
	Memory Address					
	mci0_5	mci0_4	mci0_3	mci0_2	mci0_1	mci0_0
C26	30 <sub>H</sub>	39 <sub>H</sub>	31 <sub>H</sub>	37 <sub>H</sub>	39 <sub>H</sub>	34 <sub>H</sub>
C134	33 <sub>H</sub>	30 <sub>H</sub>	30 <sub>H</sub>	35 <sub>H</sub>	39 <sub>H</sub>	35 <sub>H</sub>
B30-13	30 <sub>H</sub>	37 <sub>H</sub>	30 <sub>H</sub>	33 <sub>H</sub>	39 <sub>H</sub>	37 <sub>H</sub>
C30-11	30 <sub>H</sub>	37 <sub>H</sub>	30 <sub>H</sub>	33 <sub>H</sub>	39 <sub>H</sub>	37 <sub>H</sub>
C30-12	30 <sub>H</sub>	37 <sub>H</sub>	30 <sub>H</sub>	33 <sub>H</sub>	39 <sub>H</sub>	37 <sub>H</sub>

**Hint**                      mci0\_5 to mci0\_0 are equal to M3L-Bus registers reg8 to reg13. The version code in these M3L-Bus registers is valid after Megatext is reset until the first mci command is given.

**2.2 Example for COMPACTTEXT Initialization**

Follow the initialization example in the given sequence.

**Table 1**  
**M3L\_Register (Reference Volume1 of SDA 5273)**

M3I Register	Register Description	Value (hex)	Comment
R1	Pb_Length_1	00	
R2	Pb_Length_0	11	
R3	Pb_Adr_2	58	
R4	Pb_Adr_1	12	
R5	Pb_Adr_0	00	
R108	Acquisition_Timing_1	00	
R109	Acquisition_Timing_0	10	
R112	System_Clock_Control	00	
R114	Display_PLL_Control	08	
R113	Sync_Source_Selection	03	
R115	Black_Level_Clamp	BF	
R116	Display_Timing	00	
R117	V_Delay_Setting	00	
R81	Slicer_Control	26	



## Application Notes

**Table 1**  
**M3L\_Register (Reference Volume1 of SDA 5273) (cont'd)**

M3I Register	Register Description	Value (hex)	Comment
R82	Output_Pin_Control	07	
R83	RGB_Control	C1	
R85	Display_VCO	04	
R88	IAT_2	7C	
R89	IAT_1	07	
R90	IAT_0	C0	
R96	DEW_Start_Line	06	
R97	DEW_End_Line	17	
R98	Single_Data_Line	10	
R99	TTX_Framing_Window	62	
R100	Extra_Framing_Window	B4	

**Table 2**  
**Display\_Register (Reference Volume 1 of SDA 5273)**

Bits	Value (hex)					
	47...40	39...32	31...24	23...16	15...8	7...0
Sync_Delay_Word	00	00	00	00	0C	00
Display_Position_Word	00	00	18	E8	6C	00
Termination_Display_Word	00	20	00	01	0F	20
Outer_Screen_Mask_Register	FF	FF	FF	7F	C0	00
Inner_Screen_Mask_Register_1	FF	00	00	00	C0	00
Inner_Screen_Display_Word_1	00	00	00	00	C0	00
Inner_Screen_Mask_Register_0	FF	00	00	00	00	00
Box_Mask_Register_1	FF	00	00	00	00	00
Box_Mask_Register_0	FF	00	00	00	00	00

**Table 3**  
**User Definable Characters (Block 0 / Row 2)**

UDC	Column / Bit	Value (hex)					
		47...40	39...32	31...24	23...16	15...8	7...0
1	27	-	-	-	0C	00	3E

**Table 3**  
**User Definable Characters (Block 0 / Row 2)**

UDC	Column / Bit	Value (hex)					
		47...40	39...32	31...24	23...16	15...8	7...0
2	27	06	00	50	-	-	-
3	28	-	-	-	06	00	20
4	28	06	00	20	-	-	-
5	29	-	-	-	06	00	20
6	29	0C	00	3C	-	-	-
7	30	-	-	-	0C	00	3C
8	30	0C	00	3C	-	-	-

**Table 4**  
**Setup\_Parameter (Block 0 / Byte 4 / Row 5)**

Column	Value (hex)	Comment
0	C7	see chapter 1.4
1	F8	
2	58	
3	38	
4	18	
5	00	
6	20	
7	7F	
8	20	
9	7F	
10	06	
11	00	
12	32	
13	00	
14	00	
15	00	
16	04	
17	00	
18	00	
19	00	
20	00	
21	00	
22	00	
23	00	
24	00	
25	10	
26	00	
27	00	
28	00	

**Table 4**  
**Setup\_Parameter (Block 0 / Byte 4 / Row 5) (cont'd)**

<b>Column</b>	<b>Value (hex)</b>	<b>Comment</b>
29	03	
30	05	
31	01	
32	00	
33	6F	

**Table 5**  
**COMPACTTEXT Commands**

<b>RESET_ACQ</b>
<b>TEXT_MODE</b>

After that initialization you should have the page\_100 on screen.

## 2.3 How to Initialize COMPACTTEXT for Russian Market

### Initialize the User Set Table

**Table 6**  
**Setup\_Parameter (Block 0 / Byte 4 / Row 5)**

Column	Value (dec)
⋮	⋮
17	1
18	12
19	8
20	6
21	3
22	13
23	15
24	4
⋮	⋮

### Select the Characterset 63

**Table 7**  
**Setup\_Parameter (Block 0 / Byte 4 / Row 5)**

Column	Value (dec)
⋮	⋮
10	63
⋮	⋮

**Initialize the Twist Language**

**Table 8**  
**Setup\_Parameter (Block 0 / Byte 4 / Row 5)**

Column	Value (dec)
⋮	⋮
11	2C
⋮	⋮
26	01
⋮	⋮

**Downloading the Cyrillic Characterset for COMPACTTEXT into the PCS Memory**

Please contact your Siemens representative to get the database of the Cyrillic character set for **COMPACTTEXT**.

**Downloading the p26\_character\_tab for COMPACTTEXT**

Please contact your Siemens representative to get the database of the p26 character tab for **COMPACTTEXT**.

**Enabling the Twist Feature**

Set the TWIST\_MODE bit in the following register to 1 without modifying the rest of the bits **after the command RESET\_ACQ**.

**Block 0 / Row 0 / Byte 4 / Col 17**

x	x	x	x	TWIST_MODE	x	x	x
---	---	---	---	------------	---	---	---

**2.4 How to Initialize COMPACTTEXT for Thai Language**

**Downloading the Thai Characterset for COMPACTTEXT into the PCS Memory**

Please contact your Siemens representative to get the database of the Thai character set for **COMPACTTEXT**.

**Initialize the G0-window for the G0 Thai Characterset**

**Table 9  
Setup\_Parameter (Block 0 / Byte 4 / Row 5)**

Column	Value (dec)
⋮	⋮
6	20
7	7F
⋮	⋮

**Initialize the Twist Language**

**Table 10  
Setup\_Parameter (Block 0 / Byte 4 / Row 5)**

Column	Value (dec)
⋮	⋮
11	01
⋮	⋮

**Enable Thai Language and Twist Mode**

Set the THAI\_ENA bit and TWIST\_MODE bit in the following register to 1, without changing the rest of the bits, **after the command RESET\_ACQ**.

**Block 0 / Row 0 / Byte 4 / Col 17**

THAI_ENA	x	x	x	TWIST_MODE	x	x	x
----------	---	---	---	------------	---	---	---

**2.5 Pages to be Requested**

Overview of the pages which are currently stored in the memory.

**Table 11**  
**Block 0 / Row 7 / Col\_(0:9)**

NOT_USED	PRO- TECTED	x	x	x	M2 <sub>0</sub>	M1 <sub>0</sub>	M0 <sub>0</sub>	byte 5
PT3 <sub>0</sub>	PT2 <sub>0</sub>	PT1 <sub>0</sub>	PT0 <sub>0</sub>	PU3 <sub>0</sub>	PU2 <sub>0</sub>	PU1 <sub>0</sub>	PU0 <sub>0</sub>	byte 4
0	MT2 <sub>0</sub>	MT1 <sub>0</sub>	MT0 <sub>0</sub>	MU3 <sub>0</sub>	MU2 <sub>0</sub>	MU1 <sub>0</sub>	MU0 <sub>0</sub>	byte 3
0	0	HT1 <sub>0</sub>	HT0 <sub>0</sub>	HU3 <sub>0</sub>	HU2 <sub>0</sub>	HU1 <sub>0</sub>	HU0 <sub>0</sub>	byte 2
x	x	x	x	x	x	x	x	byte 1
TOP_PAGE	LIST_PAGE	DIS_PAGE	LIST_1	LIST_0	SUBPAGE	CHECK_1	CHECK_0	byte 0

- M(2:0):** Magazine number
- PT(3:0):** Page number tens
- PU(3:0):** Page number units
- MU(3:0):** Subpage minute units
- MT(2:0):** Subpage minute tens
- HU(3:0):** Subpage hours units
- HT(1:0):** Subpage hour tens
- CHECK(1:0):** The check bits indicate the checks to be done by acquisition.

**Table 12**

CHECK_1	CHECK_0	Mode
0	0	Normal page check: Header bytes 6 to 13 are 1-byte-hamming checked. All other bytes of the page are parity checked.
0	1	Not defined
1	0	1 byte hamming check (TOP page): Header bytes 6 to 13 are 1-byte-hamming checked. Header bytes 14 to 45 are parity checked. All bytes in packet 1 - 22 are 1-byte-hamming checked.
1	1	Mixed 1 byte hamming check: Header bytes 6 to 13 are 1-byte-hamming checked. Header bytes 14 to 45 are parity checked. Bytes 0 - 7 and bytes 20 - 27 in packet 1 - 22 are 1-byte-hamming checked. Bytes 8 - 19 and bytes 28 - 39 in packet 1 - 22 are parity checked.



---

**Application Notes**

**SUBPAGE:** This page will be requested in subpage mode

**LIST(1:0):** List page number (see **Table 13**)

**Table 13**

<b>LIST_1</b>	<b>LIST_0</b>	<b>List page No.</b>
0	0	1 (red)
0	1	2 (green)
1	0	3 (yellow)
1	1	4 (cyan)

**TOP\_PAGE:** TOP page indicator

**LIST\_PAGE:** List page indicator

**DIS\_PAGE:** Display page indicator

**NOT\_USED:** This bit shows the table elements which are not used;  
related register: Memory Allocation Register IAT(2:0)

**PROTECTED:** Indicates a protected page (list, TOP or display page).

## 2.6 Digit Input

An incomplete digit input can be erased by the external controller in the following way:

- Fetch the current display page number from the return parameter.
- Overwrite the incomplete digit input in the display memory bl\_2/row\_0/col\_2,3,4 with the display page number.
- Reset the digit counter in bl\_0/by\_1/row\_3/col\_16 to 0.

**3 Abbreviations**

ACQ:	Acquisition
AIT:	Additional Information Table
BDM:	Basic Display Memory of the COMPACTTEXT
BTT:	Basic Top Table
CDW:	Character Display Word
DRCS:	Dynamically Redefinable Character Set
FLOF:	Full Level One Feature
NVM:	Non Volatile Memory
PCS:	Programmable Character Set
PDC:	Program Delivery Control
S/P-C:	Serial/Parallel Conversion
TOP:	Table Of Pages
TV:	Television (Set)
UDC:	User Definable Characters in row0 of BDM
VBI:	Vertical Blanking Interval
VPS:	Video Program System
WSS:	Wide Screen Signaling
WST:	World System Teletext specification

**4       References**

- [1]                   IRT - Institut für Rundfunk-Technik: "TOP System for Teletext", Germany
- [2]                   MEGATEXT<sup>®</sup> documentation Volume 1
- [3]                   Enhanced Teletext Specification, European Telecommunications Standards Institute ETSI
- [4]                   Television Systems; 625-Line Television Wide Screen Signalling, European Telecommunications Standards Institute ETSI
- [5]                   IRT - Institut für Rundfunk-Technik: "Video-Programm-System", Germany