

#### **Product Features**

- 750 1000 MHz bandwidth
- 30 dB Attenuation Range
- +40 dBm Output IP3
- +21 dBm P1dB
- Constant IP3 & P1dB over attenuation range
- Single voltage supply
- 6x6 mm 28-pin QFN package
- MTTF > 100 years

## **Applications**

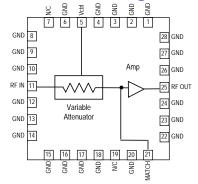
• Xmit & Rcv AGC circuitry for mobile infrastructure

#### **Product Description**

The VG101 is a cellular-band high dynamic range variable gain amplifier (VGA) packaged in a 6x6 mm surfacemount package. The +21 dBm output compression point and +40 dBm output intercept point of the amplifier are maintained over the entire attenuation range, making the VG101 ideal for use in transmitter and receiver AGC circuits and as a variable gain stage following an LNA in high dynamic range receiver front ends.

Superior thermal design allows the product to have a minimum MTTF rating of 100 years at a mounting temperature of +85° C. All devices are 100% RF & DC tested and packaged on tape and reel for automated surfacemount assembly.

## **Functional Diagram**



Function	Pin No
Gain Control	5
No Connect	7, 19
RF Input	11
Interstage Match	21
RF Output / DC bias	25
Ground	All other pins Backside copper

## **Specifications**

Parameter	Units	Min	Тур	Max	Conditions
Frequency Range	MHz	750	900	1000	See note 1
Gain at min. attenuation	dB	15	16		
Input Return Loss	dB		10		
Output Return Loss	dB		10		
Output P1dB	dBm		+21		
Output IP3	dBm	+37	+40		See note 2
Noise Figure at min. attenuation	dB		3.8		$V_{CTRL} = 0 V$
Gain Variation Range	dB		30		See note 3
Gain Variation Control Voltage, V <sub>CTRL</sub>	V	0		4.5	
Group Delay	ns		1		Frequency = 800 MHz
Supply Voltage	V		+5		
Operating Amplifier Current Range	mA	120	150	180	Pin 25
Gain Control Pin Current Range	mA	0		25	Pin 5 draws no current at maximum gain
Thermal Resistance	°C / W			59	
Junction Temperature	°C			160	See note 4

Test conditions unless otherwise noted.

# **Absolute Maximum Rating**

Parameter	Rating
Operating Case Temperature	-40 to +85 °C
Storage Temperature	-55 to +125 °C
Amplifier Supply Voltage (pin 25)	+6 V
Attenuation Control Voltage	+5.5 V
RF Input Power (continuous)	+12 dBm
Junction Temperature	+220° C

## Operation of this device above any of these parameters may cause permanent damage.

# **Ordering Information**

Part No.	Description
VG101	Cellular-band Variable Gain Amplifier
VG101-PCB	Fully Assembled Application Board

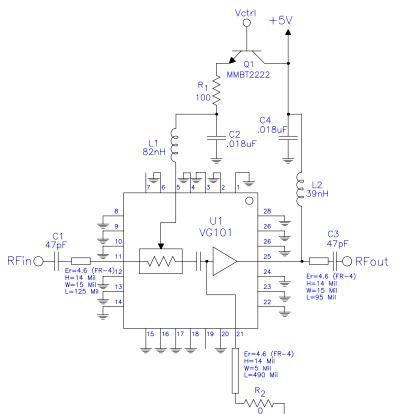
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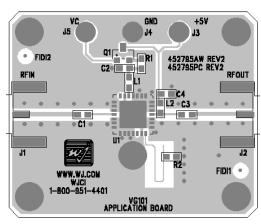
<sup>1.</sup> T = 25°C, Vdd = +5 V, Frequency = 900 MHz in an application circuit.
2. 3OIP measured with two tones at an output power of +10 dBm/tone separated by 10 MHz. The suppression on the largest IM3 product is used to calculate the 3OIP using a 2:1 rule.
3. The gain variation range is measured with 15 mA of current on gain control pin 5.

<sup>4.</sup> The junction temperature ensures a minimum MTBF rating of 1 million hours of usage.



## Application Circuit: 750 - 1000 MHz (VG101-PCB)



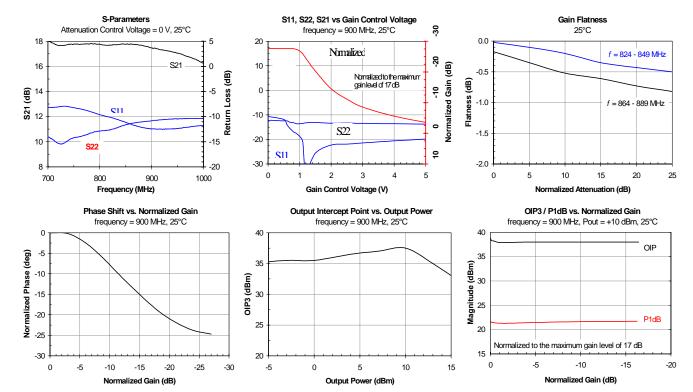


Circuit Board Material: .014" FR-4, 4 layers, .062" total thickness

- Pin 21 needs to be connected to ground through a high impedance transmission line as shown for proper interstage matching. The position of R2 can be varied for optimal performance.
- The amplifier is biased through Pin 25 and should be connected directly into a voltage regulator.
- · Distances are shown from the edge-to-edge for the land pattern.

#### **Bill of Materials**

Ref. Des.	Description	Size
C1, C3	47 pF Chip Capacitor	0603
C2, C4	0.01 μF Chip Capacitor	0603
L1	82 nH Chip Inductor	0603
L2	39 nH Chip Inductor	0603
R1	100 Ω Chip Resistor	0603
Q1	MMBT2222 Motorola Transistor	SOT-23
U1	VG101 Variable Gain Amplifier	QFN 6x6



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## **Outline Drawing**

# 2x | .10 | 6.00 | A | B | TERMINAL #1 | 6.00 | A | C | C | C | C | VG101 | 2x | .10 | C | C | C | C | 2x | .10 | C | C | C | C | C | 2x | .10 | C | C | C | C | 2x | .10 | C | C | C | C | 2x | .10 | C | C | C | 2x | .10 | C | C | C | 2x | .10 | C | C | C | 2x | .10 | C | C | C | 2x | .10 | C | C | C | 2x | .10 | .10 | .10 | 2x | .10 | .1

// .10 C

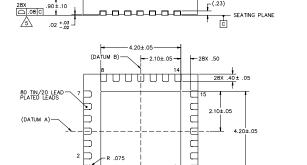
TERMINAL IDENTIFIER

◮

.65

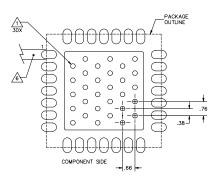
#### NOTES

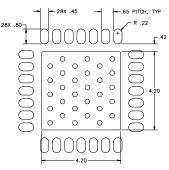
- . EXCEPT WHERE NOTED, THIS PART OUTLINE CONFORMS TO JEDEC STANDARD MO-220, ISSUE E (VARIATION VJUC) FOR THERMALLY ENHANCED PLASTIC VERY THIN FINE PITCH QUAD FLAT NO LEAD PACKAGE (QFN).
- DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.4M-1994.
- 3. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
- THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION CONFORM TO JESD 95-1 SPP-012.
- COPLANARITY APPLIES TO THE EXPOSED GROUND/THERMAL PAD AS WELL AS THE TERMINALS.
- ALPHA-NUMERIC LOT CODE.



-6X .65 (3.90)

# **Mounting Configuration / Land Pattern**





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#### NOTES:

GROUND/THERMAL VIAS ARE CRITICAL FOR THE PROPER PERFORMANC OF THIS DEVICE. VIAS SHOULD USE A .35mm (#80/.0135") DIAMETER DRILL AND HAVE A FINAL, PLATED THRU DIAMETER OF .25mm (.010").

- ADD AS MUCH COPPER AS POSSIBLE TO INNER AND OUTER LAYERS NEAR THE PART TO ENSURE OPTIMAL THERMAL PERFORMANCE.
- TO ENSURE RELIABLE OPERATION, DEVICE GROUND PADDLE-TO-GROUND PAD SOLDER JOINT IS CRITICAL.
- ADD MOUNTING SCREWS NEAR THE PART TO FASTEN THE BOARD TO A HEATSINK. ENSURE THAT THE GROUND/THERMAL VIA REGION CONTACTS THE HEATSINK
- DO NOT PUT SOLDER MASK ON THE BACK SIDE OF THE POBOARD IN THE REGION WHERE THE BOARD CONTACTS THE HEATSINK.
- RF TRACE WIDTH DEPENDS UPON THE PC BOARD MATERIAL AND CONSTRUCTION.
- 7. USE 1 OZ. COPPER MINIMUM.
- 8. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.

#### **Product Marking**

The component will be lasermarked with a "VG101" designator with a four-digit alphanumeric lot code on the top surface of the package. Tape and reel specifications for this part will be located on the website in the "Application Notes" section.

#### **ESD / MSL Information**



ESD Classification: Class 1B Value: Passes 600 V

Test: Human Body Model (HBM) Standard: JEDEC Standard JESD22-A114

ESD Classification: Class IV Value: Passes 1000 V

Test: Charged Device Model (CDM) Standard: JEDEC Standard JESD22-C101

MSL Rating: Level 1 at +250 °C convection reflow Standard: JEDEC Standard J-STD-020B

## **Functional Pin Layout**

Pin	FUNCTION	Pin	FUNCTION
1	GND	15	GND
2	GND	16	GND
3	GND	17	GND
4	GND	18	GND
5	Gain control pin	19	N/C
6	GND	20	GND
7	N/C	21	Interstage Match
8	GND	22	GND
9	GND	23	GND
10	GND	24	GND
11	RF Input	25	RF Output / Bias
12	GND	26	GND
13	GND	27	GND
14	GND	28	GND