

## 82S105 (PLS105) Field-Programmable Logic Sequencer (16 × 48 × 8)

Signetics Programmable Logic

### Product Specification

#### Military Application Specific Products

#### DESCRIPTION

The 82S105 is a bipolar programmable state machine of the Mealy type. It contains logic AND-OR gate arrays with user programmable connections which control the inputs of on-chip State and Output Registers. These consist respectively of 6  $Q_P$ , and 8  $Q_F$  edge-triggered, clocked S/R flip-flops, with an asynchronous Preset option. All flip-flops are unconditionally preset to "1" during power turn-on.

The AND array combines 16 external inputs,  $I_{0-15}$ , with six internal inputs,  $P_{0-5}$ , fed back from the State Register to form up to 48 transition terms (AND terms).

All transition terms can include True, False, or Don't Care states of the controlling variables, and are merged in the OR array to issue next-state and next-output commands to their respective registers on the Low-to-High transition of the Clock pulse. Both True and Complement transition terms can be generated by optional use of the internal variable (C) from the Complement Array. Also, if desired, the

Preset input can be converted to  $\overline{\text{Output Enable}}$  function, as an additional user-programmable option.

#### FEATURES

- Field-programmable (Ni-Cr link)
- 16 input variables
- 8 output functions
- 48 transition terms
- 6-bit State Register
- 8-bit Output Register
- Transition Complement Array
- Positive edge-trigger clock
- Programmable asynchronous preset or Output Enable
- Power-on preset to all "1" of internal registers
- $f_{\text{MAX}} = 10.5\text{MHz}$
- 650mW power dissipation (typical)
- TTL compatible

- Single +5V supply
- 3-state outputs

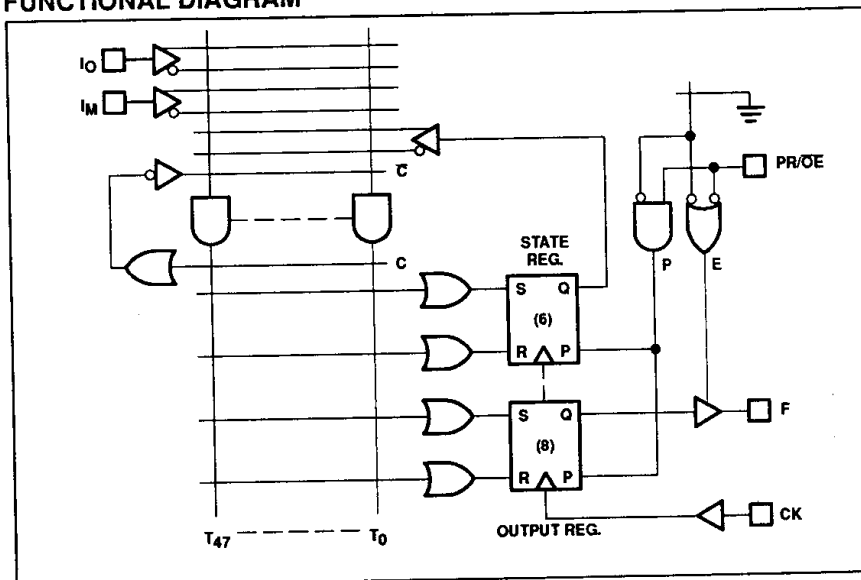
#### APPLICATIONS

- Interface protocols
- Sequence detectors
- Peripheral controllers
- Timing generators
- Sequential circuits
- Elevator controllers
- Security locking systems
- Counters
- Shift registers

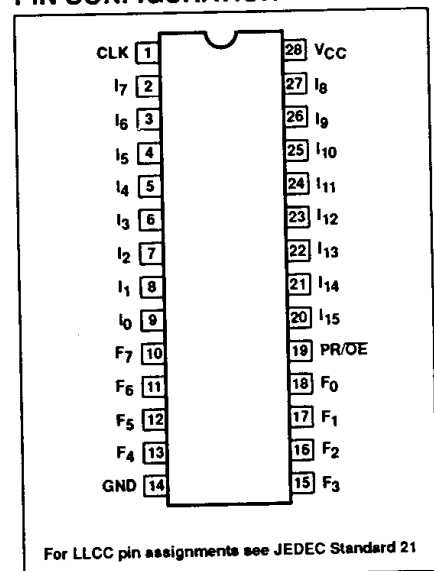
#### ORDERING INFORMATION

| DESCRIPTION                       | ORDER CODE |
|-----------------------------------|------------|
| 28-Pin Ceramic DIP<br>600mil-wide | 82S105/BXA |
| 28-Pin CLCC                       | 82S105/B3A |
| 28-Pin Ceramic FlatPack           | 82S105/BYA |

#### FUNCTIONAL DIAGRAM



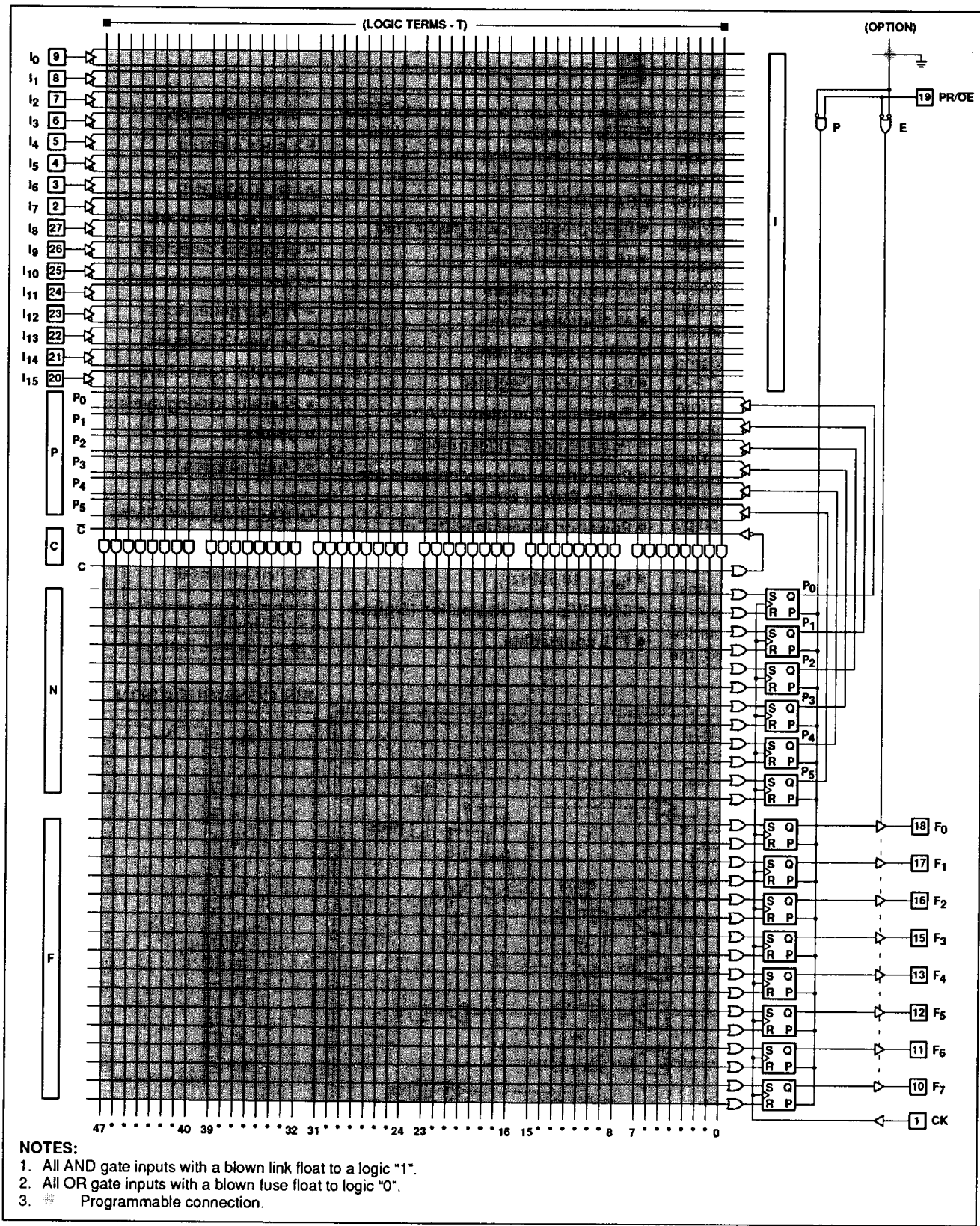
#### PIN CONFIGURATION



# Field-Programmable Logic Sequencer (16 × 48 × 8)

82S105

## FPLS LOGIC DIAGRAM



## Field-Programmable Logic Sequencer (16 × 48 × 8)

82S105

## PIN DESCRIPTION

| PIN NO.            | SYMBOL            | NAME AND FUNCTION   | POLARITY                              |
|--------------------|-------------------|---|---------------------------------------|
| 1                  | CK                | <b>Clock:</b> The Clock input to the State and Output Registers. A Low-to-High transition on this line is necessary to update the contents of both registers.   | Active-High                           |
| 2 - 8<br>20 - 27   | I <sub>1-15</sub> | <b>Logic Inputs:</b> The 15 external inputs to the AND array used to program jump conditions between machine states, as determined by a given logic sequence.   | Active-High/Low                       |
| 9                  | I <sub>0</sub>    | <b>Logic/Diagnostic Input:</b> A 16th external logic input to the AND array, as above, when exercised with standard TTL levels. When I <sub>0</sub> is held at +10V, device outputs F <sub>0-5</sub> reflect the contents of State Register bits P <sub>0-5</sub> . The contents of each Output Register remains unaltered.   | Active-High/Low                       |
| 10 - 13<br>15 - 18 | F <sub>0-7</sub>  | <b>Logic/Diagnostic Outputs:</b> Eight device outputs which normally reflect the contents of Output Register bits Q <sub>0-7</sub> , when enabled. When I <sub>0</sub> is held at +10V, F <sub>0-5</sub> = (P <sub>0-5</sub> ), and F <sub>6,7</sub> = Logic "1".   | Active-High                           |
| 19                 | PR/OE             | <b>Preset or Output Enable Input:</b> A user programmable function: <ul style="list-style-type: none"> <li><b>Preset:</b> Provides an asynchronous preset to logic "1" of all State and Output Register bits. Preset overrides Clock, and when held High, clocking is inhibited and F<sub>0-7</sub> are High. Normal clocking resumes with the first full clock pulse following a High-to-Low clock transition, after Preset goes Low.</li> <li><b>Output Enable:</b> Provides an Output Enable function to all output buffers F<sub>0-7</sub> from the Output Register.</li> </ul> | Active-High (H)<br><br>Active-Low (L) |

ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

| SYMBOL           | PARAMETER                   | RATING |       | UNIT            |
|------------------|-----------------------------|--------|-------|-----------------|
|                  |                             | Min    | Max   |                 |
| V <sub>CC</sub>  | Supply voltage              |        | +7    | V <sub>DC</sub> |
| V <sub>I</sub>   | Input voltage               |        | +10.0 | V <sub>DC</sub> |
| V <sub>O</sub>   | Output voltage              |        | +5.5  | V <sub>DC</sub> |
| I <sub>IK</sub>  | Input currents              | -30    | +30   | mA              |
| I <sub>O</sub>   | Output currents             |        | +100  | mA              |
| T <sub>A</sub>   | Operating temperature range | -55    | +125  | °C              |
| T <sub>STG</sub> | Storage temperature range   | -65    | +150  | °C              |

## Field-Programmable Logic Sequencer (16 × 48 × 8)

82S105

DC ELECTRICAL CHARACTERISTICS  $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ ,  $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ 

| SYMBOL                            | PARAMETER <sup>3</sup>                      | TEST CONDITIONS <sup>3</sup>                      | LIMITS <sup>3</sup> |                  |      | UNIT |
|-----------------------------------|---|---|---------------------|------------------|------|------|
|                                   |   |   | Min                 | Typ <sup>2</sup> | Max  |      |
| <b>Input Voltage</b>              |   |   |                     |                  |      |      |
| V <sub>IH</sub>                   | High  | V <sub>CC</sub> = 5.5V                            | 2                   |                  |      | V    |
| V <sub>IL</sub>                   | Low   | V <sub>CC</sub> = 4.5V                            |                     |                  | 0.8  | V    |
| V <sub>IK</sub>                   | Clamp <sup>4</sup>                          | V <sub>CC</sub> = Min, I <sub>IK</sub> = -18mA    |                     | -0.8             | -1.2 | V    |
| <b>Output Voltage</b>             |   |   |                     |                  |      |      |
| V <sub>OH</sub>                   | High <sup>5</sup>                           | V <sub>CC</sub> = 4.5V                            | 2.4                 |                  |      | V    |
| V <sub>OL</sub>                   | Low <sup>6</sup>                            | I <sub>OH</sub> = -2mA<br>I <sub>OL</sub> = 9.6mA |                     | 0.35             | 0.5  | V    |
| <b>Input Current</b>              |   |   |                     |                  |      |      |
| I <sub>IH</sub>                   | High  | V <sub>CC</sub> = 5.5V<br>V <sub>I</sub> = 5.5V   |                     | <1               | 50   | μA   |
| I <sub>IL</sub>                   | Low   | V <sub>I</sub> = 0.45V                            |                     | -10              | -150 | μA   |
| I <sub>IL</sub>                   | Low (CK input)                              | V <sub>I</sub> = 0.45V                            |                     | -50              | -350 | μA   |
| <b>Output Current</b>             |   |   |                     |                  |      |      |
| I <sub>O(OFF)</sub>               | Hi-Z state <sup>7</sup>                     | V <sub>CC</sub> = 5.5V<br>V <sub>O</sub> = 5.5V   |                     | 1                | 60   | μA   |
| I <sub>OS</sub>                   | Short circuit <sup>4,8</sup>                | V <sub>O</sub> = 0.45V<br>V <sub>O</sub> = 0V     | -15                 | -1               | -60  | μA   |
| I <sub>CC</sub>                   | V <sub>CC</sub> supply current <sup>9</sup> | V <sub>CC</sub> = 5.5V                            |                     | 120              | 185  | mA   |
| <b>Capacitance<sup>7,10</sup></b> |   |   |                     |                  |      |      |
| C <sub>IN</sub>                   | Input                                       | V <sub>CC</sub> = 5.0V<br>V <sub>I</sub> = 2.0V   |                     | 8                | 13   | pF   |
| C <sub>OUT</sub>                  | Output                                      | V <sub>O</sub> = 2.0V                             |                     | 10               | 15   | pF   |

## Field-Programmable Logic Sequencer (16 × 48 × 8)

82S105

AC ELECTRICAL CHARACTERISTICS -55°C ≤ T<sub>A</sub> ≤ +125°C, 4.5V ≤ V<sub>CC</sub> ≤ 5.5V

| SYMBOL                        | PARAMETER                                      | TO      | FROM              | LIMITS |                   |      | UNIT |
|-------------------------------|--|---------|-------------------|--------|-------------------|------|------|
|                               |  |         |                   | Min    | Typ <sup>11</sup> | Max  |      |
| <b>Pulse Width</b>            |  |         |                   |        |                   |      |      |
| t <sub>CKH</sub>              | Clock <sup>12</sup> High                       | CK-     | CK+               | 40     | 15                |      | ns   |
| t <sub>CKL</sub>              | Clock Low                                      | CK+     | CK-               | 40     | 15                |      | ns   |
| t <sub>CKP1</sub>             | Period (w/o C-array)                           | CK+     | CK+               | 95     | 40                |      | ns   |
| t <sub>CKP2</sub>             | Period (w/C-array) <sup>10</sup>               | CK+     | CK+               | 135    | 60                |      | ns   |
| t <sub>PRH</sub>              | Preset pulse                                   | PR+     | PR-               | 40     | 15                |      | ns   |
| <b>Setup Time</b>             |  |         |                   |        |                   |      |      |
| t <sub>IS1</sub>              | Input  | CK+     | Input±            | 60     |                   |      | ns   |
| t <sub>IS2</sub>              | Input (through Complement array) <sup>13</sup> | CK+     | Input±            | 100    |                   |      | ns   |
| t <sub>VS</sub>               | Power-on preset <sup>13</sup>                  | CK-     | V <sub>CC</sub> + | 5      | -10               |      | ns   |
| t <sub>PRS</sub>              | Preset <sup>10</sup>                           | CK-     | PR-               | 5      | -10               |      | ns   |
| <b>Hold Time</b>              |  |         |                   |        |                   |      |      |
| t <sub>IH</sub>               | Input <sup>10</sup>                            | Input±  | CK+               | 10     | -10               |      | ns   |
| <b>Propagation Delay</b>      |  |         |                   |        |                   |      |      |
| t <sub>CKO</sub>              | Clock  | Output± | CK+               |        | 15                | 35   | ns   |
| t <sub>OE</sub>               | Output Enable <sup>13</sup>                    | Output- | OE-               |        | 20                | 40   | ns   |
| t <sub>OD</sub>               | Output Disable <sup>13</sup>                   | Output+ | OE+               |        | 20                | 40   | ns   |
| t <sub>PR</sub>               | Preset   | Output+ | PR+               |        | 18                | 45   | ns   |
| t <sub>PPR</sub>              | Power-on preset <sup>10</sup>                  | Output+ | V <sub>CC</sub> + |        | 0                 | 20   | ns   |
| <b>Frequency of Operation</b> |  |         |                   |        |                   |      |      |
| f <sub>MAX</sub>              | w/o C-array                                    |         |                   |        |                   | 10.5 | MHz  |
| f <sub>MAX</sub> <sup>C</sup> | w/C-array <sup>10</sup>                        |         |                   |        |                   | 8.3  | MHz  |

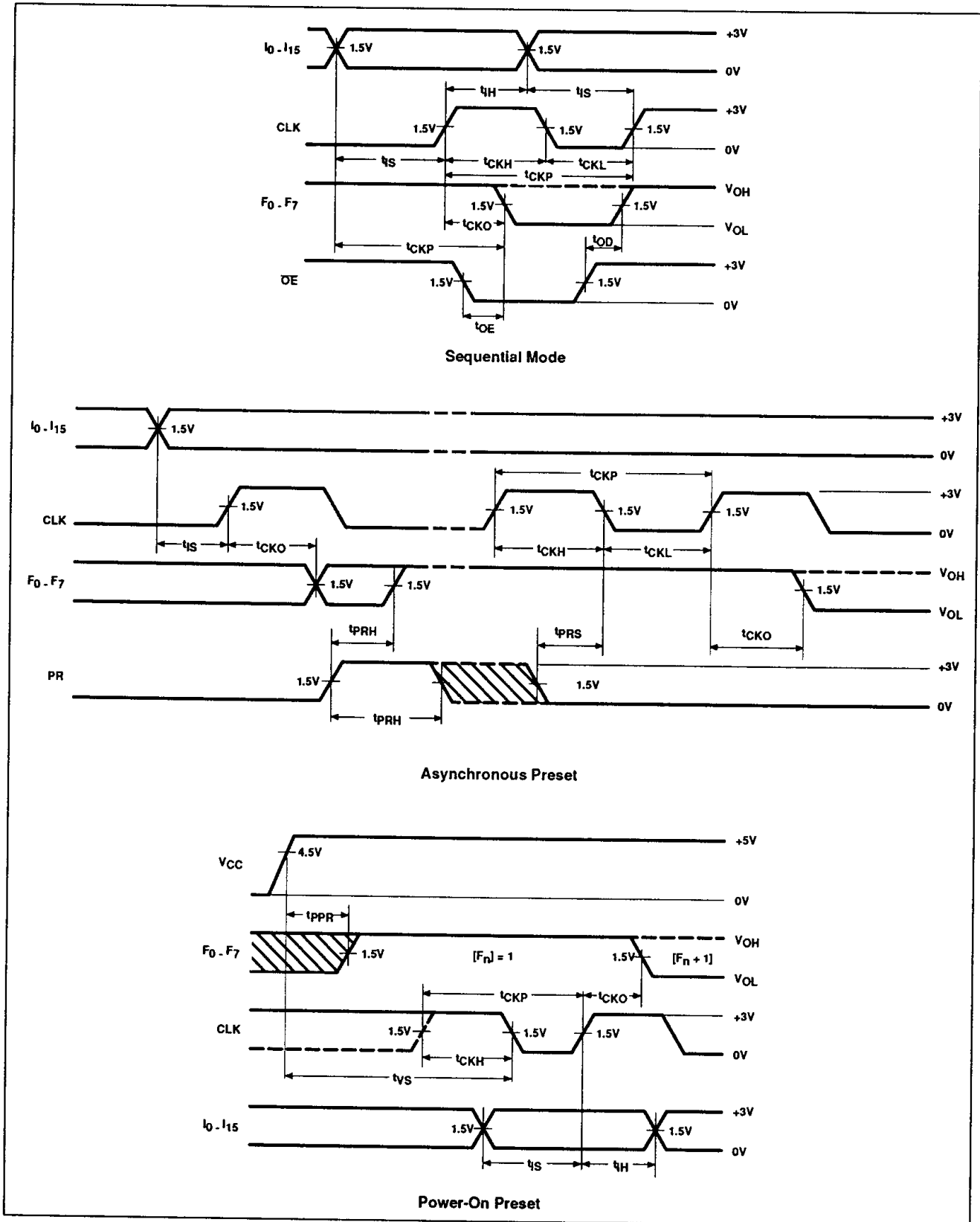
## NOTES:

- Stresses above those listed under "Absolute Maximum Ratings" may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other conditions above those indicated in the operational and programming specification of the device is not implied.
- All typical values are at V<sub>CC</sub> = 5V, T<sub>A</sub> = +25°C.
- All voltage values are with respect to network ground terminal.
- Test one at a time.
- Measured with V<sub>IL</sub> applied to OE and a logic High stored, or with V<sub>IH</sub> applied to PR.
- Measured with a programmed logic condition for which the output is at a Low logic level, and V<sub>IL</sub> applied to PR/OE. Output sink current is supplied through a resistor to V<sub>CC</sub>.
- Measured with V<sub>IH</sub> applied to PR/OE.
- Duration of short circuit should not exceed 1 second.
- I<sub>CC</sub> is measured with the PR/OE input grounded, the outputs open.
- Guaranteed, but not tested.
- All typical values are at V<sub>CC</sub> = 5V, T<sub>A</sub> = +25°C.
- To prevent spurious clocking, clock rise time (10% - 90%) ≤ 30ns.
- Not testable on unprogrammed devices.

# Field-Programmable Logic Sequencer (16 × 48 × 8)

82S105

## TIMING DIAGRAMS



# Field-Programmable Logic Sequencer (16 × 48 × 8)

82S105

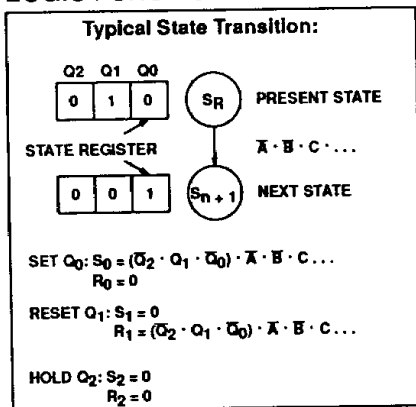
## TIMING DEFINITIONS

| SYMBOL            | PARAMETER  |
|-------------------|--|
| t <sub>CKH</sub>  | Width of input clock pulse.  |
| t <sub>CKL</sub>  | Interval between clock pulses.   |
| t <sub>CKP1</sub> | Operating period — when not using Complement Array.  |
| t <sub>IS1</sub>  | Required delay between beginning of valid input and positive transition of Clock.  |
| t <sub>CKP2</sub> | Operating period — when using Complement Array.  |
| t <sub>IS2</sub>  | Required delay between beginning of valid Input and positive transition of Clock, when using optional Complement Array (two passes necessary through the AND Array). |

| SYMBOL           | PARAMETER  |
|------------------|--|
| t <sub>VS</sub>  | Required delay between V <sub>CC</sub> (after power-on) and negative transition of Clock preceding first reliable clock pulse.           |
| t <sub>PRS</sub> | Required delay between negative transition of Asynchronous Preset and negative transition of Clock preceding first reliable clock pulse. |
| t <sub>IH</sub>  | Required delay between positive transition of Clock and end of valid Input data.   |
| t <sub>CKO</sub> | Delay between positive transition of Clock and when outputs become valid (with PR/OE Low).   |

| SYMBOL           | PARAMETER   |
|------------------|---|
| t <sub>OE</sub>  | Delay between beginning of Output Enable Low and when Outputs become valid.           |
| t <sub>OD</sub>  | Delay between beginning of Output Enable High and when Outputs are in the Off-State.  |
| t <sub>PR</sub>  | Delay between positive transition of Preset and when Outputs become valid at "1".     |
| t <sub>PPR</sub> | Delay between V <sub>CC</sub> (after power-on) and when Outputs become preset at "1". |
| t <sub>PRH</sub> | Width of preset input pulse.  |
| f <sub>MAX</sub> | Maximum clock frequency.  |

## LOGIC FUNCTION



## VIRGIN STATE

A factory shipped virgin device contains all fusible links intact, such that:

1. PR/OE option is set to PR. Thus, all outputs will be at "1", as preset by initial power-up procedure.
2. All transition terms are disabled (0).
3. All S/R flip-flop inputs are disabled (0).
4. The device can be clocked via a Test Array pre-programmed with a standard test pattern.

NOTE: The Test Array pattern must be deleted before incorporating a user program. This is accomplished automatically by any Signetics qualified programming equipment.

# Field-Programmable Logic Sequencer (16 × 48 × 8)

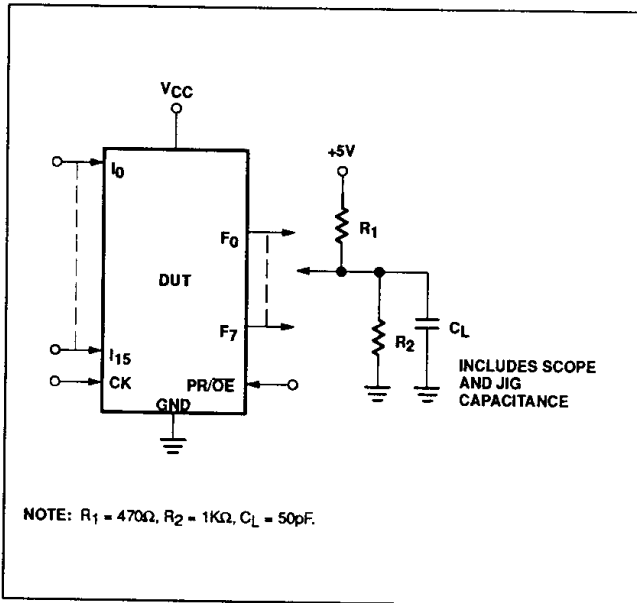
82S105

## TRUTH TABLE

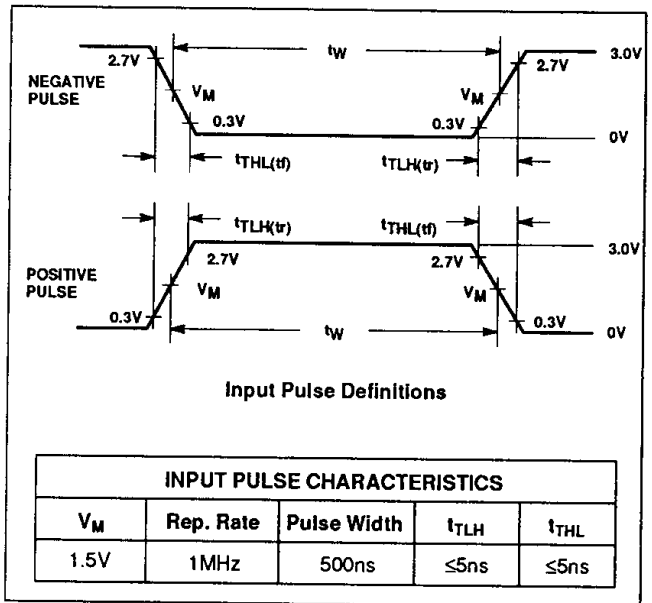
| V <sub>CC</sub> | OPTION |    | I <sub>0</sub> | CK | S | R | Q <sub>P/F</sub> | F                              |
|-----------------|--------|----|----------------|----|---|---|------------------|--------------------------------|
|                 | PR     | OE |                |    |   |   |                  |                                |
| +5V             | H      |    | *              | X  | X | X | H                | H                              |
|                 | L      |    | +10V           | X  | X | X | Q <sub>n</sub>   | (Q <sub>P</sub> ) <sub>n</sub> |
|                 | L      |    | X              | X  | X | X | Q <sub>n</sub>   | (Q <sub>F</sub> ) <sub>n</sub> |
|                 |        | H  | *              | X  | X | X | Q <sub>n</sub>   | Hi-Z                           |
|                 |        | L  | +10V           | X  | X | X | Q <sub>n</sub>   | (Q <sub>P</sub> ) <sub>n</sub> |
|                 |        | L  | X              | X  | X | X | Q <sub>n</sub>   | (Q <sub>F</sub> ) <sub>n</sub> |
|                 |        | L  | X              | ↑  | L | L | Q <sub>n</sub>   | (Q <sub>F</sub> ) <sub>n</sub> |
|                 |        | L  | X              | ↑  | L | H | L                | L                              |
|                 |        | L  | X              | ↑  | H | L | H                | H                              |
|                 |        | L  | X              | ↑  | H | H | IND.             | IND.                           |
| ↑               | X      | X  | X              | X  | X | X | H                |                                |

- NOTES:**
- Positive Logic  $S/R = T_0 + T_1 + T_2 + \dots + T_{47}$   
 $T_n = C(I_0, I_1, I_2, \dots) (P_0, P_1, \dots, P_5)$
  - Either Preset (Active-High) or Output Enable (active-Low) are available, but not both. The desired function is a user programmable option.
  - ↑ denotes transition from Low to High level.
  - R = S = High is an illegal input condition.
  - \* = H/L+10V.
  - X = Don't Care ( $\leq 5.5V$ ).

## TEST LOAD CIRCUITS



## VOLTAGE WAVEFORMS





# Field-Programmable Logic Sequencer (16 × 48 × 8)

82S105

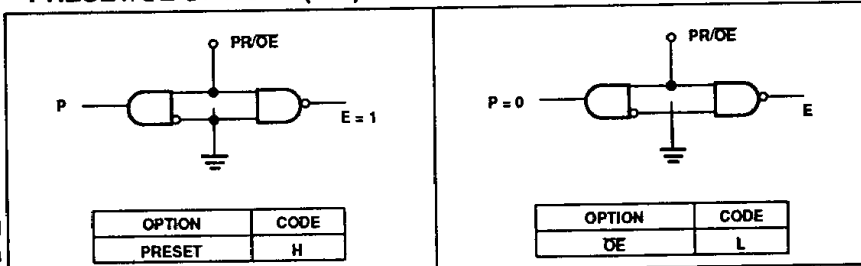
## LOGIC PROGRAMMING

The FPLS can be programmed by means of Logic programming equipment.

With Logic programming, the AND/OR gate input connections necessary to implement the desired logic function are coded directly from the State Diagram using the Program Table on the following page.

In this table, the logic state or action of control variables C, I, P, N and F, associated with each Transition Term  $T_n$  is assigned a symbol which results in the proper fusing pattern of corresponding link pairs, defined as follows:

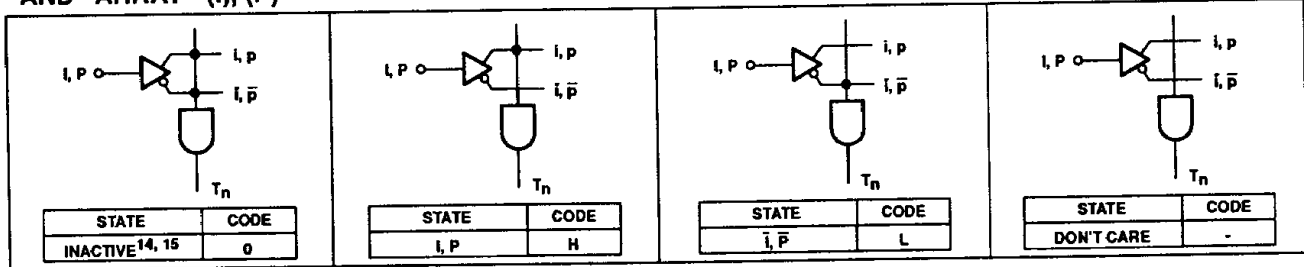
### PRESET/OE OPTION - (P/E)



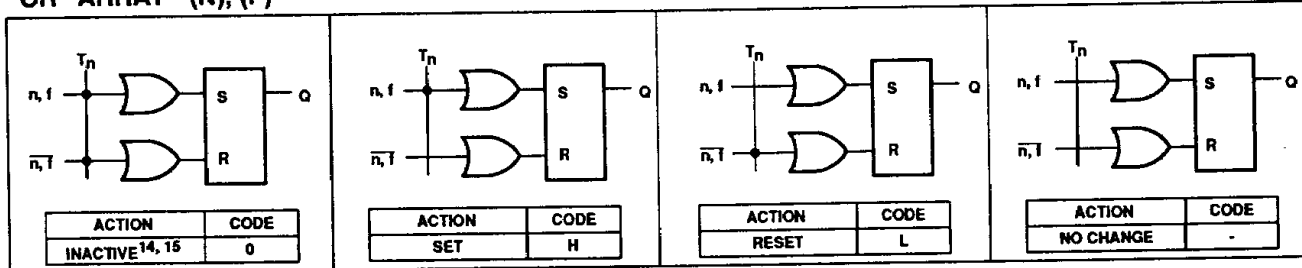
### PROGRAMMING THE 82S105:

The 82S105 has a power-up preset feature. This feature insures that the device will power-up in a known state with all register elements (State and Output Register) at logic High (H). When programming the device it is important to realize this is the initial state of the device. You *must* provide a next state jump if you do not wish to use all Highs (H) as the present state.

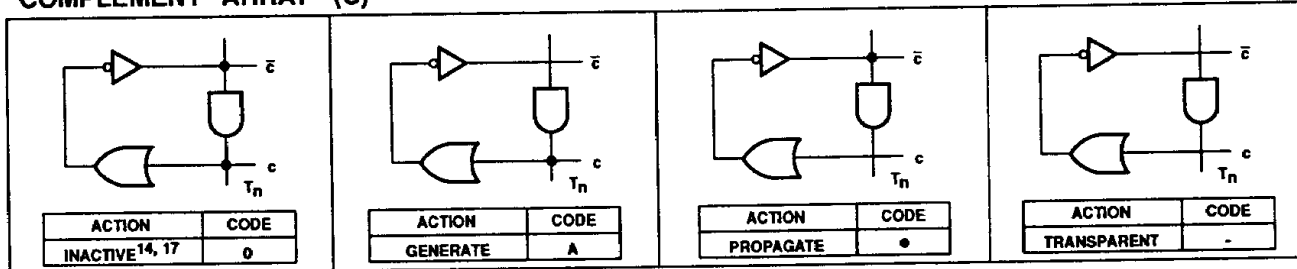
### “AND” ARRAY - (I), (P)



### “OR” ARRAY - (N), (F)



### “COMPLEMENT” ARRAY - (C)



#### NOTES:

14. This is the initial unprogrammed state of all link pairs. It is normally associated with all unused (inactive) AND gates  $T_n$ .
15. Any gate  $T_n$  will be unconditionally inhibited if any one of its I or P link pairs are left intact.
16. To prevent simultaneous Set and Reset flip-flop commands, this state is not allowed for N and F link pairs coupled to active gates  $T_n$  (see flip-flop truth tables).
17. To prevent oscillations, this state is not allowed for C link pairs coupled to active gates  $T_n$ .





# Signetics

# Packaging Information

T-90-20

## Military Products

### SIGNETICS STANDARD PACKAGE DESCRIPTIONS

All Military package case outlines and physical dimensions conform with the current revision MIL-M-38510, Appendix C, except for package types which are not included in that specification.

The physical dimensions for standard package types which are not included in Appendix C are included herein in Appendix C format. Case outline letters are assigned to these packages according to JEDEC Publication 101 as follows:

- U: Leadless chip carriers
- X: Dual-in-line packages
- Y: Flat packages
- Z: All other configurations

A case outline suffix number is assigned herein for identification purposes only, and is not marked on the product.

Signetics Military products are offered in a wide range of package configurations to optimally fit our customer needs.

- Dual-in-line Packages; Frit glass sealed CERDIP (F package family) with 8-40 leads, and side-brazed ceramic (I package family) with 48-64 leads.
- Flat Packages; Frit glass sealed alumina CERPAC (W package family) with 14-28 leads, and brazed leaded ceramic (Q package family) with 52 leads.

- Ceramic Chip Carriers; triple laminated, metal-lidded LCC (G package family) with 20-68 terminals.

- Pin Grid Array; metal-lidded ceramic pin grid (P package family) with 68-100 leads.

- Shown in Table 1 are the case outline letters assigned according to Appendix C of MIL-M-38510 and JEDEC publication 101. Unless otherwise noted, all package types are Configuration 1 and all lead finishes are hot solder dip Finish "A".

Table 1.

| Package Description | Type Designation  | Case Outline   | Theta-JC °C/Watt <sup>4</sup> |
|---------------------|-------------------|----------------|-------------------------------|
| 8DIP3               | D-4               | P              | 28                            |
| 14DIP3              | D-1               | C              | 28                            |
| 16DIP3              | D-2               | E              | 28                            |
| 18DIP3              | D-6               | V              | 28                            |
| 20DIP3              | D-8               | R              | 28                            |
| 22DIP4              | D-7               | W              | 28                            |
| 24DIP3              | D-9               | L              | 28                            |
| 24DIP4              | D-11              | X <sup>2</sup> | 28                            |
| 24DIP6              | D-3               | J              | 28                            |
| 28DIP6              | D-10              | X <sup>2</sup> | 28                            |
| 40DIP6              | D-5               | Q              | 28                            |
| 48DIP6              | D-14 <sup>1</sup> | X <sup>2</sup> | 28                            |
| 50DIP9              | D-12 <sup>1</sup> | X <sup>2</sup> | 28                            |
| 64DIP9              | D-13 <sup>1</sup> | X <sup>2</sup> | 28                            |
| 14FLAT              | F-2               | D              | 22                            |
| 16FLAT              | F-5               | F              | 22                            |
| 18FLAT              | F-10              | Y <sup>2</sup> | 22                            |
| 20FLAT              | F-9               | S              | 22                            |
| 24FLAT              | F-6               | K              | 22                            |
| 28FLAT              | F-11              | Y <sup>2</sup> | 22                            |
| 52FLAT              | Y-1 <sup>1</sup>  | Y <sup>2</sup> | 22                            |
| 18LLCC              | C-9               | U <sup>2</sup> | 20                            |
| 20LLCC              | C-2 <sup>3</sup>  | 2              | 20                            |
| 28LLCC              | C-4 <sup>3</sup>  | 3              | 20                            |
| 32LLCC              | C-12              | U <sup>2</sup> | 20                            |
| 44LLCC              | C-5               | U <sup>2</sup> | 20                            |
| 68LLCC              | C-7               | U <sup>2</sup> | 20                            |
| 68PGA               | P-AB              | Z <sup>2</sup> | 20                            |
| 84PGA               | P-AB              | Z <sup>2</sup> | 20                            |

**NOTES:**

1. Configuration 2.
2. Per JEDEC publication 101.
3. Dimension A (LLCC thickness) is 75mils maximum.
4. See RADC test report RADC-TR-86-97 for thermal resistance confidence and derating.

**Packaging Information**

T-90-20

**CASE OUTLINES Y (FLAT PACKAGES)**

**Configuration 1**

**Configuration 2**

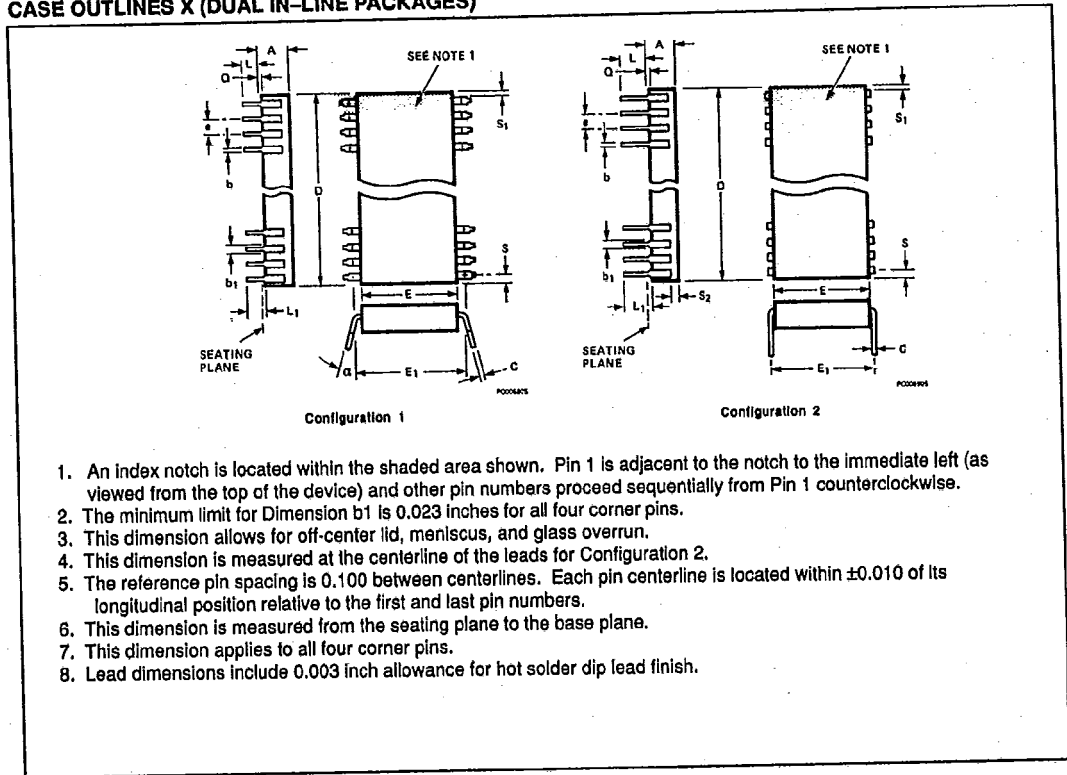
**NOTES:**

1. A lead tab (enlargement) or index dot is located within the shaded area shown at Pin 1. Other pin numbers proceed sequentially from Pin 1 counterclockwise (as viewed from the top of the device).
2. This dimension allows for off-center lid, meniscus, and glass overrun.
3. The reference pin spacing is 0.050 between centerlines. Each pin centerline is located within  $\pm 0.005$  of its longitudinal position relative to the first and last pin numbers.
4. This dimension is measured at the point of exit of the lead body.
5. This dimension applied to all four corner pins.
6. Lead dimensions include 0.003 inch allowance for hot solder dip lead finish.

| OUTLINE       | Y1        |        | NOTES |
|---------------|-----------|--------|-------|
| CONFIGURATION | 2         |        |       |
| NO. LEADS     | 52        |        |       |
| SIG. PKG.     | QP        |        |       |
| SYMBOL        | INCHES    |        |       |
|               | Min       | Max    |       |
| A             | 0.045     | 0.100  | 6     |
| b             | 0.015     | 0.026  |       |
| c             | 0.008     | 0.015  | 6     |
| D             | -         | 1.330  | 2     |
| E             | 0.620     | 0.660  | 3     |
| e             | 0.050 BSC |        |       |
| L             | 0.250     | 0.370  | 4     |
| Q             | 0.054     | 0.0666 |       |
| S             | -         | 0.045  | 5     |
| S1            | 0.005     | -      | 5     |

**Packaging Information**

**CASE OUTLINES X (DUAL IN-LINE PACKAGES)**

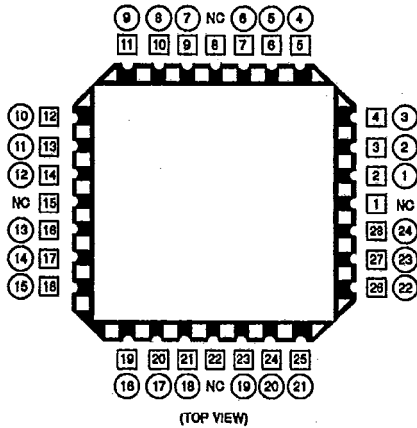


1. An index notch is located within the shaded area shown. Pin 1 is adjacent to the notch to the immediate left (as viewed from the top of the device) and other pin numbers proceed sequentially from Pin 1 counterclockwise.
2. The minimum limit for Dimension b1 is 0.023 inches for all four corner pins.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. This dimension is measured at the centerline of the leads for Configuration 2.
5. The reference pin spacing is 0.100 between centerlines. Each pin centerline is located within  $\pm 0.010$  of its longitudinal position relative to the first and last pin numbers.
6. This dimension is measured from the seating plane to the base plane.
7. This dimension applies to all four corner pins.
8. Lead dimensions include 0.003 inch allowance for hot solder dip lead finish.

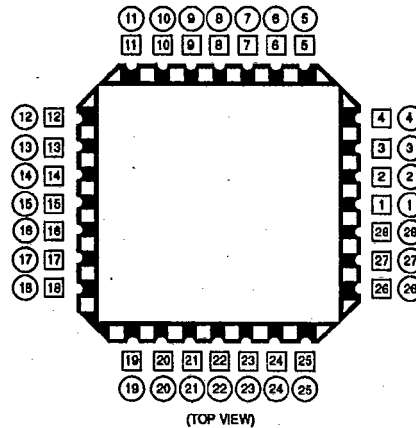
Packaging Information

T-90-20

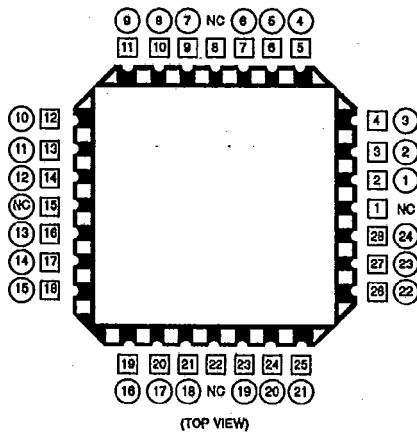
LEADLESS CHIP CARRIER (LLCC) PINOUTS



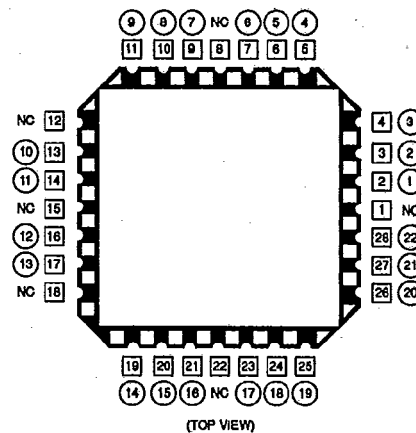
24-Lead Logic Pinout for 28 Terminal Chip Carrier



28-Lead Pinout for 28 Terminal Chip Carrier for all Device Types



24-Lead Memory Pinout for 28 Terminal Chip Carrier



22-Lead Memory Pinout for 28 Terminal Chip Carrier

□ = Chip Carrier Terminal Number  
 ○ = Dual In-Line Lead Number  
 NC = No Connect