ANALOG DEVICES

Preliminary Technical Data

AD7942

FEATURES

14-bit resolution with no missing codes
Throughput: 250 kSPS
INL: ±0.4 LSB typ, ±1 LSB max (±0.0061 % of FSR)
S/(N + D): 85 dB @ 20 kHz
THD: –100 dB @ 20 kHz
Pseudo-differential analog input range
    0 V to V$_{REF}$ with V$_{REF}$ up to VDD
No pipeline delay
Single-supply 5V operation with
    1.8 V/2.5 V/3 V/5 V logic interface
Serial interface SPI®/QSPI™/µWire/DSP compatible
Daisy chain multiple ADCs and BUSY indicator
Power dissipation
    1.15 mW @ 2.5 V/100 kSPS, 3.3 mW @ 5 V/100 kSPS,
    1.15 µW @ 2.5 V/100 SPS
Stand-by current: 1 nA
10-lead package: MSOP (MSOP-8 size) and
    3 mm × 3 mm QFN (LFCSP) (SOT-23 size)
Pin-for-pin compatible with the 16-Bit AD7685

APPLICATIONS

Battery-powered equipment
Data acquisition
Instrumentation
Medical instruments
Process control

Table 1. MSOP, QFN (LFCSP)/SOT-23 14 and16-Bit ADC

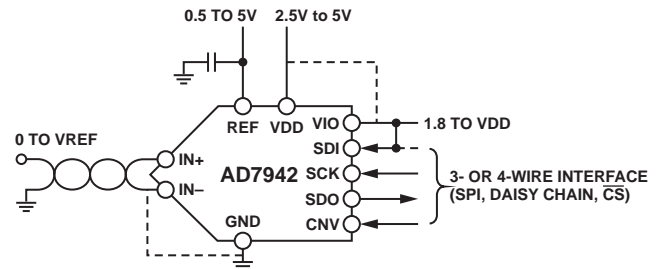| Type	100 kSPS	250 kSPS	500 kSPS
16-Bit True Differential	AD7684	AD7687	AD7688
16-Bit Pseudo Differential/Unipolar	AD7683	AD7685 AD7694	AD7686
16-Bit Unipolar	AD7680		
14-Bit Pseudo Differential/Unipolar		AD7942	AD7946
14-Bit Unipolar	AD7940		

APPLICATION DIAGRAM

Figure 1.

GENERAL DESCRIPTION

The AD7942 is a 14-bit, charge redistribution successive approximation, analog-to-digital converter (ADC) that operates from a single 5V power supply, VDD. It contains a low power, high speed, 14-bit sampling ADC with no missing codes, an internal conversion clock, and a versatile serial interface port. The part also contains a low noise, wide bandwidth, short aperture delay track-and-hold circuit. On the CNV rising edge, it samples an analog input IN+ between 0 V to REF with respect to a ground sense IN–. The reference voltage, REF, is applied externally and can be set up to the supply voltage.

Its power scales linearly with throughput.

The SPI compatible serial interface also features the ability, using the SDI input, to daisy chain several ADCs on a single 3-wire bus and provides an optional BUSY indicator. It is compatible with 1.8 V, 2.5 V, 3 V, or 5 V logic using the separate supply VIO.

The AD7942 is housed in a 10-lead MSOP or a 10-lead QFN (LFCSP) with operation specified from –40°C to +85°C.

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REVISION HISTORY

8/04—Revision B: Preliminary

SPECIFICATIONS

VDD = 2.3 V to 5.5 V, VIO = 2.3 V to VDD, V_{REF} = VDD, T_A = −40°C to +85°C, unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
RESOLUTION		14			Bits
ANALOG INPUT					
Voltage Range	IN+ − IN−	0		V_{REF}	V
Absolute Input Voltage	IN+	−0.1		VDD + 0.1	V
	IN−	−0.1		0.1	V
Analog Input CMRR	f_{IN} = 250 kHz		65		dB
Leakage Current at 25°C	Acquisition Phase		1		nA
Input Impedance		See the Analog Input section.			
ACCURACY					
No Missing Codes		14			Bits
Differential Linearity Error		−0.7	±0.25	+0.7	LSB[1]
Integral Linearity Error		−1	±0.4	+1	LSB
Transition Noise	REF = VDD = 5 V		0.33		LSB
Gain Error[2], T_{MIN} to T_{MAX}			±TBD	±TBD	LSB
Gain Error Temperature Drift			±TBD		ppm/°C
Offset Error[2], T_{MIN} to T_{MAX}			±TBD	±TBD	mV
Offset Temperature Drift			±TBD		ppm/°C
Power Supply Sensitivity	VDD = 5V ± 5%		±TBD		LSB
THROUGHPUT					
Conversion Rate	VDD = 4.5 V to 5.5 V	0		250	kSPS
	VDD = 2.3 V to 4.5 V	0		200	kSPS
Transient Response	Full-Scale Step			1.8	μs
AC ACCURACY					
Signal-to-Noise	f_{IN} = 20 kHz, V_{REF} = 5 V	83	85		dB[3]
	f_{IN} = 20 kHz, V_{REF} = 2.5 V		84		dB
Spurious-Free Dynamic Range	f_{IN} = 20 kHz		−100		dB
Total Harmonic Distortion	f_{IN} = 20 kHz		−100		dB
Signal-to-(Noise + Distortion)	f_{IN} = 20 kHz, V_{REF} = 5 V	83	85		dB
	f_{IN} = 20 kHz, V_{REF} = 5 V, −60 dB Input		25		dB
	f_{IN} = 20 kHz, V_{REF} = 2.5 V		84		dB
Intermodulation Distortion[4]			TBD		dB

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[1] LSB means least significant bit. With the 5 V input range, one LSB is 305.2 μV.
[2] See Terminology section. These specifications do include full temperature range variation but do not include the error contribution from the external reference.
[3] All specifications in dB are referred to a full-scale input FS. Tested with an input signal at 0.5 dB below full-scale, unless otherwise specified.
[4] f_{IN1} = 21.4 kHz, f_{IN2} = 18.9 kHz, each tone at −7 dB below full-scale.

VDD = 2.3 V to 5.5 V, VIO = 2.3 V to VDD, V_{REF} = VDD, T_A = −40°C to +85°C, unless otherwise noted.

Table 3.

Parameter	Conditions	Min	Typ	Max	Unit
REFERENCE					
Voltage Range		0.5		VDD + 0.3	V
Load Current	250 kSPS, REF = 5 V		TBD		µA
SAMPLING DYNAMICS					
−3 dB Input Bandwidth			2		MHz
Aperture Delay	VDD = 5 V		2.5		ns
DIGITAL INPUTS					
Logic Levels					
V_{IL}		−0.3		$0.3 \times$ VIO	V
V_{IH}		$0.7 \times$ VIO		VIO + 0.3	V
I_{IL}		−1		+1	µA
I_{IH}		−1		+1	µA
DIGITAL OUTPUTS					
Data Format			Serial 14 Bits Straight Binary		
Pipeline Delay			Conversion Results Available Immediately after Completed Conversion		
V_{OL}	I_{SINK}= +500 µA			0.4	V
V_{OH}	I_{SOURCE}= −500 µA	VIO − 0.3			V
POWER SUPPLIES					
VDD	Specified Performance	2.3		5.5	V
VIO	Specified Performance	2.3		VDD + 0.3	V
VIO Range		1.8		VDD + 0.3	V
Standby Current[1,2]	VDD and VIO = 5 V, 25°C		1	50	nA
Power Dissipation	VDD = 2.5 V, 100 SPS Throughput		1.15		µW
	VDD = 2.5 V, 100 kSPS Throughput		1.15	2	mW
	VDD = 2.5 V, 200 kSPS Throughput		2.25	4	mW
	VDD = 5 V, 100 kSPS Throughput		3.3	5	mW
	VDD = 5 V, 250 kSPS Throughput			12.5	mW
TEMPERATURE RANGE[3]					
Specified Performance	T_{MIN} to T_{MAX}	−40		+85	°C

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[1] With all digital inputs forced to VIO or GND as required.
[2] During acquisition phase.
[3] Contact Analog Devices for extended temperature range.

TIMING SPECIFICATIONS

−40°C to +85°C, VIO = 2.3 V to 5.5 V or VDD + 0.3 V, whichever is the lowest, unless otherwise stated.

Table 4. VDD = 4.5 V to 5.5 V[1]

	Symbol	Min	Typ	Max	Unit
Conversion Time: CNV Rising Edge to Data Available	t_{CONV}	0.5		2.2	µs
Acquisition Time	t_{ACQ}	1.8			µs
Time between Conversions	t_{CYC}	4			µs
CNV Pulse Width ($\overline{CS}$ Mode)	t_{CNVH}	10			ns
SCK Period ($\overline{CS}$ Mode)	t_{SCK}	15			ns
SCK Period (Chain Mode)	t_{SCK}				
VIO above 4.5 V		19			ns
VIO above 3 V		20			ns
VIO above 2.7 V		21			ns
VIO above 2.3 V		22			ns
SCK Low Time	t_{SCKL}	7			ns
SCK High Time	t_{SCKH}	7			ns
SCK Falling Edge to Data Remains Valid	t_{HSDO}	5			ns
SCK Falling Edge to Data Valid Delay	t_{DSDO}				
VIO above 4.5 V				14	ns
VIO above 3 V				15	ns
VIO above 2.7 V				16	ns
VIO above 2.3 V				17	ns
CNV or SDI Low to SDO D15 MSB Valid ($\overline{CS}$ Mode)	t_{EN}				
VIO above 4.5 V				15	ns
VIO above 2.7 V				18	ns
VIO above 2.3 V				22	ns
CNV or SDI High or Last SCK Falling Edge to SDO High Impedance ($\overline{CS}$ Mode)	t_{DIS}			25	ns
SDI Valid Setup Time from CNV Rising Edge ($\overline{CS}$ Mode)	$t_{SSDICNV}$	15			ns
SDI Valid Hold Time from CNV Rising Edge ($\overline{CS}$ Mode)	$t_{HSDICNV}$	0			ns
SCK Valid Setup Time from CNV Rising Edge (Chain Mode)	$t_{SSCKCNV}$	5			ns
SCK Valid Hold Time from CNV Rising Edge (Chain Mode)	$t_{HSCKCNV}$	5			ns
SDI Valid Setup Time from SCK Falling Edge (Chain Mode)	$t_{SSDISCK}$	5			ns
SDI Valid Hold Time from SCK Falling Edge (Chain Mode)	$t_{HSDISCK}$	4			ns
SDI High to SDO High (Chain Mode with BUSY indicator)	$t_{DSDOSDI}$				
VIO above 4.5 V				15	ns
VIO above 2.3 V				26	ns

[1] See **Error! Reference source not found.** and **Error! Reference source not found.** for load conditions.

−40°C to +85°C, VIO = 2.3 V to 4.5 V or VDD + 0.3 V, whichever is the lowest, unless otherwise stated.

Table 5. VDD = 2.3V to 4.5 V[1]

	Symbol	Min	Typ	Max	Unit
Conversion Time: CNV Rising Edge to Data Available	t_{CONV}	0.7		3.2	µs
Acquisition Time	t_{ACQ}	1.8			µs
Time between Conversions	t_{CYC}	5			µs
CNV Pulse Width ($\overline{CS}$ Mode)	t_{CNVH}	10			ns
SCK Period ($\overline{CS}$ Mode)	t_{SCK}	25			ns
SCK Period (Chain Mode)	t_{SCK}				
VIO above 3 V		29			ns
VIO above 2.7 V		35			ns
VIO above 2.3 V		40			ns
SCK Low Time	t_{SCKL}	12			ns
SCK High Time	t_{SCKH}	12			ns
SCK Falling Edge to Data Remains Valid	t_{HSDO}	5			ns
SCK Falling Edge to Data Valid Delay	t_{DSDO}				
VIO above 3 V				24	ns
VIO above 2.7 V				30	ns
VIO above 2.3 V				35	ns
CNV or SDI Low to SDO D15 MSB Valid ($\overline{CS}$ Mode)	t_{EN}				
VIO above 2.7 V				18	ns
VIO above 2.3 V				22	ns
CNV or SDI High or Last SCK Falling Edge to SDO High Impedance ($\overline{CS}$ Mode)	t_{DIS}			25	ns
SDI Valid Setup Time from CNV Rising Edge ($\overline{CS}$ Mode)	$t_{SSDICNV}$	30			ns
SDI Valid Hold Time from CNV Rising Edge ($\overline{CS}$ Mode)	$t_{HSDICNV}$	0			ns
SCK Valid Setup Time from CNV Rising Edge (Chain Mode)	$t_{SSCKCNV}$	5			ns
SCK Valid Hold Time from CNV Rising Edge (Chain Mode)	$t_{HSCKCNV}$	8			ns
SDI Valid Setup Time from SCK Falling Edge (Chain Mode)	$t_{SSDISCK}$	5			ns
SDI Valid Hold Time from SCK Falling Edge (Chain Mode)	$t_{HSDISCK}$	4			ns
SDI High to SDO High (Chain Mode with BUSY indicator)	$t_{DSDOSDI}$			26	ns

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[1] See **Error! Reference source not found.** and **Error! Reference source not found.** for load conditions.

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Analog Inputs	
IN+[3], IN−[1], REF	GND − 0.3 V to VDD + 0.3 V or ±130 mA
Supply Voltages	
VDD, VIO to GND	−0.3 V to +7 V
VDD to VIO	±7 V
Digital Inputs to GND	−0.3 V to VIO + 0.3 V
Digital Outputs to GND	−0.3 V to VIO + 0.3 V
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
θ_{JA} Thermal Impedance	200°C/W (MSOP-10)
θ_{JC} Thermal Impedance	44°C/W (MSOP-10)
Lead Temperature Range	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[3] See the Analog Input section.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.
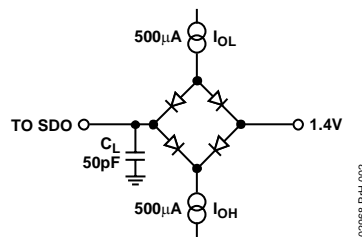
Figure 2. Load Circuit for Digital Interface Timing
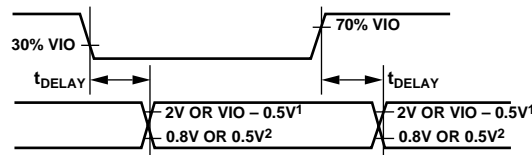
NOTES
1. 2V IF VIO ABOVE 2.5V, VIO − 0.5V IF VIO BELOW 2.5V.
2. 0.8V IF VIO ABOVE 2.5V, 0.5V IF VIO BELOW 2.5V.

Figure 3. Voltage Reference Levels for Timing

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS


```
        ┌───────────┐
REF  1 │●          │ 10 VIO
VDD  2 │           │  9 SDI
IN+  3 │  AD7942   │  8 SCK
IN−  4 │           │  7 SDO
GND  5 │           │  6 CNV
        └───────────┘
```
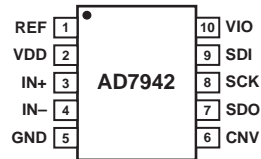
Figure 4.10-Lead MSOP and QFN (LFCSP) Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Function
1	REF	AI	Reference Input Voltage. The REF range is from 0.5 V to VDD. It is referred to the GND pin. This pin should be decoupled closely to the pin with a 10 µF capacitor.
2	VDD	P	Power Supply.
3	IN+	AI	Analog Input. It is referred to in IN−. The voltage range, i.e., the difference between IN+ and IN−, is 0 V to V_{REF}.
4	IN−	AI	Analog Input Ground Sense. To be connected to the analog ground plane or to a remote sense ground.
5	GND	P	Power Supply Ground.
6	CNV	DI	Convert Input. This input has multiple functions. On its leading edge, it initiates the conversions and selects the interface mode of the part, chain or $\overline{CS}$ mode. In $\overline{CS}$ mode, it enables the SDO pin when low. In chain mode, the data should be read when CNV is high.
7	SDO	DO	Serial Data Output. The conversion result is output on this pin. It is synchronized to SCK.
8	SCK	DI	Serial Data Clock Input. When the part is selected, the conversion result is shifted out by this clock.
9	SDI	DI	Serial Data Input. This input provides multiple features. It selects the interface mode of the ADC as follows: Chain mode is selected if SDI is low during the CNV rising edge. In this mode, SDI is used as a data input to daisy chain the conversion results of two or more ADCs onto a single SDO line. The digital data level on SDI is output on SDO with a delay of 14 SCK cycles. $\overline{CS}$ mode is selected if SDI is high during the CNV rising edge. In this mode, either SDI or CNV can enable the serial output signals when low, and if SDI or CNV is low when the conversion is complete, the BUSY indicator feature is enabled.
10	VIO	P	Input/Output Interface Digital Power. Nominally at the same supply as the host interface (1.8 V, 2.5 V, 3 V, or 5 V).

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[1]AI = Analog Input, DI = Digital Input, DO = Digital Output, and P = Power

TERMINOLOGY

Integral Nonlinearity Error (INL)
Linearity error refers to the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs 1/2 LSB before the first code transition. Positive full scale is defined as a level 1 1/2 LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line (Figure 21).

Differential Nonlinearity Error (DNL)
In an ideal ADC, code transitions are 1 LSB apart. DNL is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

Offset Error
The first transition should occur at a level 1/2 LSB above analog ground (152.6 μV for the 0 V to 5 V range). The offset error is the deviation of the actual transition from that point.

Gain Error
The last transition (from 111 . . . 10 to 111 . . . 11) should occur for an analog voltage 1 1/2 LSB below the nominal full scale (4.999542 V for the 0 V to 5 V range). The gain error is the deviation of the actual level of the last transition from the ideal level after the offset has been adjusted out.

Spurious-Free Dynamic Range (SFDR)
The difference, in decibels (dB), between the rms amplitude of the input signal and the peak spurious signal.

Effective Number of Bits (ENOB)
ENOB is a measurement of the resolution with a sine wave input. It is related to S/(N+D) by the following formula

$$\text{ENOB} = \left(S / [N + D]_{dB} - 1.76 \right) / 6.02$$

and is expressed in bits.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in dB.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in dB.

Signal-to-(Noise + Distortion) Ratio (S/[N+D])
S/(N+D) is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/(N+D) is expressed in dB.

Aperture Delay
Aperture delay is a measure of the acquisition performance and is the time between the rising edge of the CNV input and when the input signal is held for a conversion.

Transient Response
The time required for the ADC to accurately acquire its input after a full-scale step function was applied.

TYPICAL PERFORMANCE CHARACTERISTICS
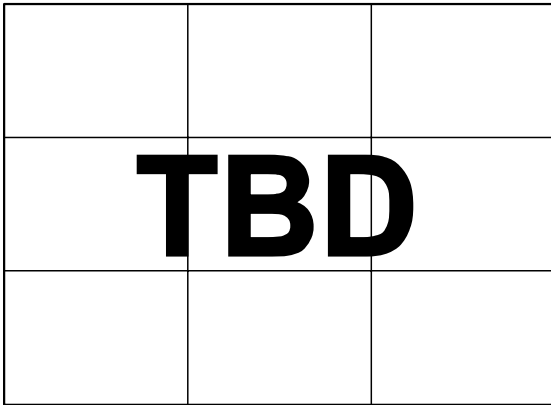
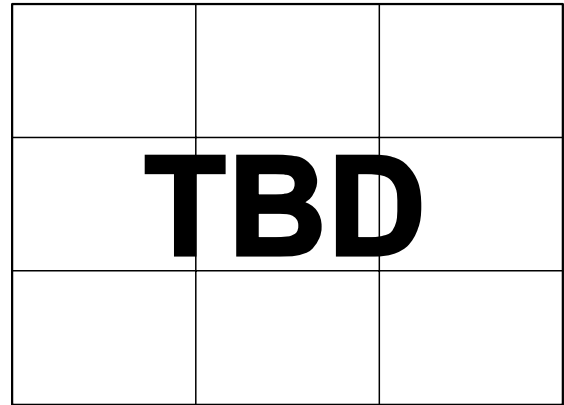*Figure 5. Integral Nonlinearity vs. Code*

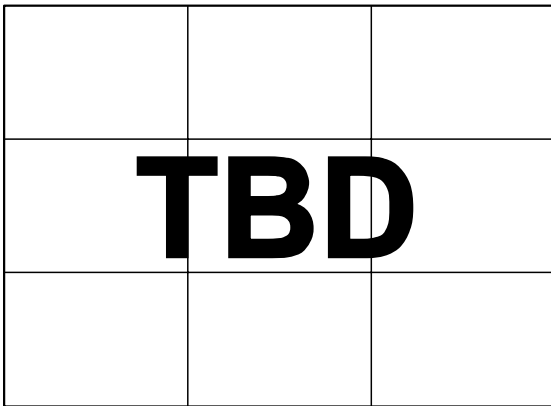*Figure 8. Differential Nonlinearity vs. Code*

Figure 6. Histogram of a DC Input at the Code Center
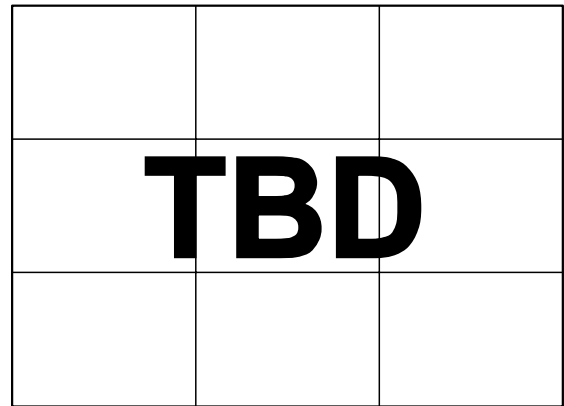

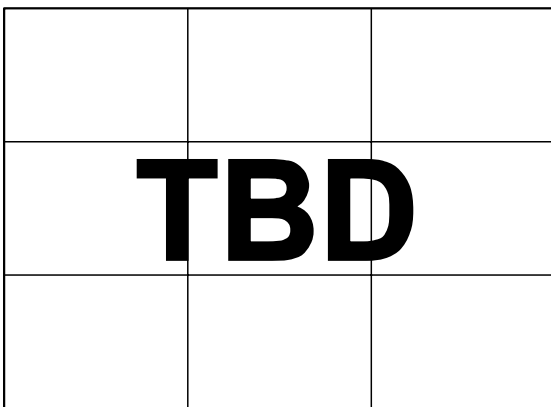*Figure 9. Histogram of a DC Input at the Code Center*

Figure 7. FFT Plot

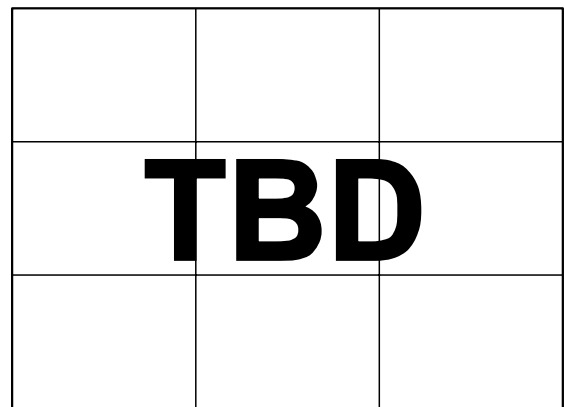*Figure 10. S/[N + D] vs. Frequency*

TBD
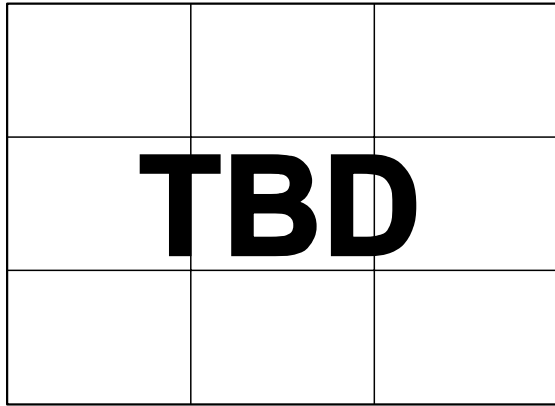
Figure 11. SNR vs. Temperature

TBD
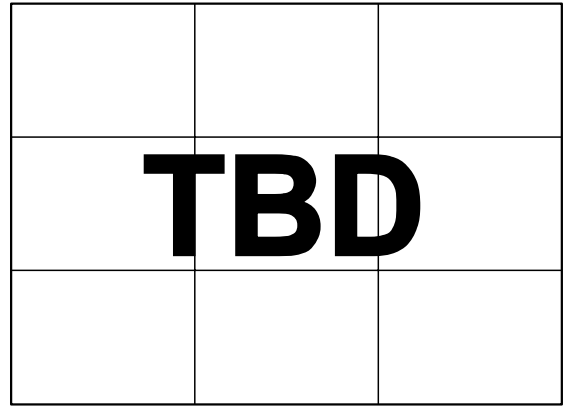
Figure 14. SNR and THD vs. Input Level

TBD
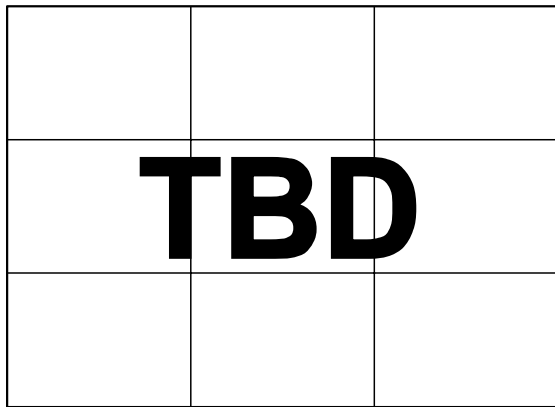
Figure 12. THD vs. Frequency

TBD
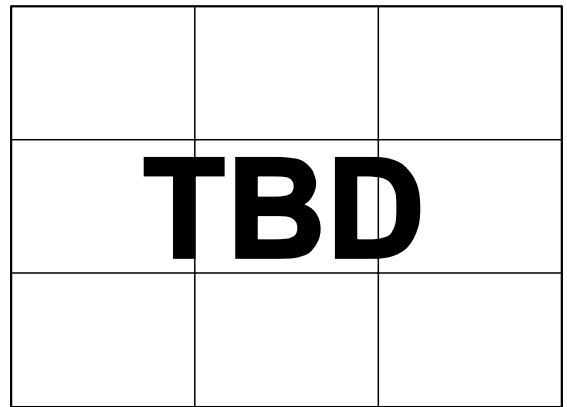
Figure 15. Operating Currents vs. Supply

TBD
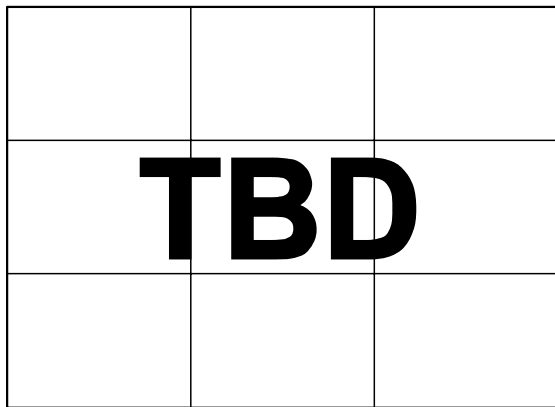
Figure 13. THD, SFDR vs. Temperature

TBD
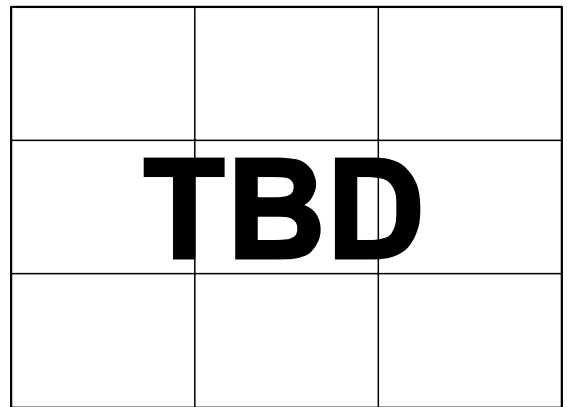
Figure 16. Power-Down Currents vs. Temperature

TBD
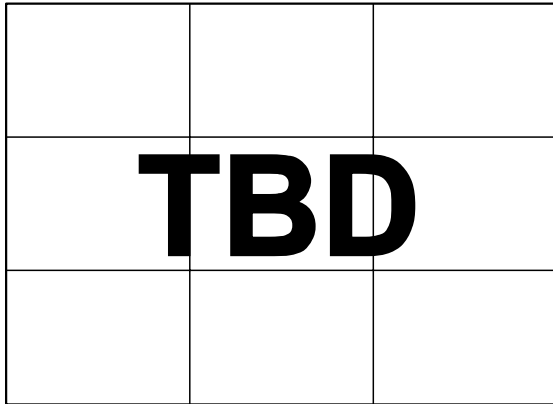
Figure 17. Operating Currents vs. Temperature

TBD
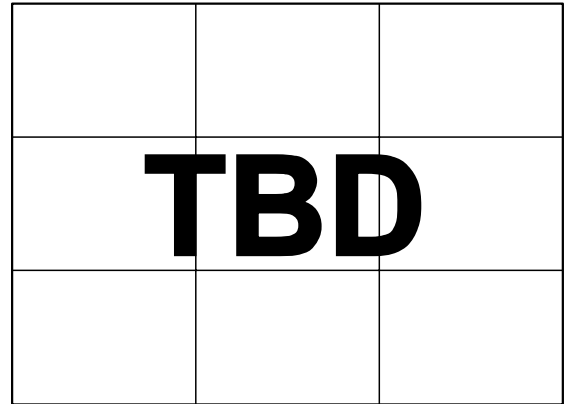
Figure 19. t_{DSDO} vs. Capacitance Load and Supply

TBD
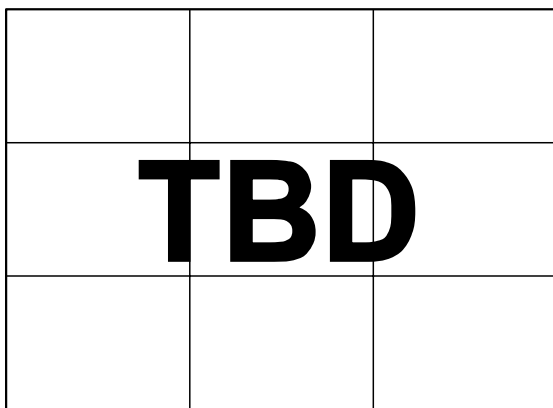
Figure 18. Offset and Gain Error vs. Temperature
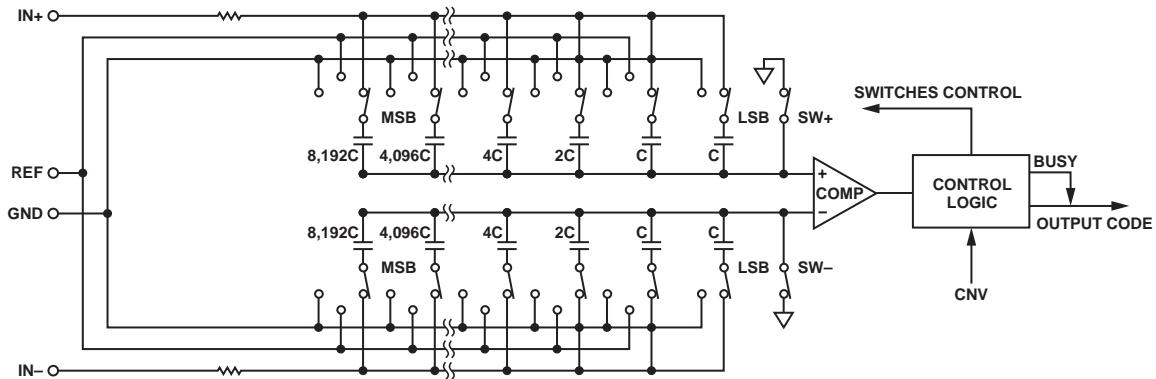
Figure 20. ADC Simplified Schematic

CIRCUIT INFORMATION

The AD7942 is a fast, low power, single-supply, precise 14-bit ADC using a successive approximation architecture.

The AD7942 is capable of converting 250,000 samples per second (250 kSPS) and powers down between conversions. When operating at 100 SPS, for example, it consumes typically 1.15μW with a 2.5V supply, ideal for battery-powered applications.

The AD7942 provides the user with an on-chip track-and-hold and does not exhibit any pipeline delay or latency, making it ideal for multiple multiplexed channel applications.

The AD7942 is specified from 2.3 V to 5.5 V, and can be interfaced to either 5 V, 3.3 V, 2.5 V, or 1.8 V digital logic. It is housed in a 10-lead MSOP or a tiny 10-lead QFN (LFCSP) that combines space savings and allows flexible configurations.

It is pin-for-pin-compatible with the 16 Bit ADC AD7685.

CONVERTER OPERATION

The AD7942 is a successive approximation ADC based on a charge redistribution DAC. Figure 20 shows the simplified schematic of the ADC. The capacitive DAC consists of two identical arrays of 14 binary weighted capacitors, which are connected to the two comparator inputs.

During the acquisition phase, terminals of the array tied to the comparator's input are connected to GND via SW+ and SW−. All independent switches are connected to the analog inputs. Thus, the capacitor arrays are used as sampling capacitors and acquire the analog signal on the IN+ and IN− inputs. When the acquisition phase is complete and the CNV input goes high, a conversion phase is initiated. When the conversion phase begins, SW+ and SW− are opened first. The two capacitor arrays are then disconnected from the inputs and connected to the GND input. Therefore, the differential voltage between the inputs IN+ and IN− captured at the end of the acquisition phase is applied to the comparator inputs, causing the comparator to become unbalanced. By switching each element of the capacitor array between GND and REF, the comparator input varies by binary weighted voltage steps ($V_{REF}/2, V_{REF}/4 \dots V_{REF}/16384$). The control logic toggles these switches, starting with the MSB, in order to bring the comparator back into a balanced condition. After the completion of this process, the part returns to the acquisition phase and the control logic generates the ADC output code and a BUSY signal indicator.

Because the AD7942 has an on-board conversion clock, the serial clock, SCK, is not required for the conversion process.

Transfer Functions

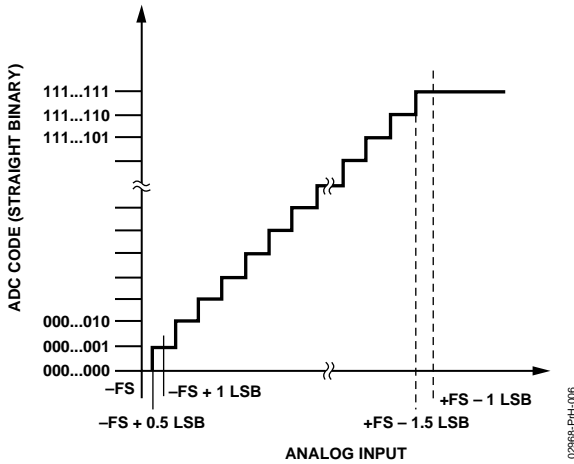The ideal transfer characteristic for the AD7942 is shown in Figure 21 and Table 8.
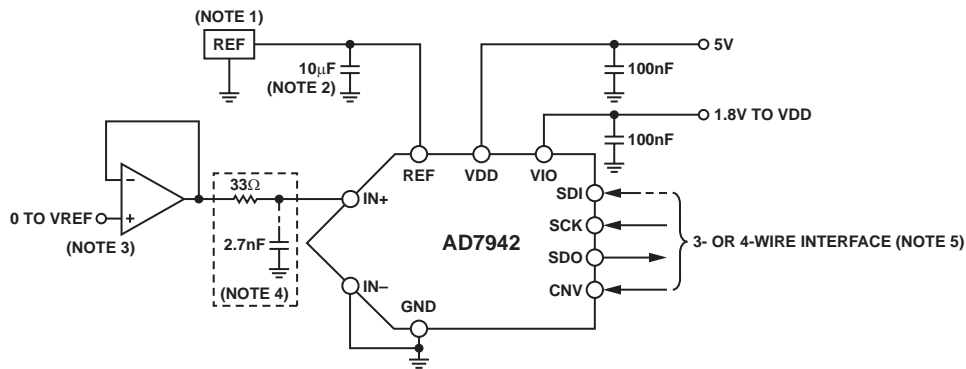

Figure 21. ADC Ideal Transfer Function

Table 8. Output Codes and Ideal Input Voltages

Description	Analog Input V_{REF} = 5 V	Digital Output Code Hexa
FSR – 1 LSB	4.999695 V	3FFF[4]
Midscale + 1 LSB	2.500305 V	2001
Midscale	2.5 V	2000
Midscale – 1 LSB	2.499695 V	1FFF
–FSR + 1 LSB	305.2 µV	0001
–FSR	0 V	0000[5]

[4] This is also the code for an overranged analog input ($V_{IN+} - V_{IN-}$ above V_{REF} – V_{GND}).

[5] This is also the code for an underranged analog input ($V_{IN+} - V_{IN-}$ below V_{GND}).

TYPICAL CONNECTION DIAGRAM

Figure 22 shows an example of the recommended connection diagram for the AD7942 when multiple supplies are available.

NOTE 1: SEE REFERENCE SECTION FOR REFERENCE SELECTION.
NOTE 2: C_{REF} IS USUALLY A 10µF CERAMIC CAPACITOR (X5R).
NOTE 3: SEE DRIVER AMPLIFIER CHOICE SECTION.
NOTE 4: OPTIONAL FILTER. SEE ANALOG INPUT SECTION.
NOTE 5: SEE DIGITAL INTERFACE FOR MOST CONVENIENT INTERFACE MODE.

Figure 22. Typical Application Diagram with multiple supplies

Analog Input

Figure 23 shows an equivalent circuit of the input structure of the AD7942.

The two diodes, D1 and D2, provide ESD protection for the analog inputs IN+ and IN−. Care must be taken to ensure that the analog input signal never exceeds the supply rails by more than 0.3 V because this will cause these diodes to become forward-biased and start conducting current. However, these diodes can handle a forward-biased current of 130 mA maximum. For instance, these conditions could eventually occur when the input buffer's (U1) supplies are different from VDD. In such a case, an input buffer with a short-circuit current limitation can be used to protect the part.
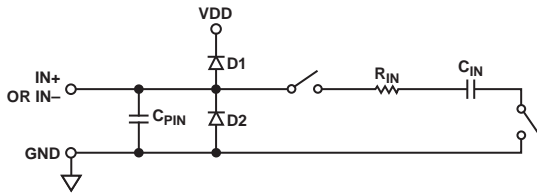
Figure 23. Equivalent Analog Input Circuit

This analog input structure allows the sampling of the differential signal between IN+ and IN−. By using this differential input, small signals common to both inputs are rejected, as shown in Figure 24, which represents the typical CMRR over frequency. For instance, by using IN− to sense a remote signal ground, ground potential differences between the sensor and the local ADC ground are eliminated.
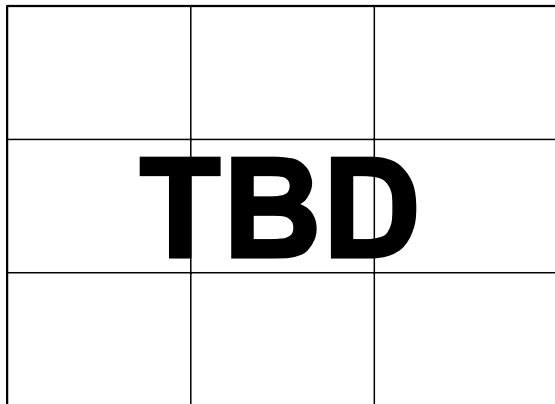
Figure 24. Analog Input CMRR vs. Frequency

During the acquisition phase, the impedance of the analog input IN+ can be modeled as a parallel combination of capacitor C_{PIN} and the network formed by the series connection of R_{IN} and C_{IN}. C_{PIN} is primarily the pin capacitance. R_{IN} is typically 3 kΩ and is a lumped component made up of some serial resistors and the on resistance of the switches. C_{IN} is typically 30 pF and is mainly the ADC sampling capacitor. During the conversion phase, where the switches are opened, the input impedance is limited to C_{PIN}. R_{IN} and C_{IN} make a 1-pole, low-pass filter that reduces undesirable aliasing effect and limits the noise.

When the source impedance of the driving circuit is low, the AD7942 can be driven directly. Large source impedances significantly affect the ac performance, especially total harmonic distortion (THD). The dc performances are less sensitive to the input impedance. The maximum source impedance depends on the amount of THD that can be tolerated. The THD degrades as a function of the source impedance and the maximum input frequency, as shown in Figure 25.
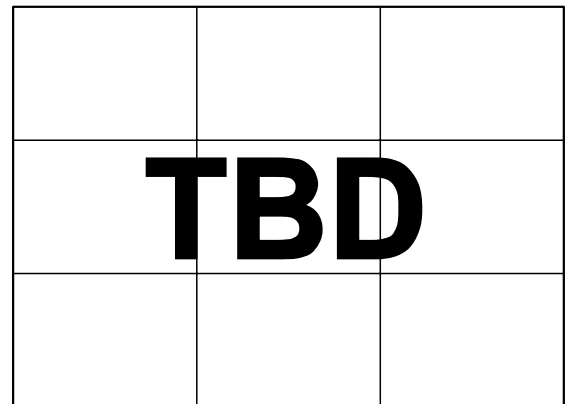
Figure 25. THD vs. Analog Input Frequency and Source Resistance

Driver Amplifier Choice

Although the AD7942 is easy to drive, the driver amplifier needs to meet the following requirements:

The noise generated by the driver amplifier needs to be kept as low as possible in order to preserve the SNR and transition noise performance of the AD7942. Note that the AD7942 has a noise much lower than most of the other 14-bit ADCs and, therefore, can be driven by a noisier op amp while preserving the same or better system performance. The noise coming from the driver is filtered by the AD7942 analog input circuit 1-pole, low-pass filter made by R1 and C2 or by the external filter, if one is used.

- For ac applications, the driver needs to have a THD performance suitable to that of the AD7942. Figure 12 gives the THD versus frequency that the driver should exceed.

- For multichannel multiplexed applications, the driver amplifier and the AD7942 analog input circuit must be able to settle for a full-scale step of the capacitor array at a 14-bit level (0.006%). In the amplifier's data sheet, settling at 0.1% to 0.01% is more commonly specified. This could differ significantly from the settling time at a 14-bit level and should be verified prior to driver selection.

Table 9. Recommended Driver Amplifiers.

Amplifier	Typical Application
AD8021	Very low noise and high frequency
AD8022	Low noise and high frequency
OP184	Low power, low noise, and low frequency
AD8605, AD8615	5 V single-supply, low power
AD8519	Small, low power and low frequency
AD8031	High frequency and low power

Voltage Reference Input

The AD7942 voltage reference input, REF, has a dynamic input impedance and should therefore be driven by a low impedance source with efficient decoupling between the REF and GND pins as explained in the Layout section.

When REF is driven by a very low impedance source, e.g., a reference buffer using the AD8031 or the AD8605, a 10 μF (X5R, 0805 size) ceramic chip capacitor is appropriate for optimum performance.

If an unbuffered reference voltage is used, the decoupling value depends on the reference used. For instance, a 22 μF (X5R, 1206 size) ceramic chip capacitor is appropriate for optimum performance using a low temperature drift ADR43x reference.

If desired, smaller reference decoupling capacitor values down to 2.2 μF can be used with a minimal impact on performance, especially DNL.

Power Supply

The AD7942 is specified over a wide operating range from 2.3 V to 5.5 V. It has, unlike other low voltage converters, a noise low enough to design a low supply (2.5V) 14-bit resolution system with respectable performance. It uses two power supply pins: a core supply VDD and a digital input/output interface supply VIO. VIO allows direct interface with any logic between 1.8 V and VDD. To reduce the supplies needed, the VIO and VDD can be tied together. The AD7942 is independent of power supply sequencing between VIO and VDD. Additionally, it is very insensitive to power supply variations over a wide frequency range, as shown in Figure 26, which represents PSRR over frequency.
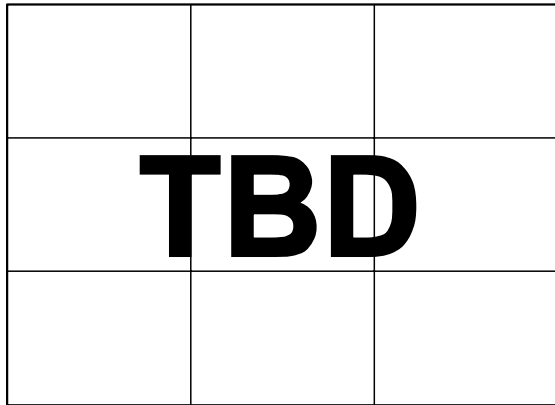
Figure 26. PSRR vs. Frequency

The AD7942 powers down automatically at the end of each conversion phase and, therefore, the power scales linearly with the sampling rate as shown in see Figure 27. This makes the part ideal for low sampling rate (even a few Hz) and low battery-powered applications.
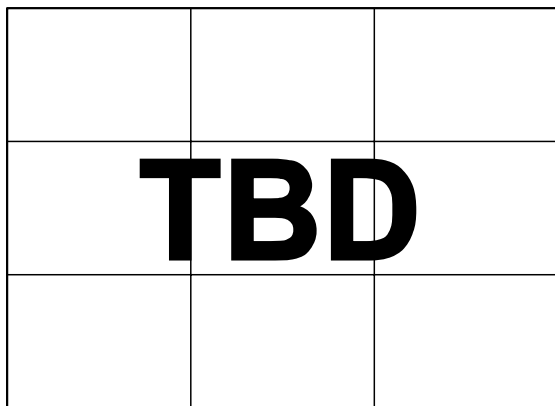

Figure 27. Operating Currents vs. Sampling Rate

Supplying the ADC from the Reference

For simplified applications, the AD7942, with its low operating current, can be supplied directly using the reference circuit, as shown in Figure 28. The reference line can be driven by either:

- The system power supply directly

- A reference voltage with enough current output capability, such as the ADR43x

- A reference buffer, such as the AD8031, that can also filter the system power supply, as shown in Figure 28.
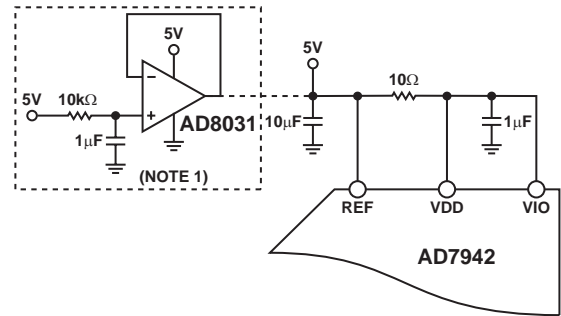
NOTE 1: OPTIONAL REFERENCE BUFFER AND FILTER

Figure 28. Example of Application Circuit

DIGITAL INTERFACE

Though the AD7942 has a reduced number of pins, it offers flexibility in its serial interface modes.

The AD7942, when in $\overline{CS}$ mode, is compatible with SPI, QSPI, digital hosts, and DSPs, e.g., Blackfin® ADSP-BF53x or ADSP-219x). This interface can use either 3-wire or 4-wire. A 3-wire interface using the CNV, SCK, and SDO signals minimizes wiring connections useful, for instance, in isolated applications. A 4-wire interface using the SDI, CNV, SCK, and SDO signals allows CNV, which initiates the conversions, to be independent of the readback timing (SDI). This is useful in low jitter sampling or simultaneous sampling applications.

The AD7942, when in chain mode, provides a daisy chain feature using the SDI input for cascading multiple ADCs on a single data line similar to a shift register.

The mode in which the part operates depends on the SDI level when the CNV rising edge occurs. The $\overline{CS}$ mode is selected if SDI is high and the chain mode is selected if SDI is low. The SDI hold time is such that when SDI and CNV are connected together, the chain mode is always selected.

In either mode, the AD7942 offers the flexibility to optionally force a start bit in front of the data bits. This start bit can be used as a BUSY signal indicator to interrupt the digital host and trigger the data reading. Otherwise, without a BUSY indicator, the user must time out the maximum conversion time prior to readback.

The BUSY indicator feature is enabled as follows:

- In the $\overline{CS}$ mode, if CNV or SDI is low when the ADC conversion ends (Figure 32 and Figure 36).
- In the chain mode, if SCK is high during the CNV rising edge (Figure 40).

$\overline{CS}$ MODE 3-Wire, No BUSY Indicator

This mode is usually used when a single AD7942 is connected to an SPI compatible digital host. The connection diagram is shown in Figure 29 and the corresponding timing is given in Figure 30.

With SDI tied to VIO, a rising edge on CNV initiates a conversion, selects the $\overline{CS}$ mode, and forces SDO to high impedance. Once a conversion is initiated, it will continue to completion irrespective of the state of CNV. For instance, it could be useful to bring CNV low to select other SPI devices, such as analog multiplexers, but CNV must be returned high before the minimum conversion time and held high until the maximum conversion time to avoid the generation of the BUSY signal indicator. When the conversion is complete, the AD7942 enters the acquisition phase and powers down. When CNV goes low, the MSB is output onto SDO. The remaining data bits are

then clocked by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can be used to capture the data, a digital host also using the SCK falling edge will allow a faster reading rate provided it has an acceptable hold time. After the 14th SCK falling edge or when CNV goes high, whichever is earlier, SDO returns to high impedance.
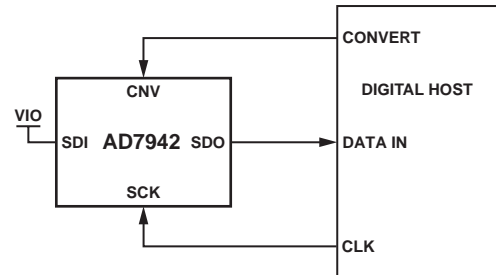

Figure 29. $\overline{CS}$ Mode 3-Wire, No BUSY Indicator Connection Diagram (SDI High)
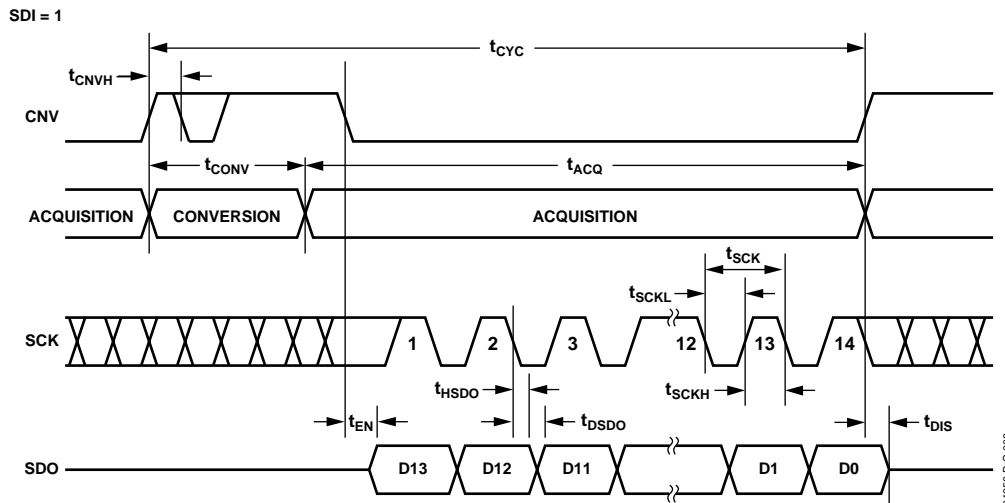

Figure 30. $\overline{CS}$ Mode 3-Wire, No BUSY Indicator Serial Interface Timing (SDI High)

$\overline{CS}$ Mode 3-Wire with BUSY Indicator

This mode is usually used when a single AD7942 is connected to an SPI compatible digital host having an interrupt input.

The connection diagram is shown in Figure 31 and the corresponding timing is given in Figure 32.

With SDI tied to VIO, a rising edge on CNV initiates a conversion, selects the $\overline{CS}$ mode, and forces SDO to high impedance. SDO is maintained in high impedance until the completion of the conversion irrespective of the state of CNV. Prior to the minimum conversion time, CNV could be used to select other SPI devices, such as analog multiplexers, but CNV must be returned low before the minimum conversion time and held low until the maximum conversion time to guarantee the generation of the BUSY signal indicator. When the conversion is complete, SDO goes from high impedance to low. With a pull-up on the SDO line, this transition can be used as an interrupt signal to initiate the data reading controlled by the digital host. The AD7942 then enters the acquisition phase and powers

down. The data bits are then clocked out, MSB first, by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can be used to capture the data, a digital host also using the SCK falling edge will allow a faster reading rate provided it has an acceptable hold time. After the optional 15th SCK falling edge, or when CNV goes high, whichever is earlier, SDO returns to high impedance.
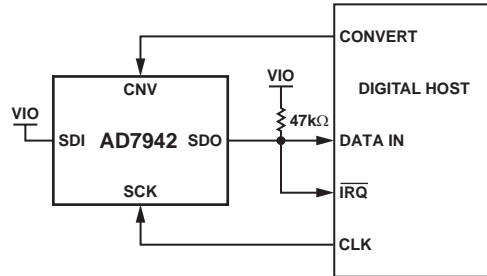

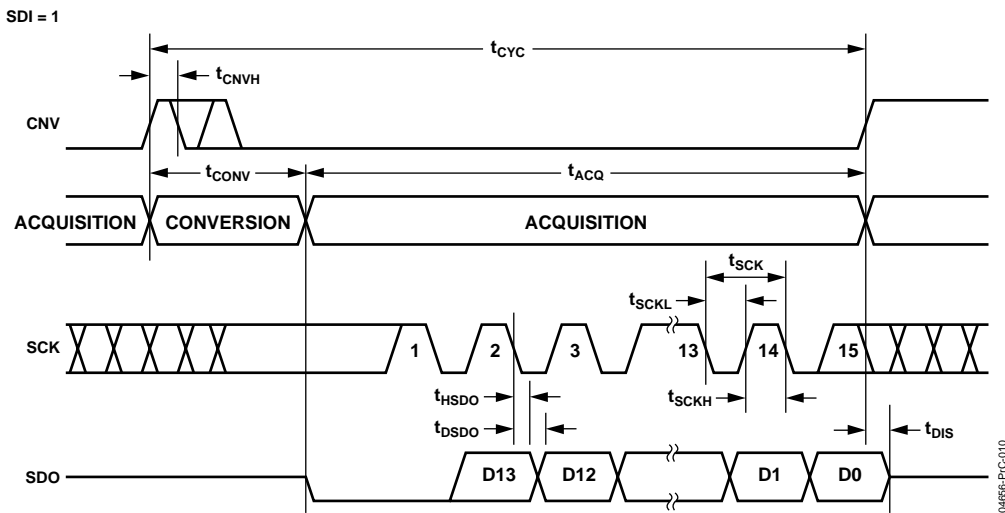*Figure 31. $\overline{CS}$ Mode 3-Wire with BUSY Indicator Connection Diagram (SDI High)*

Figure 32. $\overline{CS}$ Mode 3-Wire with BUSY Indicator Serial Interface Timing (SDI High)

$\overline{CS}$ Mode 4-Wire, No BUSY Indicator

This mode is usually used when multiple AD7942s are connected to an SPI compatible digital host.

A connection diagram example using two AD7942s is shown in Figure 33 and the corresponding timing is given in Figure 34.

With SDI high, a rising edge on CNV initiates a conversion, selects the $\overline{CS}$ mode, and forces SDO to high impedance. In this mode, CNV must be held high during the conversion phase and the subsequent data readback (if SDI and CNV are low, SDO is driven low). Prior to the minimum conversion time, SDI could be used to select other SPI devices, such as analog multiplexers,

but SDI must be returned high before the minimum conversion time and held high until the maximum conversion time to avoid the generation of the BUSY signal indicator. When the conversion is complete, the AD7942 enters the acquisition phase and powers down. Each ADC result can be read by bringing low its SDI input which consequently outputs the MSB onto SDO. The remaining data bits are then clocked by subsequent SCK driving edges. The data is valid on both SCK edges. Although the nondriving edge can be used to capture the data, a digital host also using the SCK falling edge will allow a faster reading rate provided it has an acceptable hold time. After the 14th SCK falling edge, or when SDI goes high, whichever is earlier, SDO returns to high impedance and another AD7942 can be read.
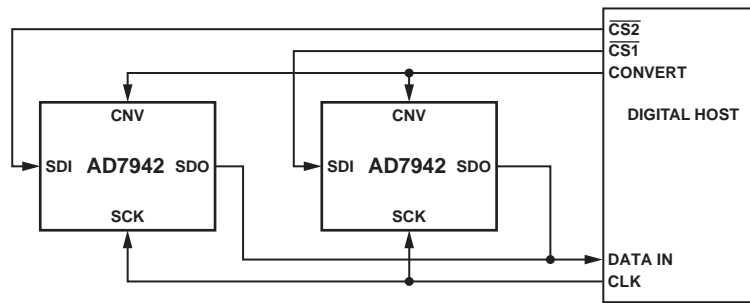

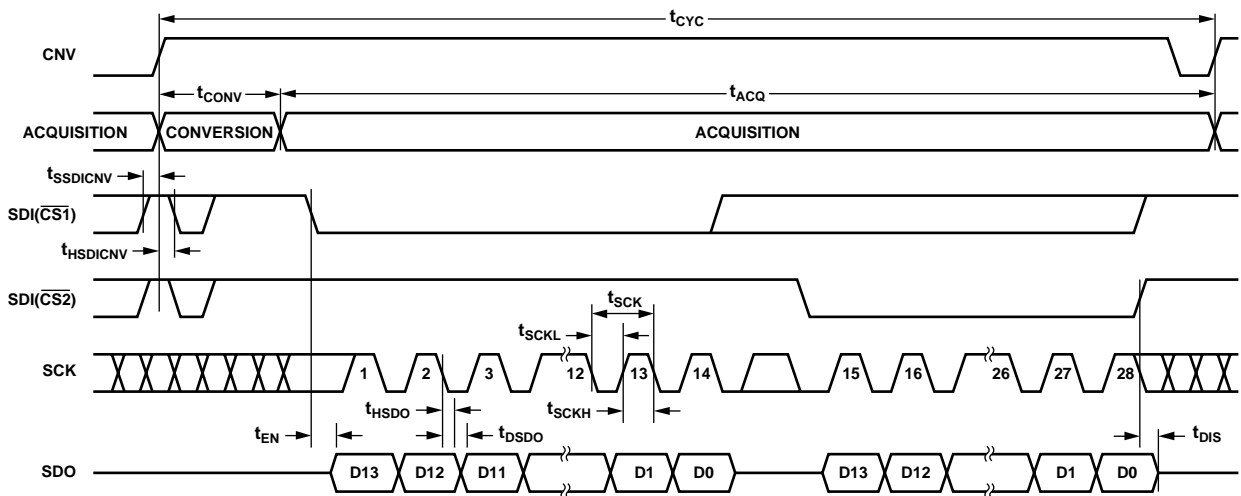Figure 33. $\overline{CS}$ Mode 4-Wire, No BUSY Indicator Connection Diagram

Figure 34. $\overline{CS}$ Mode 4-Wire, No BUSY Indicator Serial Interface Timing

$\overline{CS}$ Mode 4-Wire with BUSY Indicator

This mode is usually used when a single AD7942 is connected to an SPI compatible digital host, which has an interrupt input, and it is desired to keep CNV, which is used to sample the analog input, independent of the signal used to select the data reading. This requirement is particularly important in applications where low jitter on CNV is desired.

The connection diagram is shown in Figure 35 and the corresponding timing is given in Figure 36.

With SDI high, a rising edge on CNV initiates a conversion, selects the $\overline{CS}$ mode, and forces SDO to high impedance. In this mode, CNV must be held high during the conversion phase and the subsequent data readback (if SDI and CNV are low, SDO is driven low). Prior to the minimum conversion time, SDI could be used to select other SPI devices, such as analog multiplexers, but SDI must be returned low before the minimum conversion time and held low until the maximum conversion time to guarantee the generation of the BUSY signal indicator. When the conversion is complete, SDO goes from high impedance to

low. With a pull-up on the SDO line, this transition can be used as an interrupt signal to initiate the data readback controlled by the digital host. The AD7942 then enters the acquisition phase and powers down. The data bits are then clocked out, MSB first, by subsequent SCK driving edges. The data is valid on both SCK edges. Although the rising edge can be used to capture the data, a digital host also using the SCK falling edge will allow a faster reading rate provided it has an acceptable hold time. After the optional 15th SCK falling edge, or SDI going high, whichever is earlier, the SDO returns to high impedance.
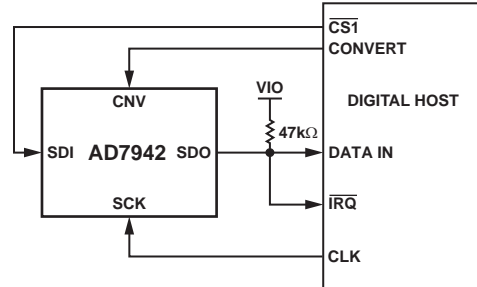

Figure 35. $\overline{CS}$ Mode 4-Wire with BUSY Indicator Connection Diagram
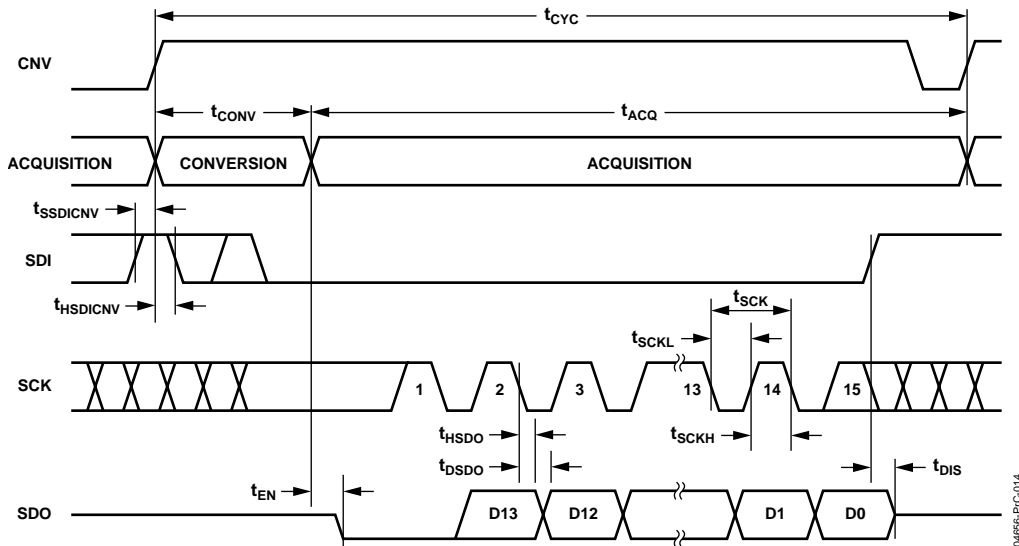

Figure 36. $\overline{CS}$ Mode 4-Wire with BUSY Indicator Serial Interface Timing

Chain Mode, No BUSY Indicator

This mode can be used to daisy chain multiple AD7942s on a 3-wire serial interface. This feature is useful for reducing component count and wiring connections, e.g., in isolated multiconverter applications or for systems with a limited interfacing capacity. Data readback is analogous to clocking a shift register.

A connection diagram example using two AD7942s is shown in Figure 37 and the corresponding timing is given in Figure 38.

When SDI and CNV are low, SDO is driven low. With SCK low, a rising edge on CNV initiates a conversion, selects the chain mode, and disables the BUSY indicator. In this mode, CNV is held high during the conversion phase and the subsequent data readback. When the conversion is complete, the MSB is output onto SDO and the AD7942 enters the acquisition phase and powers down. The remaining data bits stored in the internal shift register are then clocked by subsequent SCK falling edges. For each ADC, SDI feeds the input of the internal shift register and is clocked by the SCK falling edge. Each ADC in the chain outputs its data MSB first, and 14 × N clocks are required to readback the N ADCs. The data is valid on both SCK edges. Although the rising edge can be used to capture the data, a digital host also using the SCK falling edge will allow a faster reading rate and, consequently more AD7942s in the chain, provided the digital host has an acceptable hold time. The maximum conversion rate may be reduced due to the total readback time. For instance, with a 5 ns digital host set-up time and 3 V interface, up to six AD7942s running at a conversion rate of 250 kSPS can be daisy-chained on a 3-wire port.
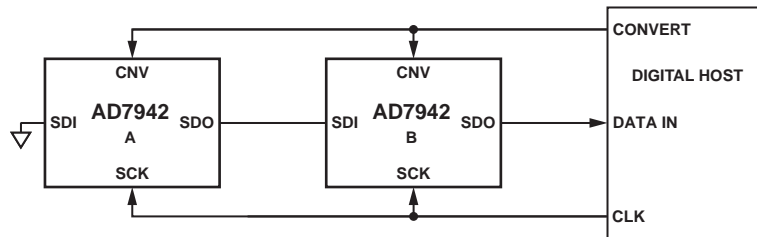

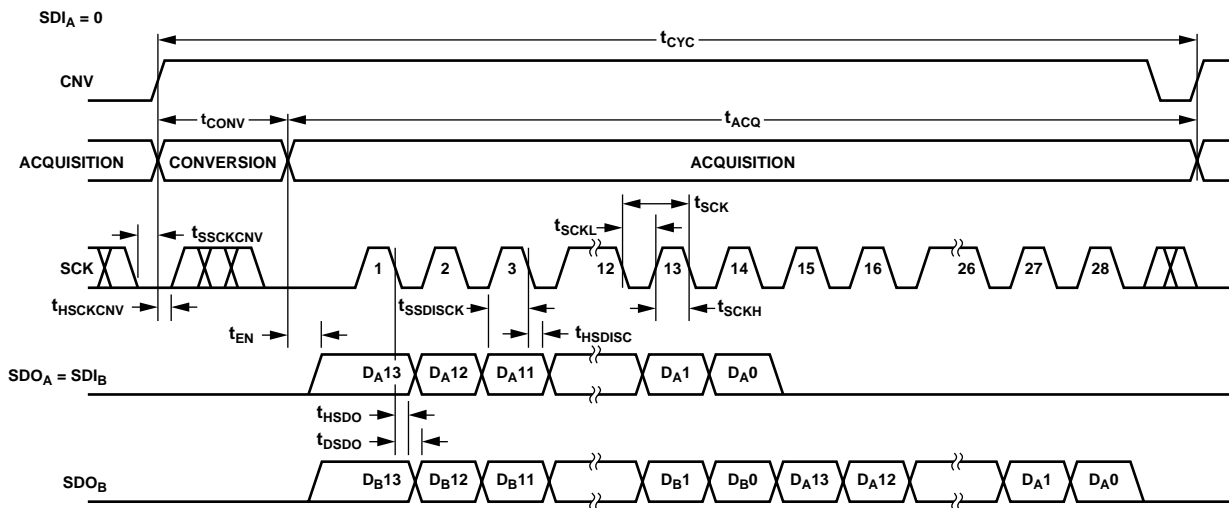Figure 37. Chain Mode, No BUSY Indicator Connection Diagram

Figure 38. Chain Mode, No BUSY Indicator Serial Interface Timing

Chain Mode with BUSY Indicator

This mode can also be used to daisy chain multiple AD7942s on a 3-wire serial interface while providing a BUSY indicator. This feature is useful for reducing component count and wiring connections, e.g., in isolated multiconverter applications or for systems with a limited interfacing capacity. Data readback is analogous to clocking a shift register.

A connection diagram example using three AD7942s is shown in Figure 39 and the corresponding timing is given in Figure 40.

When SDI and CNV are low, SDO is driven low. With SCK high, a rising edge on CNV initiates a conversion, selects the chain mode, and enables the BUSY indicator feature. In this mode, CNV is held high during the conversion phase and the subsequent data readback. When all ADCs in the chain have completed their conversions, the nearend ADC (ADC C in

Figure 39) SDO will be driven high. This transition on SDO can be used as a BUSY indicator to trigger the data readback controlled by the digital host. The AD7942 then enters the acquisition phase and powers down. The data bits stored in the internal shift register are then clocked out, MSB first, by subsequent SCK falling edges. For each ADC, SDI feeds the input of the internal shift register and is clocked by the SCK falling edge. Each ADC in the chain outputs its data MSB first, and $14 \times N + 1$ clocks are required to readback the N ADCs. Although the rising edge can be used to capture the data, a digital host also using the SCK falling edge will allow a faster reading rate and, consequently more AD7942s in the chain, provided the digital host has an acceptable hold time. For instance, with a 5 ns digital host set-up time and 3 V interface, up to six AD7942s running at a conversion rate of 250 kSPS can be daisy-chained to a single 3-wire port.
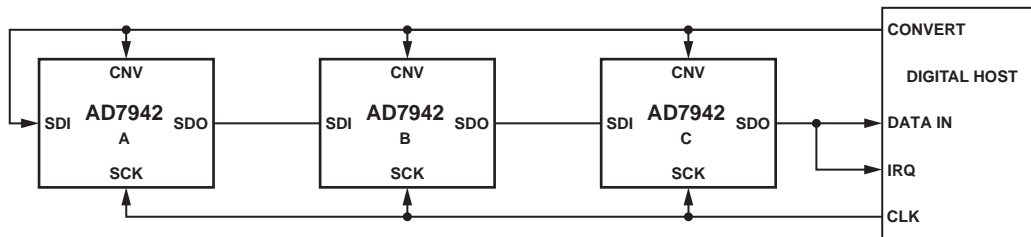

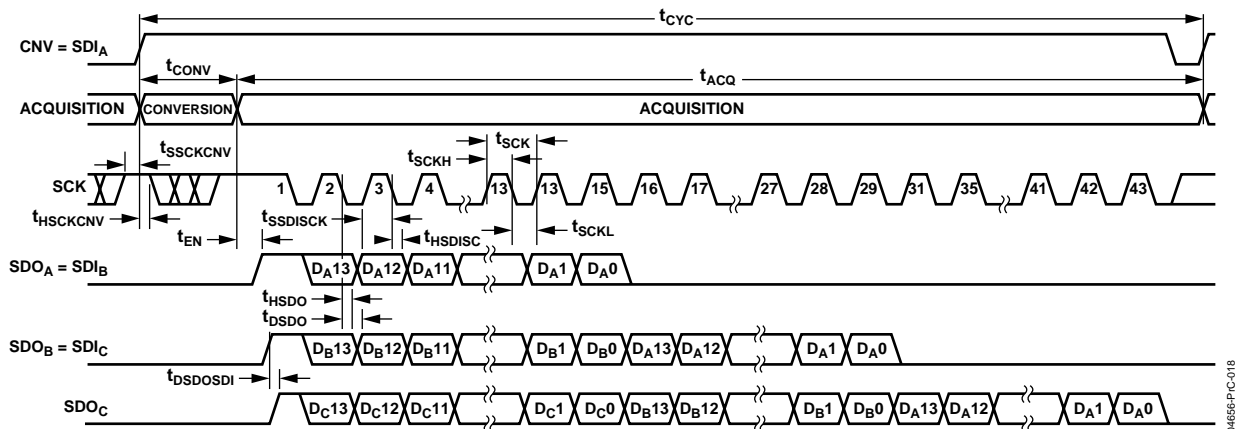Figure 39. Chain Mode with BUSY Indicator Connection Diagram

Figure 40. Chain Mode with BUSY Indicator Serial Interface Timing

APPLICATION HINTS

LAYOUT

The printed circuit board that houses the AD7942 should be designed so that the analog and digital sections are separated and confined to certain areas of the board. The pinout of the AD7942 with all its analog signals on the left side and all its digital signals on the right side eases this task.

Avoid running digital lines under the device because these couple noise onto the die, unless a ground plane under the AD7942 is used as a shield. Fast switching signals, such as CNV or clocks, should never run near analog signal paths. Crossover of digital and analog signals should be avoided

At least one ground plane should be used. It could be common or split between the digital and analog section. In such a case, it should be joined underneath the AD7942s.

The AD7942 voltage reference input REF has a dynamic input impedance and should be decoupled with minimal parasitic inductances. That is done by placing the reference decoupling ceramic capacitor close to, and ideally right up against, the REF and GND pins and connect these pins with wide, low impedance traces.

Finally, the power supply VDD and VIO of the AD7942 should be decoupled with ceramic capacitors, typically 100 nF, placed close to the AD7942 and connected using short and large traces to provide low impedance paths and reduce the effect of glitches on the power supply lines.

An example of layout following these rules is shown in Figure 41 and Figure 42.

EVALUATING THE AD7942'S PERFORMANCE

Other recommended layouts for the AD7942 are outlined in the evaluation board for the AD7942 (EVAL-AD7942). The evaluation board package includes a fully assembled and tested evaluation board, documentation, and software for controlling the board from a PC via the EVAL-CONTROL BRD2.
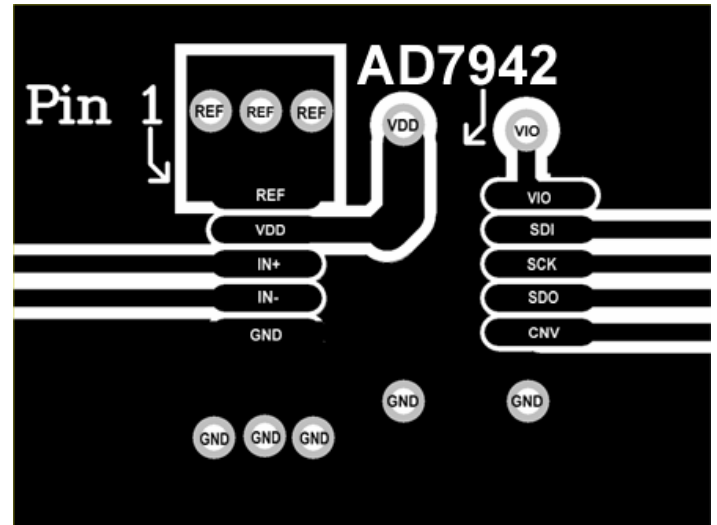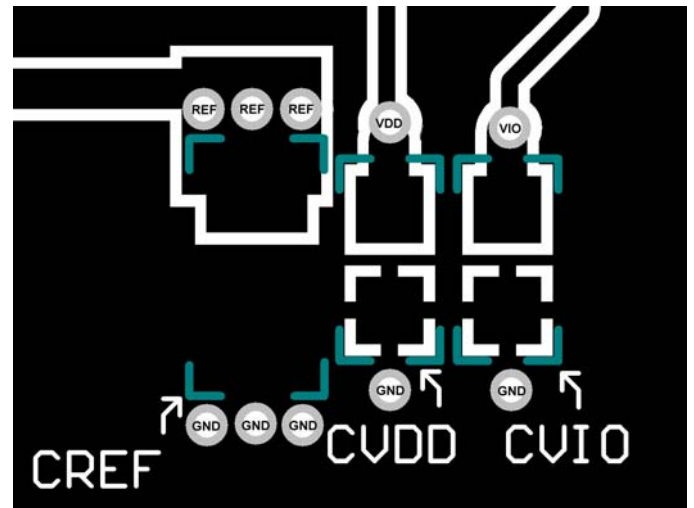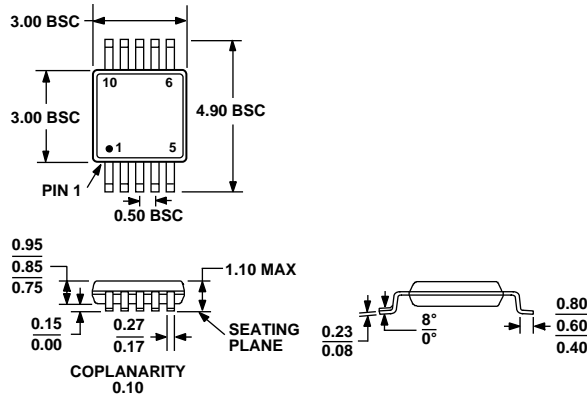

Figure 41. Example of Layout of the AD7942 (Top Layer)

Figure 42. Example of Layout of the AD7942 (Bottom Layer)

OUTLINE DIMENSIONS

COMPLIANT TO JEDEC STANDARDS MO-187BA

Figure 43.10-Lead Micro Small Outline Package [MSOP]
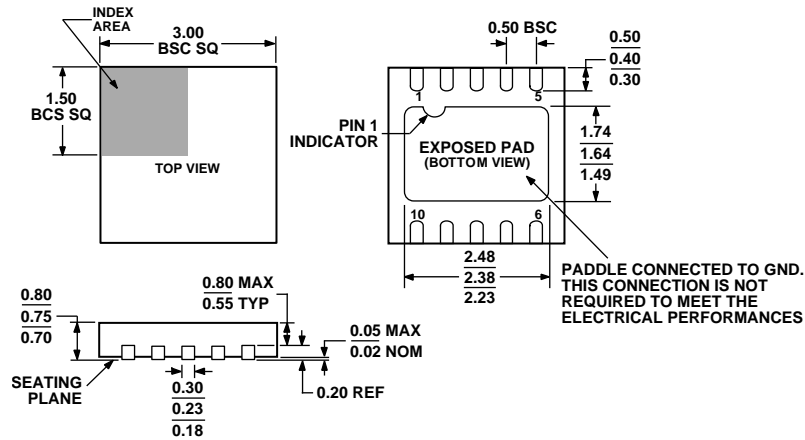*(RM-10)*
Dimensions shown in millimeters

Figure 44. 10-Lead Lead Frame Chip Scale Package [QFN (LFCSP)]
3 mm × 3 mm Body
(CP-10)
Dimensions shown in millimeters

ORDERING GUIDE

Models	Temperature Range	Package (Option)	Transport Media, Quantity	Brand
AD7942BRM	–40°C to +85°C	MSOP (RM-10)	Tube, 50	C1N
AD7942BRMRL7	–40°C to +85°C	MSOP (RM-10)	Reel, 1,000	C1N
AD7942BCPWP	–40°C to +85°C	QFN [LFCSP] (CP-10)	Waffle pack, 50	C1N
AD7942BCPRL7	–40°C to +85°C	QFN [LFCSP] (CP-10)	Reel, 1,500	C1N
EVAL-AD7942CB[6]		Evaluation Board		
EVAL-CONTROL BRD2[7]		Controller Board		
EVAL-CONTROL BRD3[2]		Controller Board		

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[6] This board can be used as a standalone evaluation board or in conjunction with the EVAL-CONTROL BRDx for evaluation/demonstration purposes.
[7] These boards allow a PC to control and communicate with all Analog Devices evaluation boards ending in the CB designators.

NOTES

www.analog.com