= PRELIMINARY = AK2397

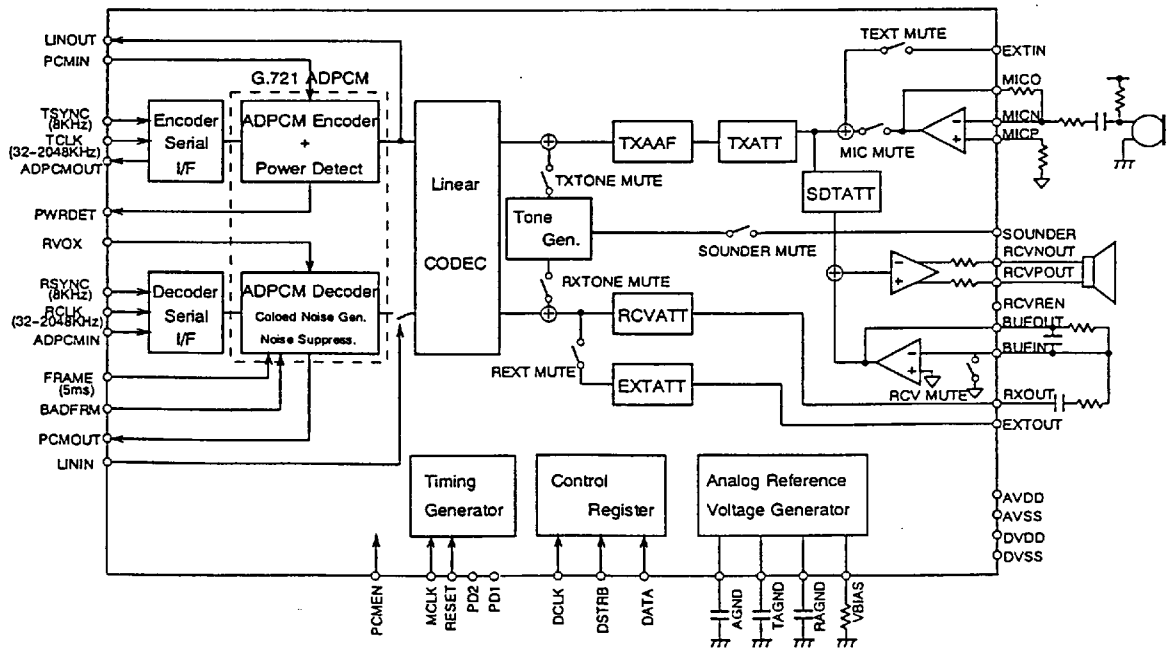
ADPCM CODEC for Digital Cordless Telephone

Features

- ADPCM (Full Duplex, Synchronous operation) which conforms to ITU-T Rec. G.721. (Previously CCITT Rec. G.721, 1988)
- Noise suppression function* for transmission error
- Power detection function for VOX transmission
- Colored noise generator function for VOX reception
- 14-bit linear CODEC
- Mic amplifier and receiver amplifier for ceramic type receiver
- Programmable dual tone generator
- RX volume and TX volumes
- Analog reference power supply
- System Clock: 19.2 MHz
- Power down mode
- Operating voltage: 2.7～3.6V single power supply
- Current consumption: 6.8 mA typ. (Operating mode)
- 48 pin LQFP package

* Patent pending (Japan)

Block Diagram

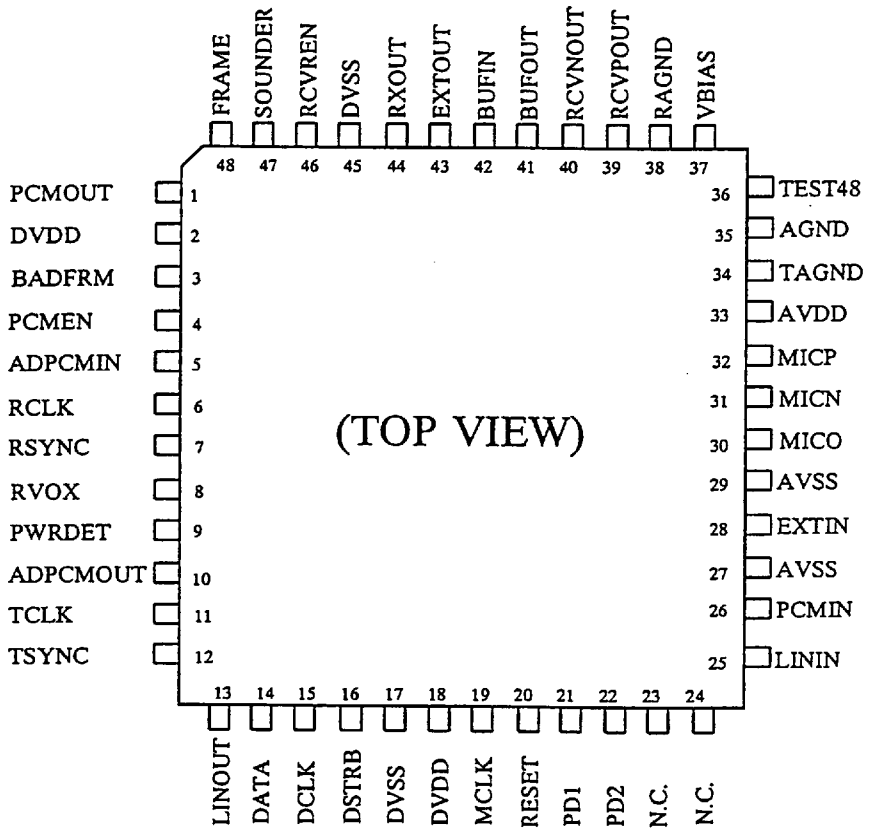


Description

The AK2397 is a 1-chip voice processing LSI developed for digital cordless telephones (PHS, Personal Handy-phone System) which houses a 14 bit linear CODEC, ADPCM transcoder, mic/receiver amp, side tone path, programmable dual tone generator and other functions. It also includes noise suppression function*, and is capable of suppressing noise caused by transmission errors in the wireless line.

* Patent pending (Japan)

■ Pin Arrangement



Pin Functions

No.	Name	I/O	Function	Remark
			Power Supply Pins	
33	AVDD	PWR	Analog power supply input pin. (3 V typ.)	
27, 29	AVSS	GND	Analog ground pins.	
2, 18	DVDD	PWR	Digital power supply input pins. (3 V typ.)	
17, 45	DVSS	GND	Digital ground pins.	
			· Analog Reference Pins	
34	TAGND	AO	Transmission system analog signal ground reference voltage output pin. In full power down mode, TAGND is high-Z output.	Note 1
38	RAGND	AO	Receiving system analog signal ground reference voltage output pin. In full power down mode, RAGND is high-Z output.	Note 1
35	AGND	AO	Analog signal ground reference voltage output pin. In full power down mode, RAGND is high-Z output.	Note 1
37	VBIAS	AO	Internal amp operating current setting resistor connection pin. In full power down mode, RAGND is AVSS level output.	Note 2
			Speech / Tone Interface pins	
28	EXTIN	AI	External analog signal input pin.	
32	MICP	AI	Mic signal amplifier non-inverted input pin.	
31	MICN	AI	Mic signal amplifier inverted input pin.	
30	MICOP	AO	Mic signal gain adjustment output pin	
47	SOUNDER	DO	SOUNDER signal output pin.	
39	RCVPOUT	AO	Differential analog output (+) pin.	
40	RCVNOUT	AO	Differential analog output (-) pin.	
43	EXTOUT	AO	Received signal external output pin.	
44	RXOUT	AO	Received signal output pin.	
42	BUFIN	AI	Received signal buffer amp input pin.	
41	BUFOUT	AO	Received signal buffer amp output pin.	

No.	Name	I/O	Function	Remark
			System Clock/Reset/Power Down Pins	
20	RESET	DI	Reset signal input pin. The control registers are initialized by reset input. Please do reset operation ,when power is on. "1" : Reset "0" : Normal operation	
19	MCLK	AI	19.2 MHz master clock input pin. Please input clipped sine signal after DC cut.	
21 22	PD1 PD2	DI	Power down control pin. PD1 PD2 0 0 Normal operation. 1 0 CODEC power down. X 1 Full power down.	
46	RCVREN	DI	Receiver amp power down control pin "1" : Active "0" : Power down	
			ADPCM Interface Pins	
10	ADPCMOUT	DO	ADPCM data output pin. The data are output from the MSB synchronous with the rising edge of TCLK and TSYNC. This pin is 3 state output.	
5	ADPCMIN	DI	ADPCM data input pin. The data are input from the MSB synchronous with the rising edge of RCLK and RSYNC, and ratched with falling edge of RCLK.	
11	TCLK	DI	Shift clock input pin for the transmitting ADPCM data. (32 kHz～2.048 MHz)	
12	TSYNC	DI	8 kHz synchronization signal input pin for the transmitting ADPCM data.	
6	RCLK	DI	Shift clock input pin for the receiving ADPCM data. (32 kHz～2.048 MHz)	
7	RSYNC	DI	8 kHz synchronization signal input pin for the receiving ADPCM data.	
48	FRAME	DI	Signal which shows the heading of the TDMA frame (5 ms) for the receiving ADPCM signal. Suppression of transmitting error noise and silent interval processing are executed in frame unites. "1" : Head data of frame "0" : Rest data of frame	
8	RVOX	DI	Signal which shows the silent interval of receiving ADPCM signals. Depending on the control register setting, muting is carried out or colored noise is generated. "1" : Mute/Colored noise generation "0" : Normal operation.	
3	BADFRM	DI	This signal activates the noise suppression function. Normally, CRC error information is input If the noise suppression function is not used, set it on "0". "1" : Frame error exist "0" : Frame error don't exist	

No.	Name	I/O	Function	Remark
			ADPCM/PCM Interface Pins (Continued)	
9	PWRDET	DI	Voice detect signal for up link VOX control. The detection level and release time can be set in the control register. "1" : Voice detected "0" : Silence detected	
			User Test Interface Pins	
26	PCMIN	DI	μ-law PCM data input pin for ADPCM encoder. The data are input from MSB synchronous with RCLK and RSYNC.	Note 3 Note 5
1	PCMOUT	DO	μ-law PCM data output pin for ADPCM decoder. The data are output from MSB synchronous with RCLK and RSYNC. When PCMEN = 0, this pin output High-Z level.	Note 3 Note 5
25	LININ	DI	Linear PCM data input for D/A converter. The data are input from MSB synchronous with RCLK and RSYNC	Note 4 Note 5
13	LININ	DI	Linear PCM data output for A/D converter. The data are output from MSB synchronous with RCLK and RSYNC. This pin is 3-state output. When PCMEN=0, this pin output High-Z level.	Note 4 Note 5
4	PCMEN	DI	μ-law PCM/linear PCM data interface enable pin. This pin is pulled down in the IC. "1" : Enable "0" : Disable	Note 5
			CPU Interface Pins	
14	DATA	DI	Serial data input pin to the control register. Data include the address + data, and are 13 bits in length. They are input synchronous with the rising edge of DCLK and are latched with the rising edge of DSTRB.	
15	DCLK	DI	Control register clock input pin.	
16	DSTRB	DI	Control register strobe input pin.	
			Other Pins	
36	TEST48	DI	Test mode input pins. This pin is pulled down in the IC. Please use with L input or open.	
23, 24	N. C	N. C	No connection pins.	

Explanatory notes)

PWR: Power Supply, GND: Ground
AO : Analog Output, AI : Analog Input
DO : Digital Output, DI : Digital Input

Note 1) Please connect capacitors for stabilization.
Note 2) Please connect a resistor (47k$\Omega \pm 5\%$).
Note 3) If RCLK < 64kHz, correct operation of μ-low data interface is not guaranteed.
Note 4) If RCLK < 128 kHz correct operation of linear data interface is not guaranteed.
Note 5) When user test interface is in use, please use with RCLK=TCLK. RSYNC=TSYCN.

Absolute Maximum Ratings

Parameters	Symbol	min	max	Units
Power Supply Voltage (Note 1, 2)				
Digital Power Supply	DVDD	-0.3	7.0	V
Analog Power Supply	AVDD	-0.3	7.0	V
Digital Input Voltage	V_{TD}	-0.3	DVDD + 0.3	V
Analog Input Voltage	V_{TA}	-0.3	AVDD + 0.3	V
Storage Temperature	T_{stg}	-55	125	℃

Note 1) Voltages are all given with the ground pin as reference. AVSS, DVSS = 0V
Note 2) Condition necessary for normal operation: AVDD ≧ DVDD
Caution: If this device is used under conditions which exceed these values, the device may be destroyed. Also, normal operation cannot be guaranteed.

Recommended Operating Conditions

Parameter	Symbol	min	typ	max	Units
Power Supply Voltage					
Digital Power Supply	DVDD	2.7	3.0	3.6	V
Analog Power Supply	AVDD	2.7	3.0	3.6	V
Operating Temperature Range	T_a	-20		70	℃

Caution: Voltages are all given with the ground pin as reference. AVSS, DVSS = 0V

Electrical Characteristics

■ DC Characteristics

DVDD, AVDD=2.7～3.6V Ta=-20～70℃
('Typ' are value at DVDD, AVDD=3.0 and room temperature)

Parameter	Pin Name	Symbol	min	typ	max	Units	Remarks
Digital Power Supply Current	DVDD	I DD		1.2		mA	Note 1)
Analog Power Supply Current	AVDD	I DA		5.6		mA	Note 1)
Power Down Current Mode 2 (CODEC power down) Mode 1 (Full power down) Mode 0 (Full power down)		 I DD2 I DD1 I DD0		 2.6 300 10	 20	 mA μA μA	 Note 2) Note 3) Note 4)
High Level Input Voltage	DI	VIH	0.7DVDD			V	
Low Level Input Voltage	DI	VIL			0.3DVDD	V	
High Level Output Voltage	DO	VOH	DVDD-0.5			V	I_{OH}=-1mA
Low Level Output Voltage	DO	VOL			0.5	V	I_{OL}= 2mA
Input Leakage Current	DI	I i			±10	μA	
Reference Voltage Output	TAGND RAGND AGND	VREF		1/2		DVDD	

Note 1: Active mode. Supplying clocks and analog input. No load at all output pins without ADPCMOUT pin. ADPCMOUT pin is connected to ADPCMIN pin. Receiver amp is active.

Note 2: CODEC P.D. mode. Supplying clocks and analog input. No load at all output pins without ADPCMOUT pin. ADPCMOUT pin is connected to ADPCMIN pin. Receiver amp is active.

Note 3: Full P.D. mode. Supplying clocks. All analog input pins are connected to TAGND. All digital input without clock are L. Receiver amp is P.D.

Note 4: Full P.D. mode. Supplying no clocks. All analog input pins are connected to TAGND. All digital input are L. Receiver amp is P.D.
Max. spec is design guaranteed value.

■ Transmitting Characteristics

DVDD, AVDD=2.7～3.6V Ta=-20～70℃ All gain setting are 0dB.
('Typ' are value at DVDD, AVDD=3.0 and room temperature)

Parameter	Condition		min	typ	max	Units	Remarks
Signal to Total Distortion (A→D) EXTIN→LINOUT	1020Hz	-45dBm0	24			dB	with C-Wgt Filter
	Tone	-40dBm0	29				
	Method	0, -30dBm0	35				
Signal to Total Distortion (D→A) LININ→EXTOUT	1020Hz	-45dBm0	24				
	Tone	-40dBm0	29				
	Method	0, -30dBm0	35				
Gain Tracking (A→D) EXTIN→LINOUT	1020Hz	-55dBm0	-0.9		0.9	dB	Ref =-10dBm0
	Tone	-50dBm0	-0.5		0.5		
	Method	0, -50dBm0	-0.2		0.2		
Gain Tracking (D→A) LININ→EXTOUT	1020Hz	-55dBm0	-0.9		0.9		
	Tone	-50dBm0	-0.4		0.4		
	Method	0, -50dBm0	-0.2		0.2		
Analog Input Level	0dBm0	EXTIN →LINOUT	0.450	0.501	0.551	Vrms	
Analog Output Level		LININ →EXTOUT	0.450	0.501	0.551		
Idle Channel Noise (A/D)	LINOUT EXTIN = AGND				20	dBrnc0	
Idle Channel Noise (D/A)	EXTOUT LININ = +0 code				15		
Cross Talk (A/D→D/A)	1020Hz 0dBm0 Input				-65	dB	
Cross Talk (D/A→A/D)					-65		
Frequency Response (A/D) EXTIN→LINOUT	Base Frequency = 1020Hz	0.06kHz	24			dB	
		0.2kHz	0		2.5		
		0.3～3.0kHz	-0.25		0.25		
		3.0～3.4kHz	-0.25		0.8		
		3.6kHz	0				
		3.78kHz	6.5				
Frequency Response (D/A) LININ→EXTOUT	Base Frequency = 1020Hz	0.3～3.0kHz	-0.25		0.25		
		3.0～3.4kHz	-0.25		0.8		
		3.6kHz	0				
		3.78kHz	6.5				

■ Microphone and receiver amp characteristics

Parameter	Condition	min	typ	max	Unit	Remarks
Mic Amp Max. output	MICO		2.04		Vpp	
Mic. Amp Gain	MICO	0		40	dB	Note 1)
Receiver Amp Max. output	RCVPOUT, RCVNOUT ZL=140nF		2.04		Vpp	
Receiver Amp Gain error	BUFOUT -> RCVPOUT, RCVNOUT ZL=140nF	-1.5		1.5	dB	

Note 1 : Design guaranteed value.

■ Tone gen. characteristics

Parameter	Condition	min	typ	max	Unit	Remarks
Single Tone Max. output	TATT1/2=0dB, RTN=1 Measured at EXTOUT		1.2		Vpp	Note 1)
Distortion	TATT1/2=0dB, RTN=1 Measured at EXTOUT		-30		dB	Note 2)

Note 1 : Tone1 is on and tone2 is off, or tone1 is off and tone2 is on.

Note 2 : Distortion is defined as "the ratio of the total power of all extraneous frequencies in the voiceband above 500Hz accompanying the signal to the power of the frequency pair."
Mathematically distortion can be expressed in dB as:

$$Dist[dB]=20\times log\frac{\sqrt{(V1)^2+(V2)^2+...+(VN)^2}}{\sqrt{(VL)^2+(VH)^2}}$$

where (V1).. (V2) are extraneous frequency (i.e., intermodulation and harmonic) components in the 500 Hz to 3400 Hz band and VL and VH are the individual frequency components of the DTMF signal.

■ ATT characteristics

Parameter		Condition	min	typ	max	Unit	Remarks
Gain Error	TXATT				±0.25	dB	
	RCVATT				±1.5		
	EXTATT				±3.0		
	SDTATT				±2.0		
	TATT1, 2				±1.5		

■ MCLK Characteristics

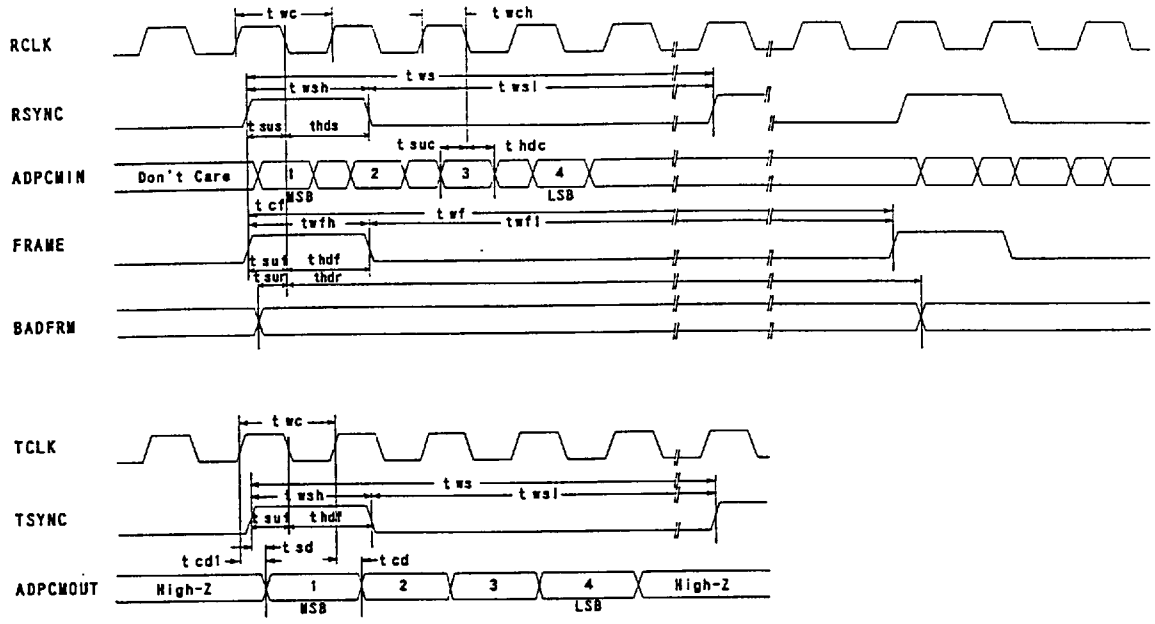
Parameter	Condition	min	typ	max	Unit	Remarks
MCLK frequency	MCLK		19.2		MHz	
MCLK input level	MCLK	0.5		1.5	Vpp	Sin wave input

■ AC Characteristics

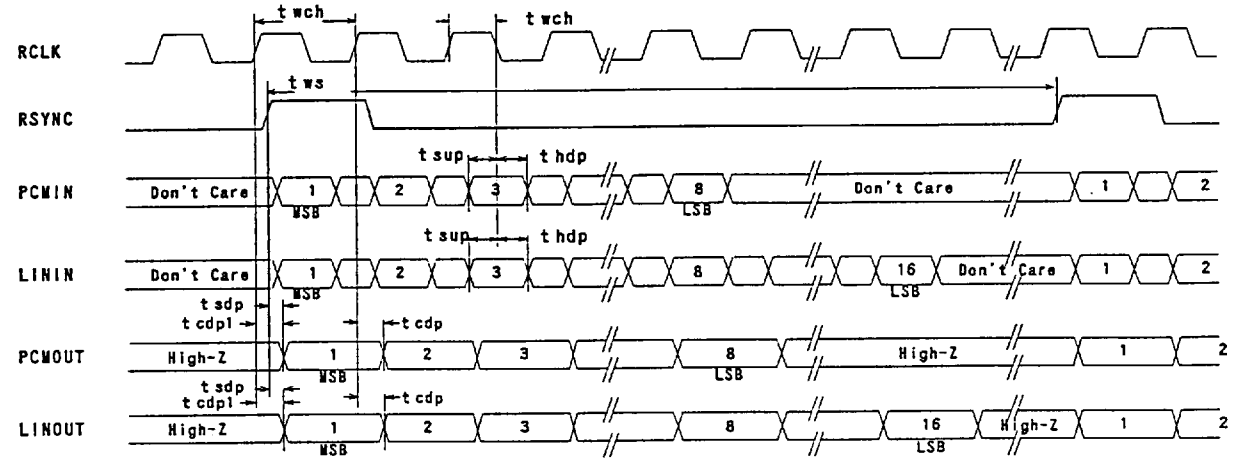
Parameter	Symbol	min	typ	max	Units	Remark
MCLK Frequency	f mck		19.2		MHz	
MCLK Duty		40	50	60	%	
ADPCM Interface Timing						
TCLK/RCLK Cycle Time	t wc	1/256		1/4	t ws	
TCLK/RCLK High Level Width	t wch		1/2		t wc	
TSYNC/RSYNC Cycle Time	t ws		125		μs	
TSYNC/RSYNC Setup Time	t sus	100			ns	
TSYNC/RSYNC Hold Time	t hds	100			ns	
TSYNC/RSYNC Pulse High Level Width	t wsh	200			ns	
TSYNC/RSYNC Pulse Low Level Width	t wsl	1			t wc	
ADPCMIN Setup Time	t suc	100			ns	
ADPCMIN Hold Time	t hdc	100			ns	
FRAME Cycle Time	t wf		5		ms	
FRAME Setup Time	t suf	100			ns	
FRAME Hold Time	t hdf	100			ns	
FRAME Pulse High Level Width	t wfh	200			ns	
FRAME Pulse Low Level Width	t wfl	1			t wc	
BADFRM Setup Time	t sur	100			ns	
BADFRM Hold Time	t hdr	100			ns	
ADPCMOUT MSB Delay Time (to TSYNC)	t sd			55	ns	Note-1
ADPCMOUT MSB Delay Time (to TCLK)	t cdl			55	ns	Note-1
ADPCMOUT Delay Time (to TCLK)	t cd			55	ns	Note-1
Test Interface Timing						
PCMIN/LININ Setup Time	t sup	100			ns	
PCMIN/LININ Hold Time	t hdp	100			ns	
PCMOUT/LINOUT MSB Delay Time (to RSYNC)	t sdp			55	ns	Note-1
PCMOUT/LINOUT MSB Delay Time (to RCLK)	t cdpl			55	ns	Note-1
PCMOUT/LINOUT Delay Time (to RCLK)	t cdp			55	ns	Note-1
CPU Interface Timing						
DCLK Frequency	f dck			3	MHz	
DATA Setup Time	t sdc	100			ns	
DATA Hold Time	t hddc	100			ns	
DSTRB Pulse High Level Width	t wds	1			1/f dck	
DSTRB Pulse Delay Time	t ds	333			ns	
DSTRB Pulse Low Level Setup Time	t sud	0			ns	

Note-1) When capacitance lord = 50pF.

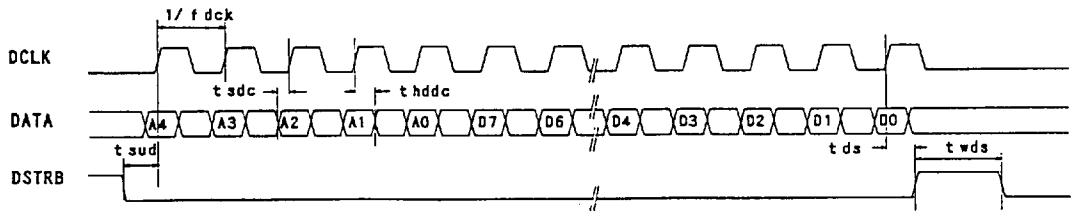
■ ADPCM Interface Timing diagram



■ Test Interface Timing diagram



■ CPU Interface Timing diagram



Explanation of Operation

■ Register Map

Address (HEX)	Name	D7	D6	D5	D4	D3	D2	D1	D0
0 0	VAD Parameter	TH LEVEL				RELEASE TIME			
0 1	Noise Generation Parameter	x	LP	NOUT	M/N	NOISE LEVEL			
0 2	Transmitting Path Control	LCT	TTN	TEXT	MIC	TXATT			
0 3	Receiving Path Control 1	LCR	REXT	RCV	EXTATT		RCVATT		
0 4	Receiving Path Control 2	x	LIN	PCM	SNDR	RTN	SDTATT		
0 5	Tone Source Parameter 1	TFREQ1							
0 6	Tone Source Parameter 2	TFREQ2							
0 7	Tone Source Parameter 3	TM2	TM1	TATT2			TATT1		
0 8 0 9 0 A 0 B 0 C 0 D	Noise Suppression Parameter 1	ATT VAL 1 ATT VAL 2 ATT VAL 3 ATT VAL 4 ATT VAL 5 ATT VAL 6				STATE WIDTH 1 STATE WIDTH 2 STATE WIDTH 3 STATE WIDTH 4 STATE WIDTH 5 STATE WIDTH 6			
0 E 0 F 1 0	Noise Suppression Parameter 2	x x x	LIMIT VAL 2 LIMIT VAL 4 LIMIT VAL 6			x x x	LIMIT VAL 1 LIMIT VAL 3 LIMIT VAL 5		
1 1	Power Down Mode	x	x	x	x	x	x	RPD2	RPD1

Note) x: Don't care

■ Control Data Format

Address					Data							
A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0

(1) VAD Parameter [R0]

This register sets the voice activity detection parameter for up link VOX control. Please set this parameter at the initialization after reset is done.

1. Release Time (D3~D0)

Set the PWRDET signal release time from silence level detection in 10ms units within a range of 0~150 ms. After reset is done, release time is set to 0ms.

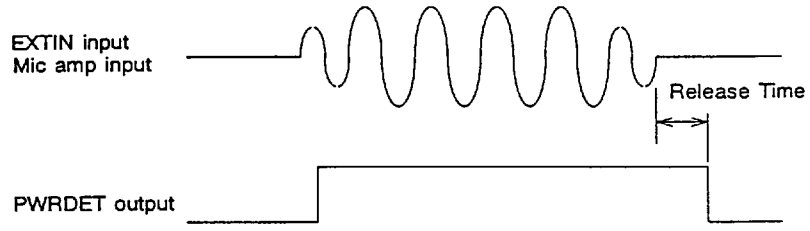
Release Time = Set Value (RELEASE TIME) * 10 (ms)

2. Detection Level (D7~D4)

Set the threshold value for tone detection. After reset is done, detection level is set to -9dbm0.

Detection Level = -9 - Set Value (TH LEVEL) * 3 (dbm0)

■ Voice Activity Detection Timing



Release time and detection level are design guaranteed.

(2) Noise Generation Parameter [R1]

This register controls the noise generation parameter for generating colored noise for silent intervals during down link VOX control and executing noise generation during long term error frame reception.

1. Noise Level (D3~D0)

After reset is done, release time is set to -24dBm0.

Noise Level = -24 - Set Value (NOISE LEVEL) * 3 (dBm0)

2. Mute/Noise Select (D4)

Sets whether or not colored noise is generated or mute when silent interval signals to the RVOX pin are received. After reset is done, noise is selected.

0: Noise
1: Mute

3. Forced Noise Generation (D5)

Sets whether or not colored noise will be generated regardless of the RVOX pin input and the noise suppression state. After reset is done, noise output is selected.

0: Noise Output
1: Normal Processing

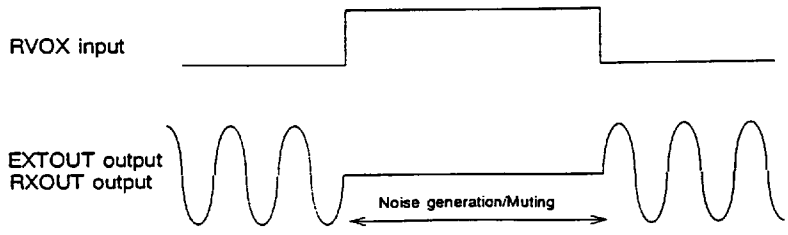
Note) After reset is done, noise output is selected. So, if mute is released, colored noise is output to RXOUT and EXTOUT. Please set this function to "Normal processing" before mute is released.

4. PCM Loopback (D6)

Loops back ADPCM decoding data to the encoder. After reset is done, normal processing is selected.

0: Normal Processing
1: PCM Loopback

■ Noise generation or muting triggered by RVOX input



(3) Transmitting Path Control [R2]

This register controls the attenuation and muting for the transmitting path (analog input to the linear CODEC) of the audio interface unit.

1. Voice Transmission Level Adjustment (D3～D0)

Sets the voice transmission level adjustment attenuation (TXATT) value in the 0 dB～-7.5 dB range. After reset is done, attenuation level is set to 0dB.

Attenuation Value = - Setting Value (TXATT) * 0.5 (dB)

2. Mic Input Path Mute (MIC MUTE) (D4)

After reset is done, mute is selected.

0: Mute
1: Connect

3. External Input Path Mute (TEXT MUTE) (D5)

After reset is done, mute is selected.

0: Mute
1: Connect

4. Transmitting Tone Mute (TXTONE MUTE) (D6)

After reset is done, mute is selected.

0: Mute
1: Connect

5. ADPCM Mute (D7)

After reset is done, mute is selected.

0: Mute Converts digital data to the ADPCM forcedly to digital zero code.
1: Connect

(4) Receiving Path Control 1 [R3]

This register controls attenuation and muting of the receiving block of audio interface (analog output from the linear CODEC and tone generator). After reset is done, attenuation level is set to 0dB.

1. Voice Receiving Level Adjustment (D2~D0)

Set the value of the voice receiving attenuator (RCVATT) in the 0dB~ -21 dB range. After reset is done, attenuation level is set to 0dB.

Attenuation Value = - Set Value (RCVATT) * 3 (dB)

2. External Output Level Adjustment (D4~D3)

Set the value of the external output level adjustment attenuation (EXTATT) in the 0dB~-18 dB range. After reset is done, attenuation level is set to 0dB.

Attenuation Value = - Set Value (ATT2) * 6 (dB)

3. Receiver Mute (RCV MUTE) (D5)

After reset is done, mute is selected.

0: Mute
1: Connect

4. External Output Path Mute (REXT MUTE) (D6)

After reset is done, mute is selected.

0: Mute
1: Connect

5. Linear CODEC Mute (D7)

After reset is done, mute is selected.

0: Mute Converts digital data to the ADPCM forcedly to digital zero code.
1: Connect

(5) Receiving Path Control 2 [R4]

1. Side Tone Gain Adjustment (D2～D0)

Set the side tone gain between the transmitting path and receiving path (SDTATT) within a range of -28～-52 dB, or at -∞. After reset is done, attenuation value is set to -∞.

Attenuation Value = -28 - Set Value (SDTATT) * 4 (dB)

SDTATT=0～6:

Attenuation Value = -∞ SDTATT=7

2. Tone Receiver Output Mute (RXTONE MUTE) (D3)

After reset is done, mute is selected.

0: Mute
1: Connect

3. SOUNDER Output Mute (SOUNDER MUTE) (D4)

After reset is done, mute is selected.

0: Mute
1: Connect

4. μ-law PCM data input select (D5)

This register sets μ-law PCM data input source selection to ADPCM encoder. After reset is done, 0 is set.

0: Input from A/D
1: Input from PCMIN

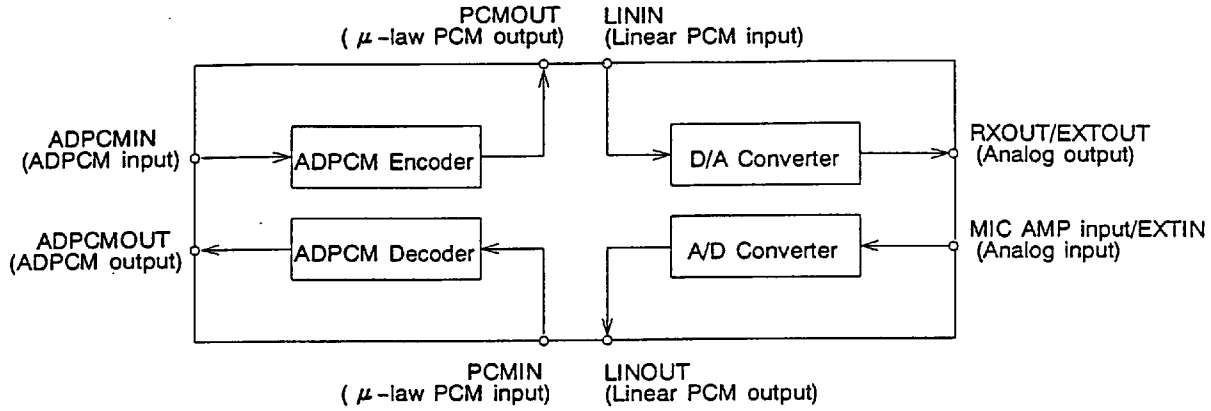
5. Linear PCM data input select (D6)

This register sets linear PCM data input source selection to D/A. After reset is done, 0 is set.

0: Input from ADPCM decoder
1: Input from LININ.

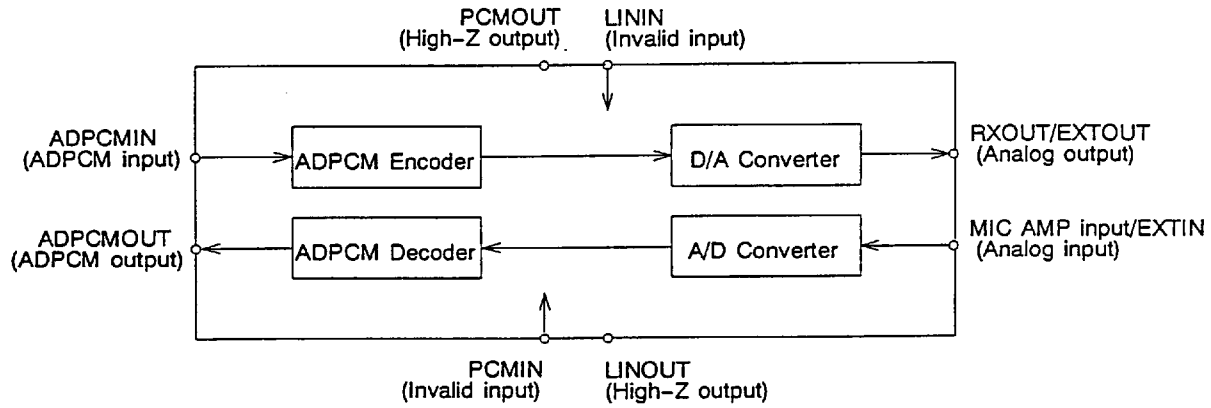
■ User Test Mode

• PCMEN = H (User Test Mode)



Note) If RCLK < 64kHz, correct operation of μ-low data interface is not guaranteed.
If RCLK < 128 kHz correct operation of linear data interface is not guaranteed.
When user test interface is in use, please use with RCLK=TCLK, RSYNC=TSYCN.

• PCMEN = L (Normal Operation Mode)



(6) Tone Generator Parameters [R5~R7]

These registers set the programmable tone generator parameters which consist of two tone sources.

1. Tone Source Parameter 1 [R5]

This sets the dividing factor of divider 1 for tone source 1. The oscillating frequency is expressed by the set value in the following formula. After reset is done, frequency is set to 233.5Hz. However, if set value = 0 then frequency is s et to 233.5Hz.

$$\text{Oscillating Frequency (Hz)} = 960\ (\text{kHz}) \times \frac{1}{16} \times \frac{1}{(\text{Set value}+1)}$$

2. Tone Source Parameter 2 [R6]

This sets the dividing factor of divider 2 for tone source 2. The oscillating frequency is set in the same way as for tone source 1.

3. Tone Source Parameter 3 [R7]

3. 1 Tone Source 1 Level (D2~D0)

Sets the value of the attenuator (TATT1) for adjusting the tone source 1 output level. After reset is done, attenuation level is set to 0dB.

Attenuation Value = - Set Value * 3 (dB)

3. 2 Tone Source 2 Level (D5~D3)

Sets the value of the attenuator (TATT2) for adjusting the tone source 2 output level. After reset is done, attenuation level is set to 0dB.

Attenuation Value = - Set Value * 3 (dB)

3. 3 Tone Source 1 Mute

After reset is done, mute is selected.

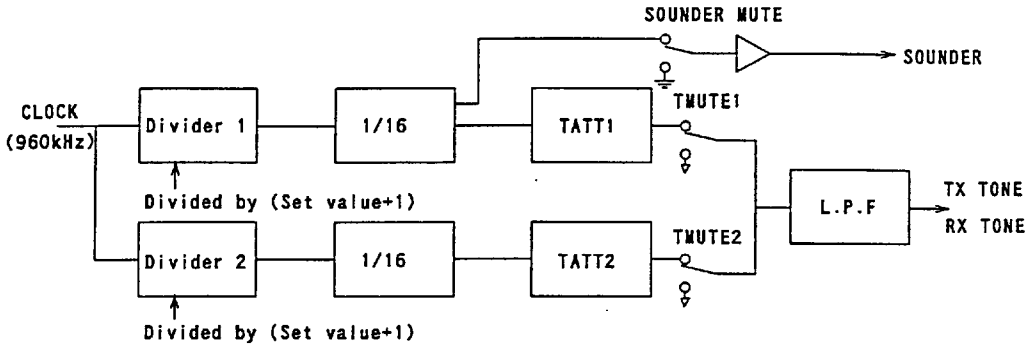
0: Mute
1: Connect

3. 4 Tone Source 2 Mute

After reset is done, mute is selected.

0: Mute
1: Connect

■ Tone Generator Configuration



■ DTMF Tone Setting Values

DTMF Frequency (Hz)	Set Value (Binary)	Actual Generated Frequency (Hz)
697	01010101	697.67 (+0.1%)
770	01001101	769.23 (-0.1%)
852	01000101	857.14 (+0.6%)
941	00111111	937.50 (-0.4%)
1209	00110000	1224.49 (+1.3%)
1336	00101100	1333.33 (-0.2%)
1477	00101000	1463.41 (-0.9%)
1633	00100100	1621.62 (-0.7%)

(7) Noise Suppression Parameter [R8 - R10]

These registers control the noise suppression parameters. After reset is done, parameters are set to our recommend values. If another values are needed, please set at the initializing.

1. Noise Suppression Parameter 1 [R8 - RD]

Set the state width (= number of frames) and the attenuation value at each state when the noise suppression is executed. The decoded ADPCM data is attenuated by setting value when the noise suppression is executed.

1. 1 State Width (D3 - D0)

State Width = set value (STATE WIDTH n) + 1

Note) The State width of state 3 is fixed at 1.
(Bit D3 to D0 of register RA are fixed at all 0)

1. 2 Attenuation Value (D7 - D4)

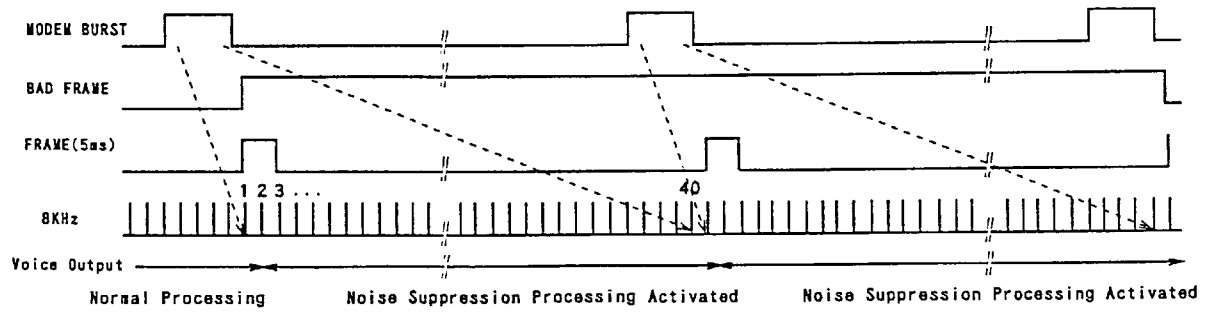
Attenuation Value = set value (ATT VAL n) * 3 (dB)

2. Noise Suppression Parameter 2 [RE - R10]

Set the limit value of the ADPCM data at each state when the noise suppression is executed. The set value is the absolute value. When the noise suppression is executed, if received ADPCM data is under the limit value then it is input to the ADPCM decoder, and if received ADPCM data is over the limit value then it is changed to positive or negative limit value and is input to the ADPCM decoder.

Limit Value = set value (LIMIT VAL n)
(D6 - D4 or D3 - D0)

■ Timing of Noise Suppression Processing during Generation of Transmission Errors



■ Noise Suppression Function

The 32 k bps ADPCM defined by ITU-T Rec. G.721 has been a wired transmission system standard, and does not envision applications with high error rate wireless channels, so there are cases of voice quality deterioration occurring as a result of transmission errors by radio.

As the countermeasure, the AK2397 have a noise suppression function (Patent pending in Japan) for burst errors. This function needs CRC error check results so it is not required especial operation at transmit side.

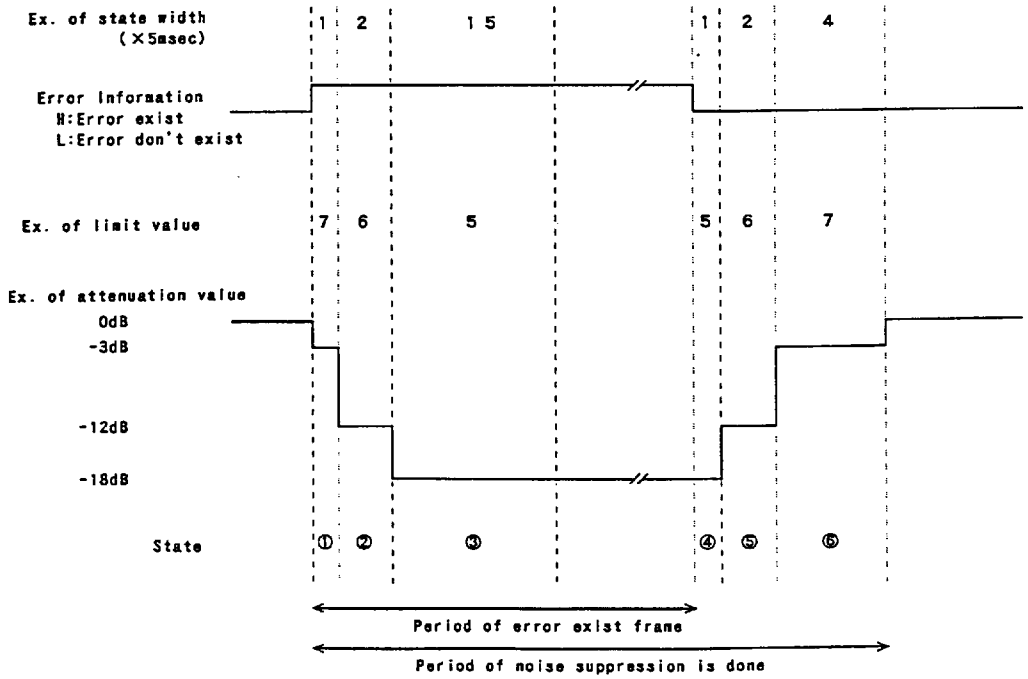
(Noise suppression)

The AK2397 reduce the voice quality deterioration that is caused by burst errors. Only transmission error information (CRC error check results etc.) is required. Overview of processing is shown below.

① Limitation of ADPCM code
If absolute value of received ADPCM code is under the limit value then it is input to the ADPCM decoder, and if absolute value of received ADPCM code is over the limit value then it is changed to positive or negative limit value and is input to the ADPCM decoder.

② Attenuation of linear PCM code
Attenuation is done to decoded linear PCM code.

Limitation value and attenuation value can be set to control registers. These values are independent at each state (=times after error occurred), so, smooth attenuation and limitation can be executed. Also, state width can be set to control registers.



(8) Power Down Mode [R11]

This register controls the power down mode. After reset is done, normal operation mode is selected.

RPD1	RPD2	Operation Mode
0	0	Normal Operation
1	0	Codec Power Down
X	1	Full Power Down

When the RPD1 and RPD2 are in use, please set PD1 and PD2 pins to L.
When the PD1 and PD2 pins are in use, please set RPD1 and RPD2 to 0.

■ Power Down Mode

The AK2397 includes three power down modes, which are set by the PD1 and PD2 pins or RPD1 and RPD2 registers.
The tone generator is also set to undergo power down automatically in accordance with the tone mute setting. The state of each block of the AK2397 is shown in the following table.

RPD1	RPD2	PD1	PD2	MODE	ADPCM	CODEC	TX analog	RX analog	TONE. G	VREF	REG. W
0	0	×	1	1	●	●	●	●	●	●	○
0	0	1	0	2	●	●	○	○	▲	○	○
0	0	0	0	3	○	○	○	○	▲	○	○
×	1	0	0	1	●	●	●	●	●	●	○
1	0	0	0	2	●	●	○	○	▲	○	○
0	0	0	0	3	○	○	○	○	▲	○	○

● : Power Save
○ : Active
▲ : Auto Power Save

- Mode 1 (Full Power Down Mode)

In this mode, writing to the register is possible. Please set the control registers after reset signal input.

- Mode 2 (CODEC Power Down Mode)

In this mode, operation of the voice receiving system analog and tone generators is possible. Shifting of operation from Mode 1 to Mode 2 takes 5 ms.

- Mode 3 (Normal operation Mode)

In this mode, operation of all circuits is possible.
Shifting of operation from Mode 1 to Mode 3 takes 5 ms.
Shifting of operation from Mode 2 to Mode 3 takes 1 ms.

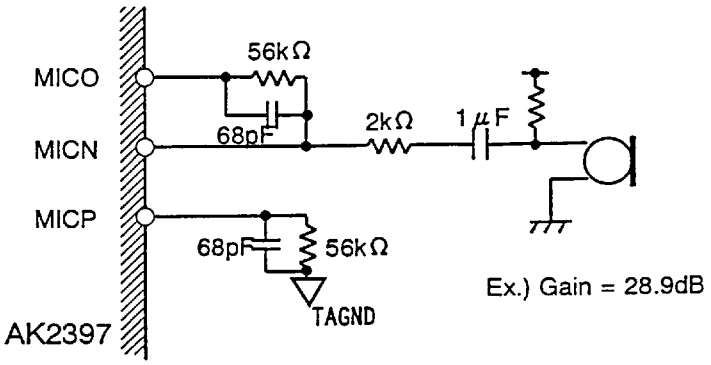
- Auto Power save of Tone Generator

If both TMUTE1 and TMUTE2 in the tone generator block are set in the mute state, the tone generator block undergoes power down automatically.

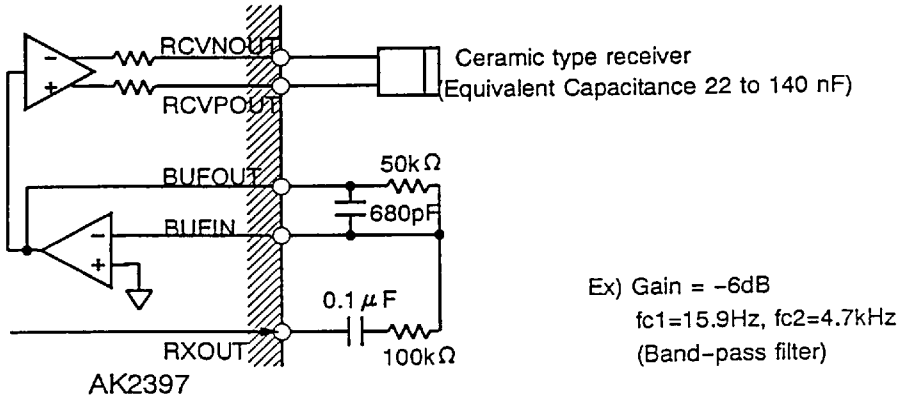
Application Circuit Examples

■ Example of External Circuits

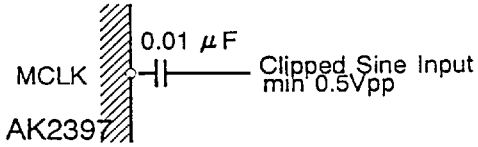
(1) Mic. Amplifier
The transmitting microphone amplifier.



(2) Receiver Amplifier
Receiver amplifier is a differential output amplifier to enable direct drive of a ceramic receiver.

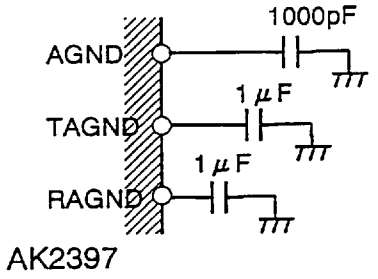


(3) DC cut of MCLK input
Clipped sine wave is input to MCLK pin via capacitor in order to DC cut.



(4) AGND stabilization capacitors

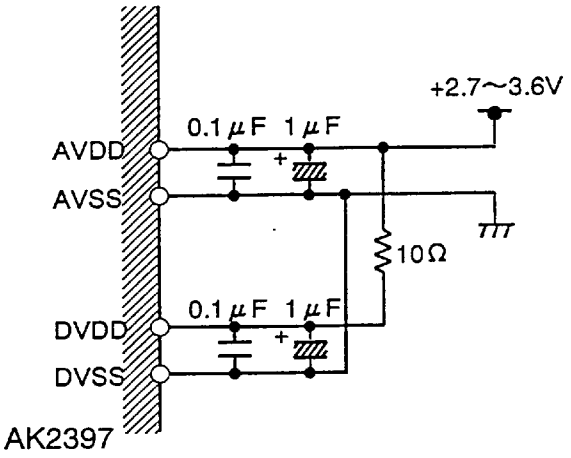
Capacitors should be connected between AGND pin and AVSS, TAGND pin and AVSS, RAGND pin and AVSS respectively in order to stabilize analog ground.



(5) Power supply stabilization capacitors

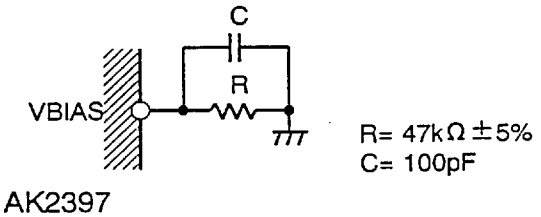
To minimize the effect of power supply noise, a couple of capacitors should be placed between pin, AVDD pin and AVSS pin, DVDD pin and DVSS pin respectively.

When different power sources are supplied to each pins, DVDD may not exceed AVDD.
When same power source is supplied to each pins, insert resistor between side and DVDD side, and supply from AVDD.



(6) Bias-current setting resistor

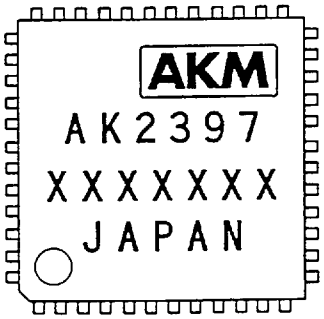
Bias-current of Op-Amp is set by connecting a resistor between VBIAS pin and AVSS pin. A 47 kΩ resistor is recommended.



Package

■ Markings

(1) Pin 1 indicated (The chamfered corner indicates pin number 1.)
(2) Date Code: XXXXXXX (7 digits)
Higher order four digits: week code
Lower order three digits: In-house control code
(3) Marketing code: AK2397
(4) Manufacturing Country Name Indication : Japan
(5) Asahi Kasei Logo



■ Package External Dimensions