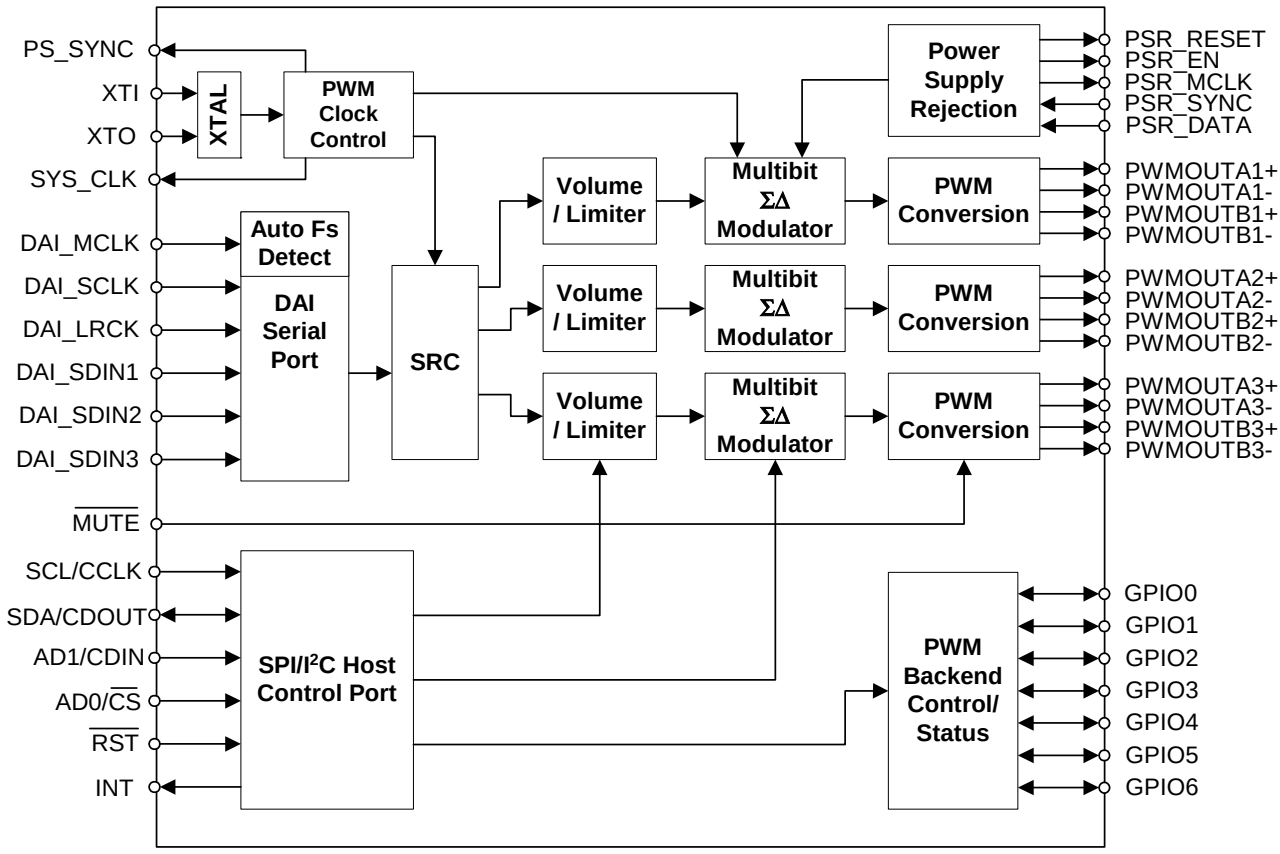
CS44600

6-Channel Digital Amplifier Controller

Features

- > 100 dB Dynamic Range - System Level
- < 0.03% THD+N @ 1 W - System Level
- 32 kHz to 192 kHz Sample Rates
- Internal Oscillator Circuit Supports 24.576 MHz to 54 MHz Crystals
- Integrated Sample Rate Converter (SRC)
  - Eliminates Clock Jitter Effects
  - Input Sample Rate Independent Operation
- Power Supply Rejection Realtime Feedback
- Spread Spectrum Modulation - Reduces Modulation Energy
- PWM PopGuard® for Single-Ended Mode
- Eliminates AM Frequency Interference
- Programmable Load Compensation Filters
- Support for up to 40 kHz Audio Bandwidth
- Digital Volume Control with Soft Ramp
  - +24 to -127 dB in 0.25 dB Steps
- Per Channel Programmable Peak Detect and Limiter
- SPI and I²C Host Control Interfaces
- Separate 2.5 V to 5.0 V Serial Port and Host Control Port Supplies



Preliminary Product Information | This document contains information for a new product.
Cirrus Logic reserves the right to modify this product without notice.

General Description

The CS44600 is a multi-channel digital-to-PWM Class D audio system controller including interpolation, sample rate conversion, half- and full-bridge PWM driver outputs, and power supply rejection feedback in a 64-pin LQFP package.The architecture uses a direct-to-digital approach that maintains digital signal integrity to the final output filter, minimizing analog interference effects which negatively affect system performance.

The CS44600 integrates on-chip digital volume control, peak detect with limiter, de-emphasis, and 7 GPIO's, allowing easy interfacing to many commonly available power stages. The PWM amplifier can achieve greater than 90% efficiency. This efficiency provides for smaller device package, less heat sink requirements, and smaller power supplies.

The CS44600 is ideal for audio systems requiring wide dynamic range, negligible distortion and low noise, such as A/V receivers, DVD receivers, digital speaker and automotive audio systems.

ORDERING INFORMATION

Product	Description	Package	Pb-Free	Temp Range	Container	Order#
CS44600	6-Channel Digital Amplifier Controller	LQFP	YES	-10° to +70°C	Rail	CS44600-CQZ
CS44600	6-Channel Digital Amplifier Controller	LQFP	YES	-10° to +70°C	Tape and Reel	CS44600-CQZR
CS44600	6-Channel Digital Amplifier Controller	LQFP	YES	-40° to +85°C	Rail	CS44600-DQZ
CS44600	6-Channel Digital Amplifier Controller	LQFP	YES	-40° to +85°C	Tape and Reel	CS44600-DQZR
CDB44800	CS44600/800 Evaluation Board	-	-	-	-	CDB44800
CRD44800	8x50 W Half-Bridge Reference Design Board	-	-	-	-	CRD44800
CRD44800-ST-FB	8x60 W Full-Bridge Reference Design Board	-	-	-	-	CRD44800-ST-FB
CRD44600-PH-FB	2x100 W Full-Bridge Reference Design Board	-	-	-	-	CRD44600-PH-FB

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1. CHARACTERISTICS AND SPECIFICATIONS

(All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at nominal supply voltages and T_A = 25°C.)

SPECIFIED OPERATING CONDITIONS

(GND = 0 V, all voltages with respect to ground)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supply						
Digital	2.5 V	VD	2.37	2.5	2.63	V
XTAL (Note 1)	2.5 V	VDX	2.37	2.5	2.63	V
	3.3 V		3.14	3.3	3.47	V
	5.0 V		4.75	5.0	5.25	V
PWM Interface	3.3 V	VDP	3.14	3.3	3.47	V
	5.0 V		4.75	5.0	5.25	V
Serial Audio Interface2.5 V	3.3 V	VLS	2.37	2.5	2.63	V
	5.0 V		3.14	3.3	3.47	V
			4.75	5.0	5.25	V
Control Interface	2.5 V	VLC	2.37	2.5	2.63	V
	3.3 V		3.14	3.3	3.47	V
	5.0 V		4.75	5.0	5.25	V
Ambient Operating Temperature						
Commercial	-CQZ	T_A	-10	-	+70	°C
Automotive	-DQZ		-40	-	+85	°C

Notes:

1. When using external crystal, VDX = 3.14 V(min). When using clock signal input, VDX = 2.37 V(min).

ABSOLUTE MAXIMUM RATINGS

(GND = 0 V; all voltages with respect to ground.)

Parameters		Symbol	Min	Max	Units
DC Power Supply	Digital	VD	-0.3	3.5	V
	XTAL	VDX	-0.3	6.0	V
	PWM Interface	VDP	-0.3	6.0	V
	Serial Audio Interface	VLS	-0.3	6.0	V
	Control Interface	VLC	-0.3	6.0	V
Input Current	(Note 2)	I_{in}	-	±10	mA
Digital Input Voltage	PWM Interface	$V_{IND-PWM}$	-0.3	VDP+0.4	V
(Note 3)	Serial Audio Interface	V_{IND-S}	-0.3	VLS+0.4	V
	Control Interface	V_{IND-C}	-0.3	VLC+0.4	V
Ambient Operating Temperature	-CQ	T_A	-20	+85	°C
(power applied)	-DQ		-50	+95	°C
Storage Temperature		T_{stg}	-65	+150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

2. Any pin except supplies. Transient currents of up to ±100 mA on the input pins will not cause SCR latch-up.
3. The maximum over/under voltage is limited by the input current.

DC ELECTRICAL CHARACTERISTICS

(GND = 0 V, all voltages with respect to ground; DAI_MCLK = 12.288 MHz, XTAL = 24.576 MHz, PWM Switch Rate = 384 kHz unless otherwise specified.)

Parameter		Symbol	Min	Typ	Max	Units
Normal Operation (Note 4)						
Power Supply Current (Note 5)	VD = 2.5 V	I_D	-	150	-	mA
	VDX = 3.3 V	I_{DX}	-	2	-	mA
	VDP = 3.3 V	I_{DP}	-	1.2	-	mA
	VLS = 3.3 V	I_{LS}	-	150	-	µA
	VLC = 3.3 V (Note 6)	I_{LC}	-	250	-	µA
Power Dissipation	VD=2.5 V, VDX = VDP = VLS = VLC = 3.3 V		-	387	500	mW
Power Supply Rejection Ratio (Note 7)	(1 kHz)	PSRR	-	15	-	dB
	(60 Hz)		-	40	-	dB
Power-Down Mode (Note 8)						
Power Supply Current	All Supplies except VDX (Note 9)	I_{pd}	-	80	-	µA

4. Normal operation is defined as $\overline{RST}$ = HI with a 997 Hz, 0 dBFS input.
5. Current consumption increases with increasing XTAL clock rates and PWM switch rates. Variance between DAI clock rates is negligible.
6. I_{LC} measured with no external loading on the SDA pin.
7. Valid with PSRR function enabled and the recommended external ADC (CS4461) and filtering.
8. Power down mode is defined as $\overline{RST}$ pin = LOW with all clock and data lines held static.
9. When $\overline{RST}$ pin = LOW, the internal oscillator is active to provide a valid clock for the SYS_CLK output.

DIGITAL INTERFACE CHARACTERISTICS

(GND = 0 V, all voltages with respect to ground)

Parameters (Note 10)		Symbol	Min	Typ	Max	Units
High-Level Input Voltage	XTAL	V_{IH}	0.7xVDX	-	-	V
	PWM Interface		0.7xVDP	-	-	V
	Serial Audio Interface		0.7xVLS	-	-	V
	Control Interface		0.7xVLC	-	-	V
Low-Level Input Voltage	XTAL	V_{IL}	-	-	0.2xVDX	V
	PWM Interface		-	-	0.2xVDP	V
	Serial Audio Interface		-	-	0.2xVLS	V
	Control Interface		-	-	0.2xVLC	V
High-Level Output Voltage at I_o = -2 mA	PWM Interface	V_{OH}	VDP-1.0	-	-	V
	Serial Audio Interface		VLS-1.0	-	-	V
	Control Interface		VLC-1.0	-	-	V
Low-Level Output Voltage at I_o = 2 mA	PWM Interface	V_{OL}	-	-	0.45	V
	Serial Audio Interface		-	-	0.45	V
	Control Interface		-	-	0.45	V
Input Leakage Current		I_{in}	-	-	±10	µA
Input Capacitance			-	-	8	pF

10. Serial Port signals include: SYS_CLK, DAI_MCLK, DAI_SCLK, DAI_LRCK, DAI_SDIN1-3
Control Port signals include: SCL/CCLK, SDA/CDOUT, AD0/$\overline{CS}$, AD1/CDIN, INT, $\overline{RST}$, MUTE
PWM signals include: PWMOUTA1-B3, PSR_MCLK, PSR_SYNC, PSR_DATA, PS_SYNC, GPIO[6:0]

PWM OUTPUT PERFORMANCE CHARACTERISTICS

(Logic “0” = GND = 0 V; Logic “1” = VLS = VLC; VD = 2.5 V; DAI_MCLK = 12.288 MHz; XTAL= 24.576 MHz; PWM Switch Rate = 384 kHz; Fs = 32 kHz to 192 kHz; Measurement bandwidth is 10 Hz to 20 kHz unless otherwise specified; Performance measurements taken with a full-scale 997 Hz.)

Parameter		Symbol	Min	Typ	Max	Unit
Dynamic Performance (Note 11)						
24-Bits	A-Weighted		102	108	-	dB
	unweighted		99	105	-	dB
16-Bits	unweighted		-	96	-	dB
Total Harmonic Distortion + Noise (Note 11)						
24-Bits	0 dB	THD+N	-	-90	-85	dB
	-20 dB		-	-77	-	dB
	-60 dB		-	-45	-	dB
Idle Channel Noise / Signal-to-Noise Ratio			-	110	-	dB
Interchannel Isolation	(1 kHz)		-	100	-	dB

11. Performance characteristics measured using filter shown in Figure 1.

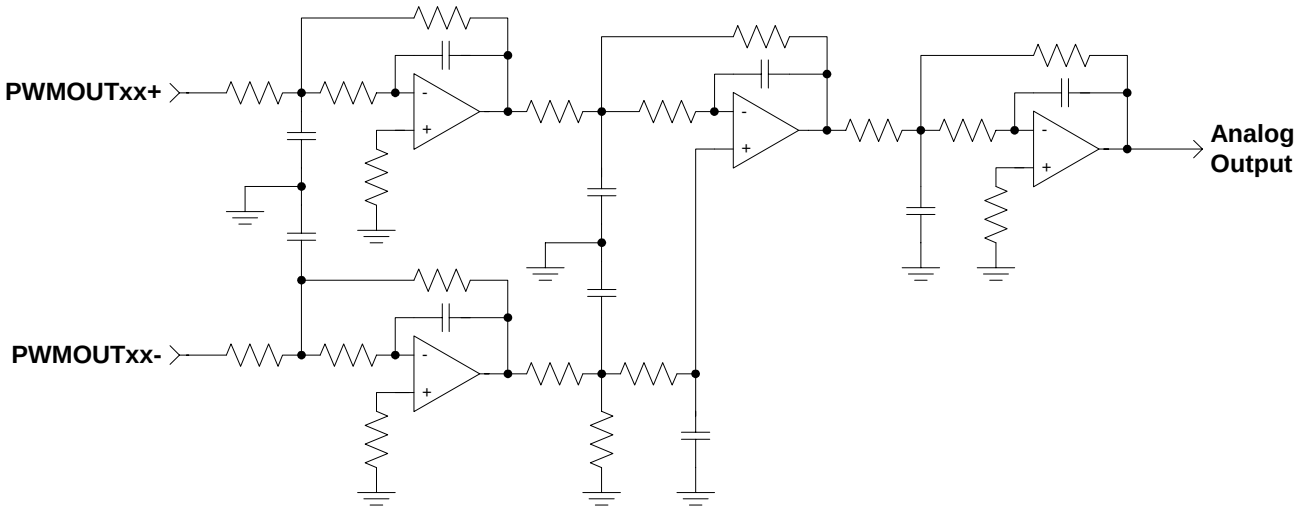


Figure 1. Performance Characteristics Evaluation Active Filter Circuit

PWM FILTER CHARACTERISTICS

(Logic “0” = GND = 0 V; Logic “1” = VLS = VLC; VD = 2.5 V; DAI_MCLK = 12.288 MHz; XTAL = 24.576 MHz; PWM Switch Rate = 384 kHz; Fs = 32 kHz to 192 kHz; Measurement bandwidth is 10 Hz to 20 kHz unless otherwise specified.)

Parameter		Min	Typ	Max	Unit
Digital Filter Response (Note 12)					
Passband					
OSRATE = 0b	to -0.01 dB corner	0	-	1.6	kHz
	to -3 dB corner	0	-	24.0	kHz
OSRATE = 1b (Note 13)	to -0.01 dB corner	0	-	3.3	kHz
	to -3 dB corner	0	-	44.5	kHz
	Frequency Response				
OSRATE = 0b	10 Hz to 20 kHz	-0.8	-	+0.02	dB
OSRATE = 1b (Note 13)	10 Hz to 40 kHz	-1.2	-	+0.02	dB
Group Delay			(Note 14)		ms
De-emphasis Error	Fs = 32 kHz	-	-	±0.23	dB
(Relative to 1 kHz)	Fs = 44.1 kHz	-	-	±0.14	dB
	Fs = 48 kHz	-	-	±0.09	dB

12. Filter response is not production tested but is characterized and guaranteed by design.
13. XTAL = 49.152 MHz; PWM Switch Rate = 768 kHz; Fs = 96 kHz to 192 kHz.
14. The equation for the group delay through the sample rate converter with OSRATE = 0b is (8.5 / Fsi) + (10 / Fso) ± (4.5 / Fsi). The equation for the group delay through the sample rate converter with OSRATE = 1b is (8.5 / Fsi) + (20 / Fso) ± (4.5 / Fsi).

SWITCHING CHARACTERISTICS - XTI

(VD = 2.5 V, VDP = VLC = VLS = 3.3 V, VDX = 2.5 V to 5.0 V; Inputs: Logic 0 = GND, Logic 1 = VDX)

Parameter	Symbol	Min	Typ	Max	Unit
XTI period	t_{clki}	18.518	---	40.69	ns
XTI high time	t_{clkih}	8.34	---	22.38	ns
XTI low time	t_{clkil}	8.34	---	22.38	ns
XTI Duty Cycle		45	50	55	%
External Crystal operating frequency		24.576	---	54	MHz

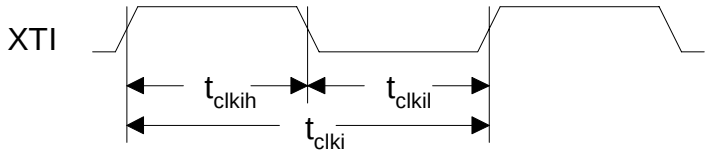


Figure 2. XTI Timings

SWITCHING CHARACTERISTICS - SYS_CLK

(VD = 2.5 V, VDP = VLC = VDX = 3.3 V, VLS = 2.5 V to 5.0 V, Cload = 50 pF)

Parameter	Symbol	Min	Typ	Max	Unit
SYS_CLK Period	t_{sclki}	18.518	---	---	ns
SYS_CLK Duty Cycle		45	50	55	%

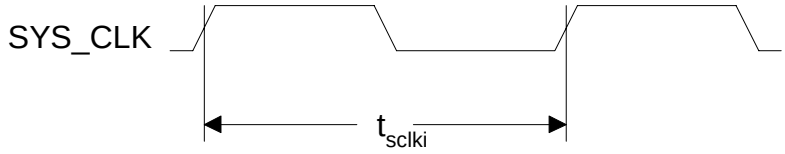


Figure 3. SYS_CLK Timings

SWITCHING CHARACTERISTICS - PWMOUTA1-B3

(VD = 2.5 V, VLS = VLC = VDX = 3.3 V, VDP = 3.3 V to 5.0 V unless otherwise specified, Cload = 10 pF)

Parameter		Symbol	Min	Typ	Max	Unit
PWMOUTxx Period		t_{pwm}	2.60	-	1.18	µs
Rise Time of PWMOUTxx	VDP = 5.0 V	t_r	-	1.6	-	ns
	VDP = 3.3 V		-	2.1	-	ns
Fall Time of PWMOUTxx	VDP = 5.0 V	t_f	-	1.1	-	ns
	VDP = 3.3 V		-	1.4	-	ns

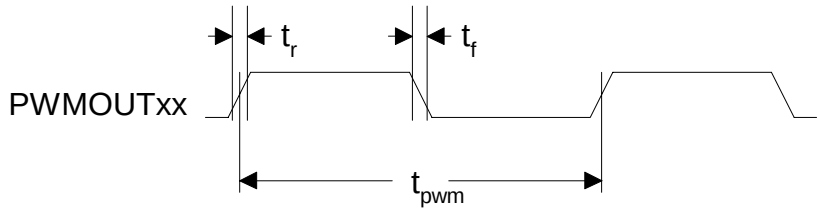


Figure 4. PWMOUTxx Timings

SWITCHING CHARACTERISTICS - PS_SYNC

(VD = 2.5 V, VLS = VLC = VDX = 3.3 V, VDP = 3.3 V to 5.0 V, Cload = 20 pF)

Parameter	Symbol	Min	Typ	Max	Unit
PS_SYNC Period	t_{psclki}	592.576	---	---	ns
PS_SYNC Duty Cycle		45	50	55	%

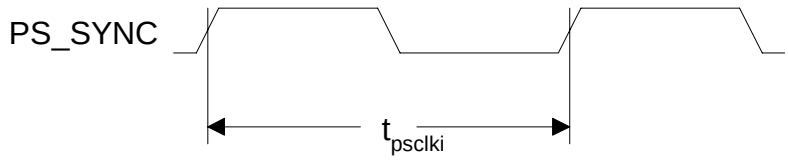


Figure 5. PS_SYNC Timings

SWITCHING CHARACTERISTICS - DAI INTERFACE

(VD = 2.5 V, VDX = VDP = VLC = 3.3 V, VLS = 2.5 V to 5.0 V; Inputs: Logic 0 = GND, Logic 1 = VLS.)

Parameters	Symbol	Min	Max	Units
$\overline{\text{RST}}$ pin Low Pulse Width (Note 15)		1	-	ms
DAI_MCLK Duty Cycle (Note 16)		40	60	%
DAI_SCLK Duty Cycle		45	55	%
DAI_LRCK Duty Cycle		45	55	%
DAI Sample Rate (Note 17)	F_s	32	192	kHz
DAI_SDIN Setup Time Before DAI_SCLK Rising Edge	t_{ds}	10	-	ns
DAI_SDIN Hold Time After DAI_SCLK Rising Edge	t_{dh}	10	-	ns
DAI_SCLK High Time	t_{sckh}	20	-	ns
DAI_SCLK Low Time	t_{sckl}	20	-	ns
DAI_LRCK Setup Time Before DAI_SCLK Rising Edge	t_{lrcks}	25	-	ns
DAI_SCLK Rising Edge Before DAI_LRCK Edge	t_{lrckd}	25	-	ns

15. After powering up, the CS44600, $\overline{\text{RST}}$ should be held low until after the power supplies and clocks are settled.
16. See Table 1 on page 26 for suggested MCLK frequencies.
17. Max DAI sample rate is 96 kHz for One Line and TDM modes of operation.

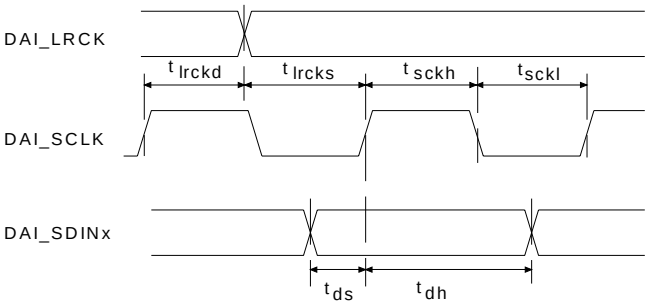


Figure 6. Serial Audio Interface Timing

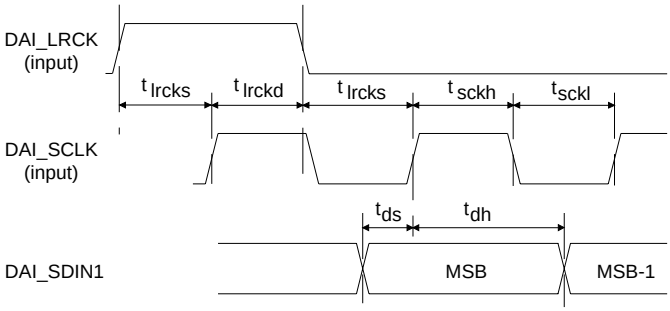


Figure 7. Serial Audio Interface Timing - TDM Mode

SWITCHING CHARACTERISTICS - CONTROL PORT - I²C FORMAT

(VD = 2.5 V, VDX = VDP = VLS = 3.3 V; VLC = 2.5 V to 5.0 V; Inputs: Logic 0 = GND, Logic 1 = VLC, C_L = 30 pF)

Parameter	Symbol	Min	Max	Unit
SCL Clock Frequency	f_{scl}	-	100	kHz
Bus Free Time between Transmissions	t_{buf}	4.7	-	µs
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	4.0	-	µs
Clock Low time	t_{low}	4.7	-	µs
Clock High Time	t_{high}	4.0	-	µs
Setup Time for Repeated Start Condition	t_{sust}	4.7	-	µs
SDA Hold Time from SCL Falling (Note 18)	t_{hdd}	10	-	ns
SDA Setup time to SCL Rising	t_{sud}	250	-	ns
Rise Time of SCL and SDA	t_r	-	1000	ns
Fall Time SCL and SDA	t_f	-	300	ns
Setup Time for Stop Condition	t_{susp}	4.7	-	µs

18. Data must be held for sufficient time to bridge the transition time, t_f, of SCL.

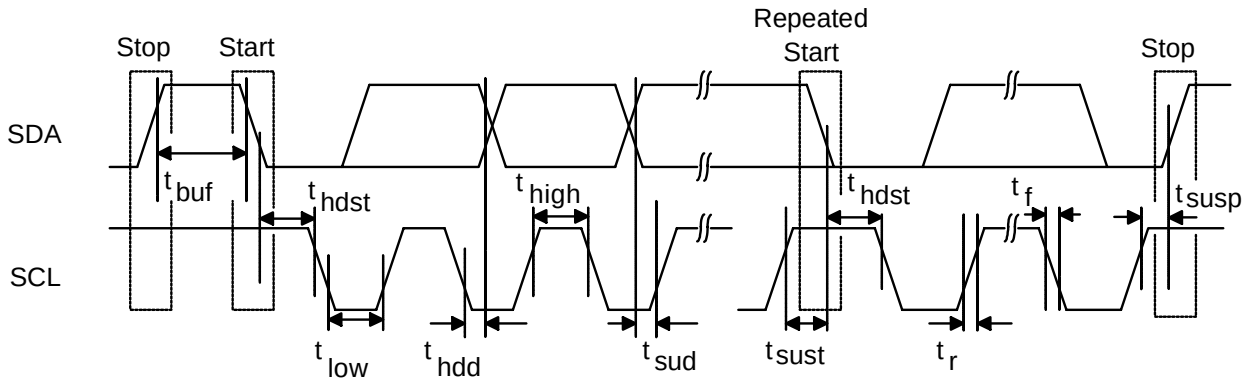


Figure 8. Control Port Timing - I²C Format

SWITCHING CHARACTERISTICS - CONTROL PORT - SPI FORMAT

(VD = 2.5 V, VDP = VLS = 3.3 V; VLC = 2.5 V to 5.0 V; Inputs: Logic 0 = GND, Logic 1 = VLC, C_L = 30 pF)

Parameter		Symbol	Min	Typ	Max	Units
CCLK Clock Frequency		f_{sck}	0	-	6.0	MHz
$\overline{CS}$ High Time between Transmissions		t_{csh}	1.0	-	-	µs
$\overline{CS}$ Falling to CCLK Edge		t_{css}	20	-	-	ns
CCLK Low Time		t_{scl}	66	-	-	ns
CCLK High Time		t_{sch}	66	-	-	ns
CDIN to CCLK Rising Setup Time		t_{dsu}	40	-	-	ns
CCLK Rising to DATA Hold Time	(Note 19)	t_{dh}	15	-	-	ns
CCLK Falling to CDOUT Stable		t_{pd}	-	-	50	ns
Rise Time of CDOUT		t_{r1}	-	-	25	ns
Fall Time of CDOUT		t_{f1}	-	-	25	ns
Rise Time of CCLK and CDIN	(Note 20)	t_{r2}	-	-	100	ns
Fall Time of CCLK and CDIN	(Note 20)	t_{f2}	-	-	100	ns

19. Data must be held for sufficient time to bridge the transition time of CCLK.
20. For f_{sck} <1 MHz.

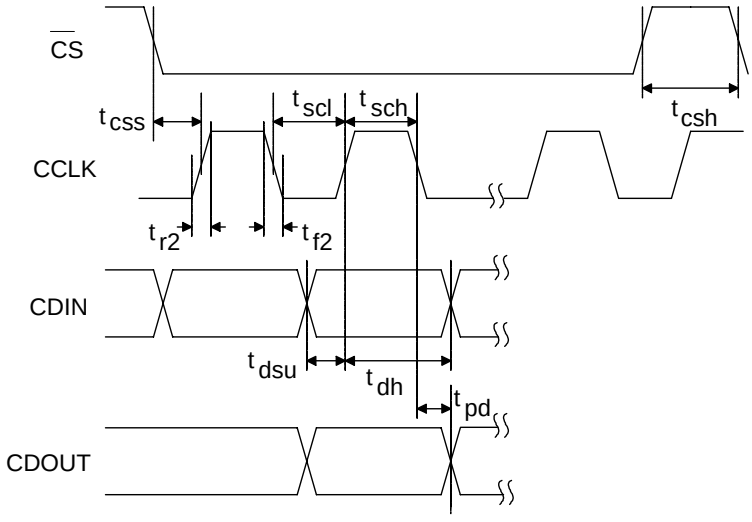


Figure 9. Control Port Timing - SPI Format

2. PIN DESCRIPTIONS

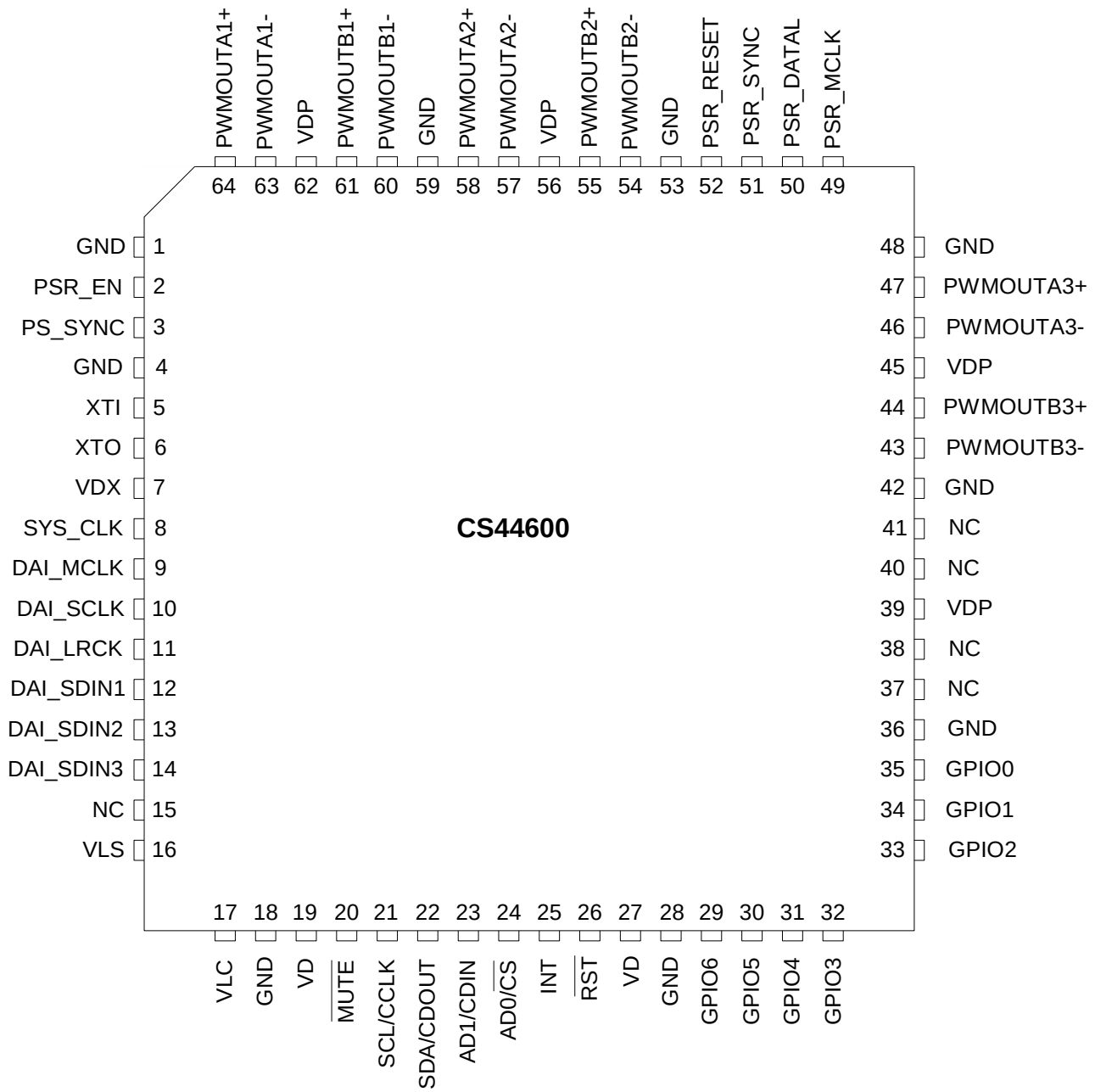


Figure 10. CS44600 Pinout Diagram

Pin Name	Pin #	Pin Description
PS_SYNC	3	**Power Supply Synchronization Clock** *(Output*) - The PWM synchronized clock to the switch mode power supply.
XTI	5	**Crystal Oscillator Input** (*Input*) - Crystal Oscillator input or accepts an external clock input signal that is used to drive the internal PWM core logic.
XTO	6	**Crystal Oscillator Output** *(Output)* - Crystal Oscillator output.
SYS_CLK	8	**External System Clock** (*Output*) - Clock output. This pin provides a divided down clock derived from the XTI input.
DAI_MCLK	9	**Digital Audio Input Master Clock** (Input) - Master audio clock.
DAI_SCLK	10	**Digital Audio Input Serial Clock** *(Input)* - Serial clock for the Digital Audio Input Interface. The clock frequency is a multiple of the Left/Right Clock running at Fs.
DAI_LRCK	11	**Digital Audio Input Left/Right Clock** (*Input*) - Determines which channel, Left or Right, is currently active on the serial audio data line. The rate is determined by the sampling frequency Fs.
DAI_SDIN1 DAI_SDIN2 DAI_SDIN3	12 13 14	**Digital Audio Input Serial Data** (*Input*) - Input for two's complement serial audio data.
MUTE	20	**Mute** (*Input*) - The device will perform a hard mute on all channels. All internal registers are not reset to their default settings.
SCL/CCLK	21	**Serial Control Port Clock** (*Input*) - Serial clock for the serial control port. Requires an external pull-up resistor to the logic interface voltage in I²C mode as shown in the Typical Connection Diagram.
SDA/CDOUT	22	**Serial Control Data** (*Input/Output*) **-** SDA is a data I/O line in I²C mode and requires an external pull-up resistor to the logic interface voltage, as shown in the Typical Connection Diagram.; CDOUT is the output data line for the control port interface in SPI mode.
AD1/CDIN	23	**Address Bit 1 (I²C)/Serial Control Data (SPI)** (*Input*) - AD1 is a chip address pin in I²C mode.;CDIN is the input data line for the control port interface in SPI mode.
AD0/$\overline{CS}$	24	**Address Bit 0 (I²C)/Control Port Chip Select (SPI)** *(Input*) - AD0 is a chip address pin in I²C mode; $\overline{CS}$ is the chip select signal in SPI mode.
INT	25	**Interrupt Request** *(Output*) - CMOS or open-drain interrupt request output. This pin is driven to the configured active state to indicate that the PWM Controller has status data that should be read by the host.
RST	26	**Reset** (*Input*) - The device enters a low power mode and all internal registers are reset to their default settings when low.
GPIO6	29	**General Purpose Input, Output** *(Input/Output*) - This pin is configured as an input following a $\overline{RST}$ condition. It can be configured as a general purpose input or output which can be individually controlled by the Host Controller.
GPIO5	30	**General Purpose Input, Output** *(Input/Output*) - This pin is configured as an input following a $\overline{RST}$ condition. It can be configured as a general purpose input or output which can be individually controlled by the Host Controller.
GPIO4	31	**General Purpose Input, Output** *(Input/Output*) - This pin is configured as an input following a $\overline{RST}$ condition. It can be configured as a general purpose input or output which can be individually controlled by the Host Controller.

GPIO3	32	**General Purpose Input, Output** *(Input/Output)* - This pin is configured as an input following a $\overline{\text{RST}}$ condition. It can be configured as a general purpose input or output which can be individually controlled by the Host Controller.
GPIO2	33	**General Purpose Input, Output** *(Input/Output)* - This pin is configured as an input following a $\overline{\text{RST}}$ condition. It can be configured as a general purpose input or output which can be individually controlled by the Host Controller.
GPIO1	34	**General Purpose Input, Output** *(Input/Output)* - This pin is configured as an input following a $\overline{\text{RST}}$ condition. It can be configured as a general purpose input or output which can be individually controlled by the Host Controller.
GPIO0	35	**General Purpose Input, Output** *(Input/Output)* - This pin is configured as an input following a $\overline{\text{RST}}$ condition. It can be configured as a general purpose input or output which can be individually controlled by the Host Controller.
PSR_MCLK	49	**Power Supply Rejection Master Clock** (*Output*) - Master audio clock for external PSR ADC (CS4461).
PSR_DATAL	50	**Power Supply Rejection Input Serial Data** (*Input*) - Input for serial audio data from external PSR ADC (CS4461).
PSR_SYNC	51	**Power Supply Rejection Sync Clock** *(Input)* - Synchronization signal for external PSR ADC (CS4461).
PSR_RESET	52	**Power Supply Rejection Reset** *(Output*) - The reset pin for the external Power Supply Rejection circuitry.
PSR_EN	2	**Power Supply Rejection Enable** *(Output*) - The enable pin for the external Power Supply Rejection circuitry.
PWMOUTA1+ PWMOUTA1- PWMOUTB1+ PWMOUTB1- PWMOUTA2+ PWMOUTA2- PWMOUTB2+ PWMOUTB2- PWMOUTA3+ PWMOUTA3- PWMOUTB3+ PWMOUTB3-	64 63 61 60 58 57 55 54 47 46 44 43	**PWM Output** (*Output*) - PWM control signals for the Class D amplifier backend.
VDX	7	**Crystal Power** (*Input*) - Positive power supply for the Crystal section.
VD	19, 27	**Digital Power** (*Input*) - Positive power supply for the digital section.
VLC	17	**Host Interface Power** (*Input*) **-** Determines the required signal level for the digital input/output signals for the host interface.
VLS	16	**Digital Audio Interface Power** (*Input*) **-** Determines the required signal level for the digital input signals for the digital audio interface.
VDP	39, 45, 56, 62	**PWM Interface Power** (*Input*) - Determines the required signal level for the digital input/output signals for the PWM and GPIO interface.
GND	1, 4, 18, 28, 36, 42, 48, 53, 59	**Digital Ground** (*Input*) - Ground reference for digital circuits.

2.1 I/O Pin Characteristics

Signal Name	Power Rail	I/O	Driver	Receiver
RST	VLC	Input	-	2.5 V and 3.3/5.0 V TTL Compatible.
SCL/CCLK	VLC	Input	-	2.5 V and 3.3/5.0 V TTL Compatible, with Hysteresis.
SDA/CDOUT	VLC	Input / Output	2.5-5.0 V, CMOS/Open Drain	2.5 V and 3.3/5.0 V TTL Compatible, with Hysteresis.
AD0/$\overline{CS}$	VLC	Input	-	2.5 V and 3.3/5.0 V TTL Compatible, Internal pull-up.
AD1/CDIN	VLC	Input	-	2.5 V and 3.3/5.0 V TTL Compatible, Internal pull-up.
INT	VLC	Output	2.5-5.0 V, CMOS/Open Drain	-
MUTE	VLC	Input	-	2.5 V and 3.3/5.0 V TTL Compatible.
DAI_SDINx	VLS	Input	-	2.5 V and 3.3/5.0 V TTL Compatible.
DAI_SCLK	VLS	Input	-	2.5 V and 3.3/5.0 V TTL Compatible.
DAI_LRCK	VLS	Input	-	2.5 V and 3.3/5.0 V TTL Compatible.
DAI_MCLK	VLS	Input	-	2.5 V and 3.3/5.0 V TTL Compatible.
SYS_CLK	VLS	Output	2.5-5.0 V, CMOS	-
XTI	VDX	Input	-	2.5 V and 3.3/5.0 V TTL Compatible, Internal pull-down.
XTO	VDX	Output	-	-
GPIOx	VDP	Input / Output	3.3/5.0 V, CMOS/Open Drain	3.3/5.0 V TTL Compatible.
PWMOUTAx+/-	VDP	Output	3.3/5.0 V, CMOS	-
PWMOUTBx+/-	VDP	Output	3.3/5.0 V, CMOS	-
PSR_MCLK	VDP	Output	3.3/5.0 V, CMOS	-
PSR_SYNC	VDP	Input	-	3.3/5.0 V TTL Compatible, Internal pull-up.
PSR_DATA	VDP	Input	-	3.3/5.0 V TTL Compatible, Internal pull-up.
PSR_EN	VDP	Output	3.3/5.0 V, CMOS	-
PSR_RESET	VDP	Output	3.3/5.0 V, CMOS	-
PS_SYNC	VDP	Output	3.3/5.0 V, CMOS	-

3. TYPICAL CONNECTION DIAGRAMS

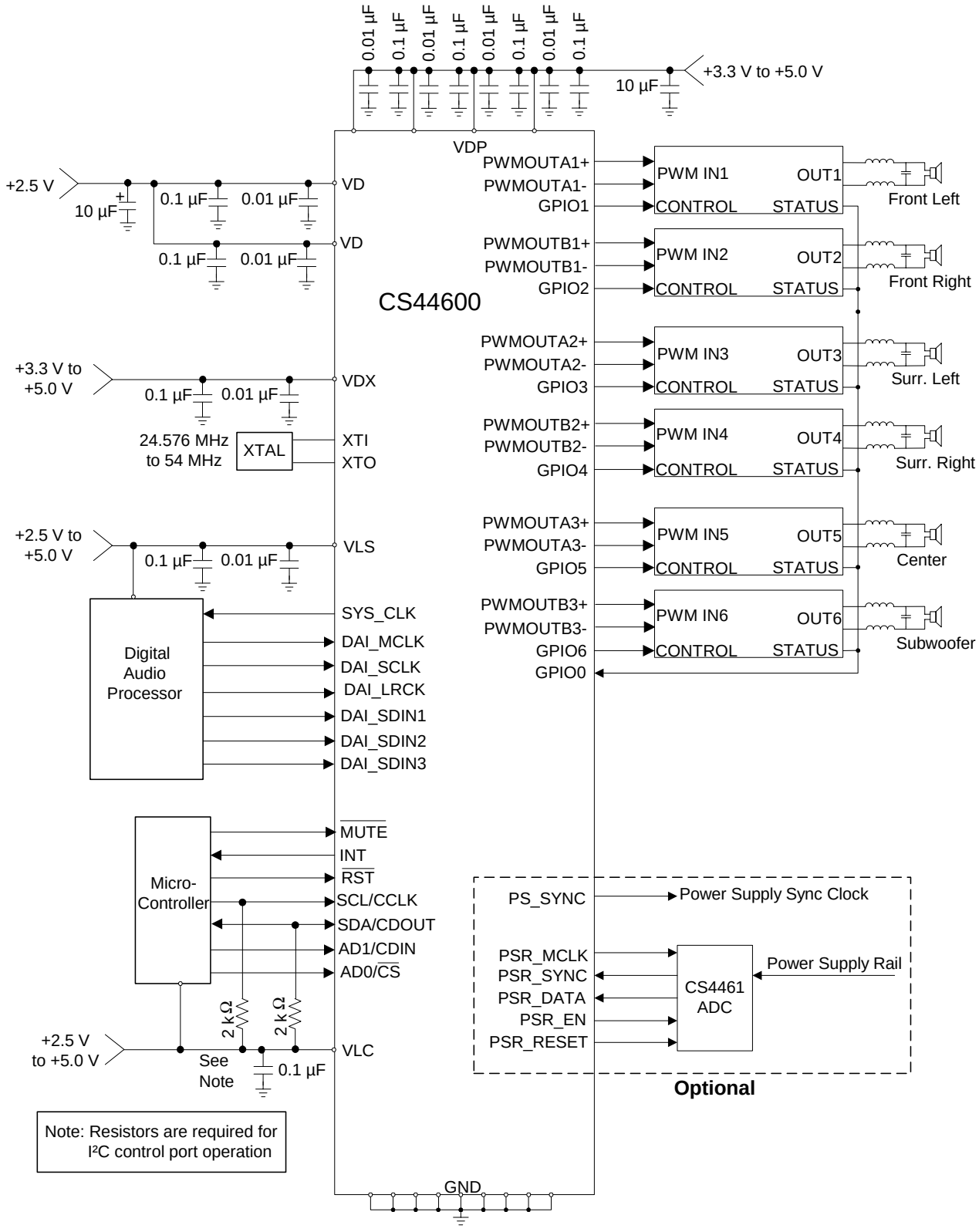


Figure 11. Typical Full-Bridge Connection Diagram

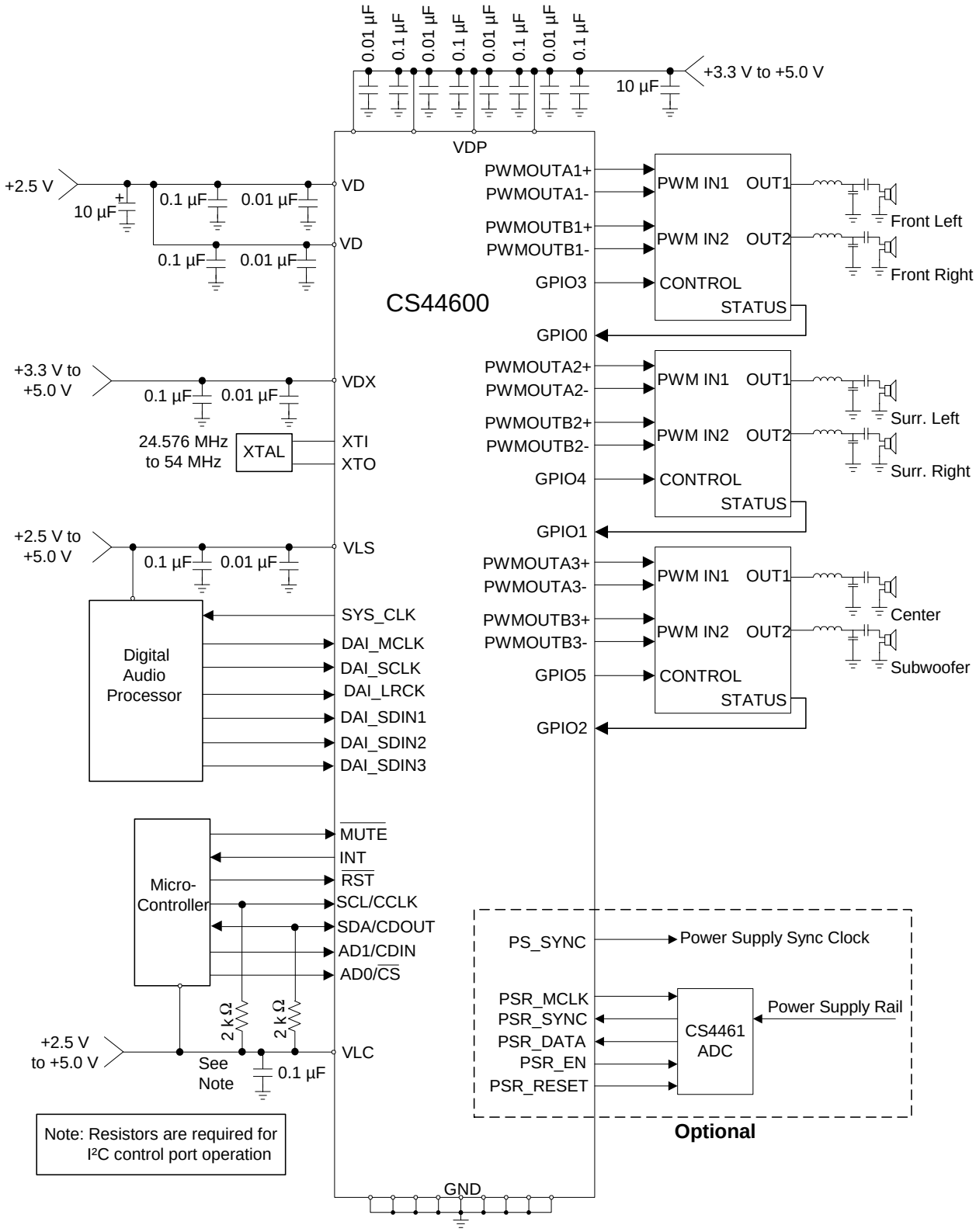


Figure 12. Typical Half-Bridge Connection Diagram

4. APPLICATIONS

4.1 Overview

The CS44600 is a multi-channel digital-to-PWM Class D audio system controller including interpolation, sample rate conversion, half- and full-bridge PWM driver outputs, and power supply rejection feedback in a 64-pin LQFP package. The architecture uses a direct-to-digital approach that maintains digital signal integrity to the final output filter, minimizing analog interference effects which negatively affect system performance.

The CS44600 integrates on-chip sample rate conversion, digital volume control, peak detect with volume limiter, de-emphasis, programmable interrupt conditions, and the ability to change the PWM switch rate to eliminate AM frequency interference. The CS44600 also has a programmable load compensation filter, which allows the speaker load to vary while the output filter remains fixed, maintaining a flat frequency response. For single-ended half-bridge applications PWM Popguard® reduces the transient pops and clicks and realtime power supply feedback reduces noise coupling from the power supply. The PWM amplifier can achieve greater than 90% efficiency. This efficiency provides for a smaller device package, less heat sink requirements, and smaller power supplies.

The CS44600 is ideal for audio systems requiring wide dynamic range, negligible distortion, and low noise such as A/V receivers, DVD receivers, digital speaker, and automotive audio systems.

4.2 Feature Set Summary

Core Features

- 2.5 V digital core voltage, VD.
- VLC voltage pin for host interface logic levels between 2.5 V and 5.0 V.
- VLS voltage pin for digital audio interface logic levels between 2.5 V and 5.0 V.
- VDP voltage pin for PWM backend interface logic levels between 3.3 V and 5.0 V.
- VDX voltage pin for clock input signals between 2.5 V and 5.0 V.

Clocking

- Minimum of 128Fs DAI_MCLK for DAI serial interface.
- DAI interface uses automatic detection of LRCK/MCLK ratio to configure internal DAI/SRC clocks.
- All PWM Processing clocks generated internally via:
  - An external crystal - 24.576 MHz to 54 MHz, or
  - XTI input pin capable of supporting a clock signal at the VDX voltage level.
- Programmable divide of XTI by 1, 2, 4, 8 for SYS_CLK output.
- Programmable divide of XTI by 32, 64, 128, 256 for PS_SYNC (power supply synchronization signal).

Digital Audio Playback

- Supports 32 kHz, 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, 176.4 kHz and 192 kHz sample frequencies.
- High performance sample rate converter.
- 16, 20 and 24 bit audio sample lengths.
- De-emphasis for 32 kHz, 44.1 kHz, 48 kHz.

- Digital volume control with soft ramp.
- Individual channel volume gain, attenuation and mute capability; +24 to -127 dB in 0.25 dB steps.
- Master volume attenuation; +24 to -127 dB in 0.25 dB steps.
- Peak Detect and Volume Limiter with programmable attack and release rates.
- Signal-clipping interrupt indicator.

Additional Features

- Contains a two-stage digital output filter for speaker impedance compensation.
- Provides 7 programmable GPIO pins with interrupt generation for easily interfacing to a variety of commonly available power state parts. Interrupts can be masked.
- Selectable over-sample rate for increased audio bandwidth.
- Power supply clock output, PS_SYNC, with programmable divider

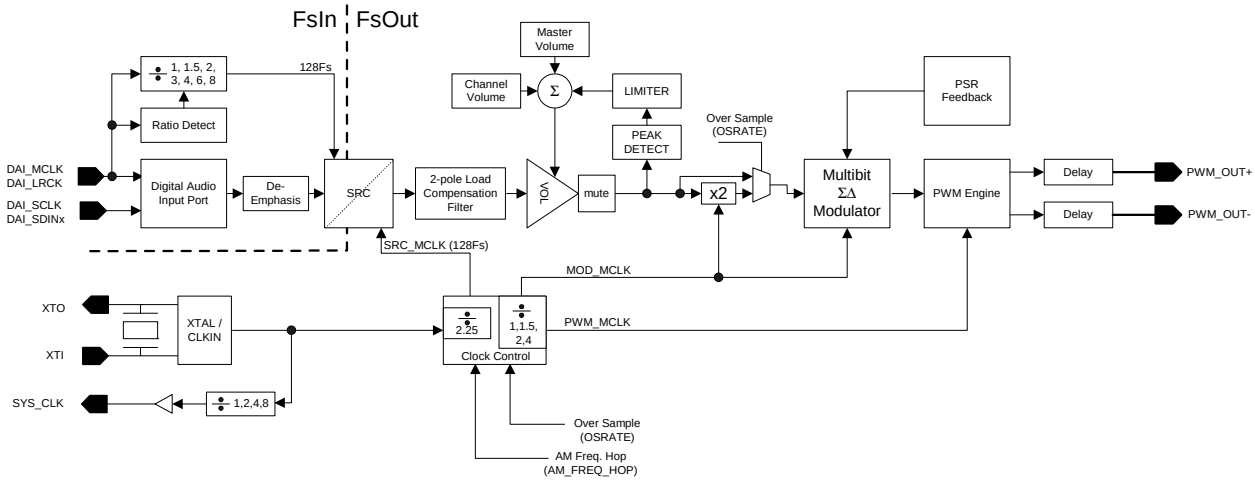


Figure 13. CS44600 Data Flow Diagram (Single Channel Shown)

4.3 Clock Generation

The sources for internal clock generation for the PWM processing are as follows:

- FsIn Domain:
  - DAI_MCLK, minimum 128Fs
- FsOut Domain:
  - XTI/XTO (Fundamental or 3rd overtone crystal), or
  - Clock signal on XTI (VDX is used to set logic voltage level)

4.3.1 FsIn Domain Clocking

Common DAI_MCLK frequencies and sample rates are shown in Table 1.

Mode (sample-rate range)	Sample Rate (kHz)	DAI_MCLK (MHz)				
DAI_MCLK/LRCK Ratio –>		**256x**	**384x**	**512x**	**768x**	**1024x**
Single Speed (4 to 50 kHz)	32	8.1920	12.2880	16.3840	24.5760	32.7680
	44.1	11.2896	16.9344	22.5792	33.8688	45.1584
	48	12.2880	18.4320	24.5760	36.8640	49.1520
DAI_MCLK/LRCK Ratio –>		**128x**	**192x**	**256x**	**384x**	**512x**
Double Speed (50 to 100 kHz)	64	8.1920	12.2880	16.3840	24.5760	32.7680
	88.2	11.2896	16.9344	22.5792	33.8688	45.1584
	96	12.2880	18.4320	24.5760	36.8640	49.1520
DAI_MCLK/LRCK Ratio –>		**64x**	**96x**	**128x**	**192x**	**256x**
Quad Speed (100 to 200 kHz)	176.4	n/a	n/a	22.5792	33.8688	45.1584
	192	n/a	n/a	24.5760	36.8640	49.1520

Table 1. Common DAI_MCLK Frequencies

4.3.2 FsOut Domain Clocking

To ensure the highest quality conversion of PWM signals, the CS44600 is capable of operating from a fundamental mode or 3rd overtone crystal, or a clock signal attached to XTI, at a frequency of 24.576 MHz to 54 MHz. If XTI is being directly driven by a clock signal, XTO can be left floating or tied to ground through a pull-down resistor and the internal oscillator should be powered down using the PDN_XTAL bit in register 02h.

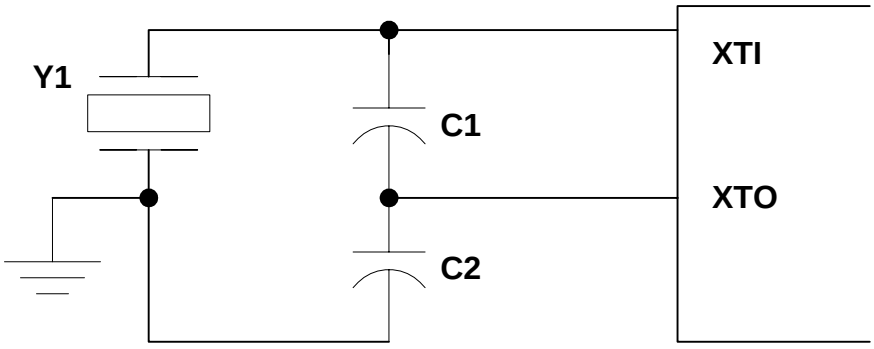


Figure 14. Fundamental Mode Crystal Configuration

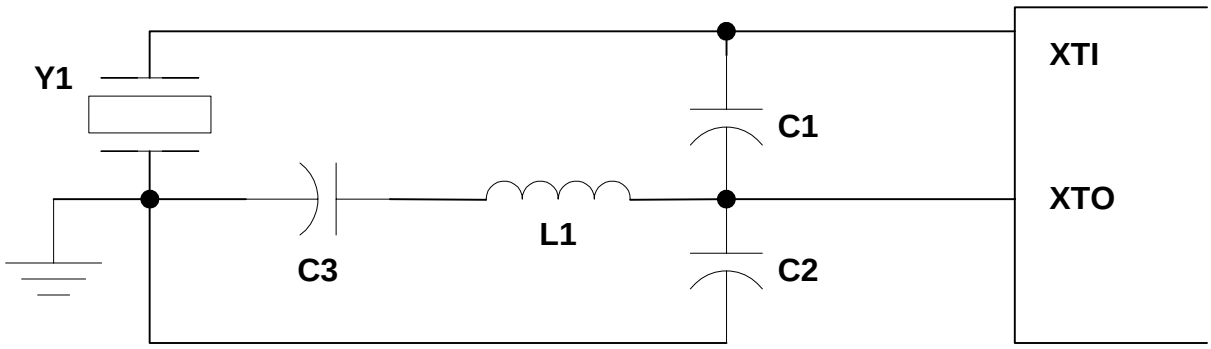


Figure 15. 3rd Overtone Crystal Configuration

Appropriate clock dividers for each functional block and a programmable divider to support an output for switched-mode power supply synchronization are provided. The clock generation for the CS44600 is shown in the Figure 16.

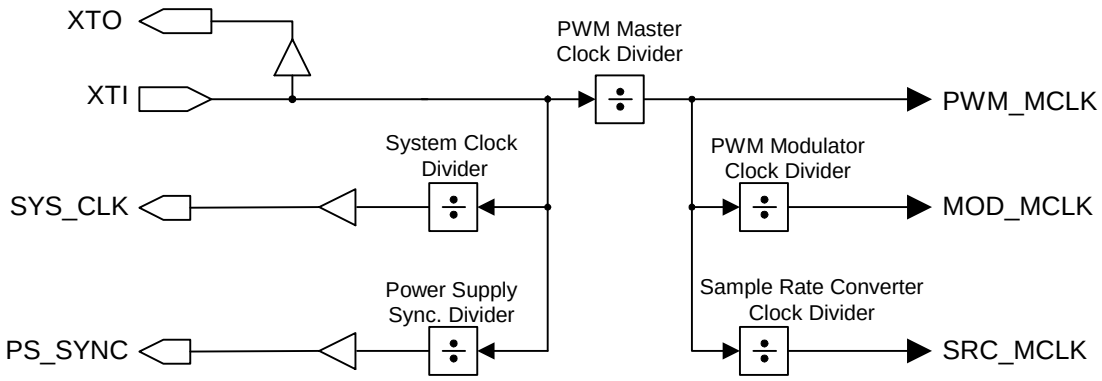


Figure 16. CS44600 Internal Clock Generation

4.4 FsIn Clock Domain Modules

4.4.1 Digital Audio Input Port

The CS44600 interfaces to an external Digital Audio Processor via the Digital Audio Input serial port, the DAI serial port. The DAI port has 3 stereo data inputs with support for I²S, left-justified and right-justified formats. The DAI port operates in slave operation only, where DAI_LRCK, DAI_SCLK and DAI_MCLK are always inputs. The signal DAI_LRCK must be equal to the sample rate, Fs and must be synchronously derived from the supplied master clock, DAI_MCLK. The serial bit clock, DAI_SCLK, is used to sample the data bits and must be synchronously derived from the master clock.

DAI_SDIN1, DAI_SDIN2, and DAI_SDIN3 are the serial data input pins supplying the associated internal PWM channel modulators. The serial data interface format selection (left-justified, right-justified, I²S, one line mode, or TDM) for the DAI serial port data input pins is configured using the appropriate bits in the register "Misc. Configuration (address 04h)" on page 52. The serial audio data is presented in 2's complement binary form with the MSB first in all formats.

When operated in One Line Data Mode, 6 channels of PWM data are input on DAI_SDIN1. In TDM mode, all 6 channels are multiplexed onto the DAI_SDIN1 data line. Table 2 outlines the serial port channel allocations.

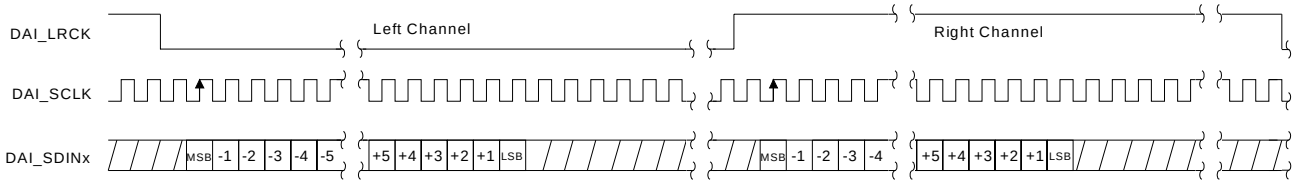
Serial Data Inputs	Data mode	Channel Assignments
DAI_SDIN1	Normal (I²S,LJ,RJ) One Line #1 or #2 TDM	PWMOUTA1(left channel)/PWMOUTB1(right channel) PWMOUTA1/A2/A3/B1/B2/B3 PWMOUTA1/A2/A3/B1/B2/B3
DAI_SDIN2	Normal (I²S,LJ,RJ) One Line #1 or #2 TDM	PWMOUTA2(left channel)/PWMOUTB2(right channel) not used not used
DAI_SDIN3	Normal (I²S,LJ,RJ) One Line #1 or #2 TDM	PWMOUTA3(left channel)/PWMOUTB3(right channel) not used not used

Table 2. DAI Serial Audio Port Channel Allocations

The DAI digital audio serial ports support 6 formats with varying bit depths from 16 to 24 as shown in Figure 17, Figure 18, Figure 19, Figure 20, Figure 21 and Figure 22. These formats are selected using the configuration bits in the "Misc. Configuration (address 04h)" on page 52.

4.4.1.1 I²S Data Format

For I²S, data is received most significant bit first, one DAI_SCLK delay after the transition of DAI_LRCK, and is valid on the rising edge of DAI_SCLK. For the I²S format, the left channel data is presented when DAI_LRCK is low; the right channel data is presented when DAI_LRCK is high.

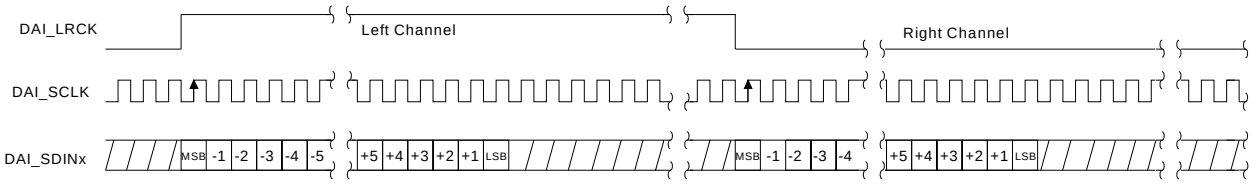


I²S Mode, Data Valid on Rising Edge of DAI_SCLK	
Bits/Sample	SCLK Rates
16	32, 48, 64, 128, 256 Fs
18 to 24	48, 64, 128, 256 Fs

Figure 17. I²S Serial Audio Formats

4.4.1.2 Left-Justified Data Format

For left-justified format, data is received most significant bit first on the first DAI_SCLK after a DAI_LRCK transition and is valid on the rising edge of DAI_SCLK. For the left-justified format, the left channel data is presented when DAI_LRCK is high and the right channel data is presented when DAI_LRCK is low.

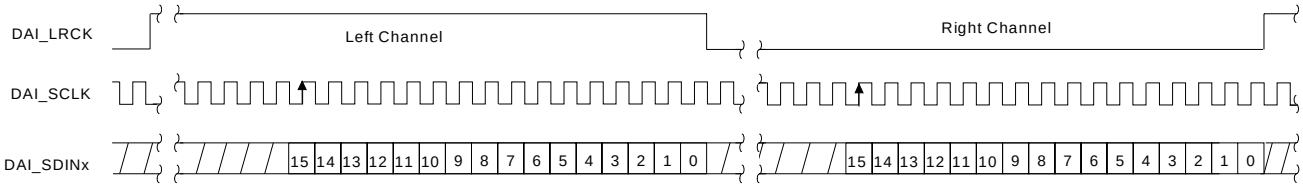


Left-Justified Mode, Data Valid on Rising Edge of DAI_SCLK	
Bits/Sample	SCLK Rate(s)
16	32, 48, 64, 128, 256 Fs
18 to 24	48, 64, 128, 256 Fs

Figure 18. Left-Justified Serial Audio Formats

4.4.1.3 Right-Justified Data Format

In the right-justified format, data is received most significant bit first and with the least significant bit presented on the last DAI_SCLK before the DAI_LRCK transition and is valid on the rising edge of DAI_SCLK. For the right-justified format, the left channel data is presented when DAI_LRCK is high and the right channel data is presented when DAI_LRCK is low. Either 16 bits per sample or 24 bits per sample are supported.



Right-Justified Mode, Data Valid on Rising Edge of DAI_SCLK	
Bits/Sample	SCLK Rate(s)
16	32, 48, 64, 128, 256 Fs
24	48, 64, 128, 256 Fs

Figure 19. Right-Justified Serial Audio Formats

4.4.1.4 One Line Mode #1

In One Line mode #1 format, data is received most significant bit first on the first DAI_SCLK after a DAI_LRCK transition and is valid on the rising edge of DAI_SCLK. DAI_SCLK must operate at a 128Fs rate. DAI_LRCK identifies the start of a new frame and is equal to the sample period. DAI_LRCK is sampled as valid on the same clock edge as the most significant bit of the first data sample and must be held high for 64 DAI_SCLK periods. Each time slot is 20 bits wide, with the valid data sample left-justified within the time slot. Valid data lengths are 16, 18, or 20 bits. Valid samples rates for this mode are 32 kHz to 96 kHz.

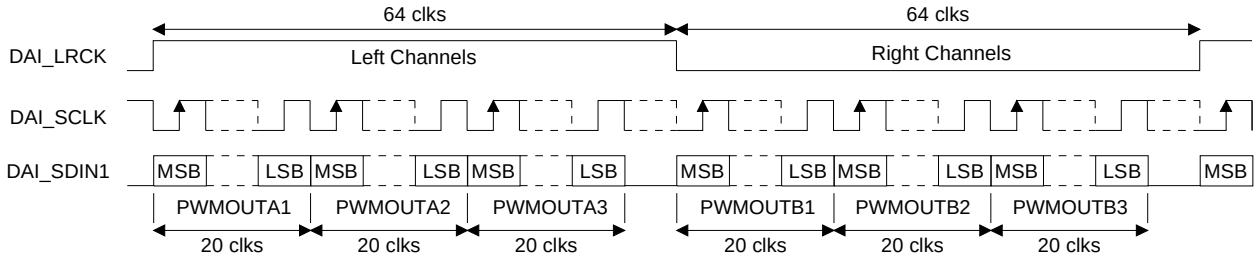


Figure 20. One Line Mode #1 Serial Audio Format

4.4.1.5 One Line Mode #2

In One Line mode #2 format, data is received most significant bit first on the first DAI_SCLK after a DAI_LRCK transition and is valid on the rising edge of DAI_SCLK. DAI_SCLK must operate at a 256 Fs rate. DAI_LRCK identifies the start of a new frame and is equal to the sample period. DAI_LRCK is sampled as valid on the same clock edge as the most significant bit of the first data sample and must be held high for 128 DAI_SCLK periods. Each time slot is 24 bits wide, with the valid data sample left-justified within the time slot. Valid data lengths are 16, 18, 20, or 24 bits. Valid samples rates for this mode are 32 kHz to 96 kHz.

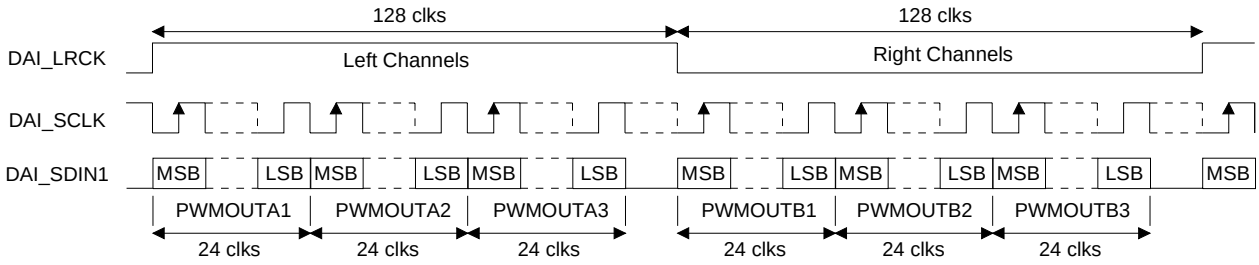


Figure 21. One Line Mode #2 Serial Audio Format

4.4.1.6 TDM Mode

In TDM mode format, data is received most significant bit first on the first DAI_SCLK after a DAI_LRCK transition and is valid on the rising edge of DAI_SCLK. DAI_SCLK must operate at a 256 Fs rate. DAI_LRCK identifies the start of a new frame and is equal to the sample period. DAI_LRCK is sampled as valid on the proceeding clock edge as the most significant bit of the first data sample and must be held valid for at least 1 DAI_SCLK period. Each time slot is 32 bits wide, with the valid data sample left-justified within the time slot. Valid data lengths are 16, 18, 20, 24 or 32 bits. Valid samples rates for this mode are 32 kHz to 96 kHz.

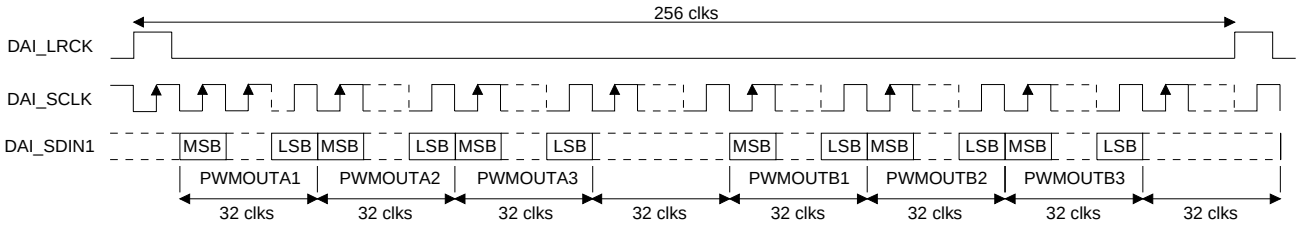


Figure 22. TDM Mode Serial Audio Format

4.4.2 Auto Rate Detect

The CS44600 will automatically determine the incoming sample rate, DAI_LRCK, to master clock, DAI_MCLK, ratio and configure the appropriate internal clock divider such that the sample rate convertor receives the required clock rate. A minimum DAI_MCLK rate of 128Fs is required for proper operation. The supported DAI_MCLK to DAI_LRCK ratios are shown in Table 1 on page 26.

4.4.3 De-Emphasis

The CS44600 includes on-chip digital de-emphasis filters. The de-emphasis feature is included to accommodate older audio recordings that utilize pre-emphasis equalization as a means of noise reduction. Figure 23 shows the de-emphasis curve. The frequency response of the de-emphasis curve will scale proportionally with changes in sample rate, Fs. The required de-emphasis filter for 32 kHz, 44.1 kHz, or 48 kHz is selected via the de-emphasis control bits in "Misc. Configuration (address 04h)" on page 52.

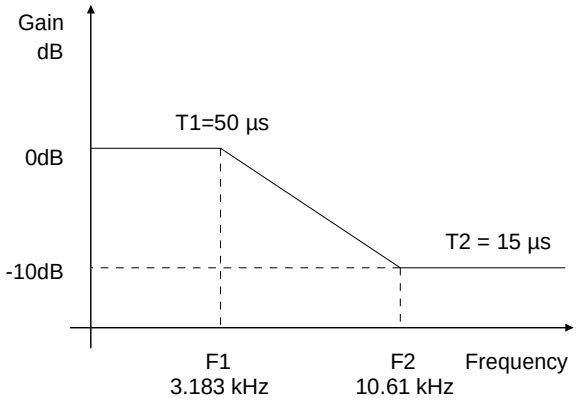


Figure 23. De-Emphasis Curve

4.5 FsOut Clock Domain Modules

4.5.1 Sample Rate Converter

One of the characteristics of a PWM amplifier is that the frequency content of out-of-band noise generated by the modulator is dependent on the PWM switching frequency. The power stage external LC and snubber filter component values are based on this switching frequency. To accommodate input sample rates ranging from 32 kHz to 192 kHz the CS44600 utilizes a Sample Rate Converter (SRC) and several clocking modes that keep the PWM switching frequency fixed.

The SRC supports a range of sample rate conversion to upsample rates from 32 kHz to 192 kHz to a fixed FsOut sample rate. This is typically 384 kHz for most audio applications. The SRC also allows the PWM modulator output to be independent of the input clock jitter since the output of the SRC is clocked from a very stable crystal or oscillator. This results in very low jitter PWM output and higher dynamic range.

4.5.2 Load Compensation Filter

To accommodate varying speaker impedances, the CS44600 incorporates a 2-pole load compensation filter to adjust the effective frequency response of the on-card L/C de-modulation filter. The frequency response of the 2-pole inductor/capacitor filter used on the board to filter out the high-frequency PWM switching clock is highly dependant on the resistive load (speaker) attached.

If the L/C filter implemented was designed for a low impedance load (4 Ω speaker), but an 8 Ω speaker was attached, the frequency response would have a large peaking near the resonant frequency of the L/C. The peaking usually starts at around 15 kHz, with about a +4 dB of gain at around 20 kHz. This phenomenon will cause the system to not meet the frequency response requirements as specified by Dolby Labs.

By using the programmable 2-pole load compensation filter, the overall frequency response of the system can be modified to cut the amount of peaking. The 2 poles of the filter are independently configurable and are concatenated to form the overall filter response. The first filter is defined as a coarse setting. This filter should be programmed to provide most of the attenuation of the peaking. The second filter, defined as the fine adjust, is used to achieve incremental improvements to the overall frequency response. Table 3 shows example register settings based on an output filter that has been designed for a 4 Ω load impedance. See “Channel Compensation Filter - Coarse Adjust (CHXX_CORS[5:0])” on page 62 and “Channel Compensation Filter - Fine Adjust (CHXX_FINE[5:0])” on page 63.

Load Impedance	Coarse Filter Setting	Fine Filter Setting
6 Ω	-1.2 dB	0 dB
8 Ω	-1.8 dB	0 dB
16 Ω	-3.4 dB	0 dB

Table 3. Load Compensation Example Settings

4.5.3 Digital Volume and Mute Control

The CS44600 provides two levels of volume control. A Master Volume Control Register is used to set the volume level across all PWM channels. The register value, which selects a volume range of +24 dB to -127 dB in 0.25 dB steps, is used to control the overall volume setting of all the amplifier channels. Volume control changes are programmable to ramp in increments of 0.125 dB at a variable rate controlled by the SZC[1:0] bits in “Volume Control Configuration (address 06h)” on page 55.

Each PWM channel’s output level is controlled via a Channel Volume Control register operating over the range of +24 dB to -127 dB attenuation with 0.25 dB resolution. See “Channel XX Volume Control - Inte-

ger (addresses 09h - 10h)" on page 58. Volume control changes are programmable to ramp in increments of 0.125 dB at a variable rate controlled by the SZC[1:0] bits.

Each PWM channel output can be independently muted via mute control bits in the register "Channel Mute (address 13h)" on page 60.

When enabled, each CHXX_MUTE bit attenuates the corresponding PWM channel to its maximum value (-127 dB). When the CHXX_MUTE bit is disabled, the corresponding PWM channel returns to the attenuation level set in the Volume Control register. The attenuation is ramped up and down at the rate specified by the SZC[1:0] bits.

4.5.4 Peak Detect / Limiter

The CS44600 has the ability to limit the maximum signal amplitude to prevent clipping. The "Peak Limiter Control Register (address 15h)" on page 60 is used to configure the peak detect and limiter engines' operation. Peak Signal Limiting is performed by digital attenuation. The attack rate is determined by the "Limiter Attack Rate (address 16h)" on page 61. The release rate is determined by the "Limiter Release Rate (address 17h)" on page 61.

4.5.5 PWM Engines

There are three stereo PWM Engines: PWM_ENG_1, PWM_ENG_2, and PWM_ENG_3. Each PWM can handle one stereo pair and connects to a driver or a pair of drivers, depending on the output configuration. Each PWM Engine receives the master clock, PWM_MCLK, from the Clock Control block, and the associated channel data and audio sample timings from the Sample Rate Converter.

The "PWM Configuration Register (address 31h)" on page 68 is used to configure the PWM engines' operation. This register controls the parameters of the PWM engines and can only be changed while the PWM engines are in the power down state.

Features:

- Up to 6 channel support
- 64 Quantization levels
- PSRR compensation feedback
- Programmable Over Sampling - interpolate times 2 (2x) or filter by-pass. By-pass is intended for 384 kHz (single-speed) PWM switch rate support. The interpolate 2x filter is used to upsample the data to support a PWM switch rate of 768 kHz (double speed mode). This enables the output frequency response to extend past 20 kHz when the DAI sample rate is 96 kHz or 192 kHz.
- Programmable registers to move PWM edges for delay adjustment. This lowers the overall noise contribution by allowing each PWM edge to switch at different times.
- Programmable Modulation Setup
  - Min/Max PWM pulse width allowed
  - Programmable Modulation index.

The table below shows the available settings for the PWM Engine for a 384 kHz/768 kHz or 421.875 kHz/843.75 kHz PWM Fswitch rate verses the supported Fsin sample rates using the SRC with a maximum PWM_MCLK of 49.152 MHz/54 MHz.

Fsin (kHz)	Fsout (kHz) using SRC	Quant Level	OSRATE	PWM Switch Rate (kHz)	Required XTAL or SYS_CLK (MHz)
32, 44.1, 48, 88.2, 96, 176.4, 192	384	64	1	384	24.576
		64	2	768	49.152
32, 44.1, 48, 88.2, 96, 176.4, 192	421.875	64	1	421.875	27.000
		64	2	843.75	54.000

Table 4. Typical PWM Switch Rate Settings

4.5.6 Interpolation Filter

The times 2 (2x) interpolation filter is part of the Quantizer and is used to up sample the data to support a higher PWM switch rate. The interpolator is controlled by the OSRATE bit in the "PWM Configuration Register (address 31h)" on page 68 and employs digital filtering to provide high quality interpolation.

4.5.7 Quantizer

The quantizer takes the input audio data at a typical 384 kHz or 768 kHz rate (depending on whether the 2x Interpolator is on or not) from the Interpolator as input. When PSRR is enabled, the quantizer takes the input from PSRR Decimator and uses it to correct for power_supply noise. It also provides protection through min/max pulse limiting hardware to generate outputs that wouldn't violate minimum pulse widths required at the PWM drivers. Its stereo outputs are running at the PWM switch rate.

4.5.8 Modulator

Each output from the Quantizer goes to the Modulator. The Modulator takes the parallel input data at a 384 kHz or 768 kHz, depending on the setting of the OSRATE bit, and changes the parallel data to serial, one-bit outputs. The result is modulated pulses at the selected switch rate with 64 level resolution. The modulator maintains low frequency audio signals, allowing the output to reproduce all low frequency audio content down to 0 Hz.

4.5.9 PWM Outputs

The Modulators outputs are followed by the PWM Configuration block. These signals are routed through delay control blocks where they generate two outputs each. These final outputs are modulated pulses running at the PWM switch rate as determined by the settings shown in Table 4.

Circuitry in the PWM Configuration block guarantees, that no pulses shorter than the minimum pulse are generated. The minimum pulse width is configured using the MIN_PULSE[4:0] bits in the "PWM Minimum Pulse Width Register (address 32h)" on page 69.

The PWM Configuration block also provides the PWM output signal delay mechanism. Adjusting the outputs' delays allows for managing the switching noise between channels, as well as differential signal noise. The "PWMOUT Delay Register (address 33h)" on page 70 specify the delay amount for each PWM Output. The delay is measured in periods of PWM_MCLK.

4.5.10 Power Supply Rejection (PSR) Real-Time Feedback

Inherent to most Class D power amplifier solutions is the requirement for a clean and well-regulated high voltage power supply. Any noise or tones present on the power rail will couple through each channel's power MOSFET output device. These spurious distortion components on the output signal consist of discrete tones, which can be audible from the speaker, and tones that modulate around the audio signal being played.

To remove the requirement for a well-regulated power supply, and therefore reduce overall system costs, the rejection of harmonic distortion from the power supply and tones coupled onto the power rail is accomplished by the patented power supply rejection realtime feedback. By using the CS4461 and associated attenuation circuitry, the scaled AC and DC components of the power supply rail are fed back into the PWM modulator. All delays through the feedback path have been minimized such that the noise cancellation is accomplished in real-time allowing for substantial noise rejection within the output audio signal.

See "Typical Connection Diagrams" on page 22 for examples on how to connect the external ADC (CS4461) to the CS44600 for PSR feedback, "Recommended PSR Calibration Sequence" on page 44, and the CS4461 datasheet.

4.6 Control Port Description and Timing

The control port is used to access the registers, allowing the CS44600 to be configured for the desired operational modes and formats. The operation of the control port may be completely asynchronous with respect to the audio sample rates. However, to avoid potential interference problems, the control port pins should remain static if no operation is required.

The control port has 2 modes: SPI and I²C, with the CS44600 acting as a slave device. SPI mode is selected if there is a high to low transition on the AD0/$\overline{CS}$ pin, after the $\overline{RST}$ pin has been brought high. I²C mode is selected by connecting the AD0/$\overline{CS}$ pin through a resistor to VLC or GND, thereby permanently selecting the desired AD0 bit address state.

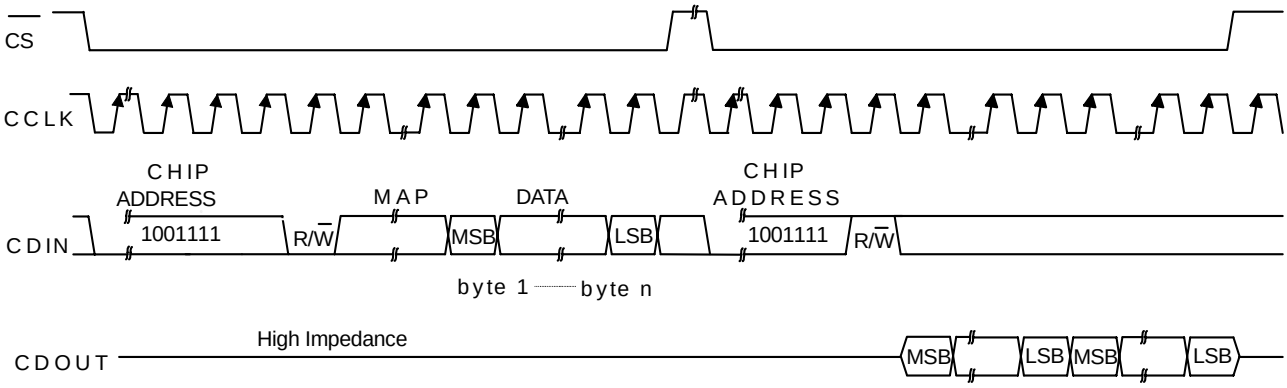
4.6.1 SPI Mode

In SPI mode, $\overline{CS}$ is the CS44600 chip select signal, CCLK is the control port bit clock (input into the CS44600 from the microcontroller), CDIN is the input data line from the microcontroller, CDOUT is the output data line to the microcontroller. Data is clocked in on the rising edge of CCLK and out on the falling edge.

Figure 24 shows the operation of the control port in SPI mode. To write to a register, bring $\overline{CS}$ low. The first seven bits on CDIN form the chip address and must be 1001111. The eighth bit is a read/write indicator (R/$\overline{W}$), which should be low to write. The next eight bits form the Memory Address Pointer (MAP), which is set to the address of the register that is to be updated. The next eight bits are the data which will be placed into the register designated by the MAP. During writes, the CDOUT output stays in the Hi-Z state. It may be externally pulled high or low with a 47 kΩ resistor, if desired

There is a MAP auto increment capability, enabled by the INCR bit in the MAP register. If INCR is a zero, the MAP will stay constant for successive read or writes. If INCR is set to a 1, the MAP will autoincrement after each byte is written, allowing block writes of successive registers. Autoincrement reads are not supported.

To read a register, the MAP has to be set to the correct address by executing a partial write cycle which finishes ($\overline{CS}$ high) immediately after the MAP byte. The MAP auto increment bit (INCR) may be set or not, as desired. To begin a read, bring $\overline{CS}$ low, send out the chip address and set the read/write bit (R/$\overline{W}$) high. The next falling edge of CCLK will clock out the MSB of the addressed register (CDOUT will leave the high impedance state).



MAP = Memory Address Pointer, 8 bits, MSB first

Figure 24. Control Port Timing in SPI Mode

4.6.2 I²C Mode

In I²C mode, SDA is a bidirectional data line. Data is clocked into and out of the part by the clock, SCL. There is no CS pin. Pins AD0 and AD1 form the two least significant bits of the chip address and should be connected through a resistor to VLC or GND as desired. The state of the pins is sensed while the CS44600 is being reset.

The signal timings for a read and write cycle are shown in Figure 25 and Figure 26. A Start condition is defined as a falling transition of SDA while the clock is high. A Stop condition is a rising transition while the clock is high. All other transitions of SDA occur while the clock is low. The first byte sent to the CS44600 after a Start condition consists of a 7 bit chip address field and a R/W bit (high for a read, low for a write). The upper 5 bits of the 7-bit address field are fixed at 10011. To communicate with a CS44600, the chip address field, which is the first byte sent to the CS44600, should match 10011 followed by the settings of the AD1 and AD0. The eighth bit of the address is the R/W bit. If the operation is a write, the next byte is the Memory Address Pointer (MAP) which selects the register to be read or written. If the operation is a read, the contents of the register pointed to by the MAP will be output. Setting the auto increment bit in MAP allows successive writes of consecutive registers. Each byte is separated by an acknowledge bit. The ACK bit is output from the CS44600 after each input byte is read, and is input to the CS44600 from the microcontroller after each transmitted byte. Autoincrement reads are not supported.

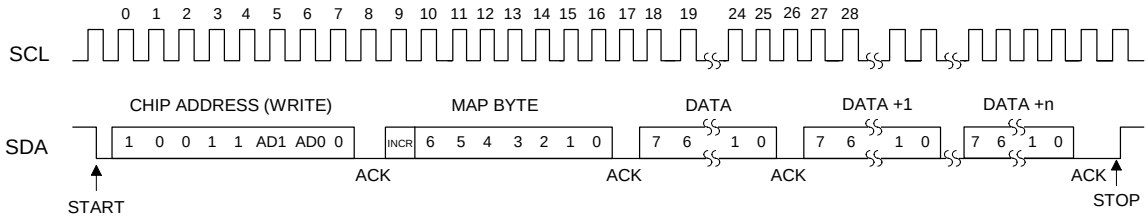


Figure 25. Control Port Timing, I²C Slave Mode Write

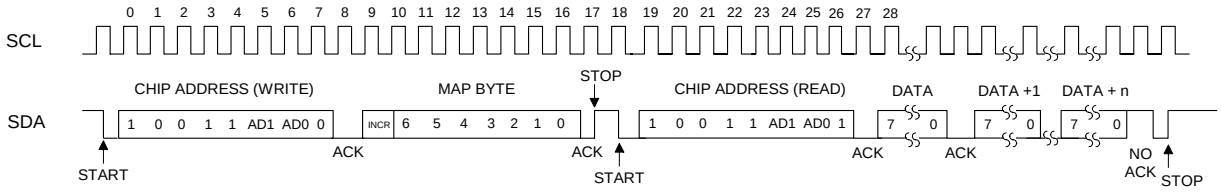


Figure 26. Control Port Timing, I²C Slave Mode Read

Since the read operation can not set the MAP, an aborted write operation is used as a preamble. As shown in Figure 26, the write operation is aborted after the acknowledge for the MAP byte by sending a stop condition. The following pseudocode illustrates an aborted write operation followed by a read operation.

```
Send start condition.
Send 10011xx0 (chip address & write operation).
Receive acknowledge bit.
Send MAP byte, auto increment off.
Receive acknowledge bit.
Send stop condition, aborting write.
Send start condition.
Send 10011xx1(chip address & read operation).
```

```
Receive acknowledge bit.
Receive byte, contents of selected register.
Send acknowledge bit.
Send stop condition.
```

Each byte is separated by an acknowledge bit.

4.6.3 GPIOs

The CS44600 GPIO pins will have the following features:

- Data direction control.
- Programmable open-drain or push-pull driver when configured as an output pin.
- Maskable interrupt for GPIO[3:0] pins when set as a general purpose input.
- Level-sensitive or edge-trigger event selector for all GPIO pins.

4.6.4 Host Interrupt

The CS44600 has a comprehensive interrupt capability. The INT output pin is intended to drive the interrupt input pin on the host microcontroller. The INT pin may be set to be active low, active high or active low with an open-drain driver. This last mode is used for active low, wired-OR hook-ups, with multiple peripherals connected to the microcontroller interrupt input pin.

Many conditions can cause an interrupt, as listed in the interrupt status register descriptions. See “Interrupt Status (address 2Ah) (read only)” on page 64. Each source may be masked off through mask register bits. In addition, each source may be set to rising edge, falling edge, or level sensitive. Combined with the option of level sensitive or edge sensitive modes within the microcontroller, many different configurations are possible, depending on the needs of the equipment designer.

5. POWER SUPPLY, GROUNDING, AND PCB LAYOUT

The CS44600 requires a 2.5 V digital power supply for the core logic. In order to support a number of PWM backend solutions, separate VDP power pins are provided to condition the interface signals to support up to 5.0 V levels. The VDP power pins control the voltage levels for all PWM interface signals, PSR interface signals and GPIO for control and status.

Extensive use of power and ground planes, ground plane fill in unused areas and surface mount decoupling capacitors are recommended. It is necessary to decouple the power supply by placing capacitors directly between the power and ground of the CS44600. The recommended procedure is to place the lowest value capacitor as close as physically possible to each power pin. Decoupling capacitors should be as near to the pins of the CS44600 as possible, with the low value ceramic capacitor being the nearest and mounted on the same side of the board as the CS44600 to minimize inductance effects.

Figure 27 shows the recommended power supply decoupling layout. U1 is the CS44600. C2, C3, C6, C8, C10, C12, C14, and C16 are 0.01 µF X7R capacitors. These should be placed as close as possible to their respective power supply pins. C1, C4, C5, C7, C9, C11, C13, C15, and C17 are 0.1 µF X7R capacitors. C18 is a 10 µF electrolytic capacitor. Top and bottom ground fill should be used as much as possible around all components shown.

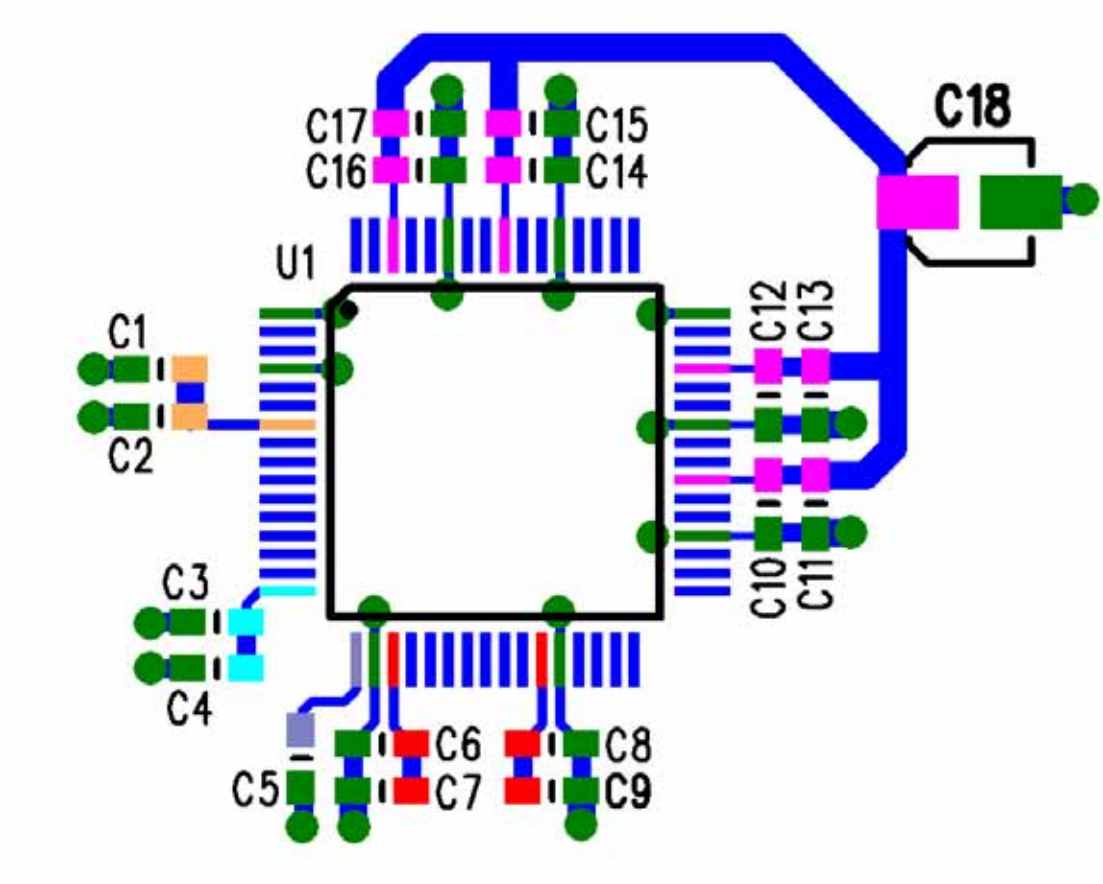


Figure 27. Recommended CS44600 Power Supply Decoupling Layout

Figure 28 shows the recommended crystal circuit layout. U1 is the CS44600. C1 and C2 are the VDX power supply decoupling capacitors. Y1 is the crystal and C3, C4, L1 and C5 are the associated components for the crystal circuit. L1 and C5 are only used for 3rd overtone crystals. C3 and C4 should have a C0G (NPO) dielectric. Care should be taken to minimize the distance between the CS44600 XTI/XTO pins and C3. Top and bottom ground fill should be used as much as possible around and in between all crystal circuit components to minimize noise.

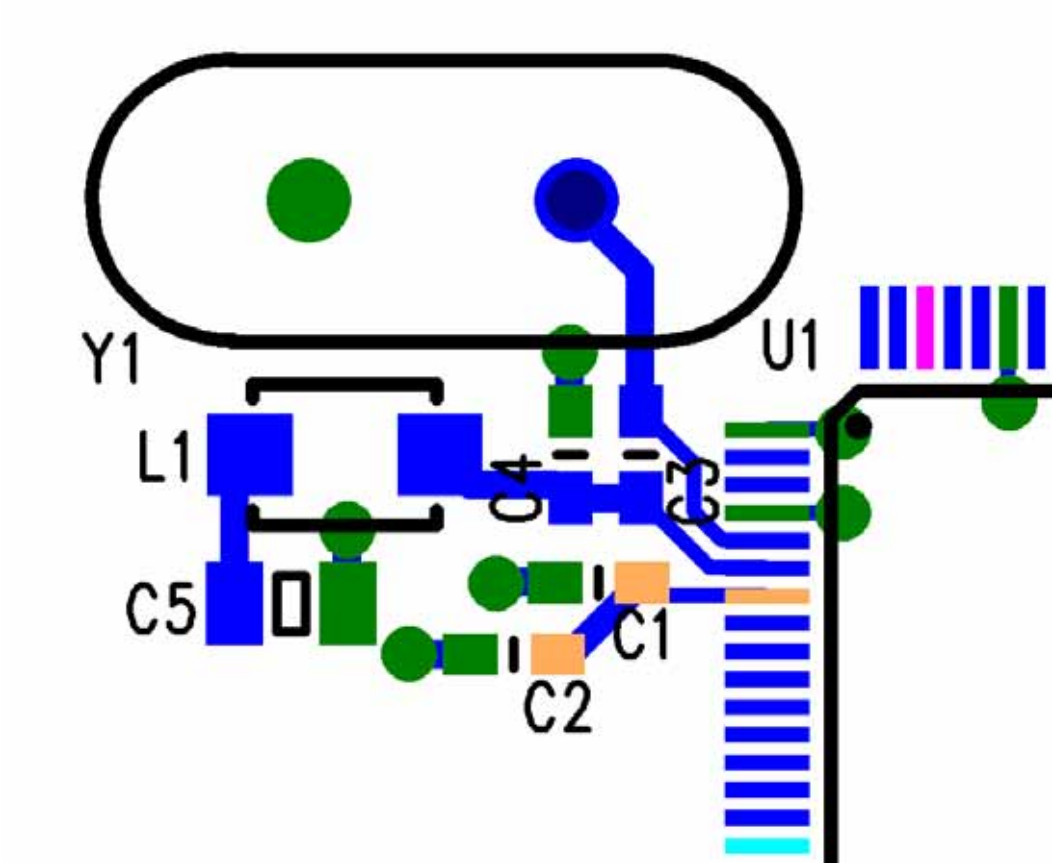


Figure 28. Recommended CS44600 Crystal Circuit Layout

Figure 29 shows the recommended PSR circuit layout. See the CS4461 datasheet for further details on the input buffer and other associated external components. U1 is the CS4461 and U2 is the input buffer op-amp. All supply decoupling should be placed as close as possible to their respective power supply pins. C4 should have a C0G (NPO) dielectric and be placed as close as possible to the CS4461 AIN+/- pins. The CS4461 and input buffer should be placed on the board between the CS44600 and the high voltage power supply. The sense point of the high voltage power supply (the point at which the input buffer taps off of the high voltage power supply) should be close to the middle of the amplifier output channels. If the sense point is taken at either end of the amplifier output channels, inaccurate reading could occur due to localized channel disturbances causing noise on the high voltage power supply. Optimally, the high voltage power connector should also be placed in the middle of the amplifier output channels

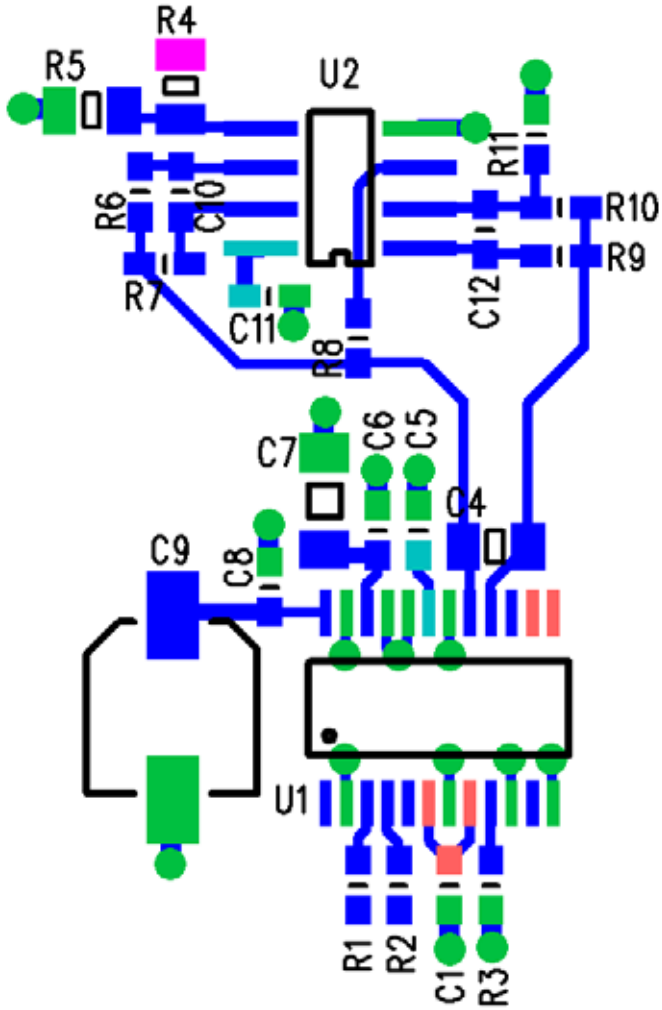


Figure 29. Recommended PSR Circuit Layout

5.1 Reset and Power-Up

Reliable power-up can be accomplished by keeping the device in reset until the power supplies, clocks, and configuration pins are stable. It is also recommended that the RST pin be activated if the voltage supplies drop below the recommended operating condition to prevent power-glitch- related issues.

When RST is low, the CS44600 enters a low-power mode and all internal states are reset, including the control port and registers. When RST is high, the control port becomes operational and the desired settings should be loaded into the control registers. Writing a 0 to the PDN bit in the Power Control Register will then cause the part to leave the low-power state and begin operation.

5.1.1 PWM PopGuard® Transient Control

The CS44600 uses PopGuard® technology to minimize the effects of output transients during power-up and power-down. This technique reduces the audio transients commonly produced by half-bridge, single-supply amplifiers when implemented with external DC-blocking capacitors connected in series with the audio outputs. Each PWM channel can individually be controlled for ramp-up and ramp-down cycles.

When the device is initially powered-up and configured for ramp-up, the PWMOUTxx outputs are clamped to GND. Following a write of a 0 to the PDN_PWMxx bit in the PWM Channel Power Down Control (address 03h) register, each output begins to increase the PWM duty cycle toward the bias voltage point. By a speed set by the RAMP_SPDx bits, the PWMOUTxx outputs will ramp from 0 V (GND) and reach the bias point (50% PWM duty cycle). This gradual voltage ramping allows time for the external DC-blocking capacitor to charge to the bias voltage, minimizing the power-up transient.

To prevent an audible transient at the next power-on, the DC-blocking capacitors must fully discharge before turning off the power. If full discharge does not occur, a transient will occur when the audio outputs are initially clamped to GND.

To prevent transients at power-down, the user must first mute the outputs. When this occurs, audio output ceases and the PWM duty cycle is approximately 50% duty cycle, which represents the mute condition. Once the channels are powered down, the PWMOUTxx outputs slowly decrease the DC offset until it reaches GND. The time required to reach GND is determined by the RAMP_SPDx bits. This allows the DC-blocking capacitors to slowly discharge. Once this charge is dissipated, the power to the device may be turned off, and the system is ready for the next power-on.

5.1.2 Recommended Power-Up Sequence

1. Hold RST low until the power supply and clocks are stable. In this state, all control port registers are reset to the default settings. The PWMOUTxx pins are driven low.
2. The SYS_CLK pin will output a divided-down clock of the signal attached to the XTI pin. If the MUTE pin is held low, SYS_CLK is equal to the XTI frequency. If the MUTE pin is held high, then SYS_CLK is equal to the XTI frequency divided by 2.
3. Bring RST high. The device will remain in a low power state and all registers will contain the specified default value. The logic state of the MUTE pin will be latched and used to specify the clock divider for SYS_CLK. The control port will be accessible at this time.
4. With the CS44600 in the power-down state, PDN bit is ‘1’b, set up the required PWM configuration registers and volume control registers. Configure the GPIO pins for normal operation. Do not enable the power stages at this time.
5. Mute all channel outputs by setting the corresponding CHxx_MUTE bits to ‘1’b.

6. When driving a single-ended (half-bridged) power output stage, set the RAMP[1:0] bits to ‘11’b and the required ramp speed, to initiate a ramp cycle when the channel is powered on. Set MIN_PULSE[4:0] to ‘00000’b.
7. Set the PDN bit to ‘0’b to take the CS44600 out of the power-down state.
8. Start all clocks on the DAI interface (DAI_MCLK, DAI_SCLK, DAI_LRCK). This will initiate the SRC to begin the lock sequence. The SRC lock function can be configured to cause an interrupt condition when lock has been completed. This will be indicated by an active $\overline{\text{INT}}$ signal.
9. Wait for the SRC to lock.
10. If using the PSR feedback, jump to “Recommended PSR Calibration Sequence” on page 44. When finished, continue to step 12. If not using PSR feedback, continue to step 12.
11. Set the appropriate GPIO pin, or other control signal, to enable the power output stage.
12. Enable each channel’s PWM modulator by setting the PDN_PWMxx bit to ‘0’b. If full-bridged, go to step 14. If single-ended (half-bridged), this will initiate a sequence which will slowly increase the DC voltage, from 0V to Vpower÷2, across the AC coupling capacitor. This will eliminate the instantaneous charge across the capacitor which would have caused an audible pop from the speaker.
13. Wait for the ramp-up sequence to complete. The ramp-up function can be configured to cause an interrupt condition when the ramp period has completed. This will be indicated by an active $\overline{\text{INT}}$ signal. Once the ramp-up sequence has completed, set the RAMP[1:0] bits to ‘01’b
14. For full-bridged power output stage configurations, the ramp-up sequence is not required. Enabling the power output stage will not cause an audible pop from the speaker.
15. If using the PSR feedback, set the FEEDBACK_EN bit to ‘1’b.
16. Un-mute all active channels.
17. At this point, the CS44600 is ready to accept audio samples and begin playback.

5.1.3 Recommended PSR Calibration Sequence

1. Set the DEC_SHIFT[2:0]/DEC_SCALE[18:0] coefficient (C_{PSR}) to decimal 1.0 (register 35h = 22h, 36h = 00h, 37h = 00h).
2. Set the PSR_RESET bit to ‘1’b.
3. Set the PSR_EN bit to ‘1’b.
4. Set the PSR_EN bit to ‘0’b.
5. Read DEC_OUTD[23:0].
6. See Figure 30 to adjust the DEC_SHIFT[2:0]/DEC_SCALE[18:0] registers.
7. Continue Recommended Power-Up Sequence.

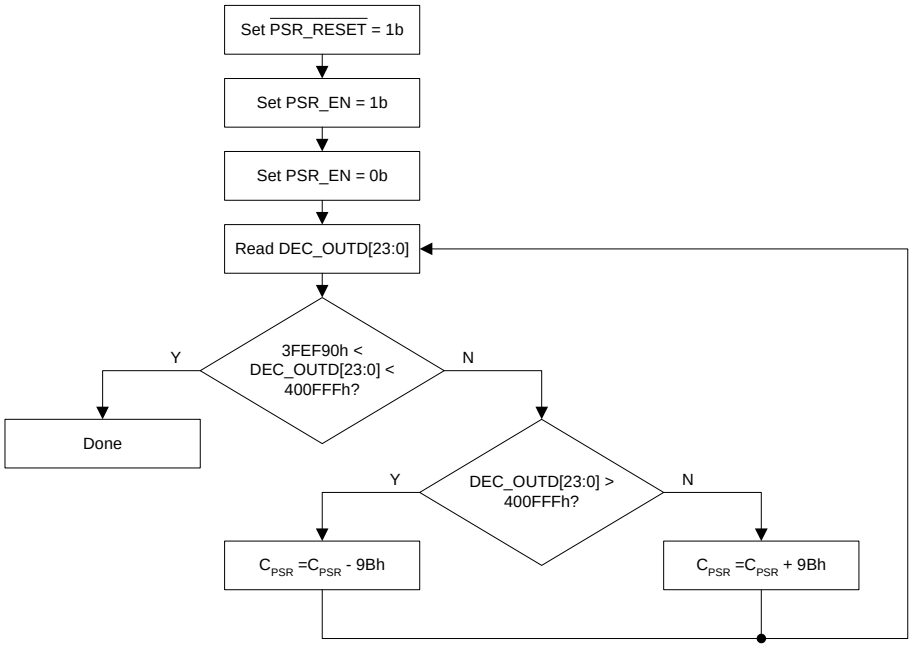


Figure 30. PSR Calibration Sequence

5.1.4 Recommended Power-Down Sequence

1. Mute all channel outputs by setting the corresponding CHxx_MUTE bits to ‘1’b.
2. When driving a single-ended (half-bridged) power output stage, set the RAMP[1:0] bits to ‘01’b and the required ramp speed, to initiate a ramp cycle when the channel is powered down.
3. Power down each channel’s PWM modulator by setting the PDN_PWMxx bit to ‘1’b. If single-ended, this will initiate a sequence which will slowly decrease the DC voltage, from Vpower÷2 to 0 V, across the AC-coupling capacitor.
4. The ramp-down function can be configured to cause an interrupt condition when the ramp period has completed. This will be indicated by an active $\overline{\text{INT}}$ signal.
5. Once the ramp-down sequence has completed, set the appropriate GPIO pin, or other control signal, to power down the power output stage.
6. For full-bridged power output stage configurations, the ramp-down sequence is not required. Powering down the power output stage will not cause an audible pop from the speaker.
7. Concurrently with the ramp-down sequence, if desired, stop all clocks on the DAI interface (DAI_MCLK, DAI_SCLK, DAI_LRCK).
8. Set the PDN bit to ‘1’b to put the CS44600 in the power down state.

6. REGISTER QUICK REFERENCE

Addr	Function	7	6	5	4	3	2	1	0
01h	ID / Rev.	CHIP_ID3	CHIP_ID2	CHIP_ID1	CHIP_ID0	REV_ID3	REV_ID2	REV_ID1	REV_ID0
	page 48 default	1	1	0	0	0	0	0	1
02h	Clock Config / Power Control	EN_SYS_CLK	SYS_CLK_DIV1	SYS_CLK_DIV0	PWM_MCLK_DIV1	PWM_MCLK_DIV0	PDN_XTAL	PDN_OUTPUT_MODE	PDN
	page 49. default	1	0	0	0	0	0	0	1
03h	Chnl Power Down	RESERVED	RESERVED	PDN_PWMB3	PDN_PWMA3	PDN_PWMB2	PDN_PWMA2	PDN_PWMB1	PDN_PWMA1
	page 50. default	1	1	1	1	1	1	1	1
04h	Misc. Config.	DIF2	DIF1	DIF0	RESERVED	AM_FREQ_HOP	FREEZE	DEM1	DEM0
	page 51 default	0	0	1	0	0	0	0	0
05h	Ramp Config	RESERVED	RESERVED	RESERVED	RAMP1	RAMP0	RESERVED	RAMP_SPD1	RAMP_SPD0
	page 52 default	0	0	0	0	0	0	0	1
06h	Vol Control Config	SNGVOL	SZC1	SZC0	RESERVED	MUTE_50/50	SRD_ERR	SRU_ERR	AMUTE
	page 53 default	0	1	0	0	0	0	0	1
07h	Master Vol. Control - Integer	MSTR_IVOL7	MSTR_IVOL6	MSTR_IVOL5	MSTR_IVOL4	MSTR_IVOL3	MSTR_IVOL2	MSTR_IVOL1	MSTR_IVOL0
	page 55 default	0	0	0	0	0	0	0	0
08h	Master Vol. Control - Fraction	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	MSTR_FVOL1	MSTR_FVOL0
	page 55 default	0	0	0	0	0	0	0	0
09h	Channel A1 Vol. Control - Integer	CHA1_IVOL7	CHA1_IVOL6	CHA1_IVOL5	CHA1_IVOL4	CHA1_IVOL3	CHA1_IVOL2	CHA1_IVOL1	CHA1_IVOL0
	page 57 default	0	0	0	0	0	0	0	0
0Ah	Channel B1 Vol. Control - Integer	CHB1_IVOL7	CHB1_IVOL6	CHB1_IVOL5	CHB1_IVOL4	CHB1_IVOL3	CHB1_IVOL2	CHB1_IVOL1	CHB1_IVOL0
	page 57 default	0	0	0	0	0	0	0	0
0Bh	Channel A2 Vol. Control - Integer	CHA2_IVOL7	CHA2_IVOL6	CHA2_IVOL5	CHA2_IVOL4	CHA2_IVOL3	CHA2_IVOL2	CHA2_IVOL1	CHA2_IVOL0
	page 57 default	0	0	0	0	0	0	0	0
0Ch	Channel B2 Vol. Control - Integer	CHB2_IVOL7	CHB2_IVOL6	CHB2_IVOL5	CHB2_IVOL4	CHB2_IVOL3	CHB2_IVOL2	CHB2_IVOL1	CHB2_IVOL0
	page 57 default	0	0	0	0	0	0	0	0
0Dh	Channel A3 Vol. Control - Integer	CHA3_IVOL7	CHA3_IVOL6	CHA3_IVOL5	CHA3_IVOL4	CHA3_IVOL3	CHA3_IVOL2	CHA3_IVOL1	CHA3_IVOL0
	page 57 default	0	0	0	0	0	0	0	0
0Eh	Channel B3 Vol. Control - Integer	CHB3_IVOL7	CHB3_IVOL6	CHB3_IVOL5	CHB3_IVOL4	CHB3_IVOL3	CHB3_IVOL2	CHB3_IVOL1	CHB3_IVOL0
	page 57 default	0	0	0	0	0	0	0	0
0Fh	Reserved	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
	default	0	0	0	0	0	0	0	0
10h	Reserved	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
	default	0	0	0	0	0	0	0	0

Addr	Function	7	6	5	4	3	2	1	0
11h	Channel Vol. Control 1-Fraction	CHB2_FVOL1	CHB2_FVOL0	CHA2_FVOL1	CHA2_FVOL0	CHB1_FVOL1	CHB1_FVOL0	CHA1_FVOL1	CHA1_FVOL0
	page 57. default	0	0	0	0	0	0	0	0
12h	Channel Vol. Control 2-Fraction	RESERVED	RESERVED	RESERVED	RESERVED	CHB3_FVOL1	CHB3_FVOL0	CHA3_FVOL1	CHA3_FVOL0
	page 57 default	0	0	0	0	0	0	0	0
13h	Channel Mute	RESERVED	RESERVED	CHB3_MUTE	CHA3_MUTE	CHB2_MUTE	CHA2_MUTE	CHB1_MUTE	CHA1_MUTE
	page 58 default	0	0	0	0	0	0	0	0
14h	Channel Invert	RESERVED	RESERVED	CHB3_INV	CHA3_INV	CHB2_INV	CHA2_INV	CHB1_INV	CHA1_INV
	page 58 default	0	0	0	0	0	0	0	0
15h	Peak Limiter Control	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	LIMIT_ALL	LIMIT_EN
	page 59 default	0	0	0	0	0	0	0	0
16h	Limiter Attack Rate	ARATE7	ARATE6	ARATE5	ARATE4	ARATE3	ARATE2	ARATE1	ARATE0
	page 59 default	0	0	0	1	0	0	0	0
17h	Limiter Release Rate	RRATE7	RRATE6	RRATE5	RRATE4	RRATE3	RRATE2	RRATE1	RRATE0
	page 60 default	0	0	1	0	0	0	0	0
18h	Chnl A1 Comp. Filter - Coarse Adj	RESERVED	RESERVED	CHA1_CORS5	CHA1_CORS4	CHA1_CORS3	CHA1_CORS2	CHA1_CORS1	CHA1_CORS0
	page 60 default	0	0	0	0	0	0	0	0
19h	Chnl A1 Comp. Filter - Fine Adj	RESERVED	RESERVED	CHA1_FINE5	CHA1_FINE4	CHA1_FINE3	CHA1_FINE2	CHA1_FINE1	CHA1_FINE0
	page 61 default	0	0	0	0	0	0	0	0
1Ah	Chnl B1 Comp. Filter - Coarse Adj	RESERVED	RESERVED	CHB1_CORS5	CHB1_CORS4	CHB1_CORS3	CHB1_CORS2	CHB1_CORS1	CHB1_CORS0
	page 60 default	0	0	0	0	0	0	0	0
1Bh	Chnl B1 Comp. Filter - Fine Adj	RESERVED	RESERVED	CHB1_FINE5	CHB1_FINE4	CHB1_FINE3	CHB1_FINE2	CHB1_FINE1	CHB1_FINE0
	page 61 default	0	0	0	0	0	0	0	0
1Ch	Chnl A2 Comp. Filter - Coarse Adj	RESERVED	RESERVED	CHA2_CORS5	CHA2_CORS4	CHA2_CORS3	CHA2_CORS2	CHA2_CORS1	CHA2_CORS0
	page 60 default	0	0	0	0	0	0	0	0
1Dh	Chnl A2 Comp. Filter - Fine Adj	RESERVED	RESERVED	CHA2_FINE5	CHA2_FINE4	CHA2_FINE3	CHA2_FINE2	CHA2_FINE1	CHA2_FINE0
	page 61 default	0	0	0	0	0	0	0	0
1Eh	Chnl B2 Comp. Filter - Coarse Adj	RESERVED	RESERVED	CHB2_CORS5	CHB2_CORS4	CHB2_CORS3	CHB2_CORS2	CHB2_CORS1	CHB2_CORS0
	page 60 default	0	0	0	0	0	0	0	0
1Fh	Chnl B2 Comp. Filter - Fine Adj	RESERVED	RESERVED	CHB2_FINE5	CHB2_FINE4	CHB2_FINE3	CHB2_FINE2	CHB2_FINE1	CHB2_FINE0
	page 61 default	0	0	0	0	0	0	0	0
20h	Chnl A3 Comp. Filter - Coarse Adj	RESERVED	RESERVED	CHA3_CORS5	CHA3_CORS4	CHA3_CORS3	CHA3_CORS2	CHA3_CORS1	CHA3_CORS0
	page 60 default	0	0	0	0	0	0	0	0

Addr	Function	7	6	5	4	3	2	1	0
21h	Chnl A3 Comp. Filter - Fine Adj	RESERVED	RESERVED	CHA3_FINE5	CHA3_FINE4	CHA3_FINE3	CHA3_FINE2	CHA3_FINE1	CHA3_FINE0
	page 61 default	0	0	0	0	0	0	0	0
22h	Chnl B3 Comp. Filter - Coarse Adj	RESERVED	RESERVED	CHB3_CORS5	CHB3_CORS4	CHB3_CORS3	CHB3_CORS2	CHB3_CORS1	CHB3_CORS0
	page 60 default	0	0	0	0	0	0	0	0
23h	Chnl B3 Comp. Filter - Fine Adj	RESERVED	RESERVED	CHB3_FINE5	CHB3_FINE4	CHB3_FINE3	CHB3_FINE2	CHB3_FINE1	CHB3_FINE0
	page 61 default	0	0	0	0	0	0	0	0
24h	Reserved	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
	default	0	0	0	0	0	0	0	0
25h	Reserved	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
	default	0	0	0	0	0	0	0	0
26h	Reserved	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
	default	0	0	0	0	0	0	0	0
27h	Reserved	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
	default	0	0	0	0	0	0	0	0
28h	Interrupt Mode Control	INT1	INT0	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	OVFL_L/E
	page 61 default	0	0	0	0	0	0	0	0
29h	Interrupt Mask	M_SRC_UNLOCK	M_SRC_LOCK	M_RMPUP_DONE	M_RMPDN_DONE	M_MUTE_DONE	M_OVFL_INT	RESERVED	RESERVED
	page 62 default	0	0	0	0	0	0	0	0
2Ah	Interrupt Status	SRC_UNLOCK	SRC_LOCK	RMPUP_DONE	RMPDN_DONE	MUTE_DONE	OVFL_INT	GPIO_INT	RESERVED
	page 62 default	0	0	0	0	0	0	0	0
2Bh	Chnl Over Flow Status	RESERVED	RESERVED	CHB3_OVFL	CHA3_OVFL	CHB2_OVFL	CHA2_OVFL	CHB1_OVFL	CHA1_OVFL
	page 64 default	0	0	0	0	0	0	0	0
2Ch	GPIO Pin I/O	RESERVED	GPIO6_I/O	GPIO5_I/O	GPIO4_I/O	GPIO3_I/O	GPIO2_I/O	GPIO1_I/O	GPIO0_I/O
	page 64 default	0	0	0	0	0	0	0	0
2Dh	GPIO Pin Polarity/Type	RESERVED	GPIO6_P/T	GPIO5_P/T	GPIO4_P/T	GPIO3_P/T	GPIO2_P/T	GPIO1_P/T	GPIO0_P/T
	ppage 64 default	0	1	1	1	1	1	1	1
2Eh	GPIO Pin Level/Edge trigger	RESERVED	GPIO6_L/E	GPIO5_L/E	GPIO4_L/E	GPIO3_L/E	GPIO2_L/E	GPIO1_L/E	GPIO0_L/E
	page 65 default	0	0	0	0	0	0	0	0
2Fh	GPIO Pin Status	RESERVED	GPIO6_STATUS	GPIO5_STATUS	GPIO4_STATUS	GPIO3_STATUS	GPIO2_STATUS	GPIO1_STATUS	GPIO0_STATUS
	page 65 default	X	X	X	X	X	X	X	X
30h	GPIO Interrupt Mask	RESERVED	RESERVED	RESERVED	RESERVED	M_GPIO3	M_GPIO2	M_GPIO1	M_GPIO0
	page 66 default	0	0	0	0	0	0	0	0
31h	PWM Config	OSRATE	RESERVED	RESERVED	A1/B1_OUT_CNFG	A2/B2_OUT_CNFG	A3_OUT_CNFG	B3_OUT_CNFG	RESERVED
	page 66 default	0	0	0	0	0	0	0	0

Addr	Function	7	6	5	4	3	2	1	0
32h	PWM Minimum Pulse Width	DISABLE_ PWMOUTxx-	RESERVED	RESERVED	MIN_PULSE4	MIN_PULSE3	MIN_PULSE2	MIN_PULSE1	MIN_PULSE0
	page 67 default	0	0	0	0	0	0	0	0
33h	PWMOUT Delay	DIFF_DLY2	DIFF_DLY1	DIFF_DLY0	CHNL_DLY4	CHNL_DLY3	CHNL_DLY2	CHNL_DLY1	CHNL_DLY0
	page 68 default	0	0	0	0	0	0	0	0
34h	PSR / Power Supply Config	PSR_EN	PSR_RESET	FEEDBACK_ EN	RESERVED	RESERVED	PS_SYNC_DIV2	PS_SYNC_DIV1	PS_SYNC_DIV0
	page 69 default	0	0	0	0	0	0	0	0
35h	PSR_Decimator Scaled	RESERVED	DEC_SHIFT2	DEC_SHIFT1	DEC_SHIFT0	RESERVED	DEC_SCALED18	DEC_SCALED17	DEC_SCALED16
	page 70 default	0	0	1	0	0	0	1	0
36h	PSR_Decimator Scaled	DEC_SCALED15	DEC_SCALED14	DEC_SCALED13	DEC_SCALED12	DEC_SCALED11	DEC_SCALED10	DEC_SCALED09	DEC_SCALED08
	page 70 default	0	1	0	1	1	0	0	0
37h	PSR_Decimator Scaled	DEC_SCALED07	DEC_SCALED06	DEC_SCALED05	DEC_SCALED04	DEC_SCALED03	DEC_SCALED02	DEC_SCALED01	DEC_SCALED00
	page 70 default	0	1	1	0	1	0	0	0
38h	Reserved	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
	default	0	0	0	0	0	0	0	0
39h	Reserved	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
	default	0	0	0	0	0	0	0	0
3Ah	Reserved	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
	default	0	0	0	0	0	0	0	0
3Bh	PSR_Decimator Outd	DEC_OUTD23	DEC_OUTD22	DEC_OUTD21	DEC_OUTD20	DEC_OUTD19	DEC_OUTD18	DEC_OUTD17	DEC_OUTD16
	page 71 default	0	0	0	0	0	0	0	0
3Ch	PSR_Decimator Outd	DEC_OUTD15	DEC_OUTD14	DEC_OUTD13	DEC_OUTD12	DEC_OUTD11	DEC_OUTD10	DEC_OUTD09	DEC_OUTD08
	page 71 default	0	0	0	0	0	0	0	0
3Dh	PSR_Decimator Outd	DEC_OUTD07	DEC_OUTD06	DEC_OUTD05	DEC_OUTD04	DEC_OUTD03	DEC_OUTD02	DEC_OUTD01	DEC_OUTD00
	page 71 default	0	0	0	0	0	0	0	0

7. REGISTER DESCRIPTION

All registers are read/write except for I.D. and Revision Register, Interrupt Status and Decimator OutD registers which are read only. See the following bit definition tables for bit assignment information. The default state of each bit after a power-up sequence or reset is listed in each bit description.

7.1 Memory Address Pointer (MAP)

Not a register

7	6	5	4	3	2	1	0
INCR	MAP6	MAP5	MAP4	MAP3	MAP2	MAP1	MAP0

7.1.1 Increment (INCR)

Default = 1
Function:

memory address pointer auto increment control

- 0 - MAP is not incremented automatically.
- 1 - Internal MAP is automatically incremented after each read or write.

7.1.2 Memory Address Pointer (MAPx)

Default = 0000001
Function:

Memory address pointer (MAP). Sets the register address that will be read or written by the control port.

7.2 CS44600 I.D. and Revision Register (address 01h) (Read Only)

7	6	5	4	3	2	1	0
CHIP_ID3	CHIP_ID2	CHIP_ID1	CHIP_ID0	REV_ID3	REV_ID2	REV_ID1	REV_ID0

7.2.1 Chip I.D. (Chip_IDx)

Default = 1101
Function:

I.D. code for the CS44600. Permanently set to 1101.

7.2.2 Chip Revision (Rev_IDx)

Default = 0001
Function:

CS44600 revision level. Revision A is coded as 0001.

7.3 Clock Configuration and Power Control (address 02h)

7	6	5	4	3	2	1	0
EN_SYS_CLK	SYS_CLK_DIV1	SYS_CLK_DIV0	PWM_MCLK_DIV1	PWM_MCLK_DIV0	PDN_XTAL	PDN_OUTPUT_MODE	PDN

7.3.1 Enable SYS_CLK Output (EN_SYS_CLK)

Default = 1
Function:

This bit enables the driver for the SYS_CLK signal. If the SYS_CLK output is unused, this bit should be set to '0'b to disable the driver.

7.3.2 SYS_CLK Clock Divider Settings (SYS_CLK_DIV[1:0])

Default = 00
Function:

These two bits determine the divider for the XTAL clock signal for generating the SYS_CLK signal. During a reset condition, with the RST input pin held low, the logic level on the MUTE input pin will determine the divider used for the SYS_CLK output. If MUTE is pulled low, the SYS_CLK divider will be set to divide the clock frequency on XTI by a factor of 1. If the MUTE pin is pulled high, the SYS_CLK output will be set to perform a divide-by-2 on the XTI clock. The state of the MUTE pin will be latched on the rising edge of the RST. The MUTE pin can then be used as defined.

SYS_CLK_DIV[1:0]	SYS_CLK Clock Divider
00	Use state of MUTE input pin following RST condition
01	Divide by 2
10	Divide by 4
11	Divide by 8

7.3.3 PWM Master Clock Divider Settings (PWM_MCLK_DIV[1:0])

Default = 00
Function:

These two bits determine the divider for the XTAL clock signal for generating the PWM_MCLK signal.

PWM_MCLK_DIV[1:0]	PWM Master Clock Divider
00	Divide by 1
01	Divide by 2
10	Divide by 4
11	Divide by 8

7.3.4 Power Down XTAL (PDN_XTAL)

Default = 0
0 - Crystal Oscillator Circuit is running.
1 - Crystal Oscillator Circuit is powered down.
Function:

This bit is used to power down the crystal oscillator circuitry when not being used. When using a clock signal attached to the XTI input, this bit should be set to '1'b.

7.3.5 Power Down Output Mode (PDN_OUTPUT_MODE)

Default = 0
0 - PWM Outputs are driven low during power down
1 - PWM Outputs are driven to the inactive state during power down
Function:

This bit is used to select the power-down state of the PWM output signals. When set to 0, each channel which has been powered down, following the ramp-down cycle if enabled, will drive the output signals, PWMOUTxx+ and PWMOUTxx-, low.

When set to 1, each channel which has been powered down, following the ramp-down cycle if enabled, will drive the output signals to the inactive state. PWMOUTxx+ is driven low and PWMOUTxx- is driven high.

7.3.6 Power Down (PDN)

Default = 1
0 - Normal Operation
1 - Power down

Function:

The entire device will enter a low-power state when this function is enabled, and the contents of the control registers are retained in this mode. The power-down bit defaults to 'enabled' on power-up and must be disabled before normal operation can occur.

7.4 PWM Channel Power Down Control (address 03h)

7	6	5	4	3	2	1	0
RESERVED	RESERVED	PDN_PWMB3	PDN_PWMA3	PDN_PWMB2	PDN_PWMA2	PDN_PWMB1	PDN_PWMA1

7.4.1 Power Down PWM Channels (PDN_PWMB3:PDN_PWMA1)

Default = 11111111
0 - Normal Operation
1 - Power down PWM channel

Function:

The specific PWM channel is in the power-down state. All processing is halted for the specific channel, but does not alter the setup or delay register values. The PWM output signals are driven to the appropriate logic level as defined by the Power-Down Output Mode bit, PDN_OUTPUT_MODE. When set to normal operation, the specific channel will power up according to the state of the RAMP[1:0] bits and the channel output configuration selected. When transitioning from normal operation to power down, the specific channel will power down according to the state of the RAMP[1:0] bits and the channel output configuration selected. Ramp control is found in "Ramp Configuration (address 05h)" on page 54.

7.5 Misc. Configuration (address 04h)

7	6	5	4	3	2	1	0
DIF2	DIF1	DIF0	RESERVED	AM_FREQ_HOP	FREEZE	DEM1	DEM0

7.5.1 Digital Interface Format (DIFX)

Default = 001
Function:

These bits select the digital interface format used for the DAI Serial Port. The required relationship between the Left/Right clock, serial clock, and serial data is defined by the Digital Interface Format and the options are detailed in Figures 17 - 22.

DIF2	DIF1	DIF0	Description	Figure
0	0	0	Left-Justified, up to 24-bit data	18
0	0	1	I²S, up to 24-bit data	17
0	1	0	Right-Justified, 16-bit data	19
0	1	1	Right-Justified, 24-bit data	19
1	0	0	One-Line mode #1, 20-bit data	20
1	0	1	One-Line mode #2, 24-bit data	21
1	1	0	TDM Mode, up to 32-bit data	22

Table 5. Digital Audio Interface Formats

7.5.2 AM Frequency Hopping (AM_FREQ_HOP)

Default = 0
Function:

Enables the modulator to alter the PWM switch timings to remove interference when the desired frequency from an AM tuner is positioned near the PWM switching rate. The PWM modulator circuitry must first be powered down using the PDN bit in the Clock Configuration and Power Control (address 02h) Register before this feature can be enabled. There will be a delay following the power-up sequence due to the re-locking of the SRC. Once this feature is enabled, the output switch rate is divided by 2.25, resulting in a lowered PWM switch rate. Care should be taken to ensure that:

PWM_MCLK / 16 > the upper frequency limit of the AM tuner used

7.5.3 Freeze Controls (FREEZE)

Default = 0
Function:

This function will freeze the previous output of, and allow modifications to be made to the Master Volume Control (address 07h-08h), Channel XX Volume Control (address 09h-12h), and Channel Mute (address 13h) registers without the changes taking effect until the FREEZE bit is disabled. To make multiple changes in these control port registers take effect simultaneously, enable the FREEZE bit, make all register changes, then disable the FREEZE bit.

7.5.4 De-Emphasis Control (DEM[1:0])

Default = 00
00 - no de-emphasis
01 - 32 kHz de-emphasis filter
10 - 44.1 kHz de-emphasis filter
11 - 48 kHz de-emphasis filter
Function:

Enables the appropriate digital filter to maintain the standard 15 ms/50 ms digital de-emphasis filter response.

7.6 Ramp Configuration (address 05h)

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RAMP1	RAMP0	RESERVED	RAMP_SPD1	RAMP_SPD0

7.6.1 Ramp-Up/Down Setting (RAMP[1:0])

Default = 00
00 - Ramp-up and ramp-down are disabled
01 - Ramp-up is disabled. Ramp-down is enabled.
10 - Reserved
11 - Ramp-up and ramp-down are enabled. Note that after a ramp-up sequence has completed, audio will not play until RAMP[1:0] is set to 01.

Function:

When ramping is enabled, the duty cycle of the output PWM signal is increased (ramp-up) or decreased (ramp-down) at a rate determined by the Ramp Speed variable (RAMP_SPDx). This function is used in single-ended applications to reduce pops in the output caused by the DC-blocking capacitor. When the ramp-up/down function is disabled in single-ended applications, there will be an abrupt change in the output signal. Refer to Section 5.1.1 .

If ramp-up or down is not needed, as in a full-bridge application, these bits should be set to 00. If ramp-up or down is needed, as in a single-ended half-bridge application, these bits must be used in the proper sequence as outlined in “Recommended Power-Up Sequence” on page 43 and “Recommended Power-Down Sequence” on page 45.

7.6.2 Ramp Speed (RAMP_SPD[1:0])

Default = 01
00 - Ramp speed = approximately 0.1 seconds
01 - Ramp speed = approximately 0.2 seconds
10 - Ramp speed = approximately 0.3 seconds
11 - Ramp speed = approximately 0.65 seconds

Function:

This feature is used in single-ended applications to reduce pops in the output caused by the DC-blocking capacitor. The Ramp Speed sets the time for the PWM signal to linearly ramp-up and down from the bias point (50% PWM duty cycle). Refer to Section 5.1.1

7.7 Volume Control Configuration (address 06h)

7	6	5	4	3	2	1	0
SNGVOL	SZC1	SZC0	RESERVED	MUTE_50/50	SRD_ERR	SRU_ERR	AMUTE

7.7.1 Single Volume Control (SNGVOL)

Default = 0
Function:

The individual channel volume levels are independently controlled by their respective Volume Control registers when this function is disabled. When enabled, the volume on all channels is determined by the A1 Channel Volume Control register. The other Volume Control registers are ignored.

7.7.2 Soft Ramp and Zero Cross Control (SZC[1:0])

Default = 10
00 - Immediate Change
01 - Zero Cross
10 - Soft Ramp
11 - Soft Ramp on Zero Crossings
Function:

Immediate Change

When Immediate Change is selected, all level changes will take effect immediately in one step.

Zero Cross

Zero Cross Enable dictates that signal level changes, either by attenuation changes or muting, will occur on a signal zero crossing to minimize audible artifacts. The requested level change will occur after a timeout period (approximately 18.7 ms for a PWM switch rate of 384/768 kHz and 17.0 ms for a PWM switch rate of 421.875/843.75 kHz) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel.

Soft Ramp

Soft Ramp allows level changes, both muting and attenuation, to be implemented by incrementally ramping, in 1/8 dB steps, from the current level to the new level at a rate of 1 dB per 8 left/right clock periods.

Soft Ramp on Zero Crossing

Soft Ramp and Zero Cross Enable dictates that signal level changes, either by attenuation changes or muting, will occur in 1/8-dB steps and be implemented on a signal zero crossing. The 1/8-dB level change will occur after a timeout period (approximately 18.7 ms for a PWM switch rate of 384/768 kHz and 17.0 ms for a PWM switch rate of 421.875/843.75 kHz) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel.

7.7.3 Enable 50% Duty Cycle for Mute Condition (MUTE_50/50)

Default = 0
0 - Disabled
1 - Enabled

Function:

This bit enables the modulator to output an exact 50%-duty-cycle PWM signal (not modulated), which corresponds to digital silence, for all mute conditions. The muting function is affected, similar to volume con-

trol changes, by the Soft and Zero Cross bits (SZC[1:0]). This bit does not cause a mute condition to occur. The MUTE_50/50 bit only defines operation during a normal mute condition.

When MUTE_50/50 is set and a mute condition occurs, PSR will not affect the output of the modulator, regardless if PSR is enabled. Output noise may be increased in this case if the noise on the high voltage power supply is greater than the system noise. Therefore, it is recommended that if a noisy power supply is used in a single-ended half-bridge configuration with PSR enabled, MUTE_50/50 should be disabled and a normal, modulated mute should be used. This will allow the modulator to use the PSR feedback to reject power supply noise and improve system performance.

7.7.4 Soft Ramp-Down on Interface Error (SRD_ERR)

Default = 0
0 - Disabled
1 - Enabled
Function:

A mute will be performed upon detection of a timing error on the Digital Audio Interface or if an SRC_LOCK error has occurred. An SRC_LOCK interrupt is an indication that the sample rate converter timings have become unstable, or have changed abruptly. Audio data from the SRC is no longer considered valid and could cause unwanted pops or clicks.

When this feature is enabled, this mute is affected, similar to attenuation changes, by the Soft and Zero Cross bits (SZC[1:0]). When disabled, an immediate mute is performed on detection of an error.

Note: For best results, it is recommended that this bit be used in conjunction with the SRU_ERR bit.

7.7.5 Soft Ramp-Up on Recovered Interface Error (SRU_ERR)

Default = 0
0 - Disabled
1 - Enabled
Function:

An un-mute will be performed after a MCLK/LRCK ratio change, recovered DAI timing error, or after the SRC has gained lock. When this feature is enabled, this un-mute is affected, similar to attenuation changes, by the Soft and Zero Cross bits (SZC[1:0]). When disabled, an immediate un-mute is performed in these instances.

Note: For best results, it is recommended that this bit be used in conjunction with the SRD_ERR bit.

7.7.6 Auto-Mute (AMUTE)

Default = 1
0 - Disabled
1 - Enabled
Function:

The PWM converters of the CS44600 will mute the output following the reception of 8192 consecutive audio samples of static 0 or -1. A single sample of non-static data will release the mute. Detection and muting is done independently for each channel. The muting function is affected, similar to volume control changes, by the Soft and Zero Cross bits (SZC[1:0]).

7.8 Master Volume Control - Integer (address 07h)

7	6	5	4	3	2	1	0
MSTR_IVOL7	MSTR_IVOL6	MSTR_IVOL5	MSTR_IVOL4	MSTR_IVOL3	MSTR_IVOL2	MSTR_IVOL1	MSTR_IVOL0

7.8.1 Master Volume Control - Integer (MSTR_IVOL[7:0])

Default = 00000000
Function:

The Master Volume Control - Integer register allows global control of the signal levels on all channels in 1 dB increments from +24 to -127 dB. Volume settings are decoded as shown in Table 6. The volume changes are implemented as specified by the Soft and Zero Cross bits (SZC[1:0]). All volume settings greater than 00011000b are equivalent to +24 dB. Binary values for integer volume settings less than 0 dB are in two's complement form.

MSTR_IVOL[7:0]	Hex Value	Volume Setting
0001 1000	18	+24 dB
0001 0111	17	+23 dB
0000 0001	01	+1 dB
0000 0000	00	0 dB
1111 1111	FF	-1 dB
1111 1110	FE	-2 dB
1000 0001	81	-127 dB

Table 6. Master Integer Volume Settings

7.9 Master Volume Control - Fraction (address 08h)

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	MSTR_FVOL1	MSTR_FVOL0

7.9.1 Master Volume Control - Fraction (MSTR_FVOL[1:0])

Default = 00
00 - +0.00 dB
01 - +0.25 dB
10 - +0.50 dB
11 - +0.75 dB

Function:

The Master Volume Control - Fraction register is an additional offset to the value in the Master Volume Control - Integer register and allows global control of the signal levels on all channels in 0.25 dB increments. Volume settings are decoded as shown in Table 7. These volume changes are implemented as specified by the Soft and Zero Cross bits (SZC[1:0]). All volume settings greater than 00011000b are equivalent to +24 dB. Binary values for integer and fractional volume settings less than 0 dB are in two's complement form.

To calculate from a positive decimal integer:fraction value to a binary positive integer:fraction value, do the following:

1. Convert the decimal integer to binary. This is MSTR_IVOL[7:0].

2. Select the bit representation of the desired 0.25 fractional increment. This is MSTR_FVOL[1:0].

To calculate from a negative decimal integer:fraction value to a binary, 2's complement integer:fraction value, do the following:

1. Convert the decimal integer to binary. This is MSTR_IVOL[7:0].
2. Select the bit representation of the desired 0.25 fractional increment. This is MSTR_FVOL[1:0].
3. Concatenate MSTR_IVOL[7:0]: MSTR_FVOL[1:0] to form a 10-bit binary value.
4. Perform a 2's complement conversion on all 10 bits.
   The upper 8 bits are now the new MSTR_FVOL[7:0] and the two lower bits are MSTR_FVOL[1:0].

To convert from a 2's complement integer:fraction value to a negative decimal, do the following:

1. Concatenate MSTR_IVOL[7:0]: MSTR_FVOL[1:0] to form a 10-bit binary value.
2. Perform a 2's complement conversion on all 10 bits.
3. Convert the 10-bit binary number to a decimal value.
4. Divide the decimal value by 4.

MSTR_IVOL[7:0]	MSTR_FVOL(1:0)	Volume Setting
0001 1000	00	+24.00 dB
0001 0111	10	+23.50 dB
0000 0001	11	+1.75 dB
0000 0001	00	+1.00 dB
0000 0000	01	+0.25 dB
0000 0000	00	0 dB
1111 1111	10	-0.50 dB
1111 1111	00	-1.00 dB
1111 1110	11	-1.25 dB
1111 1101	10	-2.50 dB
1000 0010	00	-126.00 dB
1000 0001	11	-126.25 dB
1000 0001	00	-127.00 dB

Table 7. Master Fractional Volume Settings

7.10 Channel XX Volume Control - Integer (addresses 09h - 0Eh)

7	6	5	4	3	2	1	0
CHXX_IVOL7	CHXX_IVOL6	CHXX_IVOL5	CHXX_IVOL4	CHXX_IVOL3	CHXX_IVOL2	CHXX_IVOL1	CHXX_IVOL0

7.10.1 Channel Volume Control - Integer (CHXx_IVOL[7:0])

Default = 00000000
Function:

The Channel X Volume Control - Integer register allows global control of the signal levels on all channels in 1 dB increments from +24 to -127 dB. Volume settings are decoded as shown in Table 6. The volume changes are implemented as specified by the Soft and Zero Cross bits (SZC[1:0]. All volume settings greater than 00011000b are equivalent to +24 dB. Binary values for integer volume settings less than 0 dB are in two's complement form.

CHXX_IVOL[7:0]	Hex Value	Volume Setting
0001 1000	18	+24 dB
0001 0111	17	+23 dB
0000 0001	01	+1 dB
0000 0000	00	0 dB
1111 1111	FF	-1 dB
1111 1110	FE	-2 dB
1000 0001	81	-127 dB

Table 8. Channel Integer Volume Settings

7.11 Channel XX Volume Control1 - Fraction (address 11h)

7	6	5	4	3	2	1	0
CHB2_FVOL1	CHB2_FVOL0	CHA2_FVOL1	CHA2_FVOL0	CHB1_FVOL1	CHB1_FVOL0	CHA1_FVOL1	CHA1_FVOL0

7.12 Channel XX Volume Control2 - Fraction (address 12h)

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	CHB3_FVOL1	CHB3_FVOL0	CHA3_FVOL1	CHA3_FVOL0

7.12.1 Channel Volume Control - Fraction (CHXX_FVOL[1:0])

Default = 00
00 - +0.00 dB
01 - +0.25 dB
10 - +0.50 dB
11 - +0.75 dB

Function:

The Channel X Volume Control - Fraction register is an additional offset to the value in the Channel Volume Control - Integer register and allows global control of the signal levels on all channels in 0.25 dB increments. Volume settings are decoded as shown in Table 7. These volume changes are implemented as specified by the Soft and Zero Cross bits (SZC[1:0]). All volume settings greater than 00011000b are equivalent to +24 dB. Binary values for integer and fractional volume settings less than 0 dB are in two's complement form.

See "Master Volume Control - Fraction (address 08h)" on page 57 for hints on converting decimal numbers to 2's complement binary values.

CHXX_IVOL[7:0]	CHXX_FVOL(1:0)	Volume Setting
0001 1000	00	+24.00 dB
0001 0111	10	+23.50 dB
0000 0001	11	+1.75 dB
0000 0001	00	+1.00 dB
0000 0000	01	+0.25 dB
0000 0000	00	0 dB
1111 1111	10	-0.50 dB
1111 1111	00	-1.00 dB
1111 1110	11	-1.25 dB
1111 1101	10	-2.50 dB
1000 0010	00	-126.00 dB
1000 0001	11	-126.25 dB
1000 0001	00	-127.00 dB

Table 9. Channel Fractional Volume Settings

7.13 Channel Mute (address 13h)

7	6	5	4	3	2	1	0
RESERVED	RESERVED	CHB3_MUTE	CHA3_MUTE	CHB2_MUTE	CHA2_MUTE	CHB1_MUTE	CHA1_MUTE

7.13.1 Independent Channel Mute (CHXX_MUTE)

Default = 0
0 - Disabled
1 - Enabled
Function:

The PWM outputs of the CS44600 will mute when enabled. The muting function is affected, similar to attenuation changes, by the Soft and Zero Cross bits (SZC[1:0]).

7.14 Channel Invert (address 14h)

7	6	5	4	3	2	1	0
RESERVED	RESERVED	CHB3_INV	CHA3_INV	CHB2_INV	CHA2_INV	CHB1_INV	CHA1_INV

7.14.1 Invert Signal Polarity (CHXX_INV)

Default = 0
0 - Disabled
1 - Enabled
Function:

When enabled, these bits will invert the signal polarity of their respective channels.

7.15 Peak Limiter Control Register (address 15h)

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	LIMIT_ALL	LIMIT_EN

7.15.1 Peak Signal Limit All Channels (LIMIT_ALL)

Default = 0
0 - individual channel
1 - all channels

Function:

When set to 0, the peak signal limiter will limit the maximum signal amplitude to prevent clipping on the specific channel indicating clipping. The other channels will not be affected.

When set to 1, the peak signal limiter will limit the maximum signal amplitude to prevent clipping on **ALL** channels in response to **ANY** single channel indicating clipping.

7.15.2 Peak Signal Limiter Enable (LIMIT_EN)

Default = 0
0 - Disabled
1 - Enabled

Function:

The CS44600 will limit the maximum signal amplitude to prevent clipping when this function is enabled. Peak Signal Limiting is performed by digital attenuation. The attack rate is determined by the Limiter Attack Rate register.

7.16 Limiter Attack Rate (address 16h)

7	6	5	4	3	2	1	0
ARATE7	ARATE6	ARATE5	ARATE4	ARATE3	ARATE2	ARATE1	ARATE0

7.16.1 Attack Rate (ARATE[7:0])

Default = 00010000

Function:

The limiter attack rate is user selectable. The effective rate is a function of the SRC output sampling frequency and the value in the Limiter Attack Rate register. Rates are calculated using the function RATE = (32/{value})/SRC Fs, where {value} is the decimal value in the Limiter Attack Rate register and SRC Fs is the output sample rate of the SRC which is determined by the PWM master clock frequency. SRC Fs equals 384 kHz for 24.576 MHz based clocks and 421.875 kHz for 27.000 MHz based clocks.

Note: A value of zero in this register is not recommended, as it will induce erratic behavior of the limiter. Use the LIM_EN bit to disable the limiter function (see Peak Limiter Control Register (address 15h)).

Binary Code	Decimal Value	Attack Rate - 384 kHz (µs per $^1/_8$ dB)	Attack Rate - 421.875 kHz (µs per $^1/_8$ dB)
00000001	1	83.33	75.852
00010100	20	4.167	3.793
00101000	40	2.083	1.896
00111100	60	1.389	1.264
01011010	90	0.926	0.843

Table 10. Limiter Attack Rate Settings

7.17 Limiter Release Rate (address 17h)

7	6	5	4	3	2	1	0
RRATE7	RRATE6	RRATE5	RRATE4	RRATE3	RRATE2	RRATE1	RRATE0

7.17.1 Release Rate (RRATE[7:0])

Default = 00100000

Function:

The limiter release rate is user selectable. The effective rate is a function of the SRC output sampling frequency and the value in the Release Rate register. Rates are calculated using the function RATE = (512/{value})/SRC Fs, where {value} is the decimal value in the Release Rate register and SRC Fs is the output sample rate of the SRC which is determined by the PWM master clock frequency. SRC Fs equals 384 kHz for 24.576 MHz based clocks and 421.875 kHz for 27.000 MHz based clocks.

Note: A value of zero in this register is not recommended, as it will induce erratic behavior of the limiter. Use the LIM_EN bit to disable the limiter function (see Peak Limiter Control Register (address 15h)).

Binary Code	Decimal Value	Release Rate - 384 kHz (µs per $^1/_8$ dB)	Release Rate - 421.875 kHz (µs per $^1/_8$ dB)
00000001	1	1333.333	1213.630
00010100	20	66.667	60.681
00101000	40	33.333	30.341
00111100	60	22.222	20.227
01011010	90	14.815	13.485

Table 11. Limiter Release Rate Settings

7.18 Chnl XX Load Compensation Filter - Coarse Adjust (addresses 18h, 1Ah, 1Ch, 1Eh, 20h, 22h)

7	6	5	4	3	2	1	0
RESERVED	RESERVED	CHXX_CORS5	CHXX_CORS4	CHXX_CORS3	CHXX_CORS2	CHXX_CORS1	CHXX_CORS0

7.18.1 Channel Compensation Filter - Coarse Adjust (CHXX_CORS[5:0])

Default = 000000
Function:

The Channel Load Compensation Filter Coarse Adjustment settings control the amount of attenuation of this single-pole filter and are used in conjunction with the Fine Adjustment bits to compensate for speaker impedance load variations. Each PWM channel is controlled by an associated register. The coarse adjustment bits will attenuate the audio response curve according to the table below in 0.1 dB increments. Filter setting values less than -4.0 dB will cause the PWM output to mute.

CHXX_CORS[5:0]	Coarse Filter Setting
000000	0 dB
000001	-0.1 dB
001010	-1.0 dB
011001	-2.5 dB
100000	-3.2 dB
101000	-4.0 dB

Table 12. Channel Load Compensation Filter Coarse Adjust

7.19 Chnl XX Load Compensation Filter - Fine Adjust (addresses 19h, 1Bh, 1Dh, 1Fh, 21h, 23h)

7	6	5	4	3	2	1	0
RESERVED	RESERVED	CHXX_FINE5	CHXX_FINE4	CHXX_FINE3	CHXX_FINE2	CHXX_FINE1	CHXX_FINE0

7.19.1 Channel Compensation Filter - Fine Adjust (CHXX_FINE[5:0])

Default = 000000
Function:

The Channel Load Compensation Filter Fine Adjustment settings control the amount of attenuation of this single-pole filter which follows the Coarse Adjustment Compensation Filter. These bits are used in conjunction with the Coarse Adjustment bits to fine tune the total frequency response of the system to compensate for speaker impedance load variations. Each PWM channel is controlled by an associated register. The fine adjustment bits will attenuate the audio response curve according to the table below in 0.1 dB increments. Filter setting values less than -4.0 dB will cause the PWM output to mute.

CHXX_FINE[5:0]	Fine Filter Setting
000000	0 dB
000001	-0.1 dB
001010	-1.0 dB
011001	-2.5 dB
100000	-3.2 dB
101000	-4.0 dB

Table 13. Channel Load Compensation Filter Fine Adjust

7.20 Interrupt Mode Control (address 28h)

7	6	5	4	3	2	1	0
INT1	INT0	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	OVFL_L/E

7.20.1 Interrupt Pin Control (INT1/INT0)

Default = 00
00 - Active high, high output indicates interrupt condition has occurred
01 - Active low, low output indicates an interrupt condition has occurred
10 - Open drain, active low. Requires an external pull-up resistor on the INT pin.
11 - Reserved
Function:

Determines how the interrupt pin (INT) will indicate an interrupt condition. If any of the mask bits in the Interrupt Mask Register are set to a 1b, read the Interrupt Status Register to determine which condition caused the interrupt.

7.20.2 Overflow Level/Edge Select (OVFL_L/E)

Default = 0
Function:

This bit defines the OVFL interrupt type (0 = level sensitive, 1 = edge trigger). The Over Flow status of all the audio channels when configured as “edge trigger” is cleared by reading the *Channel Over Flow Status (address 2Bh) (Read Only)*, and by reset. After a Reset this bit defaults to 0b, specifying “level sensitive”.

7.21 Interrupt Mask (address 29h)

7	6	5	4	3	2	1	0
M_SRC_UNLOCK	M_SRC_LOCK	M_RMPUP_DONE	M_RMPDN_DONE	M_MUTE_DONE	M_OVFL_INT	RESERVED	RESERVED

Default = 00000000
Function:

The bits of this register serve as a mask for the interrupt sources found in the Interrupt Status register. If a mask bit is set to 1b, the interrupt is unmasked, meaning that its occurrence will affect the INT pin and the Interrupt Status register. If a mask bit is set to 0b, the condition is masked, meaning that its occurrence will not affect the INT pin. The bit positions align with the corresponding bits in the Interrupt Status register. The mask bits for the GPIO_INT interrupt are located in the GPIO Interrupt Mask Register.

7.22 Interrupt Status (address 2Ah) (Read Only)

7	6	5	4	3	2	1	0
SRC_UNLOCK	SRC_LOCK	RMPUP_DONE	RMPDN_DONE	MUTE_DONE	OVFL_INT	GPIO_INT	RESERVED

For all bits in this register, a ‘1’ means the associated interrupt condition has occurred at least once since the register was last read. A ‘0’ means the associated interrupt condition has NOT occurred since the last reading of the register. Reading the register resets the SRC_UNLOCK, SRC_LOCK, RMPUP_DONE, RMPDN_DONE and MUTE_DONE bits to 0. These bits are considered “edge-trigger” interrupts.

The OVFL_INT and GPIO_INT bits will not reset to 0 by reading this register. The OVFL_INT bit will be set to 0 by a read to the “Channel Over Flow Status (address 2Bh) (Read Only)” on page 66 only when the interrupt type is set to “edge-trigger”. The GPIO_INT bit will be set to 0 by a read to the “GPIO Status Register (address 2Fh)” on page 67 only when the interrupt type is set to “edge trigger”. If either of these interrupt types are configured as “level sensitive”, then reading the appropriate status register will not clear the corresponding status bit in this register. OVFL_INT or GPIO_INT will remain set as long as the logic active level is present. Once the level is cleared, then a read to the proper status register will clear the status bit.

7.22.1 SRC Unlock Interrupt (SRC_UNLOCK)

Default = 0
Function:

When high, indicates that the DAI interface has detected an error condition and/or the SRC has lost lock. Conditions which cause the SRC to loose lock, such as loss of DAI_LRCK, DAI_MCLK or a DAI_LRCK/DAI_MCLK ratio change, will cause an interrupt condition. This interrupt is an edge-triggered event.

If this bit is set to a 1b, indicating an unlock condition, and an SRC_LOCK interrupt is detected, then this bit will be reset to 0b before a read of the Interrupt Status Register. Only the last valid state of the SRC will be reported.

7.22.2 SRC Lock Interrupt (SRC_LOCK)

Default = 0
Function:

When high, indicates that on all active channels, the sample rate converters have achieved lock. This interrupt is an edge-triggered event.

If this bit is set to a 1b, indicating a lock condition, and an SRC_UNLOCK condition is detected, then this bit will be reset to 0b before a read of the Interrupt Status Register. Only the last valid state of the SRC will be reported.

7.22.3 Ramp-Up Complete Interrupt (RMPUP_DONE)

Default = 0
Function:

When high, indicates that all active channels have completed the configured ramp-up interval.

7.22.4 Ramp-Down Complete Interrupt (RMPDN_DONE)

Default = 0
Function:

When high, indicates that all active channels have completed the configured ramp-down interval.

7.22.5 Mute Complete Interrupt (Mute_DONE)

Default = 0
Function:

When high, indicates that all muted channels have completed the mute cycle-down interval as defined by the SZC[1:0] bits in the “Volume Control Configuration (address 06h)” on page 55.

7.22.6 Channel Over Flow Interrupt (OVFL_INT)

Default = 0
Function:

When high, indicates that the magnitude of an output sample on one of the channels has exceeded full scale and has been clipped to positive or negative full scale as appropriate. This bit is the logical OR of all the bits in the Channel Over Flow Status Register. Read the Channel Over Flow Status Register to determine which channel(s) had the overflow condition.

7.22.7 GPIO Interrupt Condition (GPIO_INT)

Default = 0
Function:

When high, indicates that a transition as configured on one of the un-masked GPIO pins has occurred. This bit is the logical OR of all the supported un-masked bits in the GPIO Status Register. Read the GPIO Status Register to determine which GPIO input(s) caused the interrupt condition. The GPIO interrupt is not removed by reading this register. The GPIO Status Register must be read to clear this interrupt. If the GPIO input is configured as “edge trigger” the interrupt will clear. If the GPIO input is configured as “level sensitive”, the interrupt condition will remain as long as the GPIO input remains at the active level.

7.23 Channel Over Flow Status (address 2Bh) (Read Only)

7	6	5	4	3	2	1	0
RESERVED	RESERVED	CHB3_OVFL	CHA3_OVFL	CHB2_OVFL	CHA2_OVFL	CHB1_OVFL	CHA1_OVFL

For all bits in this register, a '1' means the associated condition has occurred at least once since the register was last read. A '0' means the associated condition has NOT occurred since the last reading of the register. Reading the register resets all bits to 0 if the Overflow Level/Edge interrupt type is set to "edge trigger". These channel overflow status bits are not effected by the interrupt mask bit, M_OVFL_INT. The overflow condition of each channel can be polled instead of generating an interrupt as required.

7.23.1 ChXX_OVFL

Default = 0
Function:

When high, indicates that the magnitude of the current output sample on the associated channel has exceeded full scale and has been clipped to positive or negative full scale as appropriate.

7.24 GPIO Pin In/Out (address 2Ch)

7	6	5	4	3	2	1	0
RESERVED	GPIO6_I/O	GPIO5_I/O	GPIO4_I/O	GPIO3_I/O	GPIO2_I/O	GPIO1_I/O	GPIO0_I/O

7.24.1 GPIO In/Out Selection (GPIOX_I/O)

Default = 0
0 - General Purpose Input
1 - General Purpose Output
Function:

General Purpose Input - The pin is configured as an input.

General Purpose Output - The pin is configured as a general purpose output.

7.25 GPIO Pin Polarity/Type (address 2Dh)

7	6	5	4	3	2	1	0
RESERVED	GPIO6_P/T	GPIO5_P/T	GPIO4_P/T	GPIO3_P/T	GPIO2_P/T	GPIO1_P/T	GPIO0_P/T

7.25.1 GPIO Polarity/Type Selection (GPIOX_P/T)

Default = 1
Function:

General Purpose Input - If the pin is configured as an input, this bit defines the input polarity (0 = Active Low, 1 = Active High).

General Purpose Output - If the pin is configured as a general purpose output, this bit defines the GPIO output type (0 = CMOS, 1 = OPEN-DRAIN).

7.26 GPIO Pin Level/Edge Trigger (address 2Eh)

7	6	5	4	3	2	1	0
RESERVED	GPIO6_L/E	GPIO5_L/E	GPIO4_L/E	GPIO3_L/E	GPIO2_L/E	GPIO1_L/E	GPIO0_L/E

7.26.1 GPIO Level/Edge Input Sensitive (GPIOX_L/E)

Default = 0
Function:

General Purpose Input - This bit defines the GPIO input type (0 = level sensitive, 1 = edge trigger) when a GPIO pin is configured as an input. The GPIO pin status of an input configured as “edge trigger” is cleared by reading the GPIO Status Register when not enabled to generate an interrupt (MASK bit equals 0b) and by reset. After a reset this bit defaults to 0b, specifying “level sensitive”.

General Purpose Output - Not Used.

7.27 GPIO Status Register (address 2Fh)

7	6	5	4	3	2	1	0
RESERVED	GPIO6_STATUS	GPIO5_STATUS	GPIO4_STATUS	GPIO3_STATUS	GPIO2_STATUS	GPIO1_STATUS	GPIO0_STATUS

7.27.1 GPIO Pin Status (GPIOX_STATUS)

Default = x
Function:

General Purpose Input - Bits in this register are read only when the corresponding GPIO pin is configured as an input. Each bit indicates the status of the GPIO pin. The corresponding bit of a GPIO input configured as “edge trigger” is cleared by reading the GPIO Status Register. GPIO inputs configured as “level sensitive” will not be automatically cleared, but will reflect the logic state on the GPIO input. The mask bits in the GPIO Interrupt Mask Register have no effect on the operation of these status bits.

When a GPIO is un-masked and enabled to generate an interrupt, and is configured as “edge trigger”, a read operation to this register will clear the status bit and remove the interrupt condition. A read operation to the *Interrupt Status (address 2Ah) (read only)* when a GPIO is configured to generate an interrupt condition will not clear any bits in this register.

General Purpose Output - For GPIO pins configured as outputs, these bits are used to control the output signal level. A 1b written to a particular bit will cause the corresponding GPIO pin to be driven to a logic high. A 0b will cause a logic low.

7.28 GPIO Interrupt Mask Register (address 30h)

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	M_GPIO3	M_GPIO2	M_GPIO1	M_GPIO0

7.28.1 GPIO Pin Interrupt Mask (M_GPIOX)

Default = 0
Function:

General Purpose Input - The bits of this register serve as a mask for GPIO[3:0] interrupt sources. If a mask bit is set to 1, the interrupt is unmasked, meaning that its occurrence will affect the INT pin and the Interrupt Status register. If a mask bit is set to 0, the condition is masked, meaning that its occurrence will not affect the INT pin or Interrupt Status Register. The proper pin status will be reported in the GPIO Status Register. The bit positions align with the corresponding bits in the GPIO Status register.

General Purpose Output - This register is not used.

7.29 PWM Configuration Register (address 31h)

7	6	5	4	3	2	1	0
OSRATE	RESERVED	RESERVED	A1/B1_OUT_CNFG	A2/B2_OUT_CNFG	A3_OUT_CNFG	B3_OUT_CNFG	RESERVED

7.29.1 Over Sample Rate Selection (OSRATE)

Default = 0
0 - modulated PWM output pulses run at single-mode switch rate. Typically 384 kHz or 421.875 kHz.
1 - modulated PWM output pulses run at double-mode switch rate. Typically 768 kHz or 843.75 kHz.
Function:

Enables the interpolation filter in the modulator to over-sample the incoming audio to support a double-speed PWM switch rate. This parameter can only be changed when all modulators and associated logic are in the power-down state by setting the PDN bit in the register "Clock Configuration and Power Control (address 02h)" on page 51 to a 1b. Attempts to write this register while the PDN is not set will be ignored.

7.29.2 Channels A1 and B1 Output Configuration (A1/B1_OUT_CNFG)

Default = 0
0 - pwm outputs for both channels A1 and B1 are configured for half-bridge operation
1 - pwm outputs for both channels A1 and B1 are configured for full-bridge operation
Function:

Identifies the output configuration. The value selected for this bit is applicable to the outputs for channels A1 and B1. This parameter can only be changed when all modulators and associated logic are in the power-down state by setting the PDN bit in the register "Clock Configuration and Power Control (address 02h)" on page 51 to a 1b. Attempts to write this register while the PDN is not set will be ignored.

7.29.3 Channels A2 and B2 Output Configuration (A2/B2_OUT_CNFG)

Default = 0
0 - pwm outputs for both channels A2 and B2 are configured for half-bridge operation
1 - pwm outputs for both channels A2 and B2 are configured for full-bridge operation
Function:

Identifies the output configuration. The value selected for this bit is applicable to the outputs for channels A2 and B2. This parameter can only be changed when all modulators and associated logic are in the pow-

er-down state by setting the PDN bit in the register "Clock Configuration and Power Control (address 02h)" on page 51 to a 1b. Attempts to write this register while the PDN is not set will be ignored.

7.29.4 Channel A3 Output Configuration (A3_OUT_CNFG)

Default = 0
0 - pwm outputs for channel A3 are configured for half-bridge operation
1 - pwm outputs for channel A3 are configured for full-bridge operation
Function:

Identifies the output configuration. The value selected for this bit is applicable to the outputs for only channel A3. This parameter can only be changed when all modulators and associated logic are in the power down state by setting the PDN bit in the register "Clock Configuration and Power Control (address 02h)" on page 51 to a '1'b. Attempts to write this register while the PDN is not set will be ignored.

7.29.5 Channel B3 Output Configuration (B3_OUT_CNFG)

Default = 0
0 - pwm outputs for channel B3 are configured for half-bridge operation
1 - pwm outputs for channel B3 are configured for full-bridge operation
Function:

Identifies the output configuration. The value selected for this bit is applicable to the outputs for only channel B3. This parameter can only be changed when all modulators and associated logic are in the power-down state by setting the PDN bit in the register "Clock Configuration and Power Control (address 02h)" on page 51 to a 1b. Attempts to write this register while the PDN is not set will be ignored.

7.30 PWM Minimum Pulse Width Register (address 32h)

7	6	5	4	3	2	1	0
DISABLE_PWMOUTXX-	RESERVED	RESERVED	MIN_PULSE4	MIN_PULSE3	MIN_PULSE2	MIN_PULSE1	MIN_PULSE0

7.30.1 Disable PWMOUTXX - Signal (DISABLE_PWMOUTXX-)

Default = 0
0 - PWM minus ("-") differential signal is operational when PWM channel is configured for half-bridge.
1 - PWM minus ("-") differential signal is disabled when PWM channel is configured for half-bridge.
Function:

Determines if the PWM minus ("-") differential signal is disabled when the particular PWM channel is configured for half-bridge operation. This bit is ignored for channels configured for full-bridge operation. The value selected for this bit is applicable to the outputs for all channels configured for half-bridge operation. This parameter can only be changed when all modulators and associated logic are in the power-down state by setting the PDN bit in the register "Clock Configuration and Power Control (address 02h)" on page 51 to a 1b. Attempts to write this register while the PDN is not set will be ignored.

7.30.2 Minimum PWM Output Pulse Settings (MIN_PULSE[4:0])

Default = 00000
Function:

The PWM Minimum Pulse registers allow settings for the minimum allowable pulse width on each of the PWMOUT differential signal pairs, PWMOUTxx+ and PWMOUTxx-. The value selected in this register is applicable to all PWM channels. The effective minimum pulse is calculated by multiplying the register value by the period of the PWM_MCLK. This parameter can only be changed when all modulators and associated logic are in the power-down state by setting the PDN bit in the register "Clock Configuration and

Power Control (address 02h)" on page 51 to a 1b. Attempts to write this register while the PDN is not set will be ignored.

Binary Code MIN_PULSE[4:0]	Minimum Pulse Setting (multiply by PWM_MCLK period)
00000	0 - no minimum
00110	6
10100	20
11111	31

Table 14. PWM Minimum Pulse Width Settings

7.31 PWMOUT Delay Register (address 33h)

7	6	5	4	3	2	1	0
DIFF_DLY2	DIFF_DLY1	DIFF_DLY0	CHNL_DLY4	CHNL_DLY3	CHNL_DLY2	CHNL_DLY1	CHNL_DLY0

7.31.1 Differential Signal Delay (DIFF_DLY[2:0])

Default = 000
Function:

The Differential Signal Delay bits allow delay adjustment between each channel's differential signals, PWMOUTxx+ and PWMOUTxx-. This set of bits control the delay between PWMOUTxx+ and PWMOUTxx- across all active channels. The value of this register determines the amount of delay inserted in the output path. The effective delay is calculated by multiplying the register value by the period of the PWM_MCLK. This parameter can only be changed when all modulators and associated logic are in the power-down state by setting the PDN bit in the register "Clock Configuration and Power Control (address 02h)" on page 51 to a 1b. Attempts to write this register while the PDN is not set will be ignored.

Binary Code	Delay Setting (multiply by PWM_MCLK period)
000	0 - no delay
001	1
100	4
111	7

Table 15. Differential Signal Delay Settings

7.31.2 Channel Delay Settings (CHNL_DLY[4:0])

Default = 00000
Function:

The Channel Delay bits allow delay adjustment of each of the PWMOUT differential signal pairs, PWMOUTAx+/PWMOUTAx- from the associated PWMOUTBx+/PWMOUTBx-. The value of this register determines the amount of delay inserted in the output path. The effective delay is calculated by multiplying the register value by the period of the PWM_MCLK. This parameter can only be changed when all modulators and associated logic are in the power-down state by setting the PDN bit in the register "Clock Configuration and Power Control (address 02h)" on page 51 to a 1b. Attempts to write this register while the PDN is not set will be ignored.

Binary Code	Delay Setting(multiply by PWM_MCLK period)
00000	0 - no delay
00110	6
11000	24
11111	31

Table 16. Channel Delay Settings

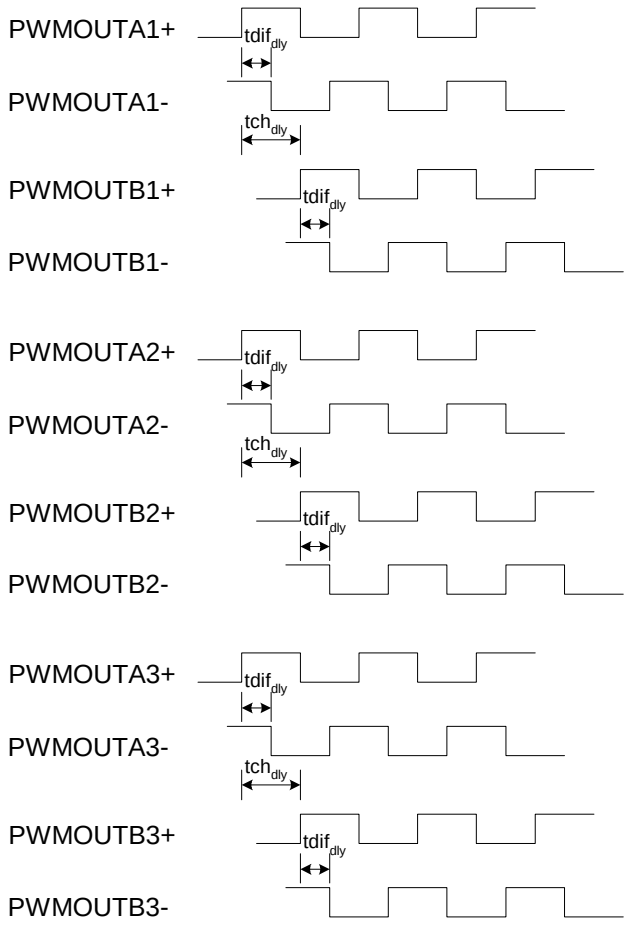


Figure 31. PWM Output Delay

7.32 PSR and Power Supply Configuration (address 34h)

7	6	5	4	3	2	1	0
PSR_EN	PSR_RESET	FEEDBACK_EN	RESERVED	RESERVED	PS_SYNC_DIV2	PS_SYNC_DIV1	PS_SYNC_DIV0

7.32.1 Power Supply Rejection Enable (PSR_EN)

Default = 0
0 - disable
1 - enable
Function:

Enables the on-card and internal power supply rejection circuitry. This bit will cause the PSR_EN output signal to change logic level. A ‘0’b in this bit will cause the PSR_EN to drive a logic low. A ‘1’b will drive a logic high.

7.32.2 Power Supply Rejection Reset (PSR_RESET)

Default = 0
0 - force reset condition
1 - remove reset condition
Function:

This bit is used to assert a reset condition to the on-card PSR components. When set to a '0'b, the PSR_RESET signal will be asserted low. The reset condition will continue as long as this bit is set to a '0'b. This bit must be set to a '1'b for proper PSR operation.

7.32.3 Power Supply Rejection Feedback Enable (FEEDBACK_EN)

Default = 0
0 - disable
1 - enable
Function:

Enables the internal power supply rejection feedback logic.

7.32.4 Power Supply Sync Clock Divider Settings (PS_SYNC_DIV[2:0])

Default = 000
Function:

These three bits determine the divider for the XTAL clock signal for generating the PS_SYNC clock signal.

PS_SYNC_DIV[2:0]	PS_SYNC Clock Divider
000	Output Disabled
001	Divide by 32
010	Divide by 64
011	Divide by 128
100	Divide by 256
101	Divide by 512
110	Divide by 1024

Table 17. Power Supply Sync Clock Divider Settings

7.33 Decimator Shift/Scale (addresses 35h, 36h, 37h)

7	6	5	4	3	2	1	0
RESERVED	DEC_SHIFT2	DEC_SHIFT1	DEC_SHIFT0	RESERVED	DEC_SCALE18	DEC_SCALE17	DEC_SCALE16
7	6	5	4	3	2	1	0
DEC_SCALE15	DEC_SCALE14	DEC_SCALE13	DEC_SCALE12	DEC_SCALE11	DEC_SCALE10	DEC_SCALE09	DEC_SCALE08
7	6	5	4	3	2	1	0
DEC_SCALE07	DEC_SCALE06	DEC_SCALE05	DEC_SCALE04	DEC_SCALE03	DEC_SCALE02	DEC_SCALE01	DEC_SCALE00

7.33.1 Decimator Shift (DEC_SHIFT[2:0])

Default = 010
Function:

These bits are used to scale the power supply reading (Decimator Outd (addresses 3Bh, 3Ch, 3Dh)) during the PSR feedback calibration sequence. The combination of shift and scale factors (DEC_SCALE[18:0]*2^(DEC_SHIFT[2:0])) can be viewed as a floating point coefficient. The floating point coefficient will be determined during the PSR feedback calibration sequence. See Decimator Scale (DEC_SCALE[18:0]) register description and "Recommended PSR Calibration Sequence" on page 44.

7.33.2 Decimator Scale (DEC_SCALE[18:0])

Default = 25868h
Function:

These bits are used to scale the power supply reading (Decimator Outd (addresses 3Bh, 3Ch, 3Dh)) during the PSR feedback calibration sequence. DEC_SCALE[18:0] has 19-bit precision, formatted as signed 1.18 with decimal values from -1 to 1-2^(-18). The combination of shift and scale factors (DEC_SCALE[18:0]*2^(DEC_SHIFT[2:0])) can be viewed as a floating point coefficient. The floating point coefficient will be determined during the PSR feedback calibration sequence. See Decimator Shift (DEC_SHIFT[2:0]) register description and "Recommended PSR Calibration Sequence" on page 44.

DEC_SCALE[18:0]	DEC_SHIFT[2:0]	Calculated Coefficient (C_{PSR})
20000h=0.5	001b=1	0.5*2^(1)=1
28851h=0.6331	010b=2	0.6331*2^(2)=2.5325

Table 18. Decimator Shift/Scale Coefficient Calculation Examples

7.34 Decimator Outd (addresses 3Bh, 3Ch, 3Dh)

7	6	5	4	3	2	1	0
DEC_OUTD23	DEC_OUTD22	DEC_OUTD21	DEC_OUTD20	DEC_OUTD19	DEC_OUTD18	DEC_OUTD17	DEC_OUTD16
7	6	5	4	3	2	1	0
DEC_OUTD15	DEC_OUTD14	DEC_OUTD13	DEC_OUTD12	DEC_OUTD11	DEC_OUTD10	DEC_OUTD09	DEC_OUTD08
7	6	5	4	3	2	1	0
DEC_OUTD07	DEC_OUTD06	DEC_OUTD05	DEC_OUTD04	DEC_OUTD03	DEC_OUTD02	DEC_OUTD01	DEC_OUTD00

7.34.1 Decimator Outd (DEC_OUTD[23:0])

Default = 000000h (Read Only)
Function:

These bits reflect the real-time power supply value as measured by the external PSR feedback circuit. DEC_OUTD[23:0] has 24-bit precision, formatted as signed 2.22 with decimal values from -4 to 4-2^(-22). Calibration needs to be done to correlate the value of DEC_OUTD[23:0] with the real power supply value. A quiet DC power supply without any ripple is treated as 1.0 with DEC_OUTD[23:0] calibrated at 400000h. See "Recommended PSR Calibration Sequence" on page 44.

8. PARAMETER DEFINITIONS

Dynamic Range (DR)

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth, typically 20 Hz to 20 kHz. Dynamic Range is a signal-to-noise ratio measurement over the specified band width made with a -60 dBFS signal. 60 dB is then added to the resulting measurement to refer the measurement to full-scale, with units in dB FS A. This technique ensures that the distortion components are below the noise level and do not effect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307.

Frequency Response (FR)

FR is the deviation in signal level verses frequency. The 0 dB reference point is 1 kHz. The amplitude corner, Ac, lists the maximum deviation in amplitude above and below the 1 kHz reference point. The listed minimum and maximum frequencies are guaranteed to be within the Ac from minimum frequency to maximum frequency inclusive.

Interchannel Isolation

A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with no signal to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch

The gain difference between left and right channels. Units in decibels.

Gain Error

The deviation from the nominal full-scale analog output for a full-scale digital input.

Gain Drift

The change in gain value with temperature. Units in ppm/°C.

Offset Error

The deviation of the mid-scale transition (111...111 to 000...000) from the ideal. Units in mV.

dB FS A

dB FS is defined as dB relative to full-scale. The “A” indicates an A weighting filter was used.

Differential Nonlinearity

The worst case deviation from the ideal code width. Units in LSB.

FFT

Fast Fourier Transform.

Fs

Sampling Frequency.

Resolution

The number of bits in the output words to the DACs, and in the input words to the ADCs.

Signal to Noise Ratio (SNR)

SNR, similar to DR, is the ratio of an arbitrary sinusoidal input signal to the RMS sum of the noise floor, in the presence of a signal. It is measured over a 20 Hz to 20 kHz bandwidth with units in dB.

SRC

Sample Rate Converter. Converts data derived at one sample rate to a differing sample rate. The CS44600 operates at a fixed sample frequency. The internal sample rate converter is used to convert digital audio streams playing back at other frequencies to the PWM output rate.

Total Harmonic Distortion + Noise (THD+N)

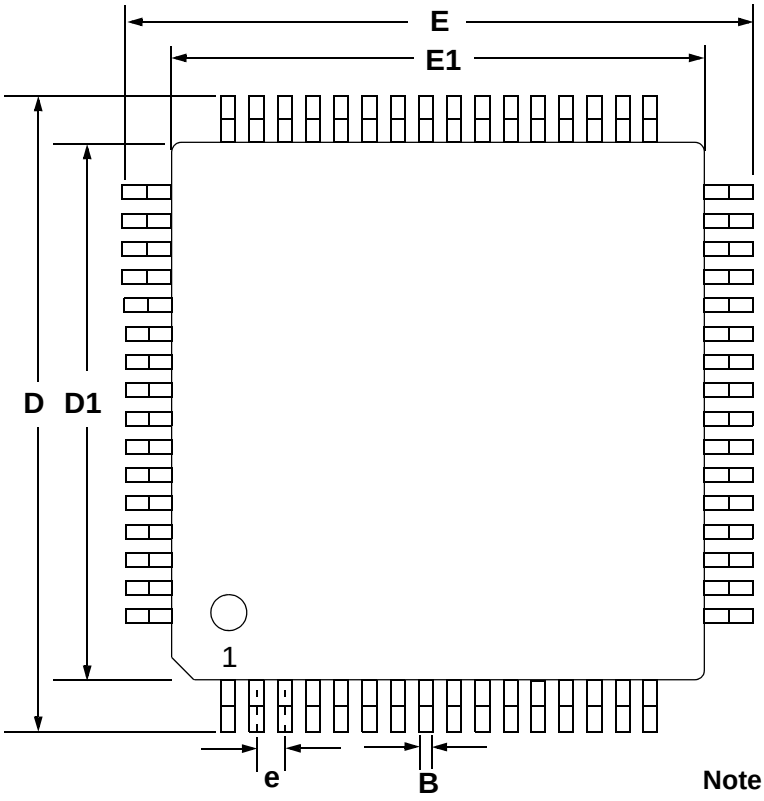
The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified band width (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels. Measured at -1 and -20 dBFS as suggested in AES17-1991 Annex A.

9. REFERENCES

1. Cirrus Logic, "*Audio Quality Measurement Specification*," Version 1.0, 1997. http://www.cirrus.com/products/papers/meas/meas.html
2. Cirrus Logic, "*AN18: Layout and Design Rules for Data Converters and Other Mixed Signal Devices*," Version 6.0, February 1998.
3. Cirrus Logic, "*AN22: Overview of Digital Audio Interface Data Structures*, *Version 2.0*", February 1998.; A useful tutorial on digital audio specifications.
4. Philips Semiconductor, "*The I²C-Bus Specification: Version 2*," Dec. 1998. http://www.semiconductors.philips.com

10.PACKAGE DIMENSIONS

64L LQFP PACKAGE DRAWING



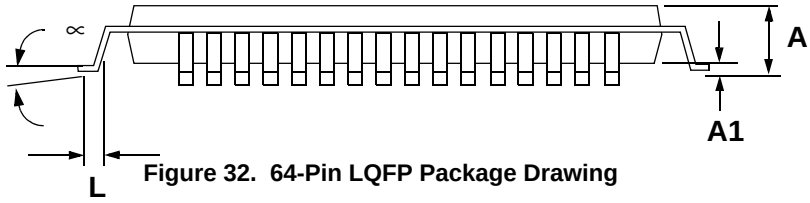


Figure 32. 64-Pin LQFP Package Drawing

	INCHES			MILLIMETERS		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	---	0.55	0.063	---	1.40	1.60
A1	0.002	0.004	0.006	0.05	0.10	0.15
B	0.007	0.008	0.011	0.17	0.20	0.27
D	0.461	0.472 BSC	0.484	11.70	12.0 BSC	12.30
D1	0.390	0.393 BSC	0.398	9.90	10.0 BSC	10.10
E	0.461	0.472 BSC	0.484	11.70	12.0 BSC	12.30
E1	0.390	0.393 BSC	0.398	9.90	10.0 BSC	10.10
e*	0.016	0.020 BSC	0.024	0.40	0.50 BSC	0.60
L	0.018	0.024	0.030	0.45	0.60	0.75
∝	0.000°	4°	7.000°	0.00°	4°	7.00°

* Nominal pin pitch is 0.50 mmControlling dimension is mm.
JEDEC Designation: MS022

11.THERMAL CHARACTERISTICS

Parameter		Symbol	Min	Typ	Max	Units
Junction to Ambient Thermal Impedance	2 Layer Board	θ_{JA}	-	48	-	°C/Watt
	4 Layer Board		-	38	-	

12.REVISION HISTORY

Release	Date	Changes
A1	May 2004	1st Advance Release
A2	September 2004	Updated lead-free device ordering information
A3	October 2004	-Updated “Features” on page 1 -Updated “External Crystal operating frequency” on page 11 -Updated “Typical Full-Bridge Connection Diagram” on page 22 -Updated “Typical Half-Bridge Connection Diagram” on page 23 -Updated Section 4.2 "Feature Set Summary" on page 22 -Updated “FsOut Domain Clocking” on page 24 -Updated “Sample Rate Converter” on page 31 -Updated “PWM Engines” on page 32 -Updated Table 4, “Typical PWM Switch Rate Settings,” on page 33 -Updated Section 4.5.8 "Modulator" on page 33 -Updated Section 4.5.10 on page 34 -Updated Section 4.6.1 "SPI Mode" on page 35 -Updated Section 4.6.2 "I²C Mode" on page 36 -Updated Section 5. "Power Supply, Grounding, and PCB layout" on page 38 -Updated Section 5.1 "Reset and Power-Up" on page 41 -Updated Section 5.1.1 "PWM PopGuard® Transient Control" on page 41 -Updated Section 5.1.2 "Recommended Power-Up Sequence" on page 41 -Updated Section 5.1.3 "Recommended PSR Calibration Sequence" on page 42 -Updated Section 5.1.4 "Recommended Power-Down Sequence" on page 43 -Updated Section 6. "Register Quick Reference" on page 44 -Updated Section 7.5.2 "AM Frequency Hopping (AM_FREQ_HOP)" on page 51 -Updated Section 7.6 "Ramp Configuration (address 05h)" on page 52 -Updated Section 7.7.3 on page 53 -Corrected Table 7, “Master Fractional Volume Settings,” on page 56 -Corrected Table 9, “Channel Fractional Volume Settings,” on page 58 -Corrected Table 11, “Limiter Release Rate Settings,” on page 60 -Updated Table 7.18, “Chnl XX Load Compensation Filter - Coarse Adjust (addresses 18h, 1Ah, 1Ch, 1Eh, 20h, 22h),” on page 60 -Updated Table 7.19, “Chnl XX Load Compensation Filter - Fine Adjust (addresses 19h, 1Bh, 1Dh, 1Fh, 21h, 23h),” on page 61 -Updated Section 7.26 "GPIO Pin Level/Edge Trigger (address 2Eh)" on page 65 -Updated Section 7.29 "PWM Configuration Register (address 31h)" on page 66
PP1	May 2005	-Updated “Features” on page 1 -Updated “Ordering Information” on page 2 -Correcte “Power Supply Current” on page 9 -Corrected “High-Level Input Voltage” on page 9 -Corrected “Low-Level Input Voltage” on page 9 -Corrected “High-Level Output Voltage at Io = -2 mA” on page 9 -Corrected “Low-Level Output Voltage at Io = 2 mA” on page 9 -Corrected “Digital Filter Response (Note 12)” on page 11 -Updated “Typical Full-Bridge Connection Diagram” on page 22 -Updated “Typical Half-Bridge Connection Diagram” on page 23 -Corrected Figure 13 on page 23 -Updated Section 7.5.2 "AM Frequency Hopping (AM_FREQ_HOP)" on page 51

Table 19. Revision History

Contacting Cirrus Logic Support
For all product questions and inquiries contact a Cirrus Logic Sales Representative.
To find the one nearest to you go to **www.cirrus.com**