Preliminary Data Sheet

D6005B

Digital Speech/ Signal Processor for an All Digital Answering Machine

GENERAL DESCRIPTION

The D6005B chipset is a digital speech/signal processing subsystem that implements all the functions of speech compression, telephone line signal processing and memory management, for an all digital telephone answering machine. The D6005B is fully controlled by the system host through a simple interface protocol. The host processor provides activation and control of all chipset functions such as speech recording and playback, DTMF generation and line monitoring.

The fully digital solution uses no moving parts, yielding high reliability. The flexibility of a programmable system enables a range of answering device features for the end user. The D6005B includes a digital signal processor, analog I/O interface chip, ARAM memory, and an ASIC.

FEATURES

- **High quality, low rate digital speech compression**
- **Flexible storage of ICM/OGM**
- **Voice activated recording**
- **DTMF receive/transmit**
- **Near-end echo cancellation improves DTMF detection**
- **Highly reliable—no moving parts**
- **Minimal chip count**
- **Programmable, modular design**
- **8-bit HOST interface**
- **Speed dial**
- **Telephone number storage**

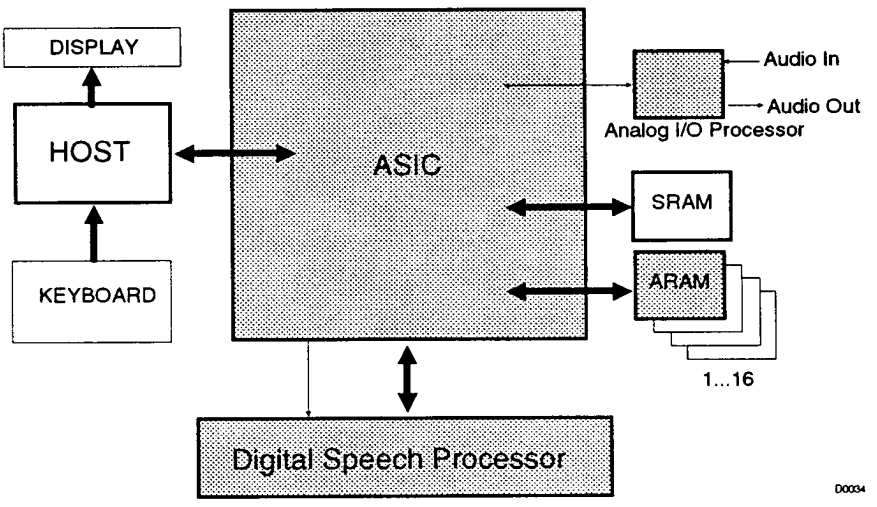


Figure 1. D6005B Block Diagram

All specifications are subject to change without prior notice

DSP GROUP, INC., 4050 MOORPARK AVE., SAN JOSE, CA 95117
PH: 408-985-0722 FAX: 408-985-2108

CHIPSET CONFIGURATION

- D6005B-11A Digital Speech Processor (64-pin PQFP)—1 each
- D6005A-71B ASIC (80-pin PQFP)—1 each
- D0000-26 or D0000-29 Analog I/O Interface (16-pin DIP)—1 each
- D0000-31A 1Mbit ARAM Message Memory (18-pin DIP or SOJ)—1 to 16 each
  or
  D0000-34A 4Mbit ARAM Message Memory (SOJ)—1 to 4 each

Note: An 8K × 8 static RAM chip will be supplied by the customer.

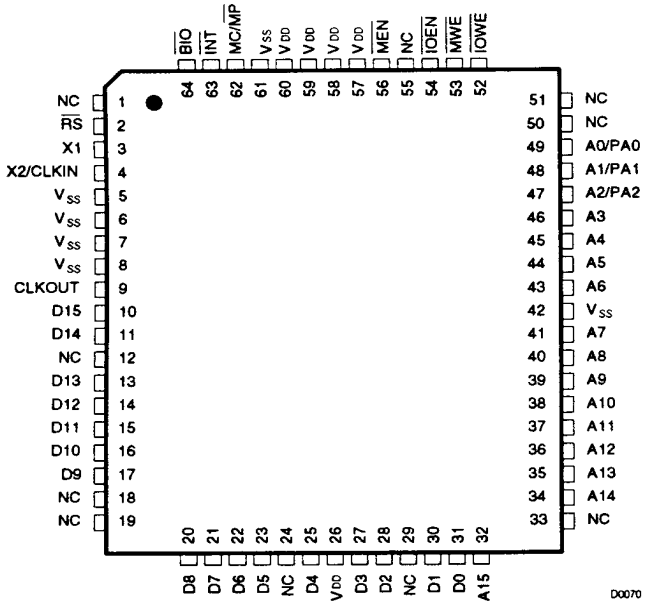


Figure 2. D6005B-11A

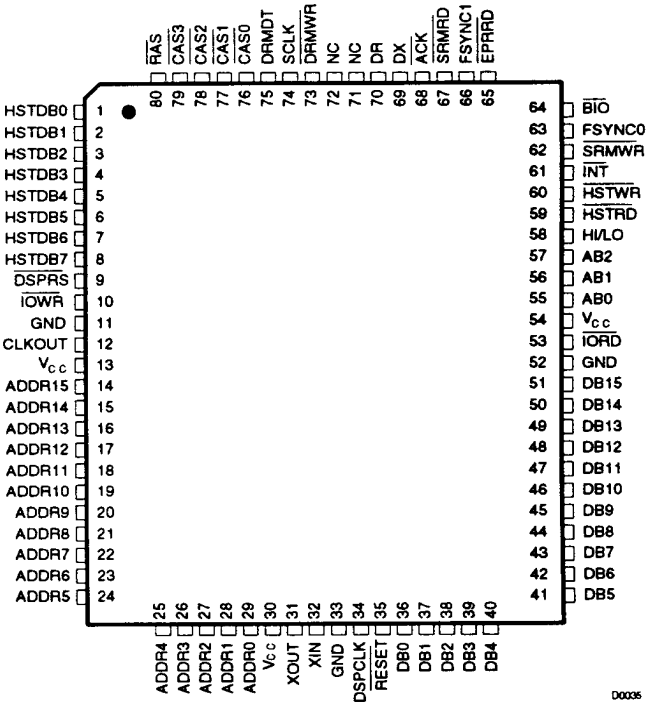


Figure 3. D6005A-71B

DSP GROUP, INC., 4050 MOORPARK AVE., SAN JOSE, CA 95117
PH: 408-985-0722 FAX: 408-985-2108

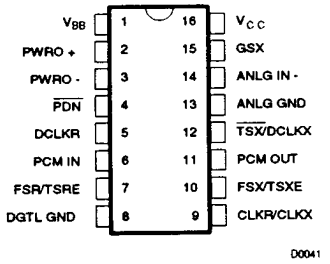


Figure 4. D0000-26 DIP

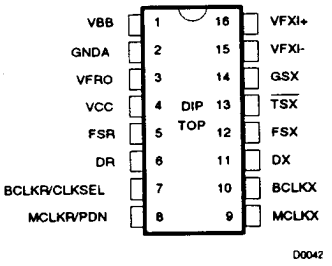


Figure 5. D0000-29 DIP

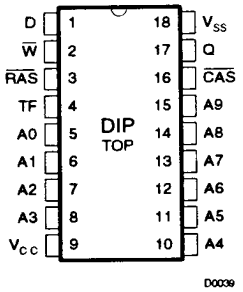


Figure 6. D0000-31A DIP

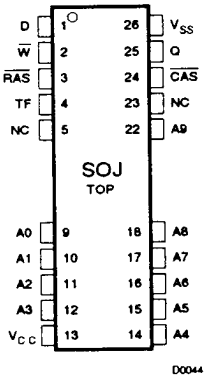


Figure 7. D0000-31A SOJ

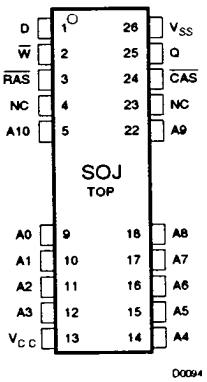


Figure 8. D0000-34A (SOJ)

PIN DESCRIPTIONS

D6005B-11A (DSP)			
ADDRESS/DATA BUSES			
Pin		**I/O/Z***	**Description**
Name	**No.**		
A15 MSB	32	O	Program memory address bus A15 (MSB) through A0 (LSB) and port addresses PA2 (MSB) through PA0 (LSB). Addresses A15 through A0 are always active and never go to high impedance. During execution of the IN and OUT instructions, pins A2 through A0 carry the port addresses. (Address pins A15 through A3 are always driven low on IN and OUT instruction).
A14	34		
A13	35		
A12	36		
A11	37		
A10	38		
A9	39		
A8	40		
A7	41		
A6	43		
A5	44		
A4	45		
A3	46		
A2/PA2	47		
A1/PA1	48		
A0/PA0	49		
D15 MSB	10	I/O/Z	Parallel data bus D15 (MSB) through D0 (LSB). The data bus is always in the high-impedance state except when $\overline{\text{IOWE}}$ or $\overline{\text{MWE}}$ are active (low).
D14	11		
D13	13		
D12	14		
D11	15		
D10	16		
D9	17		
D8	20		
D7	21		
D6	22		
D5	23		
D4	25		
D3	27		
D2	28		
D1	30		
D0 LSB	31		

*Input/Output/High-Impedance state.

DSP GROUP, INC., 4050 MOORPARK AVE., SAN JOSE, CA 95117
PH: 408-985-0722 FAX: 408-985-2108

PIN DESCRIPTIONS (CONTINUED)

D6005B-11A (DSP)			
INTERRUPT AND MISCELLANEOUS SIGNALS			
Pin		**I/O/Z***	**Description**
Name	**No.**		
$\overline{BIO}$	64	I	External polling input.
$\overline{IOEN}$	54	O	Data enable for device input data. When active (low), $\overline{IOEN}$ indicates that the device will accept data from the data bus. When $\overline{IOEN}$ is active, $\overline{MEN}$, $\overline{IOWE}$, and $\overline{MWE}$ will always be inactive (high).
$\overline{IOWE}$	52	O	Write enable for device output data. When active (low), $\overline{IOWE}$ indicates that data will be output from the device on the data bus. When $\overline{IOWE}$ is active, $\overline{MEN}$, $\overline{IOEN}$, and $\overline{MWE}$ will always be inactive (high).
$\overline{INT}$	63	I	External interrupt input. The interrupt signals generated by applying a negative-going edge to the $\overline{INT}$ pin. The edge is used to latch the interrupt flag register INTF) until an interrupt is granted by the device. An active low level will also be sensed.
MC/$\overline{MP}$	62	I	Memory mode select pin. High selects the microcomputer mode, in which internal on-chip program memory is available. This pin should be tied to V_{DD} at all times.
$\overline{MEN}$	56	O	Memory enable. $\overline{MEN}$ is an active low control signal generated by the device to enable instruction fetches from program memory. $\overline{MEN}$ will be active on instructions fetched from both internal and external memory. When $\overline{MEN}$ is active, $\overline{MWE}$, $\overline{IOWE}$, and IOEN will be inactive (high).
$\overline{MWE}$	12	O	Write enable for device output data. When active (low), $\overline{MWE}$ indicates that data will be output from the device on the data bus. When $\overline{MWE}$ is active, $\overline{MEN}$, $\overline{IOEN}$, and $\overline{IOWE}$ will always be inactive (high).
NC	1, 12, 18, 19, 24, 29, 33, 50, 51, 55		No connection.
$\overline{RS}$	2	I	Schmitt-triggered input for initializing the device. When held active for a minimum of five clock cycles, $\overline{IOEN}$, $\overline{IOWE}$, $\overline{MWE}$, and $\overline{MEN}$ are forced high; and, the data bus (D15 through D0) is not driven. The program counter (PC) and the address bus (A15 through A0) are then synchronously cleared after the next complete clock cycle from the falling edge of $\overline{RS}$. Reset also disables the interrupt, clears the interrupt flag register, and leaves the overflow mode register unchanged. The device can be held in the reset state indefinitely.

SUPPLY/OSCILLATOR SIGNALS			
Pin		**I/O/Z***	**Description**
Name	**No.**		
CLKOUT	9	O	System clock output (one-fourth crystal/CLKIN frequency).
V_{DD}	26, 57, 58, 59, 60	I	5V supply pins.
V_{SS}	5, 6, 7, 8, 42, 61	I	Ground pins.
X1	3	O	Crystal output pin for internal oscillator. If the internal oscillator is not used, this pin should be left unconnected.
X2/CLKIN	4	I	Input pin to the internal oscillator (X2) from the crystal. Alternatively, an input pin for an external oscillator (CLKIN). The crystal or external oscillator frequency must be 22.25 MHz.

DSP GROUP, INC., 4050 MOORPARK AVE., SAN JOSE, CA 95117
PH: 408-985-0722 FAX: 408-985-2108

PIN DESCRIPTIONS (CONTINUED)

D0000-26 (Analog I/O interface)			
Pin		I/O/Z*	Description
Name	No.		
V_{BB}	1	PWR	Negative supply voltage; –5V.
PWRO+	2	O	Noninverting output of power amplifier. Can drive transformer hybrids or high-impedance loads directly in either a differential or a single-ended configuration.
PWRO–	3	O	Inverting output of power amplifier; functionally identical with and complementary to PWRO+.
$\overline{PDN}$	4	I	Power-down select. The device is inactive with a TTL low-level input to this pin and active with a TTL high-level input to the pin.
DCLKR	5	I	Selects fixed or variable data-rate operation. When this pin is connected to V_{BB}, the device operates in the fixed-data-rate mode. When DCLKR is not connected to V_{BB}, the device operates in the variable-data-rate mode, and DCLKR becomes the receive data clock, which operates at frequencies from 64 KHz to 2.048 MHz.
PCM IN	6	I	Receive PCM input. PCM data is clocked in on this pin on eight consecutive negative transitions of the receive data clock, which is CLKN in fixed-data-rate timing and DCLKR in variable-data-rate timing.
FSR/TSRE	7	I	Frame synchronization clock input/time slot enable for receive channel. In the fixed-data-rate mode, FSR distinguishes between signalling and non-signalling frames by a double- or single-length pulse, respectively. In the variable-data-rate mode, this signal must remain high for the duration of the timeslot. The receive channel enters the standby state when FSR is TTL low for 300ms.
DGTL GND	8	PWR	Digital ground for all internal logic circuits. Not internally connected to ANLG GND.
CLKR/ CLKX	9	I	Transmit/Receive master clock and data clock for the fixed-data-rate mode. Transmit/Receive master clock only for variable-data-rate mode.
FSX/TSXE	10	I	Frame synchronization clock input/time-slot enable for transmit channel. Operates independently of, but in an analogous manner to, FSR/TSRE. The transmit channel enters the standby state when FSX is low for 300ms.
PCM OUT	11	O	Transmit PCM output. PCM data is clocked out on this output on eight consecutive positive transitions of the transmit data clock, which is CLKX in fixed-data-rate timing and DCLKX in variable-date-rate timing.
$\overline{TSX}$/ DCLKX	12	I/O	Transmit channel time slot strobe (output) or data clock (input) for the transmit channel. In the fixed-data-rate mode, this pin is an open-drain output to be used as an enable signal for a three-state buffer. In the variable-data-rate mode, DCLKX becomes the transmit data clock, which operates at TTL levels from 64 KHz to 2.048 MHz.
ANLG GND	13	PWR	Analog ground return for all internal voice circuits. Not internally connected to DGTL GND.
ANLG IN–	14	I	Inverting analog input to uncommitted transmit operational amplifier.
GSX	15	O	Output terminal of internal uncommitted operational amplifier. Internally, this is the voice signal input to the transmit filter.
V_{CC}	16	PWR	Positive supply voltage; 5V.

PIN DESCRIPTIONS (CONTINUED)

D0000-29 (Analog I/O Interface)			
Pin		I/O/Z*	Description
Name	No.		
V_{BB}	1	PWR	Negative power supply pin. V_{BB} = -5V
GNDA	2	PWR	Analog ground. All signals are referenced to this pin.
VFR_O	3	O	Analog output of the receive power amplifier.
V_{CC}	4	PWR	Positive power supply pin. VCC = +5V.
FS_R	5	I	Receive frame sync pulse which enables $BCLK_R$ to shift PCM data into D_R.
D_R	6	I	Receive data input. PCM data is shifted into D_R following the FS_R leading edge.
$BCLK_R$/ CLKSEL	7	I	Logic input which selects either 1.536 MHz/1.544 MHz or 2.048 MHz for master clock in synchronous mode and $BCLK_X$ is used for both transmit and receive directions. This input should be tied to ground.
$MCLK_R$/ PDN	8	I	Receive master clock. When $MCLK_R$ is connected continuously low, $MCLK_X$ is selected for all internal timing. When $MCLK_R$ is connected continuously high, the device is powered down.
$MCLK_X$	9	I	Transmit master clock. Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with $MCLK_R$. Best performance is realized from synchronous operation.
$BCLK_X$	10	I	The bit clock which shifts out the PCM data on DX. May vary from 64 KHz to 2.048 MHz, but must be synchronous with $MCLK_X$.
D_X	11	O/Z	PCM data output which is enabled by FS_X.
FS_X	12	I	Transmit frame sync pulse input which enables $BCLK_X$ to shift out the PCM data on D_X. FS_X is an 8 KHz pulse train.
$\overline{TS_X}$	13	O	Open drain output which pulses low during the encoder time slot.
GS_X	14	O	Analog output of the transmit input amplifier. Used to externally set gain.
VF_XI-	15	I	Inverting input of the transmit input amplifier.
VF_XI+	16	I	Non-inverting input of the transmit input amplifier.

DSP GROUP, INC., 4050 MOORPARK AVE., SAN JOSE, CA 95117
PH: 408-985-0722 FAX: 408-985-2108

PIN DESCRIPTIONS (CONTINUED)

D0000-31 (SOJ)			
Pin		I/O/Z*	Description
Name	No.		
A0	9	I	Row and column address bits. Row address bits are latched in the chip by the $\overline{RAS}$ signal. Column address bits are latched in by the $\overline{CAS}$ signal.
A1	10	I	
A2	11	I	
A3	12	I	
A4	14	I	
A5	15	I	
A6	16	I	
A7	17	I	
A8	18	I	
A9	22	I	
$\overline{RAS}$	3	I	Row address strobe
$\overline{CAS}$	24	I	Column address strobe
D	1	I	Data input
Q	25	O	Data output
$\overline{W}$	2	I	Write enable input which selects read or write mode
VCC	13	–	+5V supply
VSS	26	–	Ground
TF	4	I	No connection

D0000-34 (SOJ)			
Pin		I/O/Z*	Description
Name	No.		
A0	9	I	Row and column address bits. Row address bits are latched in the chip by the $\overline{RAS}$ signal. Column address bits are latched in by the $\overline{CAS}$ signal.
A1	10	I	
A2	11	I	
A3	12	I	
A4	14	I	
A5	15	I	
A6	16	I	
A7	17	I	
A8	18	I	
A9	22	I	
A10	5	I	
$\overline{RAS}$	3	I	Row address strobe
$\overline{CAS}$	24	I	Column address strobe
D	1	I	Data input
Q	25	O	Data output
$\overline{W}$	2	I	Write enable input which selects read or write mode
VCC	13	–	+5V supply
VSS	26	–	Ground
TF	4	I	No connection

DSP GROUP, INC., 4050 MOORPARK AVE., SAN JOSE, CA 95117
PH: 408-985-0722 FAX: 408-985-2108

PIN DESCRIPTIONS (CONTINUED)

D6005A-71B (ASIC)			
Pin		I/O/Z*	Description
Name	No.		
AB0	55	I	DSP ADDRESS
AB1	56	I	DSP ADDRESS
AB2	57	I	DSP ADDRESS
$\overline{ACK}$	68	O	HOST INTERRUPT
ADDR0	29	O	MEMORY ADDRESS BUS (LSB)
ADDR1	28	O	MEMORY ADDRESS
ADDR2	27	O	MEMORY ADDRESS
ADDR3	26	O	MEMORY ADDRESS
ADDR4	25	O	MEMORY ADDRESS
ADDR5	24	O	MEMORY ADDRESS
ADDR6	23	O	MEMORY ADDRESS
ADDR7	22	O	MEMORY ADDRESS
ADDR8	21	O	MEMORY ADDRESS
ADDR9	20	O	MEMORY ADDRESS
ADDR10	19	O	MEMORY ADDRESS
ADDR11	18	O	MEMORY ADDRESS
ADDR12	17	O	MEMORY ADDRESS
ADDR13	16	O	MEMORY ADDRESS
ADDR14	15	O	MEMORY ADDRESS
ADDR15	14	O	MEMORY ADDRESS BUS (MSB)
$\overline{BIO}$	64	O	DSP BIO
$\overline{CAS0}$	76	O	ARAM CAS
$\overline{CAS1}$	77	O	ARAM CAS
$\overline{CAS2}$	78	O	ARAM CAS
$\overline{CAS3}$	79	O	ARAM CAS
$\overline{RAS}$	80	O	ARAM RAS
DB0	36	I/O/Z	DSP DATA BUS (LSB)
DB1	37	I/O/Z	DSP DATA BUS
DB2	38	I/O/Z	DSP DATA BUS
DB3	39	I/O/Z	DSP DATA BUS
DB4	40	I/O/Z	DSP DATA BUS
DB5	41	I/O/Z	DSP DATA BUS
DB6	42	I/O/Z	DSP DATA BUS
DB7	43	I/O/Z	DSP DATA BUS
DB8	44	I/O/Z	DSP DATA BUS
DB9	45	I/O/Z	DSP DATA BUS
DB10	46	I/O/Z	DSP DATA BUS
DB11	47	I/O/Z	DSP DATA BUS
DB12	48	I/O/Z	DSP DATA BUS
DB13	49	I/O/Z	DSP DATA BUS
DB14	50	I/O/Z	DSP DATA BUS
DB15	51	I/O/Z	DSP DATA BUS (MSB)
DR	70	I	PCM IN
NC	72	I	
DRMDT	75	I/O/Z	ARAM DATA

DSP GROUP, INC., 4050 MOORPARK AVE., SAN JOSE, CA 95117
PH: 408-985-0722 FAX: 408-985-2108

PIN DESCRIPTIONS (CONTINUED)

D6005A-71B (ASIC)			
Pin		I/O/Z*	Description
Name	No.		
$\overline{\text{DRMWR}}$	73	O	ARAM WRITE
DSPCLK	34	O	DSP CLOCK
$\overline{\text{DSPRS}}$	9	O	DSP RESET
DX	69	O	PCM OUT
NC	71	O	
FSYNC0	63	O	CODEC0 FSYNC
FSYNC1	66	O	CODEC1 FSYNC
HI/LO	58	I	HIGH/LOW BYTE SELECT
HSTDB0	1	I/O/Z	HOST DATA BUS
HSTDB1	2	I/O/Z	HOST DATA BUS
HSTDB2	3	I/O/Z	HOST DATA BUS
HSTDB3	4	I/O/Z	HOST DATA BUS
HSTDB4	5	I/O/Z	HOST DATA BUS
HSTDB5	6	I/O/Z	HOST DATA BUS
HSTDB6	7	I/O/Z	HOST DATA BUS
HSTDB7	8	I/O/Z	HOST DATA BUS
$\overline{\text{HSTRD}}$	59	I	HOST READ
$\overline{\text{HSTWR}}$	60	I	HOST WRITE
$\overline{\text{INT}}$	61	O	DSP INTERRUPT
$\overline{\text{IORD}}$	53	I	DSP IO READ
$\overline{\text{IOWR}}$	10	I	DSP IO WRITE
$\overline{\text{RESET}}$	35	I	ACTIVE LOW ASIC RESET INPUT
SCLK	74	O	CODEC SER. CLK
$\overline{\text{SRMRD}}$	67	O	SRAM READ
$\overline{\text{SRMWR}}$	62	O	SRAM WRITE
$\overline{\text{EPRRD}}$	65	O	EPROM READ
XIN	32	I	XTAL IN
XOUT	31	O	XTAL OUT
CLKOUT	12	I	DSP CLKOUT
GND	52	PWR	GROUND PIN
GND	33	PWR	GROUND PIN
GND	11	PWR	GROUND PIN
V_{CC}	54	PWR	5V PIN
V_{CC}	30	PWR	5V PIN
V_{CC}	13	PWR	5V PIN

NOTE: CODEC 1 and EPROM interfaces are reserved for advanced features.

DSP GROUP, INC., 4050 MOORPARK AVE., SAN JOSE, CA 95117
PH: 408-985-0722 FAX: 408-985-2108

FUNCTIONAL DESCRIPTION

Voice Message Storage—Incoming and Outgoing Messages

The D6005B chipset supports up to 26 minutes of voice storage. The voice messages are stored in audio grade RAMs (ARAMs) in configurations of 4-Mbit or 1-Mbit devices. The chipset enables the recording of a total of up to 64 variable length incoming and outgoing messages. Multiple outgoing messages are supported. The message storage memory may be enlarged by adding memory chips up to a total of 16 Megabits. Each 1 Megabit memory chip allows an additional message storage time of 103 seconds.

The D6005B message storage uses a proprietary high quality speech compression technique at a rate of 10.2 Kbps. The compression technique used is enhanced by an error correction algorithm that enables use of ARAM (Audio grade DRAMs) memory without degradation of speech quality.

The D6005B is capable to report to the host the status of the currently available memory storage area, as well as the overall status of the ARAMs (number of recorded messages).

Digital voice activated recording (VOX)

The digital speech detection is implemented in the DSP chip. The DSP chip performs speech detection at 22ms intervals, at the end of which it indicates to the HOST whether a speech frame has been detected. The HOST reads this status information and decides accordingly whether to stop the recording of this message. During recording, the D6005B performs telephone line monitoring. The host is capable of terminating the recording with a deletion of the last n*0.7 seconds from the memory (Tail Cut function).

Playback of Messages

The D6005B supports random playback of any message previously recorded. Playback from the beginning or from a predefined offset time may be performed. During the playback, the D6005B performs monitoring of the telephone line.

Pause and Offset Report

The playback of the prerecorded message can be stopped by a PAUSE command, initiated by the host. The DSP responds with a time offset (from the beginning of the current message) information if Read Offset bit (bit 10) was set. The offset may be received on a continuous basis during normal playback as well. After PAUSE, playback may be resumed from the same point.

Message Deletion

The D6005B enables random deletion of any prerecorded message from the memory. After each deletion message directory is updated accordingly. To improve memory utilization, the D6005B supports "Garbage Collection," which eliminates empty spaces in the message memory.

Time Stamp of Messages

The host may send a 16-bit time indication to the D6005B, which can be used for time stamping of the message recorded.

DTMF Detection

The DTMF detection is implemented by the DSP in software. This function may be used for remote control operation of the answering device. The identification code of one of 12 detected DTMF signals is transferred to the host for further processing.

Tone Generation

DTMF signals are generated in accordance with the requirements of EIA RS-470. Voice processing is disabled during DTMF generation. Each tone pair may be selected by a host controller command. Thus, the duration of the tone is controlled by the host. The host processor controls the tone signal level.

Call Progress Tone

The D6005B monitors the line for incoming telephone line signals and detects the presence of a call progress tone in a predefined frequency region. The D6005B supports Call Progress Tones detection by utilizing one out of two filter/detectors. Selection of the detector is done during initialization (Self Test). The wide filter is 335-650 Hz and the narrow one is 330-500 Hz. Indication of call progress tone presence is transferred to the host processor every 22ms.

Speed Dial Telephone Number Storage

The host may store in the static RAM controlled by the D6005B up to 32 different telephone numbers, each with up to 16 digits.

Self Test and Parameter Initialization

The D6005B supports a self test function which is responsible for testing of both the ARAMs and the SRAM. Status indication about the success of each device test is returned to the host.

HOST Interface

The host interface is an 8-bit parallel data port, used for control and status information transfer. The host controls the operation of the D6005B using a simple command protocol. The D6005B status information is updated after each command.

The command and status protocol enables the host to have full control over the functions of the D6005B. The protocol is described in the next section.

MODES OF OPERATION

There are 13 modes of operation. The entrance to each of these modes from the monitor program is made through an IDLE mode. Following is the list of the 13 modes:

1. **IDLE**—In this mode the DSP performs command polling. It checks the command register in the HOST-DSP interface and transfers to the requested operation mode.
2. **Record mode**—In this mode the DSP performs speech compression and message recording into the ARAM.
3. **Playback mode**—In this mode the DSP performs message playback using compressed speech data stored in the ARAM.
4. **Read Memory status**—In this mode the DSP returns to the HOST information on the Memory status (Number of messages stored, availability of memory for recording the next message, ROM checksum and SRAM status).
5. **Write Tel. #**—In this mode the DSP receives a 16 digit telephone number from HOST and stores it in the SRAM in the telephone number directory.
6. **Read Tel. #**—In this mode the DSP returns to the HOST a telephone number stored in the telephone directory under the index number given by the HOST.
7. **Tone generation mode**—In this mode the DSP generates a tone signal – a dual tone out of 16 or one of 15 general purpose tones. The index number of the tone to be generated is sent by the HOST in the command word.
8. **Line monitoring mode**—In this mode the DSP monitors the telephone line for detection of either a DTMF signal or any other Call Progress tone. The DSP reports on any such detection to the HOST in the status word.
9. **Delete message**—In this mode the DSP erases the memory message entry whose ID is specified by the HOST from the messages directory. It then shifts all the other entries one entry down. If the message entry number sent by the HOST is 7FH, the DSP performs a "Garbage Collection" process, getting rid of unused memory space between messages.
10. **Write current time**—In this mode the HOST sends to the DSP the current time & date stamp.
11. **Get time stamp**—In this mode the DSP returns to the HOST the time & date stamp pertaining to the message whose ID is specified by the HOST in the command word.
12. **Get available record time**—In this mode the DSP reports available record time.
13. **Self test & Init ARAM** —In this mode the DSP performs Static RAM and DRAM testing. The test results are returned to the HOST indicating the status of SRAM and ARAMs.

DESCRIPTION OF MODES OF OPERATION

IDLE mode

This is a polling mode in which the DSP monitors the DSP-HOST interface waiting for HOST commands. Transition to any other mode is always done through the IDLE MODE.

Record mode

In this mode the DSP performs speech compression and message recording into the ARAM. The DSP starts to store the message to ARAM after detecting VOX. While in this mode, the DSP continuously monitors (every 22ms) a communication port for HOST command. If no new command has been detected, the DSP continues message recording. If a new command detected is a record command, the DSP returns the VOX, line monitoring (tone detection information) and ARAM status to the HOST. Otherwise the DSP ends recording, updates the message directory and returns to IDLE mode. The DSP indicates this to the HOST by sending the IDLE mode status word.

When the DSP is in RECORD mode, the host can stop recording of message with a deletion of the last n*0.7 seconds from the memory (Tail Cut function). After this command the DSP returns to IDLE mode.

The Memory Full (bit 5) in the status word is set if the ARAM is full. In the case that the ARAM is full, the DSP remains in record mode, stops recording, but continues to perform line monitoring and VOX functions.

Playback mode

In playback mode, the DSP performs message playback and line monitoring. This mode is entered upon receiving a playback command while in IDLE mode. The DSP returns the same word as a status command. The second word that the HOST sends to the DSP is an OFFSET indicating where to start playback from the beginning of the message, in units of 1.4 seconds. The DSP returns the OFFSET word to the HOST. Then, it begins playing the message from that point on.

The DSP checks the HOST port every 22ms for new commands. If no new command has been detected, the DSP continues to play the message. If the new command is not a Playback command, the DSP exits Playback mode and returns to IDLE mode. It indicates this to the HOST by sending the IDLE mode status word. During playback, the host can read the offset and pause the recording by issuing respective additional playback commands.

Read Memory Status

In this mode the DSP returns to the HOST the status of the ARAM indicating whether there is space in the ARAM for recording of a new message. It also returns the number of the last message recorded. When 64 messages were recorded or when there is no available memory space for recording further messages, Memory Full bit is set. When 64 messages were recorded, 8 LSB bits of status word are '1'.

The SRAM self test includes writing of fixed patterns to predefined locations. SRAM status bit indicates whether reading back these patterns back and comparing them to its known values was successful. The checksum status indicates result of DSP internal ROM checksum test.

WriteTelephone Number

In this mode the DSP receives from the HOST a word containing 4 telephone digits and writes it in the telephone directory under the entry number specified in the command word (the first word). The DSP automatically returns to the IDLE mode after this command.

Read Telephone Number

In this mode the DSP returns to the HOST a word containing 4 telephone digits from the telephone directory using the entry specified in the first command word.

Tone Generation mode

In this mode the DSP generates a DTMF signal or one of 15 general purpose tones. The index for the signal/tone to be generated is sent by the HOST in the command word.

The indices are as follows:

GEN CODE	DTMF CODE	FREQ 1	FREQ 2
0	No Tone		
1	1	697	1209
2	2	697	1336
3	3	697	1477
4	4	770	1209
5	5	770	1336
6	6	770	1477
7	7	852	1209
8	8	852	1336
9	9	852	1447
A	*	941	1209
B	0	941	1336
C	#	941	1477
D		800	
E		1000	
F		1250	
10		950	
11		1100	
12		1400	
13		1500	
14		1600	
15		1800	
16		2100	
17		1300	
18		2450	
19		350	440
1A		440	480
1B		480	620
1C	A	697	1633
1D	B	770	1633
1E	C	852	1633
1F	D	941	1633

The DSP checks the host port every 22ms for a new HOST command. Whenever a new tone generation command is sent, the DSP retrieves the tone index from command word and starts generating the new tone. In case that the command is not a TONE generation command, the DSP returns to the IDLE mode.

If no new command is sent, the DSP continues generating the previously generated tone.

Line Monitoring mode

In this mode the DSP monitors the telephone line for the detection of a DTMF signal or any of the Call Progress tones. Again, the DSP checks for a new HOST command each 22ms.

In case that HOST sends a Line monitoring command, the DSP returns a status word to the HOST containing the index of the signal that has been detected:

INDEX	DESCRIPTION
0	No signal has been detected.
1–12	A DTMF signal ID.

In addition the status word reports the presence of a Call Progress tone.

If the command is not a Line monitoring command, the DSP returns to the IDLE mode. In case that no command has been sent, it continues in the Line monitoring mode.

Delete Message

In this mode the DSP performs one of the following two functions:

1. If the message number is from 0 to 63, the DSP removes the message entry from the message directory and shifts all message entries above one place down in the directory. It then updates the last message number to be lower by one.
2. If the message number is 7FH, the DSP performs GARBAGE COLLECTION to get rid of empty spaces in the message memory. It then updates the message directory accordingly. When the DSP completes performing this process, it sends a status word to the HOST.

Write Current Time

In this mode the HOST sends to the DSP the current time & date mark that will be used for time stamping of the next message to be recorded. This time stamp is attached to the message and can be retrived by Get Time Stamp command.

Get Time Stamp

In this mode the DSP sends to the HOST the time & date stamp of the message specified in the command word.

Get Available Record Time

In this mode, the DSP sends to the HOST the available record time in 1.4s units.

Self Test & Init ARAM

In this mode the DSP performs testing of both the Static RAM and the ARAM. The DSP returns status bits indicating Pass or Fail for SRAM and ARAM memory space status. This command erases the contents of both SRAM and ARAMs. Therefore, it should be used only on first power-up.

In addition this command selects which call progress tone filter will be used - narrow or wide. The host processor can skip the initialization of the SRAM and ARAM memory and just select call progress filter.

If the memories were not initialized after first power-up, the D6005B assumes that the system has 16 Mbit ARAM memory.

HOST INTERFACE PERFORMANCE

The D6005B maximal response times to host commands are listed on the following table:

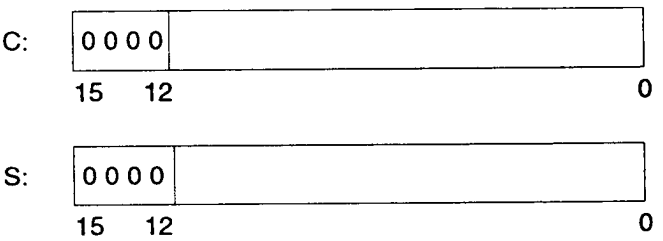
COMMAND	MAX STATUS RESPONSE TIME
Idle	22 msec
Record	22 msec
First Playback	1 msec
Second Playback (offset)	1 msec
Next Playback (continue)	22 msec
Line Monitor	22 msec
Delete Message without Garbage Collection	1 msec
Delete Message with Garbage Collection	5 sec **
Set Current Time	1 msec
Get Time	1 msec
Get Available Record Time	1 msec
Read ARAM Status	1 msec
Write Telephone Number	1 msec
Read Telephone Number	1 msec
DTMF Generation	1 msec ***
Self Test	40 sec *

* execution time for 6005B system with 8 Mbit ARAM

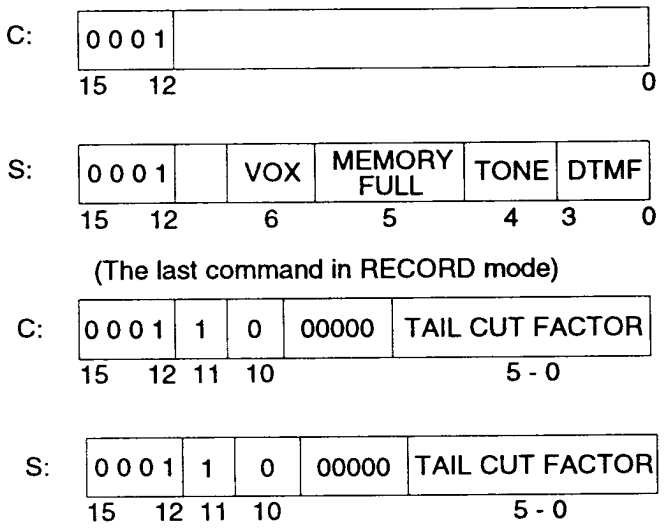
** execution time for D6005B system with 7 minutes of recorded messages

*** status response is less than 1 ms. The tone is generated in less than 5 ms.

0. IDLE



1. Record



Cutting Factor – Message tail cutting in units of 0.7 seconds.
00000 – Message tail is not cut.

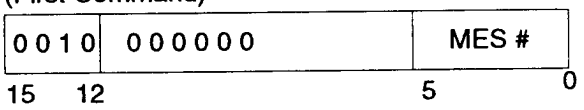
NOTE: This command is optional and does not have to be sent.

DSP GROUP, INC., 4050 MOORPARK AVE., SAN JOSE, CA 95117
PH: 408-985-0722 FAX: 408-985-2108

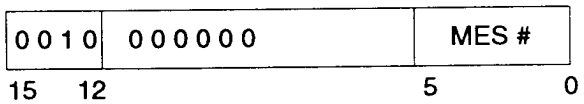
2. Playback

(First Command)

C:

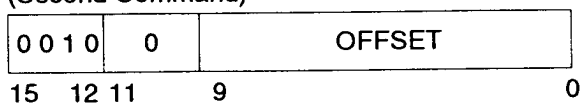


S:

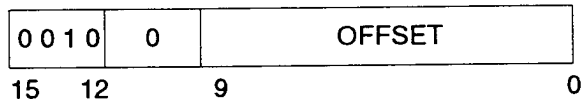


(Second Command)

C:



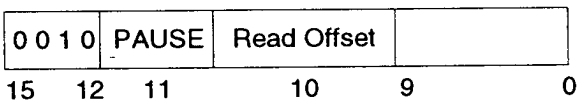
S:



OFFSET (10 BIT) IN UNITS OF 1.4 Sec.

The next Playback command is a playback internal command for monitoring the playback mode:

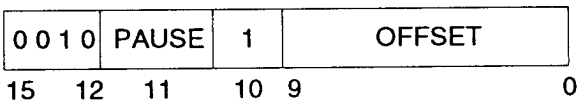
C:



PAUSE = 1 PLAYBACK stop
PAUSE = 0 Continue PLAYBACK

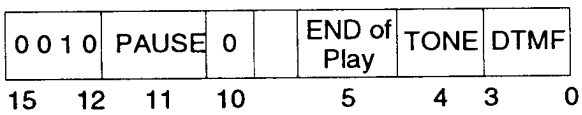
If Read Offset = 1 then:

S:



If Read Offset = 0 then:

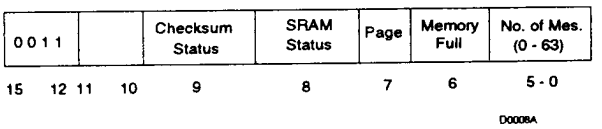
S:



3. Read Memory Status

C:

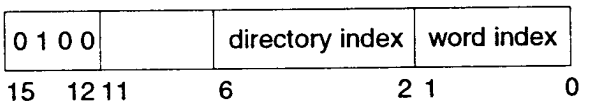
S:



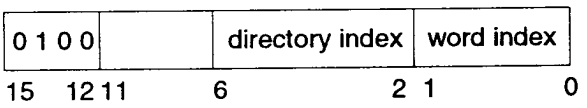
Page = 1 for messages #64 - 126 (reserved)
SRAM status and Checksum status – '0' when OK. When set indicate error.

4. Write Telephone Number

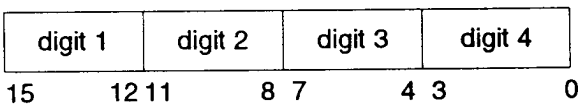
C:



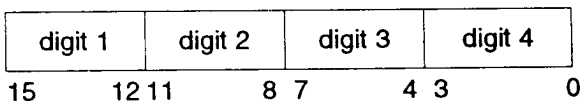
S:



C:

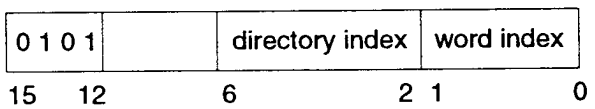


S:

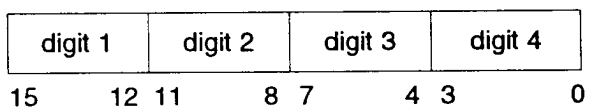


5. Read Telephone Number

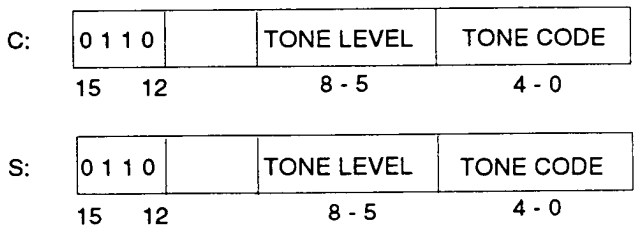
C:



S:



6. Tone Generation



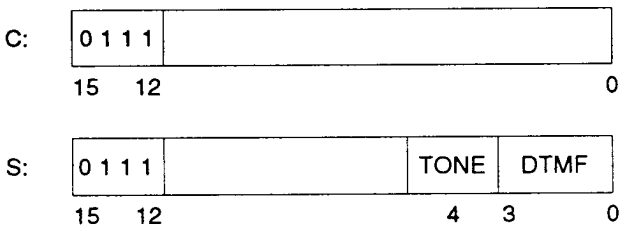
TONE CODE = 0 No Tone
1-12, 28 - 31 DTMF
13 - 27 General purpose tones

TONE LEVEL = 0000 – Normal (0 dB = 0.267 V RMS)
0001 - 0111 – Gain level (+2dB steps)
1001 - 1111 – Attenuation level (-2dB steps)

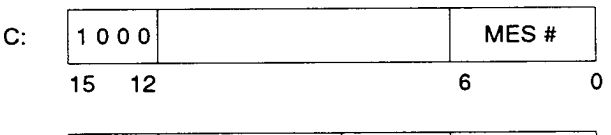
NOTE: DTMF levels are -1 dB for DTMFLO and +1 dB for DTMFHI relative to the tone level.

Gain of 14 dB is not supported.

7. Line Monitor



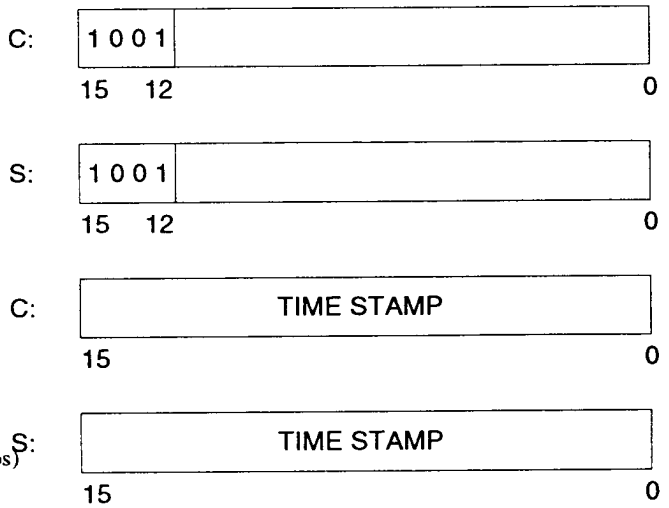
8. Delete Message



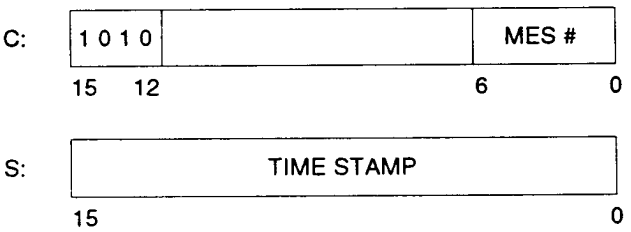
MES #:		STATUS:
0 - 63	Del MES.	00 - OK
127 -	Garbage Collection	01 - Empty Message
		10 - Garbage Collection

D0013

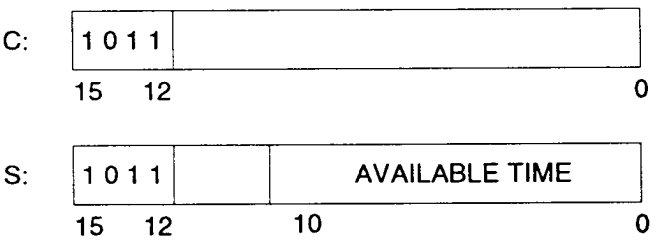
9. Set Current Time



10. Get Time Stamp



11. Get Available Record Time

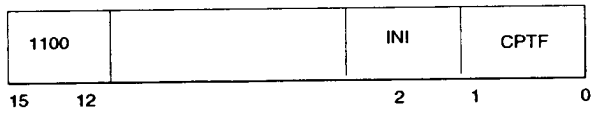


AVAILABLE TIME: in units of 1.4 Sec.

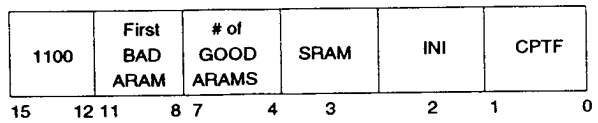
DSP GROUP, INC., 4050 MOORPARK AVE., SAN JOSE, CA 95117
PH: 408–985-0722 FAX: 408–985-2108

12. Self Test & Initialize Memory

C:



S:



No. of GOOD ARAMS – no. of good 1Mbit ARAMS (If 16 then = 0000 and index of 1st bad = 0001)

INDEX OF FIRST BAD ARAM –
Position of 1st BAD ARAM from the beginning of ARAM ARRAY

SRAM STATUS – 0 SRAM OK

1 SRAM BAD

CPTF – Call Progress Tone Filter
00 = Narrow (330 - 530 Hz)
01 = Wide (330 - 660 Hz)

INI – Memory Initialize
0 = Initialize memory
1 = Do not initialize memory

FUNCTIONAL BLOCKS

The block diagram in Figure 10 shows the D6005A-71B and its functional blocks and interfaces.

ARAM INTERFACE

The ARAM interface offers up to 16Mbits of ARAM storage for message storage. This interface can support up to 4 chips of 4Mbit x 1 ARAMS without external logic, or up to 16 chips of 1Mbit x 1 ARAM with additional logic (2 chips of 74HC139).

This block consits of two parts:

a. ARAM read/write logic

b. Refresh logic

The 12 address lines shared with address lines of SRAM. When accessing SRAM, refresh is disabled and the address bus is switched to SRAM address via the Address MUX.

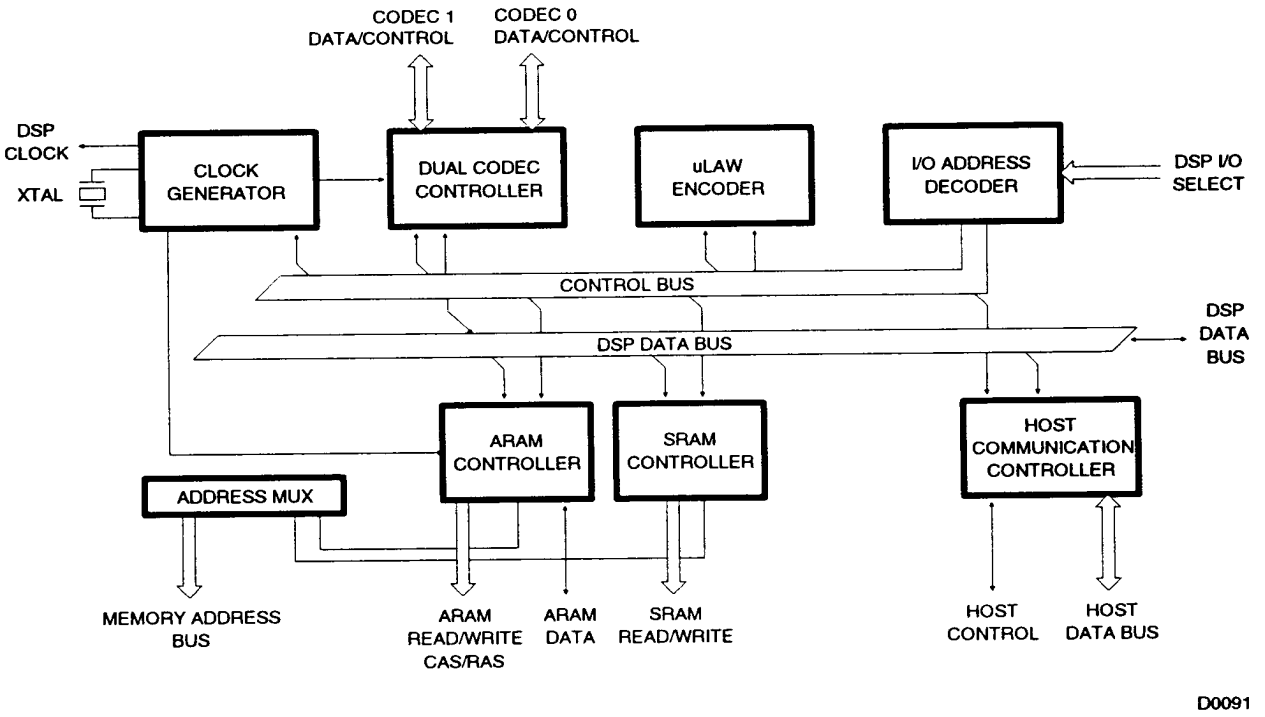


Figure 9. D6005A-71B (ASIC) Block Diagram

DSP GROUP, INC., 4050 MOORPARK AVE., SAN JOSE, CA 95117
PH: 408-985-0722 FAX: 408-985-2108

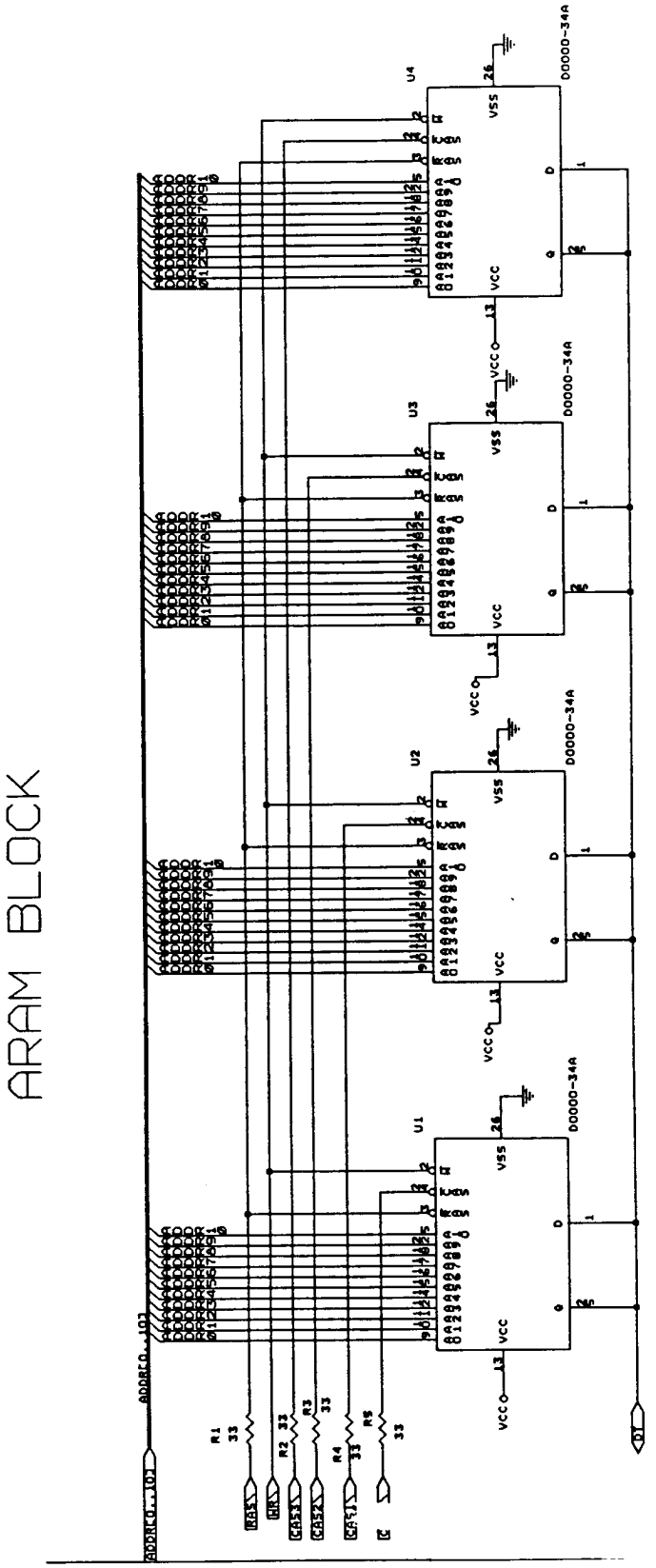


Figure 10. ARAM Block—4 Meg Devices (D0000-34)

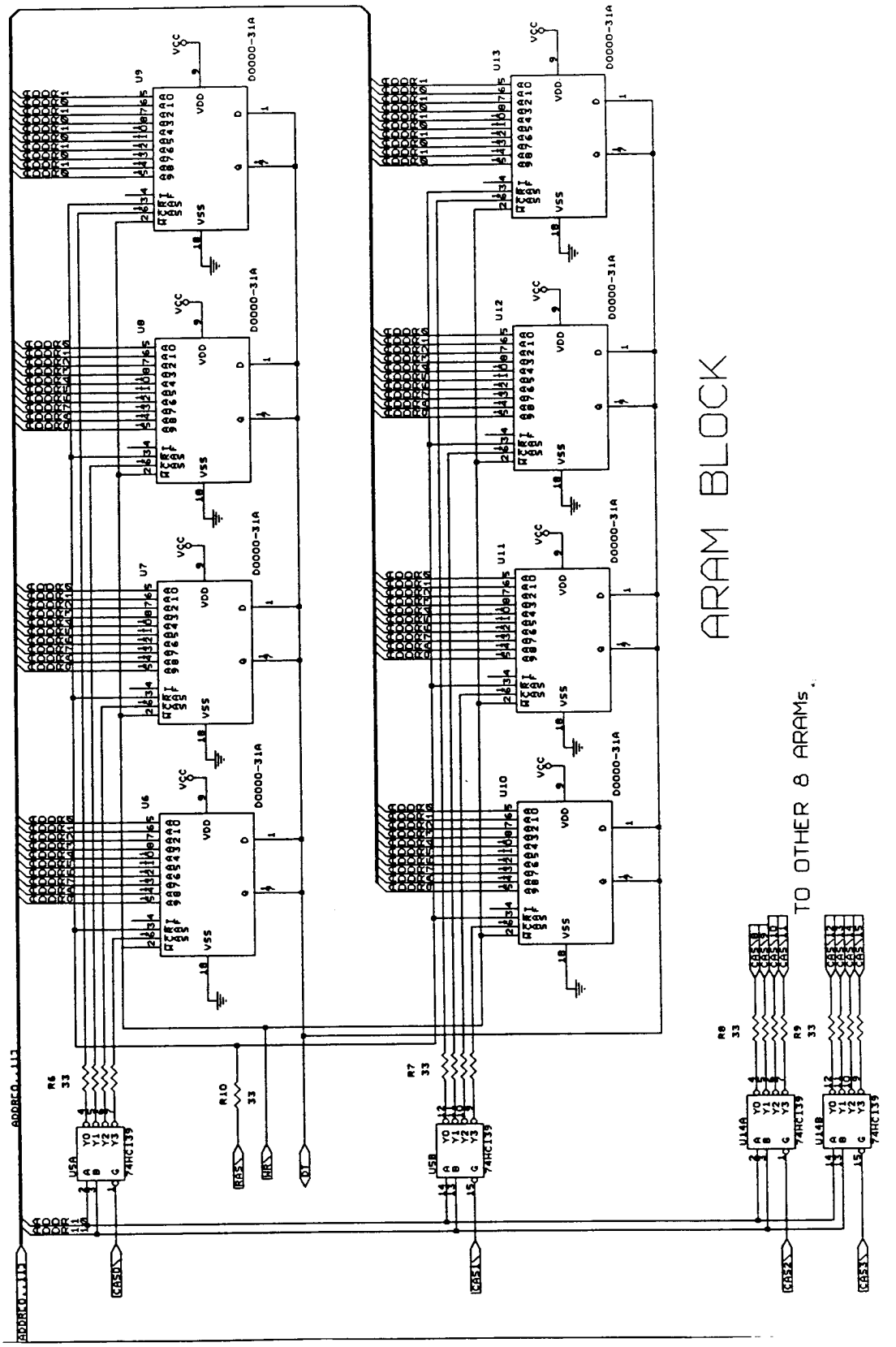


Figure 11. ARAM Block—1 Meg Devices (D0000-31)

DSP GROUP, INC., 4050 MOORPARK AVE., SAN JOSE, CA 95117
PH: 408-985-0722 FAX: 408-985-2108

SRAM INTERFACE

The SRAM interface supports access to single chip SRAM 8K x 8 with access time up to 100ns (at 22.25 MHz). The DSP will read/write from/to this static memory using the 16-bit bus. The D6005A-71B prepares the data before DSP reads by reading one byte from SRAM into an internal 18-bit register.

When the DSP reads this register it initiates the data read from SRAM in the next successful cycle. Loading address will also initiate data preparation in the D6005A-71B. When the DSP writes data to the internal register, in the next-following cycle, this data will be written by the D6005A-71B to the SRAM. The SRAM data bus will be connected to the same data bus as the DSP, using the high byte of this bus. The choice of accessing either SRAM or EPROM (reserved) is determined by the loading address: under 32K is SRAM, over 32K is EPROM (A15). Figures 13 and 14 show timing data for the SRAM interface.

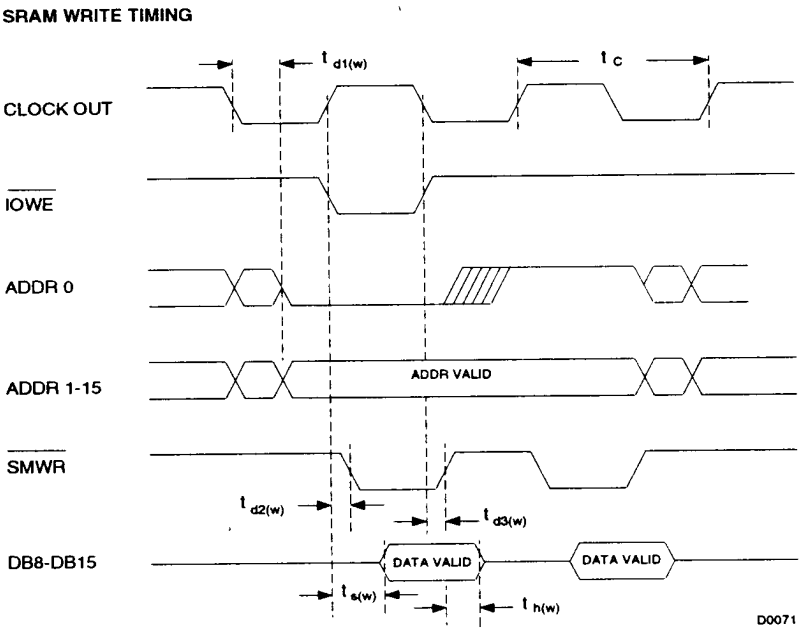


Figure 12. Timing data for the SRAM Interface—WRITE

$t_{d1(w)}$ = 65ns max
$t_{d2(w)}$ = 20ns max
$t_{d3(w)}$ = 15ns max
$t_{s(w)}$ = 27ns max
$t_{h(w)}$ = 3ns min

"t_C" in all the timing diagrams is 180ns nominal.

DSP GROUP, INC., 4050 MOORPARK AVE., SAN JOSE, CA 95117
PH: 408-985-0722 FAX: 408-985-2108

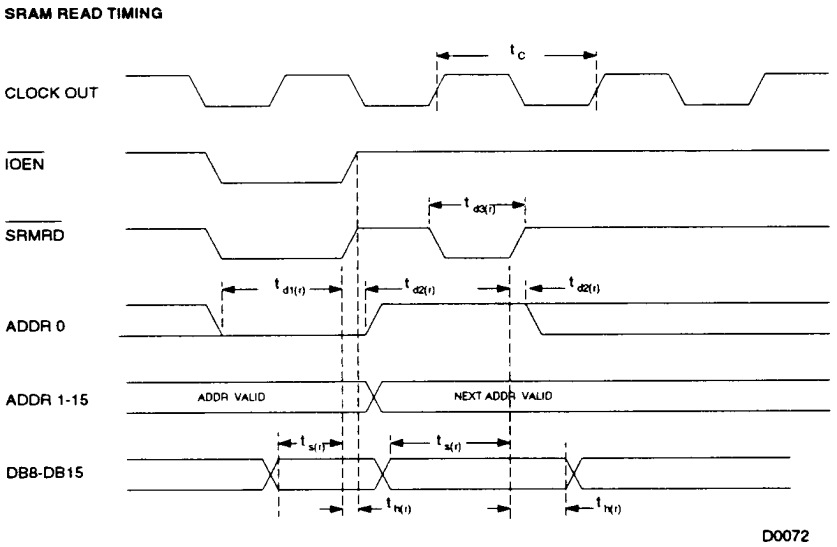


Figure 13. Timing data for the SRAM Interface—READ

$t_{d1(r)}$	= 110ns max
$t_{d2(r)}$	= 0ns max
$t_{d3(r)}$	= 90ns max
$t_{s(r)}$	= 30ns min
$t_{h(r)}$	= 0ns min

Power Down Mode

When the D6005B chipset is disconnected from its external power supply, it enters Power Down Mode. In this mode, power is supplied by internal TAD batteries. In Power Down mode, power is supplied to the D6005A-71B, SRAM and ARAMs in order to retain the essential data. The SRAM should be in non active mode (CE, WR, OE High), ARAM in minimum refresh mode and the DSP disconnected from its power supply, with the address decoder locked. Power Down Mode will be entered by applying a RESET signal to the D6005A-71B. When in power down mode the clock to the DSP will be held in low level to prevent contention. Figure 15 shows timing data for power down mode:

μ–LAW ENCODER

This is an interface implemented in the D6005A-71B to convert linear code (14-bit) to 8-bit μ-law PCM code. It works by writing 14-bit linear data to this interface. By next reading from this port we will get 8-bit PCM data.

Analog I/O Controller

The Analog I/O Controller implements the data transfer and synchronization functions required to interface the DSP with Analog I/O Interface (codec) chips. The data transfer to/from the codecs is serial, while shift registers enable an 8-bit parallel link with the DSP. The $\overline{INT}$ interrupt signal informs the DSP that a data byte is received or has to be transmitted.

Clock Generator

The clock generator is connected to an external 22.25MHz crystal, and generates clock signals for the DSP, Analog I/O Controller and memory controllers.

I/O Address Decoder

The I/O Address Decoder receives three DSP address lines (AB0–2) with I/O access control signals, and generates the required I/O read and write pulses for the DSP peripheral devices.

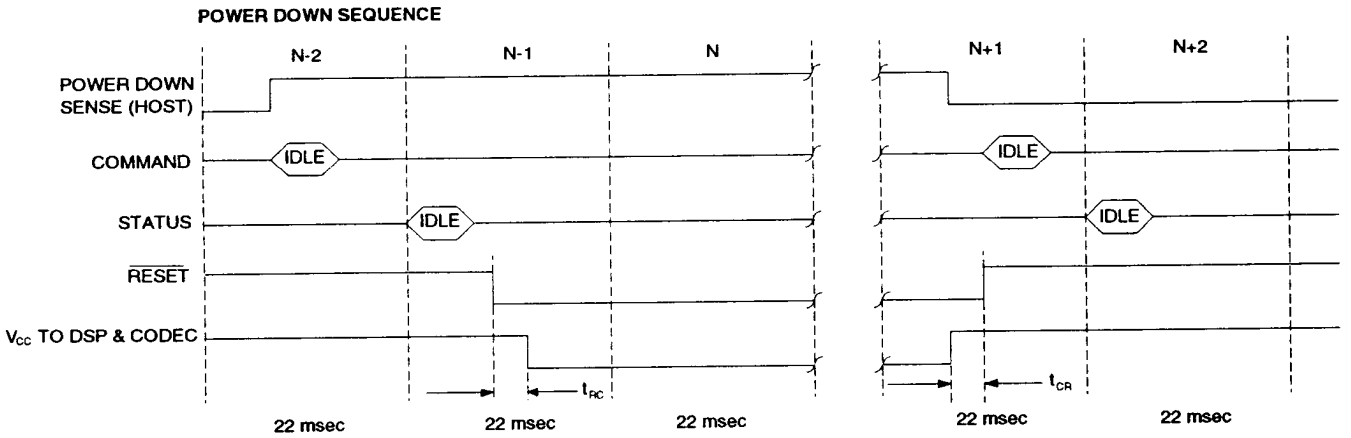


Figure 14. Timing data for the Power Down Sequence

tRC = 5µs min
tCR = 5µs min

HOST—DSP COMMUNICATION CONTROLLER

The host communication port is a 16-bit bidirectional register. The DSP will access this register by one 16-bit width access. HOST will access this register in two accesses, using the 8-bit bus: low byte and high byte. When HOST writes to High byte of this register it will set an internal flag, which is connected to the DSP BIO pin.

When the DSP reads the communication register this flag will be reset. When the DSP writes to the communication register it sets the ACK pin (External pin) which is connected to HOST for indication. When HOST reads the high byte of this register it will clear this ACK bit. The choice of high/low byte for host will be made by pin HI/LO. HOST will write to the communication register by strobing the HSTWR pin and by reading the HSTRD pin.

Table 1. Communication Interface Signals

Pin Name	Type(*)	Description
HSTD[0..7]	Input/Output	HOST 8-bit data bus
$\overline{HSTR}$	Input	HOST READ line from register
$\overline{HSTW}$	Input	HOST WRITE line into register
$\overline{ACK}$	Output	Flag to HOST–status byte ready in register
HI/$\overline{LO}$	Input	High or Low byte select

*Input and Output are referenced to the D6005B-71B.

Note that HOST will first write the low byte and second the high byte. Figure 16 shows the host interface for the D6005B—8051. Figure 17 shows timing data for the DSP Communication Interface. Table 1 summarizes the communication interface signals.

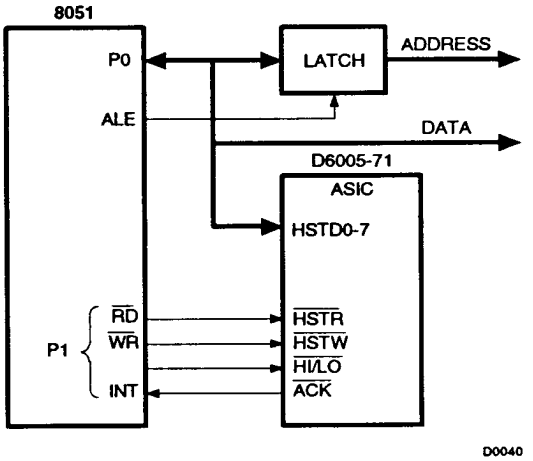


Figure 16. Host Interface D6005B—8051

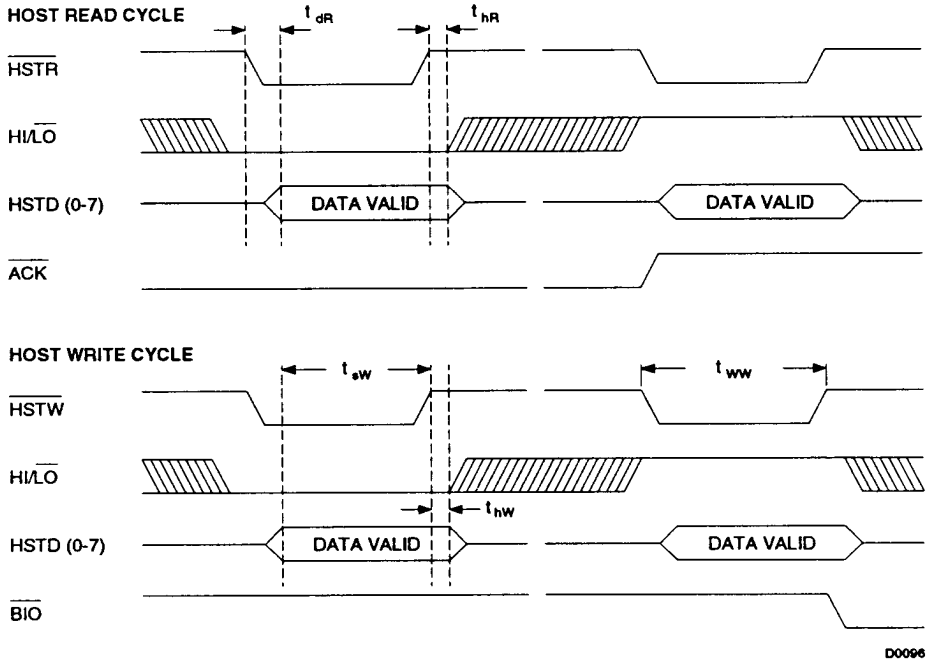


Figure 15. D6005B DSP—HOST Interface Timing Data

t_{hR}:	= 5ns min
t_{dR}	= 25ns max
t_{hW}:	= 5ns min
t_{sW}:	= 20ns min
tWW:	= 20ns min

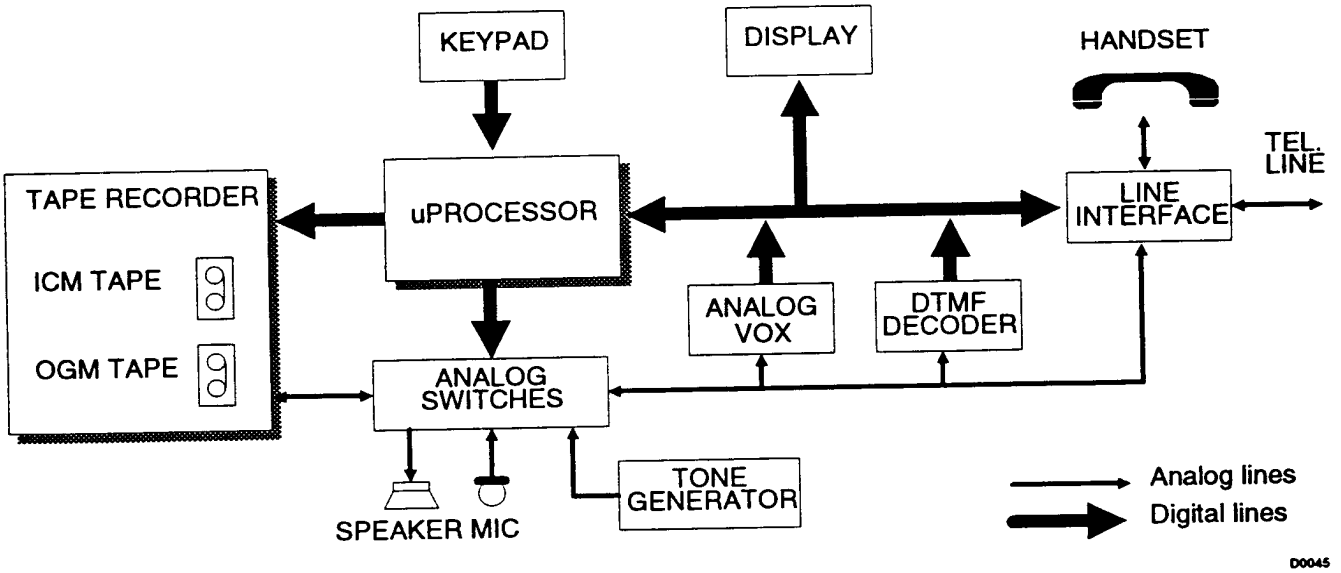


Figure 17. Conventional TAM

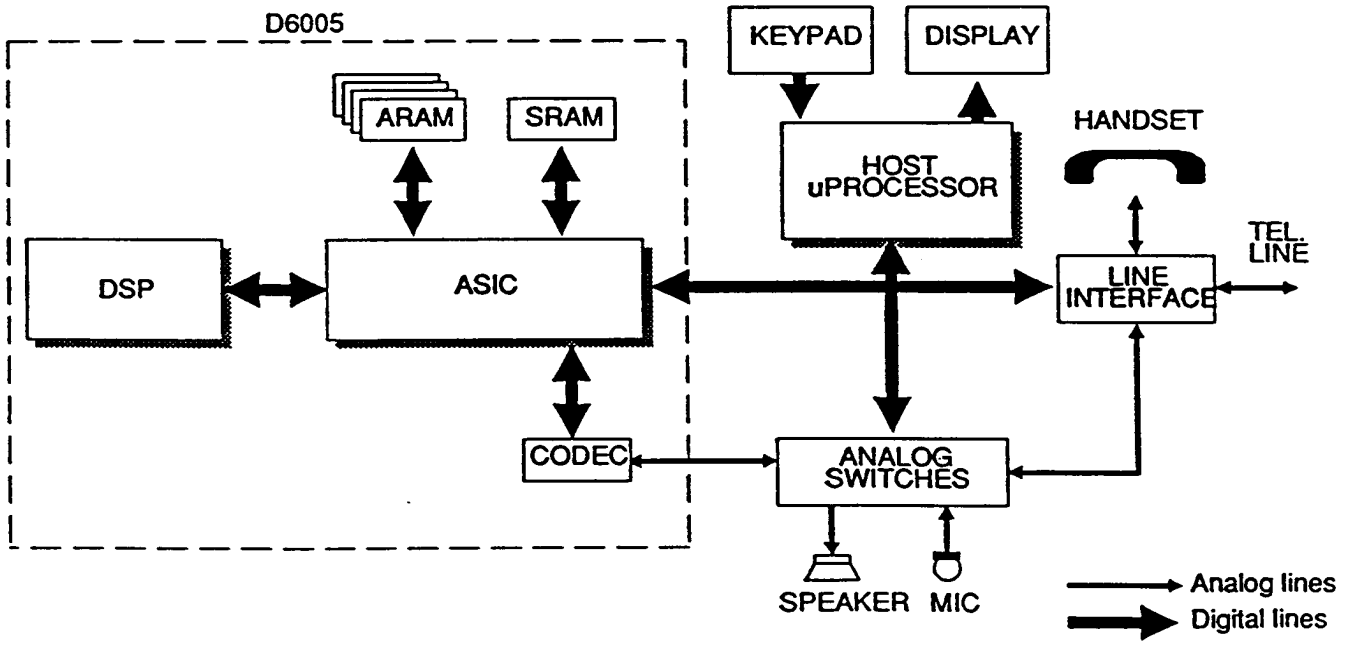


Figure 18. Digital TAM D6005A Implementation

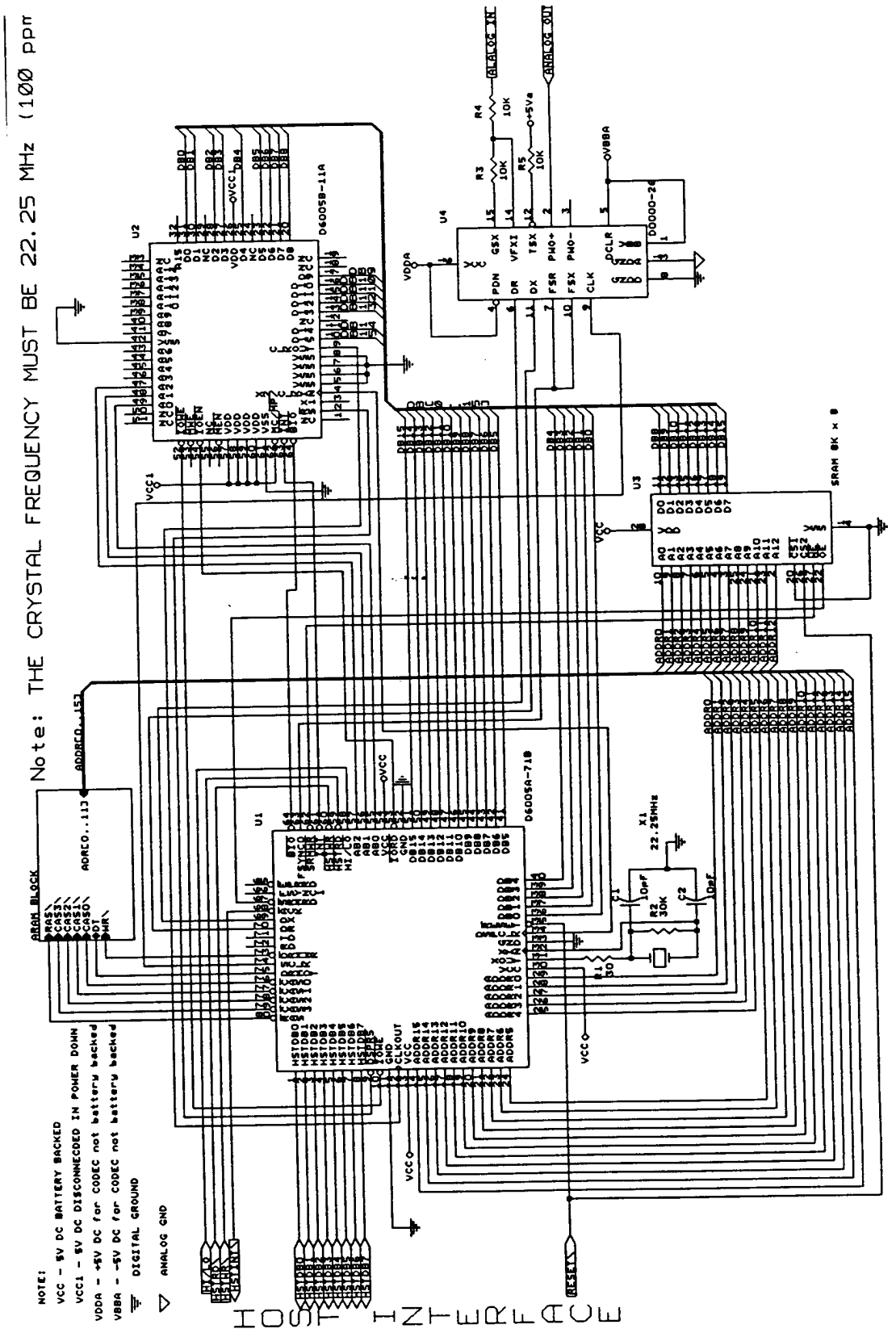


Figure 19. Chipset Interconnection Diagram with D0000-26 I/O Interface

DSP GROUP, INC., 4050 MOORPARK AVE. SAN JOSE CA 95117
PH: 408-985-0722 FAX: 408-985-2108

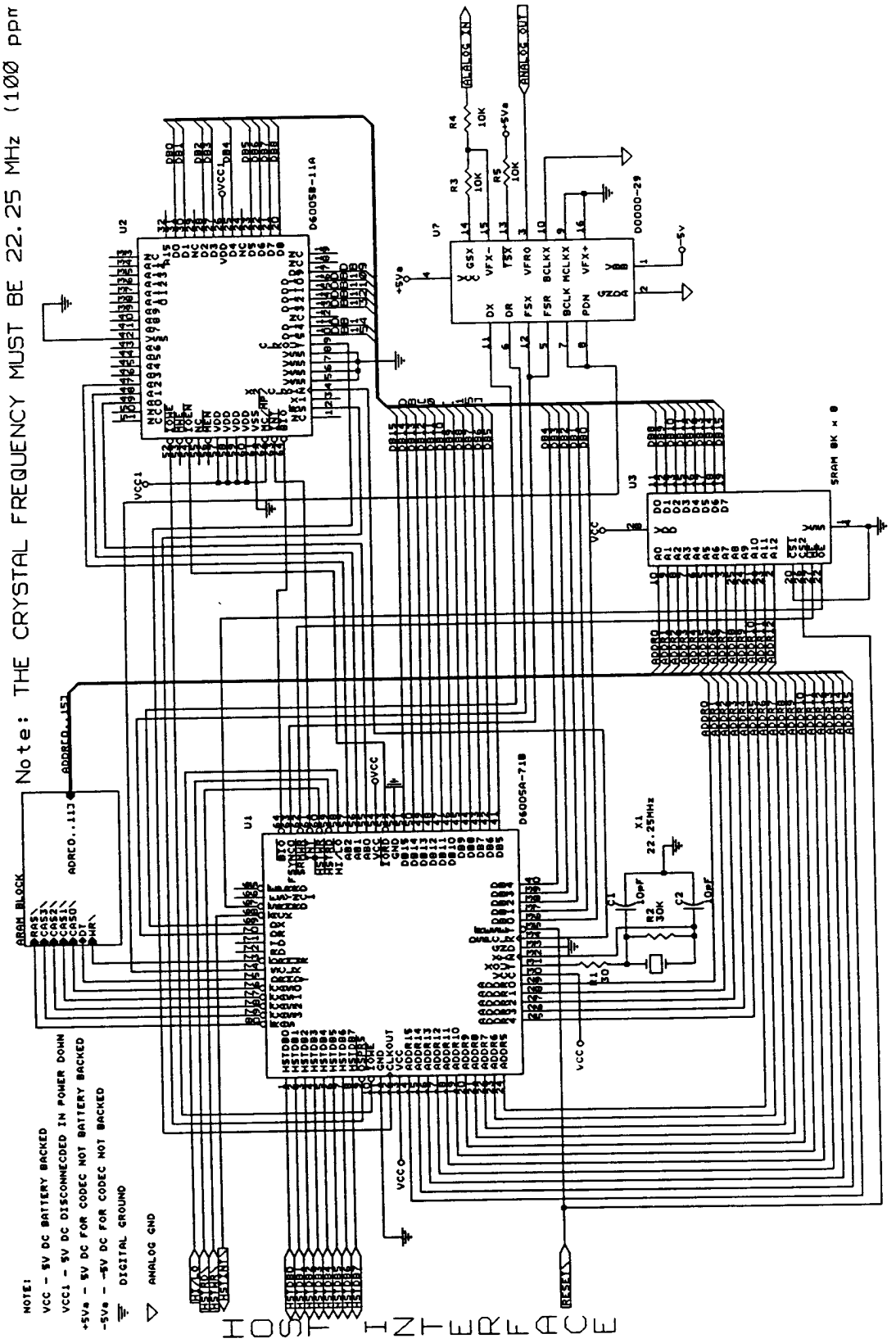


Figure 20. Chipset Interconnection Diagram with D0000-29 I/O Interface

DSP GROUP, INC., 4050 MOORPARK AVE. SAN JOSE CA 95117
PH: 408-985-0722 FAX: 408-985-2108

APPLICATION HINTS

Good printed circuit board (PCB) layout is as important as the overall circuit design itself in achieving high audio quality. To achieve this, the designer has to be conscious of noise both in the D6005A chipset and the front-end analog circuitry. Switching mode power supplies are not recommended as the switching spikes will feed through. Other causes of concerns are ground loops and digital feedthrough.

Layout Hints

Ensure that the layout for printed circuit board has digital and analog signal lines separated as much as possible. Take care not to run any digital track along side an analog signal. Guard the analog input with GNDA. Establish a single point analog ground separate from the digital ground. Low impedance analog and digital power supply common returns are essential to low noise operation.

Power Supply Considerations

Since the D6005A is a chipset with analog input and output, its performance (especially the analog front-end) may be adversely affected by the noise of the power supply. In order to prevent mixing of noise, observe the following cautions:

- Separate the power supply to the digital parts and analog parts.
- GNDs of two power supplies should be connected at only one point. Furthermore, that connecting point should be close to the supplies. This will minimize the effect of noise from the digital power supply to the analog power supply.

The power supply should have the least ripple possible, and a series regulator power supply is recommended for best condition. If a switching power supply is used, it should be stabilized by a three-terminal regulator.

Microphone and Speaker Considerations

An often overlooked fact is that the sound quality produced by D6005A chipset is directly related to the quality of the microphone and speaker connected to them. Use a good quality microphone and speaker with good frequency response. Design carefully the microphone preamplifier circuit. The physical location of the microphone, along with the characteristics of the microphone, play a large role in the playback sound quality.

Codec Input/Output Gain

There is difference in input and output gain of the two codecs D0000-26 and D0000-29 that can be used in the D6005A chipset. The gain of transmit and receive path is measured at 1020 Hz with 600 ohm load. For the D0000-29 the nominal gain for both paths is 4 dBm. The D0000-26 has 2.76 dBm gain in the transmit path and 5.76 dBm gain in the receive path. This causes that the D0000-26 has 3 dB gain when in loopback mode while the D0000-29 gain is 0 dB. To get completely identical gains in the both paths we recommend to the following modifications in the D6005A chipset with D0000-29 codec:

1. Increase the value of resistor R3 from 10K to 11.2K to compensate for the higher gain of the transmit path . The difference is 1.24 dBm (1.153).
2. Add additional external gain to the analog output to compensate for the lower gain of the receive path. The difference is 1.76 dBm (1.224).

Battery Backup

While the D6005A is in power down mode, power is supplied to the D6005A-71B (ASIC), SRAM and DRAMs. In this mode the D6005A-71B generates the neccessary refresh cycles for the DRAMs and the SRAM is not active. The typical power dissipation of the D6005A-71B is 4 mA. The typical power dissipation of D0000-31 (1M × 1 ARAM) and D0000-34 are 4 and 3 mA respectively. Following is analysis for several chipset configurations and available backup time.

Battery Type	Configuration	Recording time	Battery Backup
4 × AAA (850 mAH)	4 × D0000-31	7 minutes	42 hours
4 × AA (1700 mAH)	4 × D0000-31	7 minutes	85 hours
4 × AA (1700 mAH)	8 × D0000-31	14 minutes	47 hours
1 × 9V (500 mAH)	4 × D0000-31	7 minutes	25 hours
4 × AAA (850 mAH)	1 × D0000-34	7 minutes	121 hours
4 × AA (1700 mAH)	2 × D0000-34	14 minutes	170 hours
NiCd 4 × AA(500 mAH)	4 × D0000-31	7 minutes	25 hours

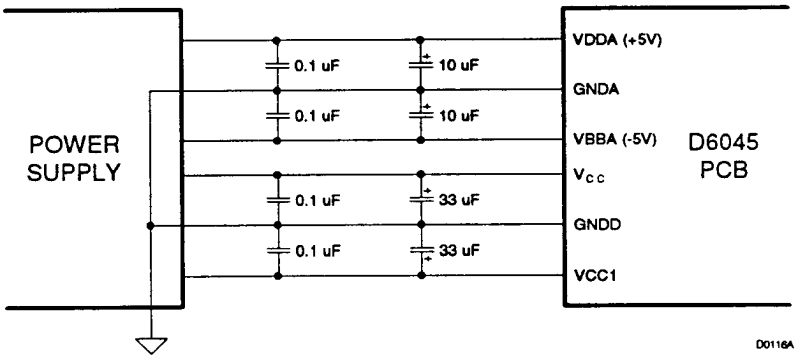


Figure 21. Power Supply

DSP GROUP, INC., 4050 MOORPARK AVE. SAN JOSE CA 95117
PH: 408-985-0722 FAX: 408-985-2108

ELECTRICAL CHARACTERISTICS

D6005A-11A (DSP)

Absolute maximum ratings over specified temperature range

Supply voltage range, V_{CC}	–0.3 V to 7 V
Input voltage range	–0.3 V to 7 V
Output voltage range	–0.3 V to 7 V
Continuous power dissipation	0.5 W
Operating free-air temperature range	0°C to 70°C
Storage temperature range	–55°C to 150°C

Recommended operating conditions

		MIN	TYP	MAX	UNIT
V_{CC} Supply voltage		4.75	5	5.25	V
V_{SS} Supply voltage			0		V
V_{IH} High-level input voltage	All inputs except CLKIN and RS	2			V
	CLKIN	3			V
V_{IL} Low-level input voltage	All inputs except RS			0.8	V
V_{T+} Positive-going $\overline{RS}$ threshold voltage		1.8			V
V_{T-} Negative-going $\overline{RS}$ threshold voltage				1.3	V
I_{OH} High-level output current				–300	µA
I_{OL} Low-level output current				2	mA
T_A Operating free-air temperature		0		70	°C

Electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH} High-level output voltage		I_{OH} = MAX		2.4	3		V
		I_{OH} = 20 mA		V_{CC}–0.4			
V_{OL} Low-level output voltage		I_{OL} = MAX			0.3	0.5	V
I_{oz} Off-state output current		V_{CC} = MAX	V_O = 2.4 V			20	µA
			V_O = 0.4 V			–20	µA
I_I Input current		V_I = V_{SS} to V_{CC}	All inputs except CLKIN			±20	µA
			CLKIN			±50	µA
ICC Supply current		f = 22 MHz, V_{CC} = 5.5 V			42	54	mA
C_I Input capacitance	Data bus	f = 1 MHz, All other pins 0 V			25		pF
	All others				15		
C_O Output capacitance	Data bus	f = 1 MHz, All other pins 0 V			25		pF
	All others				10		

D0000-26 (Analog I/O interface)

Absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	–0.3 V to 15 V
Output voltage, V_O	–0.3 V to 15 V
Input voltage, V_I	–0.3 V to 15 V
Digital ground voltage	–0.3 V to 15 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	–65°C to 150°C

Recommended operating conditions

		MIN	TYP	MAX	UNIT
V_{CC} Supply voltage		4.75	5	5.25	V
V_{BB} Supply voltage		–4.75	–5	–5.25	V
V_{IH} High-level input voltage, all inputs except CLKSEL		2.2			V
V_{IL} Low-level input voltage, all inputs except CLKSEL				0.8	V
R_L Load resistance	At GSX	10			kΩ
	At PWRO+ and/or PWRO–	300			Ω
C_L Load capacitance	At GSX			50	pF
	At PWRO+ and/or PWRO–			100	
T_A Operating free-air temperature		0		70	°C

Electrical characteristics over recommended ranges of supply voltage and operating free-air temperature supply current, f_{DCLK} 2.048 MHz, outputs not loaded

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
I_{CC} Supply current from V_{CC}	Operating		7	9	mA
	Standby	FSX or FSR at V_{IL} after 300ms	0.5	1	
	Power-down	$\overline{PDN}$ V_{IL} after 10 mS	0.3	0.8	
I_{BB} Supply Current from V_{BB}	Operating		–7	–9	mA
	Standby	FSX or FSR at V_{IL} after 300ms	–0.5	–1	
	Power-down	$\overline{PDN}$ V_{IL} after 10 mS	–0.3	–0.8	
Power dissipation	Operating		70	90	mW
	Standby	FSX or FSR at V_{IL} after 300ms	5	10	
	Power-down	$\overline{PDN}$ V_{IL} after 10 mS	3	8	

Transmit amplifier input

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input current at ANLG IN+, ANLG IN –	V_I = –2.17 V to 2.17 V			±100	nA
Input offset voltage at ANLG IN+, ANLG IN –	V_I = –2.17 V to 2.17 V			±25	mV
Common-mode rejection at ANLG IN+, ANLG IN –	V_I = –2.17 V to 2.17 V	55			dB
Open-loop voltage amplification at GSX		5000			V/V
Open-loop unity-gain bandwidth at GSX			1		MHz
Input resistance at ANLG IN+, ANLG IN –		10			MΩ

Receive filter output

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output offset voltage PWRO+, PWRO – (single-ended)	Relative to ANLG GND		80		mV
Output resistance at PWRO+, PWRO –			1		Ω

D0000-29 (Analog I/O interface)

Absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	–0.3 V to 7 V
Output voltage, V_O	–0.3 V to 7 V
Input voltage, V_I	–0.3 V to 7 V
Digital ground voltage	–0.3 V to 7 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	–65°C to 150°C

Recommended operating conditions

		MIN	TYP	MAX	UNIT
V_{CC} Supply voltage		4.75	5	5.25	V
V_{BB} Supply voltage		–4.75	–5	–5.25	V
V_{IH} High-level input voltage, all inputs except CLKSEL		2.2			V
V_{IL} Low-level input voltage, all inputs except CLKSEL				0.6	V
R_L Load resistance	No change transmit	10			kΩ
	At VFR0 Receive	600			Ω
C_L Load capacitance	At GSX			50	pF
	At VFR0			500	
T_A Operating free-air temperature		0		70	°C

Electrical characteristics over recommended ranges of supply voltage and operating free-air temperature supply current, f_{DCLK} 2.048 MHz, outputs not loaded

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
I_{CC} Supply current from V_{CC}	Operating		6	9	mA
	Power-down		0.5	1.5	
I_{BB} Supply Current from V_{BB}	Operating		–6	–9	mA
	Power-down		–0.5	–1.5	
Power dissipation	Operating		60	90	mW
	Power-down		5	15	

Transmit amplifier input

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input current at ANLG IN+, ANLG IN –	V_I = –2.17 V to 2.17 V			±200	nA
Input offset voltage at ANLG IN+, ANLG IN –	V_I = –2.17 V to 2.17 V			±20	mV
Common-mode rejection at ANLG IN+, ANLG IN –	V_I = –2.17 V to 2.17 V	60			dB
Open-loop voltage amplification at GSX		5000			V/V
Open-loop unity-gain bandwidth at GSX			2		MHz
Input resistance at ANLG IN+, ANLG IN –		10			MΩ

Receive filter output

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output offset voltage PWRO+, PWRO – (single-ended)	Relative to ANLG GND	–200		200	mV
Output resistance at PWRO+, PWRO –			1		Ω

D0000-31 (1 Mbit ARAM)

Absolute maximum ratings over operating temperature range

Voltage range on any pin	–1 V to 7 V
Voltage range on V_{CC}	–1 V to 7 V
Short circuit output current	50 mA
Power dissipation	1 W
Operating free-air temperature range	0°C to 70°C
Storage temperature range	–65°C to 150°C

Recommended operating conditions

	MIN	TYP	MAX	UNIT
V_{CC} Supply voltage	4.75	5	5.25	V
V_{IH} High-level input voltage	2.4		5.25	V
V_{IL} Low-level input voltage	–1.0		0.8	V
T_A Operating free-air temperature range	0		70	°C

Electrical characteristics over full range of recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TYP	MAX	UNIT
V_{OH} High level output voltage	I_{OH} = –5 mA	2.4		V
V_{OL} Low-level output voltage	I_{OL} = 4.2 mA		0.4	V
I_I Input current (leakage)	V_I = 0 V to 6.5 V, V_{CC} = 5.25 V, all other pins = 0 V to V_{CC}		±20	µA
I_O Output current (leakage)	V_O = 0 V to V_{CC}, V_{CC} = 5.25 V, $\overline{CAS}$ high		±20	µA
I_{CC1} Read or write cycle current	Minimum cycle, V_{CC} = 5.25 V		55	mA
I_{CC2} Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V		5	mA
I_{CC3} Average refresh current	Minimum cycle, V_{CC} = 5.25 V $\overline{RAS}$ cycling, $\overline{CAS}$ high		50	mA
I_{CC4} Average page (word) current	$t_{C(P)}$ = minimum, V_{CC} = 5.25 V $\overline{RAS}$ low, $\overline{CAS}$ cycling		30	mA

D0000-34A (4 Mbit ARAM)

Absolute maximum ratings over operating temperature range

Voltage range on any pin	–1 V to 5.50 V
Voltage range on V_{CC}	–1 V to 5.50 V
Short circuit output current	50 mA
Power dissipation	1 W
Operating free-air temperature range	0°C to 70°C
Storage temperature range	–55°C to 150°C

Recommended operating conditions

	MIN	TYP	MAX	UNIT
V_{CC} Supply voltage	4.75	5	5.25	V
V_{IH} High-level input voltage	2.4		5.25	V
V_{IL} Low-level input voltage	–0.5		0.4	V
V_{OH} High-level output voltage	2.4			V
V_{OL} Low-level output voltage			0.4	V
T_A Operating free-air temperature range	0		70	°C

Electrical characteristics over full range of recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TYP	MAX	UNIT
V_{OH} High level output voltage	I_{OH} = –mA	2.4		V
V_{OL} Low-level output voltage	I_{OL} = 3.0 mA		0.4	V
I_I Input current (leakage)	V_I = 0 V to 5.5 V, V_{CC} = 5.25 V, all other pins = 0 V to V_{CC}		±20	µA
I_O Output current (leakage)	V_O = 0 V to V_{CC}, V_{CC} = 5.25 V, $\overline{CAS}$ high		±20	µA
I_{CC1} Read or write cycle current	Minimum cycle, V_{CC} = 5.25 V		80	mA
I_{CC2} Standby cycle	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.2 V		5	mA
I_{CC3} Average refresh current	Minimum cycle, V_{CC} = 5.25 V $\overline{RAS}$ cycling, $\overline{CAS}$ high		70	mA
I_{CC4} Average page (word) current	$t_{C(P)}$ = minimum, V_{CC} = 5.25 V $\overline{RAS}$ low, $\overline{CAS}$ cycling		35	mA

DSP GROUP, INC., 4050 MOORPARK AVE. SAN JOSE CA 95117
PH: 408-985-0722 FAX: 408-985-2108

D6005A-71B (ASIC)

Absolute maximum ratings over specified temperature range

Supply voltage range, V_{CC}	–0.3 V to 7 V
Input voltage range	–0.3 V to 7 V
Output voltage range	–0.3 V to 7 V
Continuous power dissipation	0.5 W
Operating free-air temperature range	0°C to 70°C
Storage temperature range	–55°C to 150°C

Recommended operating conditions—GENERAL DATA

	MIN	TYP	MAX	UNIT
V_{CC} Supply voltage	4.5	5	5.5	V
I_{CC} Supply current		4		mA
V_{IH} High-level input voltage	2			V
V_{IL} Low-level input voltage			0.8	V
T_A Operating temperature range	0		70	°C

Electrical characteristics over recommended ranges of supply voltage and operating temperature

ADDR 0–11					
PARAMETER	**TEST CONDITIONS**	**MIN**	**TYP***	**MAX**	**UNIT**
V_{OH} High-level output voltage	I_{OH} = –8 mA	3.7			V
	I_{OH} = –20 mA		V_{CC}–0.1		
V_{OL} Low-level output voltage	I_{OL} = 8 mA		0.2	0.4	V
	I_{OL} = 20 mA		0.05	0.1	
$\overline{ACK}$, ADDR 12–15					
V_{OH} High-level output voltage	I_{OH} = –4 mA	3.7			V
	I_{OH} = –20 mA	V_{CC}–0.1			
V_{OL} Low-level output voltage	I_{OL} = 4 mA		0.2	0.5	V
	I_{OL} = 20 mA		0.05	0.1	
HSTDB0-7, DB8-DB15					
PARAMETER	**TEST CONDITIONS**	**MIN**	**TYP***	**MAX**	**UNIT**
V_T Input threshold voltage			2.5		V
V_{OH} High-level output voltage	I_{OH} = –4 mA	3.7			V
	I_{OH} = –20 mA	V_{CC}–0.1			
V_{OL} Low-level output voltage	I_{OL} = 4 mA			0.5	V
	I_{OL} = 20 mA			0.1	V
I_{OZ} Off-state output current	$V_O = V_{CC}$			±10	µA
	V_O = 0		–70		µA
$\overline{HSTRD}$, $\overline{HSTWR}$, HI/LO					
V_T Input threshold voltage			2.5		V
I_I Input current	$V_I = V_{CC}$			±1	µA
	V_I = 0		–70		
$\overline{RESET}$					
V_{T+} Positive-going threshold level			3.35	3.85	V
V_{T-} Negative-going threshold level		0.9	1.65		V

*Typical values are at V_{CC} = 5 V, T_A = 25°C.

DTMF & VOX Characteristics

PARAMETER	MIN	TYP	MAX	UNIT
DTMF Signal level for detection *	-35		0	dB
DTMF Twist (High/Low Tone)			6	dB
DTMF Frequency Detect Band width	±(1.5% + 2Hz)		4.1%	%fc
DTMF Noise tolerance**			-12	dB
DTMF signal duration for detection	20		40	ms
VOX detection***	-30		0	dB
Tone generator frequency accuracy			±1%	
Tone generator level accuracy			±1	dB

*1V RMS is defined as 0 dB

**BW limited (0–3.4KHz) Gaussian noise

*** 1.4V RMS is defined as 0 dB

CALL PROGRESS TONE DETECTOR PERFORMANCE

Narrow band detection level: minimum -35dB
Narrow band rejection level: less than -40dB
Narrow band rejection frequency range: less than 250Hz or greater than 600Hz
Narrow band detection frequency range: between 330Hz and 500Hz
Wide band detection level: minimum -35dB
Wide band rejection level: less than -40dB
Wide band rejection frequency range: less than 250Hz or greater than 750Hz
Wide band detection frequency range: between 335Hz and 650Hz

DSP GROUP, INC., 4050 MOORPARK AVE. SAN JOSE CA 95117
PH: 408-985-0722 FAX: 408-985-2108

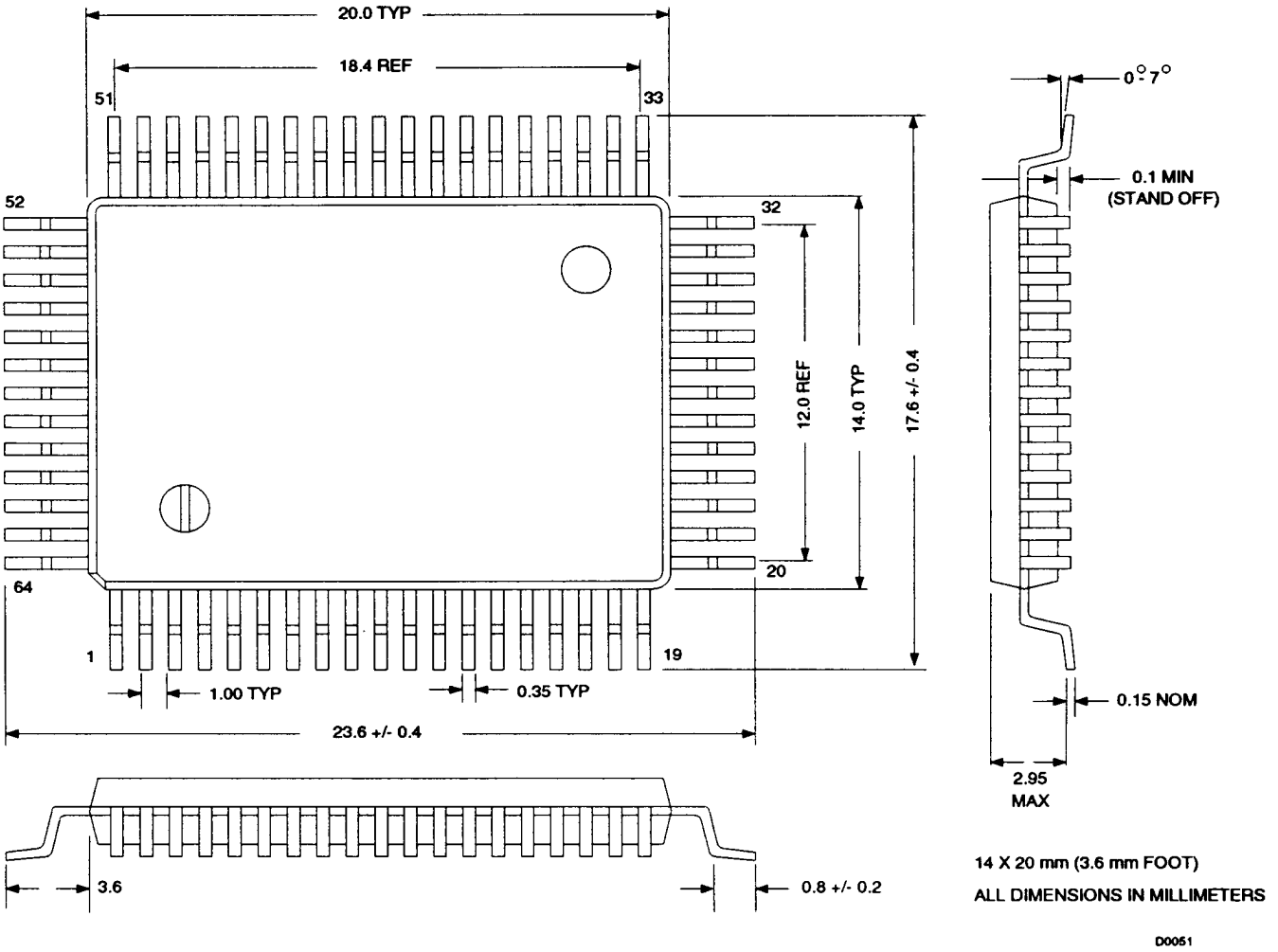


Figure 22. D6005A-11A Mechanical Data

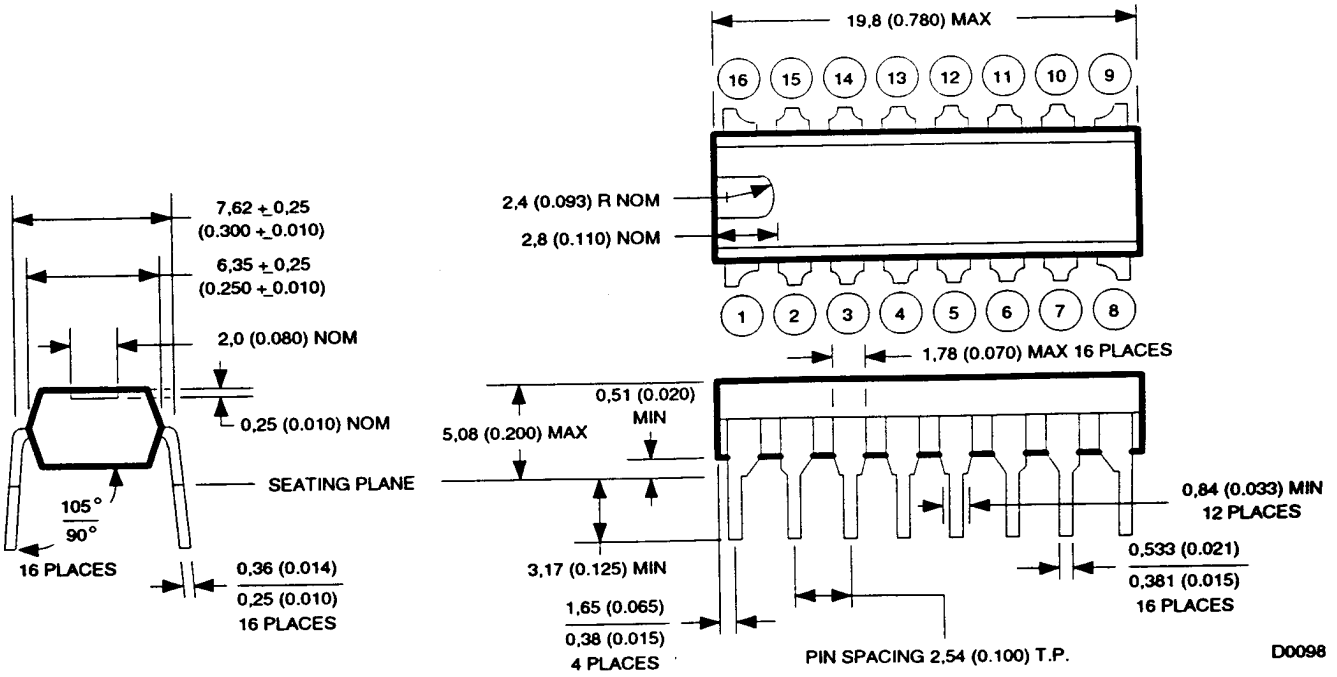


Figure 23. D0000-26 Codec Mechanical Data

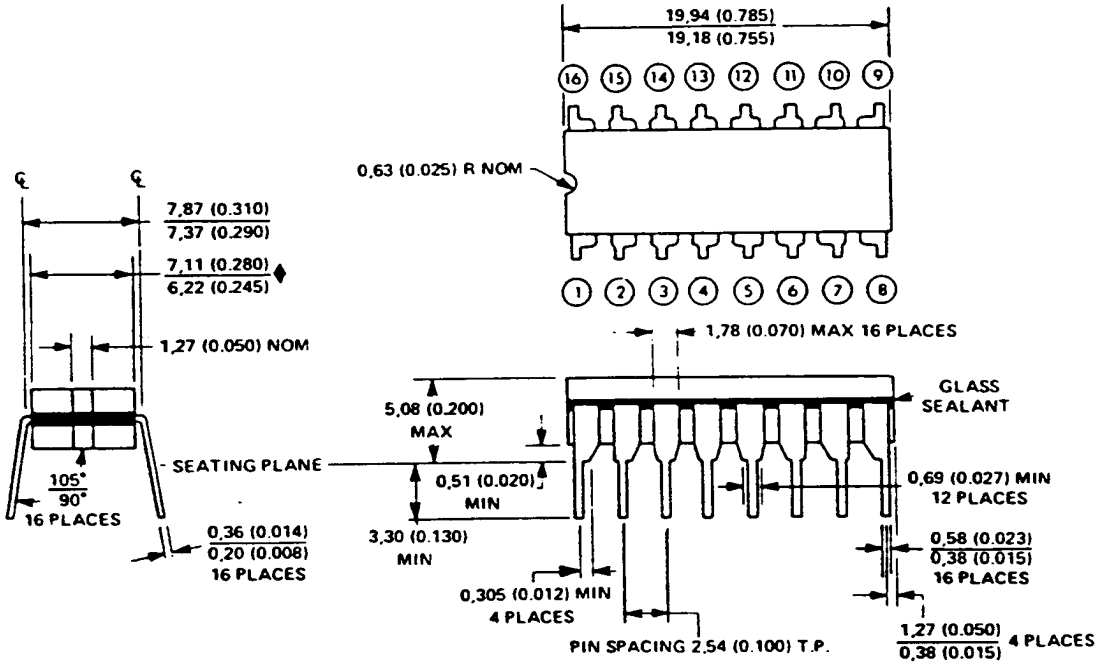


Figure 24. D0000-29 Codec Mechanical Data

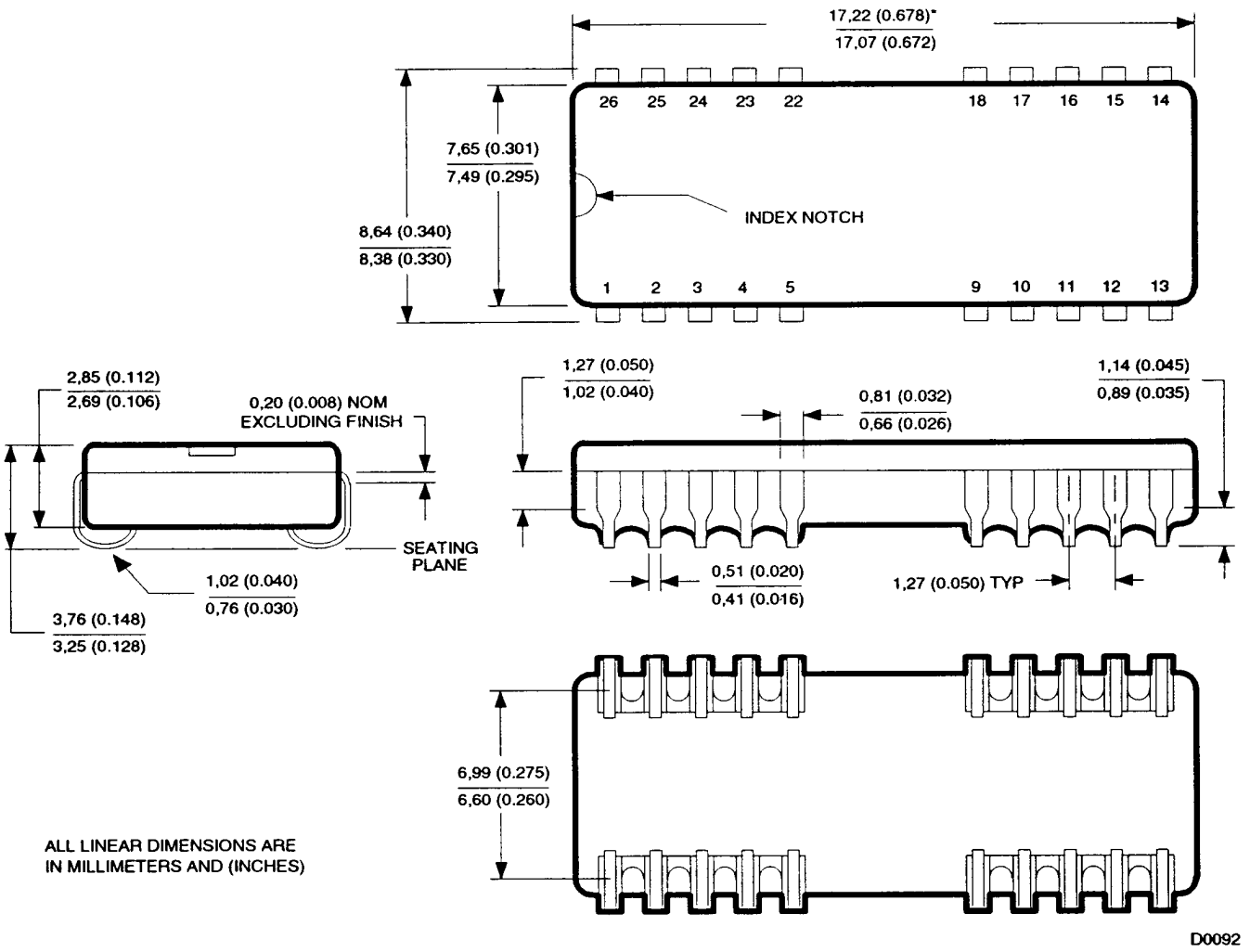


Figure 25 D0000-31 or -34 ARAM SOJ Mechanical Data

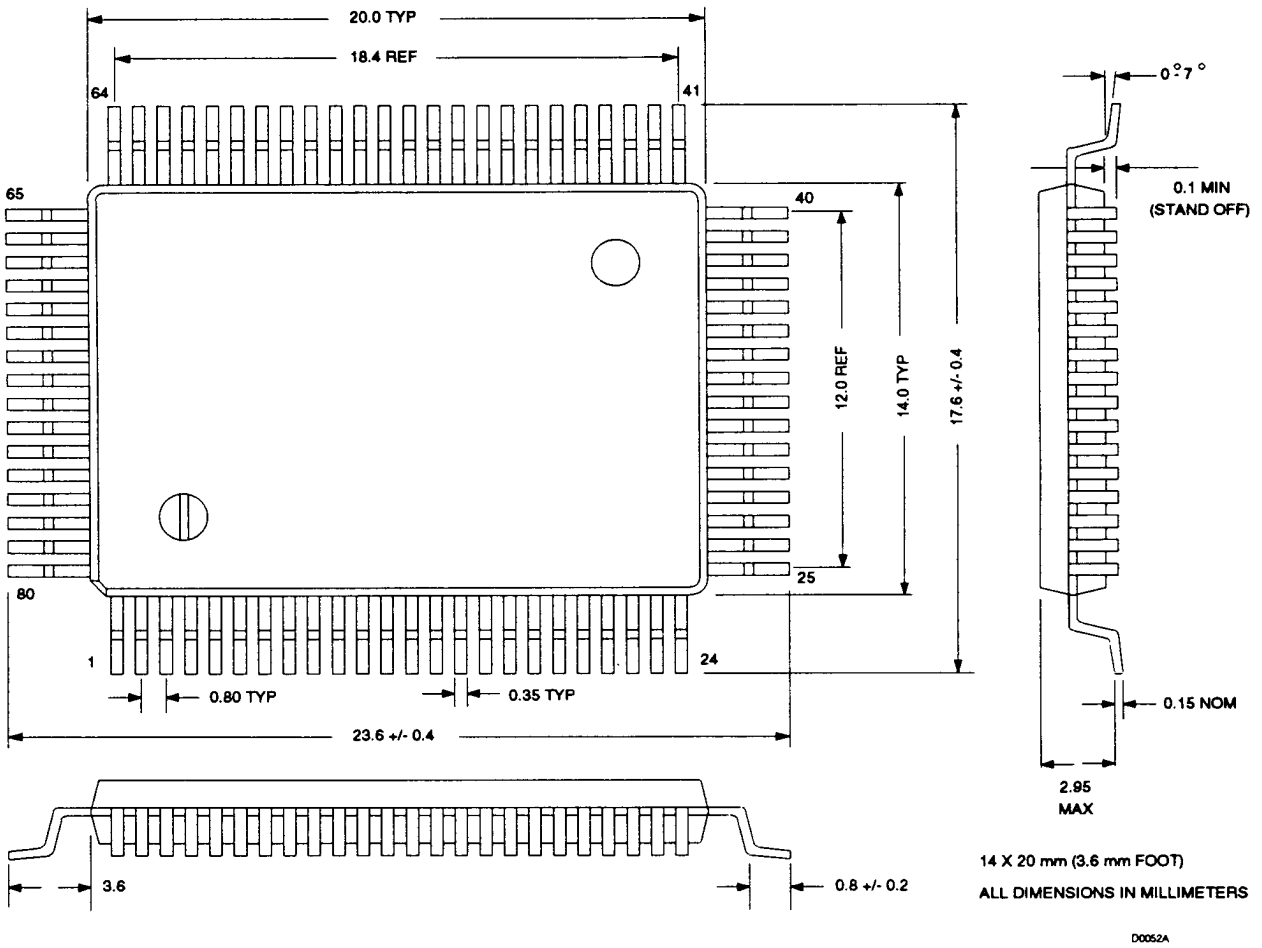


Figure 26. D6005A-71B ASIC Mechanical Data

DSP GROUP, INC.

4050 Moorpark Avenue
San Jose, CA 95117
Telephone: (408) 985-0722
Facsimile: (408) 985-2108

JAPAN OFFICE

Nihon DSP Group, K.K.
Gotanda Alpha Building - 9th Floor
29-9-2 Chome Nishi Gotanda
Shinagawa-ku, Tokyo 141 Japan
Telephone: (81) 3-5496-1611
Facsimile: (81) 3-5496-1615

ASIA PACIFIC TECHNICAL SUPPORT CENTER

A19, 10th Floor
Proficient Ind. Center
6, Wang Kwun Road
Kowloon, Hong Kong
Telephone: (852) 753-6736
Facsimile: (852) 795-7839

EUROPEAN OFFICE

DSP Group, Inc.
11, Ben Gurion Street
Givat Shmuel 51905, Israel
Telephone: (972) 3-713300
Facsimile: (972) 3-713303