2.5 V 184-pin Unbuffered DDR-I SDRAM Modules

256 MByte & 512 MByte Modules
PC1600 & PC2100

- 184-pin Unbuffered 8-Byte Dual-In-Line DDR-I SDRAM non-parity and ECC-Modules for PC and Server main memory applications
- One bank 32M × 64, 32M x 72 and two bank 64M x 64, 64M × 72 organization
- JEDEC standard Double Data Rate Synchronous DRAMs (DDR-I SDRAM) Single + 2.5 V (± 0.2 V) power supply
- Built with 256 Mbit DDR-I SDRAMs organised as 32Mb x 8 in 66-Lead TSOPII package
- Programmable $\overline{\text{CAS}}$ Latency, Burst Length, and Wrap Sequence (Sequential & Interleave)
- Auto Refresh (CBR) and Self Refresh
- All inputs and outputs SSTL_2 compatible
- Serial Presence Detect with E^2PROM
- Jedec standard MO-206 form factor: 133.35 mm × 31.75 mm × 4.00 mm max.
- Jedec standard reference layout
- Gold plated contacts

- Performance:

		-7	-8	Unit
	Component Speed Grade	DDR266A	DDR200	
	Module Speed Grade	PC2100	PC1600	
f_{CK}	Clock Frequency (max.) @ CL = 2.5	143	125	MHz
f_{CK}	Clock Frequency (max.) @ CL = 2	133	100	MHz

The HYS64/72D32000GU and HYS64/72D64020GU are industry standard 184-pin 8-byte Dual in-line Memory Modules (DIMMs) organized as 32M × 64 and 64M × 64 for non-parity and 32M x 72 and 64M x 72 for ECC main memory applications. The memory array is designed with 256Mbit Double Data Rate Synchronous DRAMs. A variety of decoupling capacitors are mounted on the PC board. The DIMMs feature serial presence detect based on a serial E^2PROM device using the 2-pin I^2C protocol. The first 128 bytes are programmed with configuration data and the second 128 bytes are available to the customer.

Ordering Information

Type	Compliance Code	Description	SDRAM Technology
PC2100 (CL=2):			
HYS64D32000GU-7-A	PC2100-20330-B1	one bank 256 MB DIMM	256 MBit
HYS64D32000GU-7-B	PC2100-20330-A1	one bank 256 MB DIMM	256 MBit
HYS72D32000GU-7-A	PC2100-20330-B1	one bank 256 MB ECC-DIMM	256 Mbit
HYS72D32000GU-7-B	PC2100-20330-A1	one bank 256 MB ECC-DIMM	256 Mbit
HYS64D64020GU-7-A HYS64D64020GU-7-B	PC2100-20330-B1	two banks 512 MB DIMM	256 MBit
HYS72D64020GU-7-A HYS72D64020GU-7-B	PC2100-20330-B1	two banks 512 MB ECC-DIMM	256 MBit
PC1600 (CL=2):			
HYS64D32000GU-8-A	PC1600-20220-B1	one bank 256 MB DIMM	256 MBit
HYS64D32000GU-8-B	PC1600-20220-A1	one bank 256 MB DIMM	256 MBit
HYS72D32000GU-8-A	PC1600-20220-B1	one bank 256 MB ECC-DIMM	256 Mbit
HYS72D32000GU-8-B	PC1600-20220-A1	one bank 256 MB ECC-DIMM	256 Mbit
HYS64D64020GU-8-A HYS64D64020GU-8-B	PC1600-20220-B1	two banks 512 MB DIMM	256 MBit
HYS72D64020GU-8-A HYS72D64020GU-8-B	PC1600-20220-B1	two banks 512 MB ECC-DIMM	256 MBit

Note: All part numbers end with a place code, designating the silicon-die revision. Reference information available on request. Example: HYS 72D32000GU-8-A, indicating Rev.A dies are used for the SDRAM components.
The Compliance Code is printed on the module labels and describes the speed sort fe. “PC2100”, the latencies (f.e. “20330” means CAS latency = 2, trcd latency = 3 and trp latency =3) and the Raw Card used for this module.

Pin Definitions and Functions

A0 - A12	Address Inputs	$\overline{S0}$, $\overline{S1}$	Chip Selects
BA0, BA1	Bank Selects	V_{DD}	Power (+ 2.5 V)
DQ0 - DQ63	Data Input/Output	V_{SS}	Ground
CB0 - CB7	Check Bits (x72 organization only)	V_{DDQ}	I/O Driver power supply
$\overline{RAS}$	Row Address Strobe	V_{DDID}	VDD Indentification flag
$\overline{CAS}$	Column Address Strobe	V_{REF}	I/O reference supply
$\overline{WE}$	Read/Write Input	V_{DDSPD}	Serial EEPROM power supply
CKE0 - CKE1	Clock Enable	SCL	Serial bus clock
DQS0 - DQS8	SDRAM low data strobes	SDA	Serial bus data line
CLK0 - CLK2,	SDRAM clock (positive lines)	SA0 - SA2	slave address select
$\overline{CLK0}$ - $\overline{CLK2}$	SDRAM clock (negative lines)	NC	no connect
DM0 - DM8 DQS9 - DQS17	SDRAM low data mask/ high data strobes		

note: $\overline{S1}$ and CKE1 are used on two bank modules only

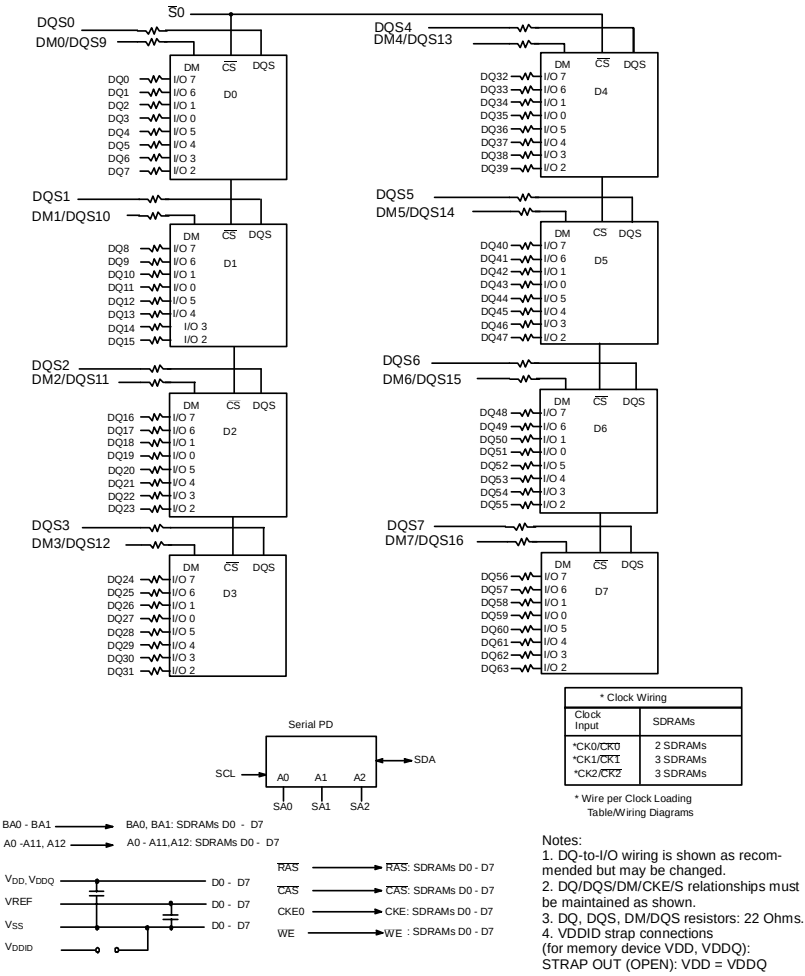
Address Format

Density	Organization	Memory Banks	SDRAMs	# of SDRAMs	# of row/bank/ columns bits	Refresh	Period	Interval
256 MB	32M x 64	1	32M x 8	8	13/2/10	8k	64 ms	7.8 µs
256 MB	32M x 72	1	32M x 8	9	13/2/10	8k	64 ms	7.8 µs
512 MB	64M × 64	2	32M x 8	16	13/2/10	8k	64 ms	7.8 µs
512 MB	64M × 72	2	32M x 8	18	13/2/10	8k	64 ms	7.8 µs

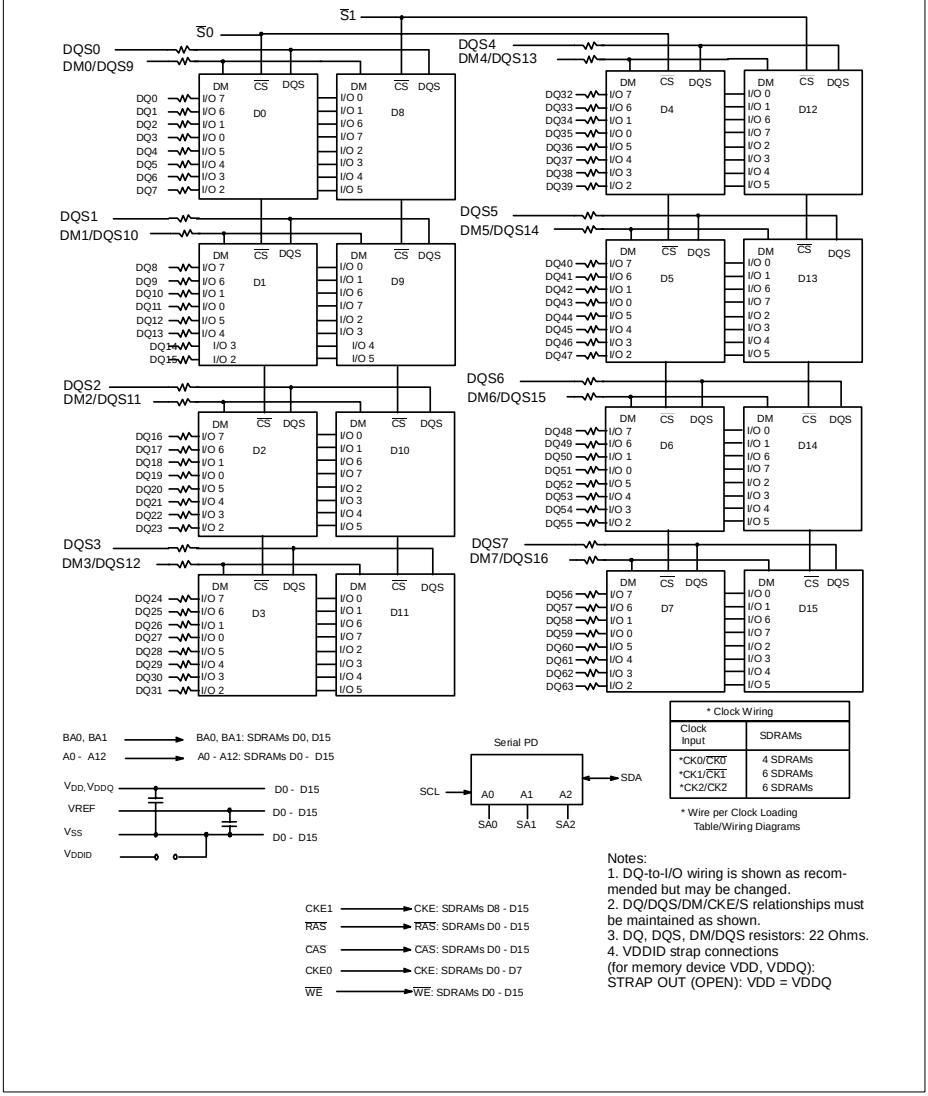
Pin Configuration

Frontside		Frontside		Backside		Backside	
PIN#	Symbol	PIN#	Symbol	PIN#	Symbol	PIN#	Symbol
1	VREF	48	A0	93	VSS	140	NC / DM8/DQS17
2	DQ0	49	NC / CB2	94	DQ4	141	A10
3	VSS	50	VSS	95	DQ5	142	NC / CB6
4	DQ1	51	NC / CB3	96	VDDQ	143	VDDQ
5	DQS0	52	BA1	97	DM0/DQS9	144	NC / CB7
6	DQ2	KEY		98	DQ6	KEY	
7	VDD	53	DQ32	99	DQ7	145	VSS
8	DQ3	54	VDDQ	100	VSS	146	DQ36
9	NC	55	DQ33	101	NC	147	DQ37
10	NC	56	DQS4	102	NC	148	VDD
11	VSS	57	DQ34	103	NC	149	DM4/DQS13
12	DQ8	58	VSS	104	VDDQ	150	DQ38
13	DQ9	59	BA0	105	DQ12	151	DQ39
14	DQS1	60	DQ35	106	DQ13	152	VSS
15	VDDQ	61	DQ40	107	DM1/DQS10	153	DQ44
16	CLK1	62	VDDQ	108	VDD	154	$\overline{RAS}$
17	$\overline{CLK1}$	63	$\overline{WE}$	109	DQ14	155	DQ45
18	VSS	64	DQ41	110	DQ15	156	VDDQ
19	DQ10	65	$\overline{CAS}$	111	CKE1	157	$\overline{S0}$
20	DQ11	66	VSS	112	VDDQ	158	$\overline{S1}$
21	CKE0	67	DQS5	113	NC (BA2)	159	DM5/DQS14
22	VDDQ	68	DQ42	114	DQ20	160	VSS
23	DQ16	69	DQ43	115	NC / A12	161	DQ46
24	DQ17	70	VDD	116	VSS	162	DQ47
25	DQS2	71	NC	117	DQ21	163	NC
26	VSS	72	DQ48	118	A11	164	VDDQ
27	A9	73	DQ49	119	DM2/DQS11	165	DQ52
28	DQ18	74	VSS	120	VDD	166	DQ53
29	A7	75	$\overline{CLK2}$	121	DQ22	167	NC (A13)
30	VDDQ	76	CLK2	122	A8	168	VDD
31	DQ19	77	VDDQ	123	DQ23	169	DM6/DQS15
32	A5	78	DQS6	124	VSS	170	DQ54
33	DQ24	79	DQ50	125	A6	171	DQ55
34	VSS	80	DQ51	126	DQ28	172	VDDQ
35	DQ25	81	VSS	127	DQ29	173	NC
36	DQS3	82	VDDID	128	VDDQ	174	DQ60
37	A4	83	DQ56	129	DM3/DQS12	175	DQ61
38	VDD	84	DQ57	130	A3	176	VSS
39	DQ26	85	VDD	131	DQ30	177	DM7/DQS16
40	DQ27	86	DQS7	132	VSS	178	DQ62
41	A2	87	DQ58	133	DQ31	179	DQ63
42	VSS	88	DQ59	134	NC / CB4	180	VDDQ
43	A1	89	VSS	135	NC / CB5	181	SA0
44	NC / CB0	90	NC	136	VDDQ	182	SA1
45	NC / CB1	91	SDA	137	CK0	183	SA2
46	VDD	92	SCL	138	$\overline{CK0}$	184	VDDSPD
47	NC / DQS8			139	VSS		

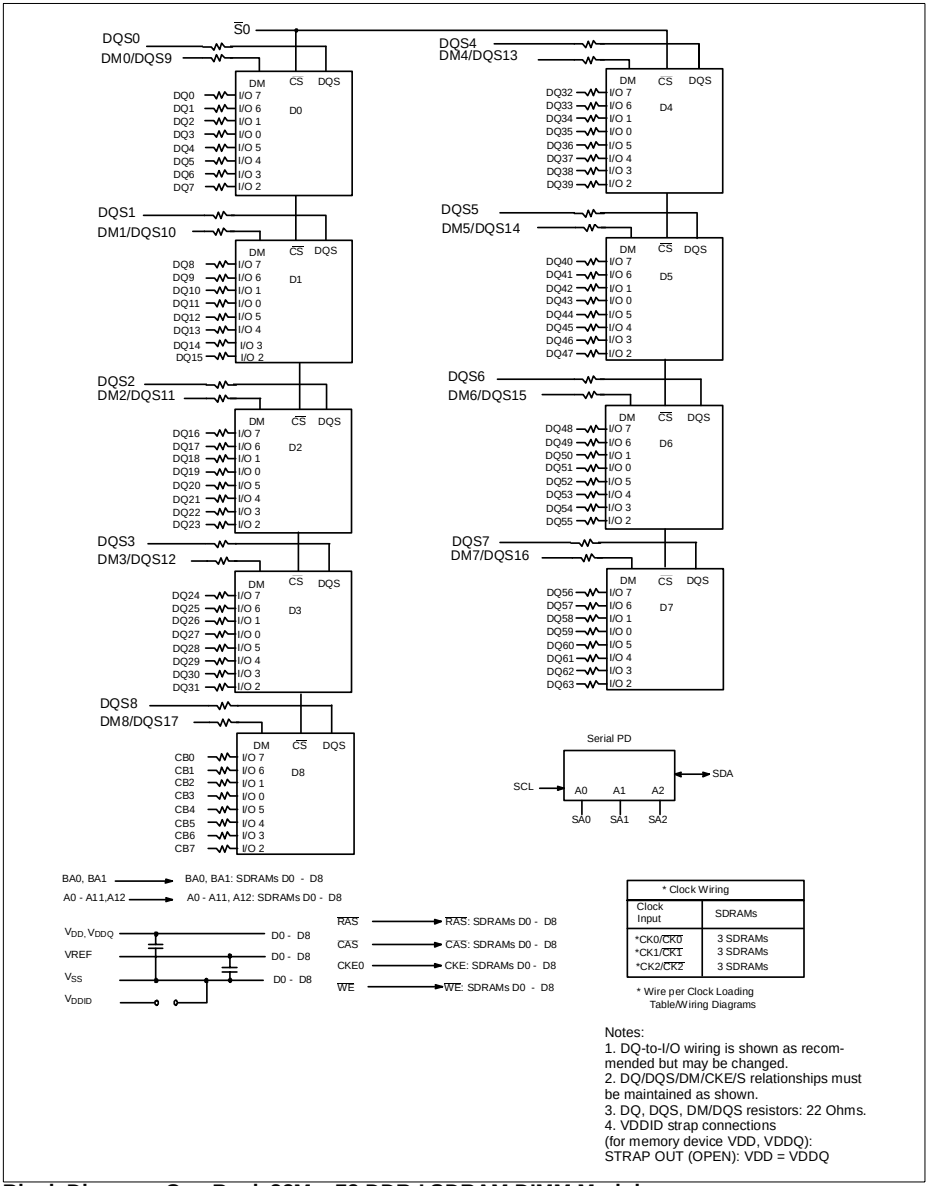
Note: Pins 44, 45, 47, 49, 51, 134, 135, 140 and 144 are NC (“no-connects”) on x64 organised non-ECC modules. A12 is used for 256Mbit based modules only



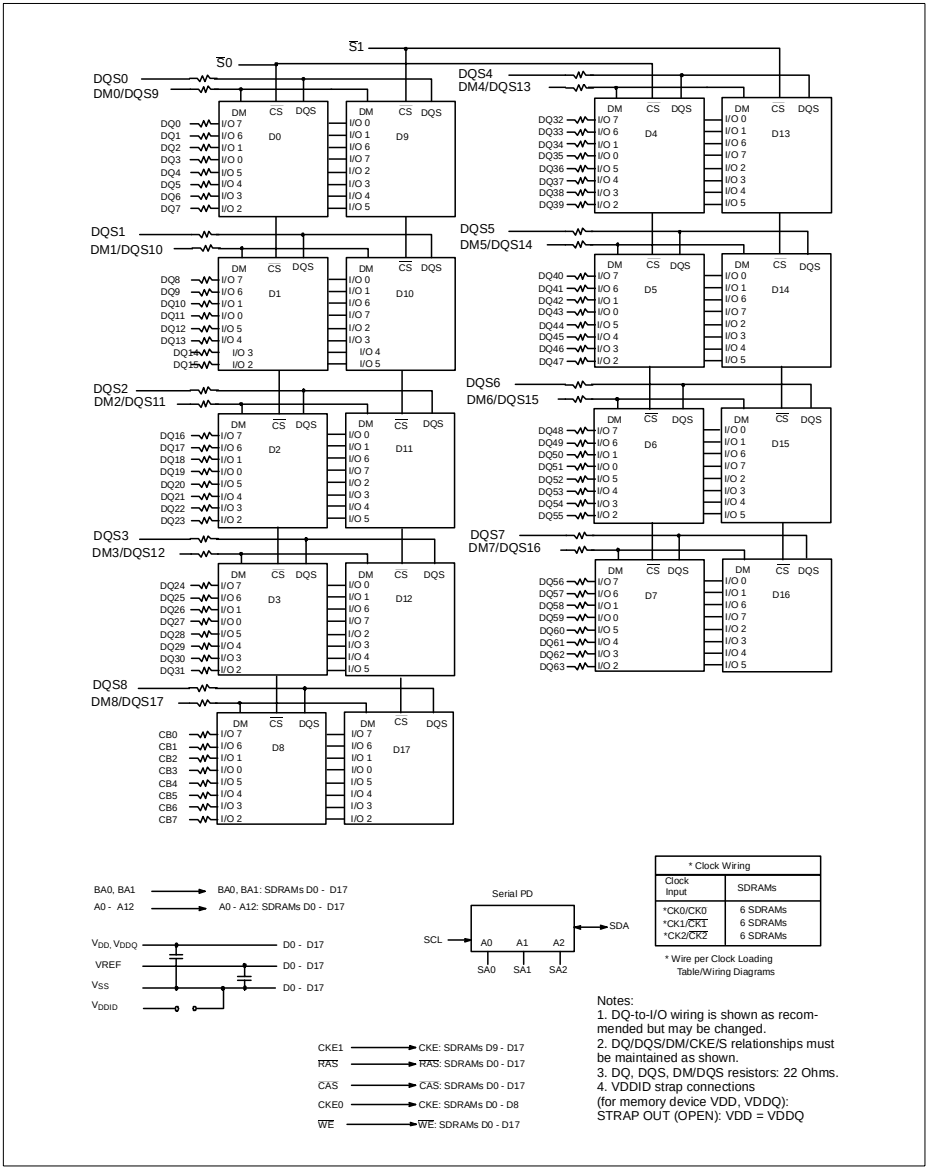
Block Diagram: One Bank 32M x 64 DDR-I SDRAM DIMM Module HYS64D32000GU using x8 organized SDRAMs



Block Diagram: Two Bank 64M x 64 DDR-I SDRAM DIMM Modules
HYS64D64020GU using x8 Organized SDRAMs

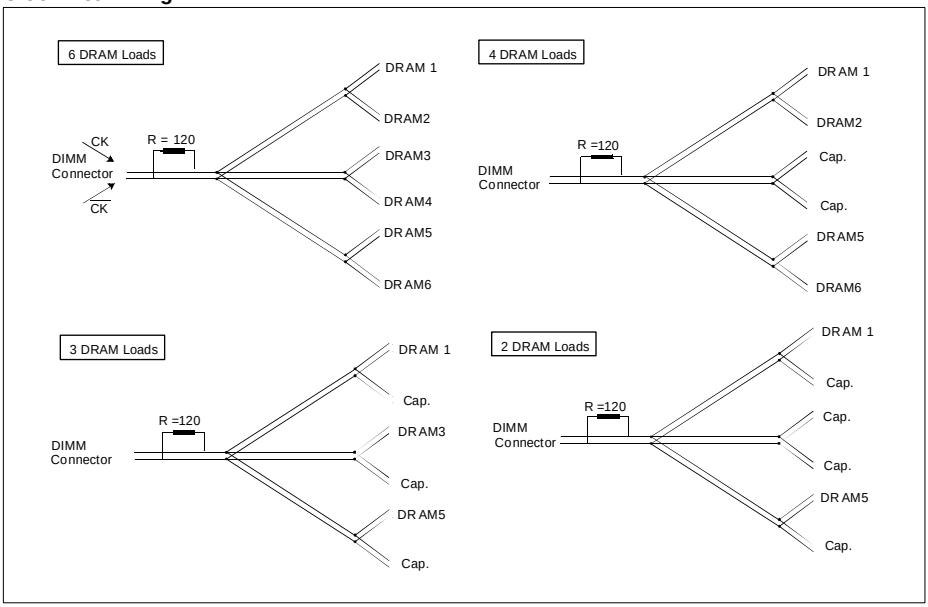


Block Diagram: One Bank 32M x 72 DDR-I SDRAM DIMM Module
HYS72D32000GU using x8 organized SDRAMs



Block Diagram: Two Bank 64M x 72 DDR-I SDRAM DIMM Modules
HYS72D64020GU using x8 Organized SDRAMs

Clock Net Wiring



Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input / Output voltage relative to V_{SS}	V_{IN}, V_{OUT}	– 0.5	3.6	V
Power supply voltage on V_{DD}/V_{DDQ} to V_{SS}	V_{DD}, V_{DDQ}	– 0.5	3.6	V
Storage temperature range	T_{STG}	-55	+150	°C
Power dissipation (per SDRAM component)	P_D	–	1	W
Data out current (short circuit)	I_{OS}	–	50	mA

Permanent device damage may occur if “Absolute Maximum Ratings” are exceeded.
Functional operation should be restricted to recommended operation conditions.
Exposure to higher than recommended voltage for extended periods of time affect device reliability

Supply Voltage Levels

Parameter	Symbol	Limit Values			Unit	Notes
		min.	nom.	max.		
Device Supply Voltage	V_{DD}	2.3	2.5	2.7	V	–
Output Supply Voltage	V_{DDQ}	2.3	2.5	2.7	V	1)
Input Reference Voltage	V_{REF}	0.49 x V_{DDQ}	0.5 x V_{DDQ}	0.51 x V_{DDQ}	V	2)
Termination Voltage	V_{TT}	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V	3)
EEPROM supply voltage	V_{DDSPD}	2.3	2.5	3.6	V	

1) Under all conditions, V_{DDQ} must be less than or equal to V_{DD}.

2) Peak to peak AC noise on V_{REF} may not exceed ± 2% $V_{REF\ (DC)}$. V_{REF} is also expected to track noise variations in V_{DDQ}.

3) V_{TT} of the transmitting device must track V_{REF} of the receiving device.

DC Operating Conditions (SSTL_2 Inputs)

(V_{DDQ} = 2.5 V, T_A = 70 °C, Voltage Referenced to V_{SS})

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
DC Input Logic High	$V_{IH\ (DC)}$	V_{REF} + 0.15	V_{DDQ} + 0.3	V	1)
DC Input Logic Low	$V_{IL\ (DC)}$	– 0.30	V_{REF} – 0.15	V	–
Input Leakage Current	I_{IL}	– 5	5	µA	2)
Output Leakage Current	I_{OL}	– 5	5	µA	2)

1) The relationship between the V_{DDQ} of the driving device and the V_{REF} of the receiving device is what determines noise margins. However, in the case of $V_{IH\ (max)}$ (input overdrive), it is the V_{DDQ} of the receiving device that is referenced. In the case where a device is implemented such that it supports SSTL_2 inputs but has no SSTL_2 outputs (such as a translator), and therefore no V_{DDQ} supply voltage connection, inputs must tolerate input overdrive to 3.0 V (High corner V_{DDQ} + 300 mV).

2) For any pin under test input of 0 V ≤ V_{IN} ≤ V_{DDQ} + 0.3 V. Values are shown per DDR-SDRAM component-

Operating, Standby and Refresh Currents (PC1600)

Symbol	Parameter/Condition	HYS64D32000GU-8-A	HYS72D32000GU-8-A	HYS64D64020GU-8-A	HYS72D64020GU-8-A	Unit	Notes
	DRAM Technology:	256Mbit					
		typ.	typ.	typ.	typ.		
I_{DD0}	**Operating Current - One bank Active - Precharge**; $t_{RC} = t_{RC\ MIN}$; t_{CK} = 10 ns; DQ, DM, and DQS inputs changing once per clock cycle; address and control inputs changing once per every two cycles	592	666	944	1062	mA	1,3
I_{DD1}	**Operating Current - One bank Active / Read / Precharge**; Burst = 4; Reads; Refer to the detailed test conditions in the component datasheet	568	639	920	1035	mA	1,3
I_{DD2P}	**Precharge Power-Down Standby Current**: all banks idle; power-down mode; CKE ≤ $V_{IL\ MAX}$; t_{CK} = 10 ns	88	99	176	198	mA	1,4
I_{DD2F}	**Precharge Floating Standby Current**: $\overline{CS} \geq V_{IH\ MIN}$, all banks idle; CKE ≥ $V_{IH\ MIN}$; t_{CK} = 10 ns, address and other control inputs changing once per clock cycle, $V_{IN} = V_{REF}$ for DQ, DQS and DM.	200	225	400	450	mA	1,4
I_{DD2Q}	**Precharge Quiet Standby Current**: $\overline{CS} \geq V_{IH\ MIN}$, all banks idle; CKE ≥ $V_{IH\ MIN}$; t_{CK} = 10 ns,address and other control inputs stable at ≥ $V_{IH\ MIN}$ or ≤ $V_{IL\ MAX}$; $V_{IN} = V_{REF}$ for DQ, DQS and DM.	192	216	383	432	mA	1,4
I_{DD3P}	**Active Power-Down Standby Current**: one bank active; power-down mode; CKE ≤ $V_{IL\ MAX}$; t_{CK} = 10 ns	88	99	176	198	mA	1,4
I_{DD3N}	**Active Standby Current**: one bank; active / precharge; $\overline{CS} \geq V_{IH\ MIN}$; CKE ≥ $V_{IH\ MIN}$; $t_{RC} = t_{RAS\ MAX}$; t_{CK} = 10 ns; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	352	396	704	792	mA	1,4
I_{DD4R}	**Operating Current - Burst Read:** one bank; Burst = 2; reads; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS outputs changing twice per clock cycle; CL = 2; t_{CK} = 10 ns; I_{OUT} = 0mA	872	981	1224	1377	mA	1,3
I_{DD4W}	**Operating Current - Burst Write:** one bank; Burst = 2; writes; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS inputs changing twice per clock cycle; CL = 2; t_{CK} = 10 ns	872	981	1224	1377	mA	1,3
I_{DD5}	**Auto-Refresh Current**: $t_{RC} = t_{RFC\ MIN}$, distributed refresh	984	1107	1968	2214	mA	1,4
I_{DD6}	**Self-Refresh Current**: CKE ≤ 0.2V	15.2	17.1	30.4	34.2	mA	1,2,4
I_{DD7}	**Operating Current - Four bank operation**; four bank interleaving with BL=4; Refer to the detailed test conditions in the component datasheet	1456	1638	1808	2034	mA	1,3

1. I_{DD} currents are measured after the device is properly initialized. Typical values are obtained from characterisation data measured at VDD = 2.5 V and R.T. with an input slew rate = 1V/ns.
2. Enables on-chip refresh and address counters.
3. For two bank modules only : the other bank is in IDD3N mode
4. For two bank modules only : both banks operate in the same current mode

Operating, Standby and Refresh Currents (PC2100)

Symbol	Parameter/Condition	HYS64D32000GU-7-A	HYS72D32000GU-7-A	HYS64D64020GU-7-A	HYS72D64020GU-7-A	Unit	Notes
	DRAM Technology:	256Mbit					
		typ.	typ.	typ.	typ.		
I_{DD0}	**Operating Current - One bank Active - Precharge**; $t_{RC} = t_{RC\ MIN}$; t_{CK} = 7.5 ns; DQ, DM, and DQS inputs changing once per clock cycle; address and control inputs changing once per every two cycles	680	765	1104	1242	mA	1,3
I_{DD1}	**Operating Current - One bank Active / Read / Precharge**; Burst = 4; Reads; Refer to the detailed test conditions in the component datasheet	704	792	1128	1269	mA	1,3
I_{DD2P}	**Precharge Power-Down Standby Current**: all banks idle; power-down mode; CKE ≤ $V_{IL\ MAX}$; t_{CK} = 7.5 ns	104	117	208	234	mA	1,4
I_{DD2F}	**Precharge Floating Standby Current**: $\overline{CS}$ ≥ $V_{IH\ MIN}$, all banks idle; CKE ≥ $V_{IH\ MIN}$; t_{CK} = 7.5 ns, address and other control inputs changing once per clock cycle, $V_{IN} = V_{REF}$ for DQ, DQS and DM.	232	261	464	522	mA	1,4
I_{DD2Q}	**Precharge Quiet Standby Current**: $\overline{CS}$ ≥ $V_{IH\ MIN}$, all banks idle; CKE ≥ $V_{IH\ MIN}$; t_{CK} = 7.5 ns,address and other control inputs stable at ≥ $V_{IH\ MIN}$ or ≤ $V_{IL\ MAX}$; $V_{IN} = V_{REF}$ for DQ, DQS and DM.	216	243	432	486	mA	1,4
I_{DD3P}	**Active Power-Down Standby Current**: one bank active; power-down mode; CKE ≤ $V_{IL\ MAX}$; t_{CK} = 7.5 ns	104	117	208	234	mA	1,4
I_{DD3N}	**Active Standby Current**: one bank; active / precharge; $\overline{CS}$ ≥ $V_{IH\ MIN}$; CKE ≥ $V_{IH\ MIN}$; $t_{RC} = t_{RAS\ MAX}$; t_{CK} = 7.5 ns; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	424	477	848	954	mA	1,4
I_{DD4R}	**Operating Current - Burst Read:** one bank; Burst = 2; reads; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS outputs changing twice per clock cycle; CL = 2; t_{CK} = 7.5 ns; I_{OUT} = 0mA	1088	1224	1512	1701	mA	1,3
I_{DD4W}	**Operating Current - Burst Write:** one bank; Burst = 2; writes; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS inputs changing twice per clock cycle; CL = 2; t_{CK} = 7.5 ns	1112	1251	1536	1728	mA	1,3
I_{DD5}	**Auto-Refresh Current**: $t_{RC} = t_{RFC\ MIN}$, distributed refresh	1352	1521	2704	3042	mA	1,4
I_{DD6}	**Self-Refresh Current**: CKE ≤ 0.2V	15.2	17.1	30.4	34.2	mA	1,2,4
I_{DD7}	**Operating Current - Four bank operation**; four bank inter-leaving with BL=4; Refer to the detailed test conditions in the component datasheet	1576	1773	2000	2250	mA	1,3

1. I_{DD} currents are measured after the device is properly initialized. Typical values are obtained from characterisation data measured at VDD = 2.5 V and R.T. with an input slew rate = 1V/ns.
2. Enables on-chip refresh and address counters.
3. For two bank modules only : the other bank is in IDD3N mode
4. For two bank modules only : both banks operate in the same current mode

Electrical Characteristics & AC Timing for DDR-I components

(for reference only)

(0 °C ≤ T_A ≤ 70 °C; V_{DDQ} = 2.5V ± 0.2V; V_{DD} = 2.5V ± 0.2V)

Symbol	Parameter		DDR266A -7		DDR200 -8		Unit	Notes
			Min	Max	Min	Max		
t_{AC}	DQ output access time from CK/$\overline{CK}$		– 0.75	+ 0.75	– 0.8	+ 0.8	ns	1-4
t_{DQSCK}	DQS output access time from CK/$\overline{CK}$		– 0.75	+ 0.75	– 0.8	+ 0.8	ns	1-4
t_{CH}	CK high-level width		0.45	0.55	0.45	0.55	t_{CK}	1-4
t_{CL}	CK low-level width		0.45	0.55	0.45	0.55	t_{CK}	1-4
t_{HP}	Clock Half Period		min (t_{CL}, t_{CH})		min (t_{CL}, t_{CH})		ns	1-4
t_{CK}	Clock cycle time	CL = 2.5	7	12	8	12	ns	1-4
t_{CK}		CL = 2.0	7.5	12	10	12	ns	1-4
t_{DH}	DQ and DM input hold time		0.5		0.6		ns	1-4
t_{DS}	DQ and DM input setup time		0.5		0.6		ns	1-4
t_{IPW}	Control and Addr. input pulse width (each input)		2.2		2.5		ns	1, 10
t_{DIPW}	DQ and DM input pulse width (each input)		1.75		2		ns	1-4, 11
t_{HZ}	Data-out high-impedence time from CK/$\overline{CK}$		– 0.75	+ 0.75	– 0.8	+ 0.8	ns	1-4, 5
t_{LZ}	Data-out low-impedence time from CK/$\overline{CK}$		– 0.75	+ 0.75	– 0.8	+ 0.8	ns	1-4, 5
t_{DQSS}	Write command to 1st DQS latching transition		0.75	1.25	0.75	1.25	t_{CK}	1-4
t_{DQSQ}	DQS-DQ skew (for DQS & associated DQ signals)			+ 0.5		+ 0.6	ns	1-4
t_{QHS}	Data hold skew factor			+ 0.75		+ 1.0	ns	1-4
t_{QH}	Data Output hold time from DQS		t_{HP}-t_{QHS}		t_{HP}-t_{QHS}		ns	1-4
$t_{DQSL,H}$	DQS input low (high) pulse width (write cycle)		0.35		0.35		t_{CK}	1-4
t_{DSS}	DQS falling edge to CK setup time (write cycle)		0.2		0.2		t_{CK}	1-4
t_{DSH}	DQS falling edge hold time from CK (write cycle)		0.2		0.2		t_{CK}	1-4
t_{MRD}	Mode register set command cycle time		14		16		ns	1-4
t_{WPRES}	Write preamble setup time		0		0		ns	1-4, 7
t_{WPST}	Write postamble		0.40	0.60	0.40	0.60	t_{CK}	1-4, 6
t_{WPRE}	Write preamble		0.25		0.25		t_{CK}	1-4
t_{IS}	Address and control input setup time	fast slew rate	0.9		1.1		ns	2-4, 10,11
		slow slew rate	1.0		1.1		ns	
t_{IH}	Address and control input hold time	fast slew rate	0.9		1.1		ns	
		slow slew rate	1.0		1.1		ns	
t_{RPRE}	Read preamble		0.9	1.1	0.9	1.1	t_{CK}	1-4
t_{RPST}	Read postamble		0.40	0.60	0.40	0.60	t_{CK}	1-4
t_{RAS}	Active to Precharge command		45	120,000	50	120,000	ns	1-4
t_{RC}	Active to Active/Auto-refresh command period		65		70		ns	1-4

Electrical Characteristics & AC Timing for DDR-I components

(for reference only)

(0 °C ≤ T_A ≤ 70 °C; V_{DDQ} = 2.5V ± 0.2V; V_{DD} = 2.5V ± 0.2V)

Symbol	Parameter		DDR266A -7		DDR200 -8		Unit	Notes
			Min	Max	Min	Max		
t_{RFC}	Auto-refresh to Active/Auto-refresh command period		75		80		ns	1-4
t_{RCD}	Active to Read or Write delay		20		20		ns	1-4
t_{RP}	Precharge command period		20		20		ns	1-4
t_{RRD}	Active bank A to Active bank B command		15		15		ns	1-4
t_{WR}	Write recovery time		15		15		ns	1-4
t_{DAL}	Auto precharge write recovery + precharge time		(twr/tck) + (trp/tck)				t_{CK}	1-4,9
t_{WTR}	Internal write to read command delay		1		1		t_{CK}	1-4
t_{XSNR}	Exit self-refresh to non-read command		75		80		ns	1-4
t_{XSRD}	Exit self-refresh to read command		200		200		t_{CK}	1-4
t_{REFI}	Average Periodic Refresh Interval	128Mbit based		15.6		15.6	µs	1-4, 8
		256 Mbit based		7.8		7.8	µs	1-4, 8

1. Input slew rate >=1V/ns for DDR266 and = 1V/ns for DDR200.
2. The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross: the input reference level for signals other than CK/$\overline{CK}$, is V_{REF}. CK/$\overline{CK}$ slew rate are >= 1.0 V/ns.
3. Inputs are not recognized as valid until V_{REF} stabilizes.
4. The Output timing reference level, as measured at the timing reference point indicated in AC Characteristics (Note 3) is V_{TT}.
5. t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving (HZ), or begins driving (LZ).
6. The maximum limit for this parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.
7. The specific requirement is that DQS be valid (HIGH, LOW, or some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from Hi-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on t_{DQSS}.
8. A maximum of eight Autorefresh commands can be posted to any given DDR SDRAM device.
9. For each of the terms, if not already an integer, round to the next highest integer. tCK is equal to the actual system clock cycle time.
10. These parameters guarantee device timing, but they are not necessarily tested on each device
11. Fast slew rate >= 1.0 V/ns , slow slew rate >= 0.5 V/ns and < 1V/ns for command/address and CK & $\overline{CK}$ slew rate >1.0 V/ns, measured between VOH(ac) and VOL(ac)

SPD Codes for PC1600 Modules "-8"

Byte#	Description	SPD Entry Value	Hex			
			256MByte one bank x64	256 MByte one bank x72	512 MByte two banks x64	512 MByte two banks x72
0	Number of SPD Bytes	128	80			
1	Total Bytes in Serial PD	256	08			
2	Memory Type	DDR-SDRAM	07			
3	Number of Row Addresses	12 / 13	0D			
4	Number of Column Addresses	10	0A			
5	Number of DIMM Banks	1 / 2	01	01	02	02
6	Module Data Width	x64 / x72	40	48	40	48
7	Module Data Width (cont'd)	0	00			
8	Module Interface Levels	SSTL_2.5	04			
9	SDRAM Cycle Time at CL = 2.5	8 ns	80			
10	Access Time from Clock at CL = 2.5	0.8 ns	80			
11	DIMM Config	non-ECC / ECC	00	02	00	02
12	Refresh Rate/Type	Self-Refresh, 7.8 µs	82			
13	SDRAM Width, Primary	x8	08			
14	Error Checking SDRAM Data Width	na / x8	00	08	00	08
15	Minimum Clock Delay for Back-to-Back Random Column Address	t_{CCD} = 1 CLK	01			
16	Burst Length Supported	2, 4 & 8	0E			
17	Number of SDRAM Banks	4	04			
18	Supported $\overline{CAS}$ Latencies	$\overline{CAS}$ latency = 2 & 2.5	0C			
19	$\overline{CS}$ Latencies	$\overline{CS}$ latency = 0	01			
20	$\overline{WE}$ Latencies	Write latency = 1	02			
21	SDRAM DIMM Module Attributes	unbuffered	20			
22	SDRAM Device Attributes: General		C0			
23	Min. Clock Cycle Time at $\overline{CAS}$ Latency = 2	10.0 ns	A0			
24	Access Time from Clock for CL = 2	0.8 ns	80			
25	Minimum Clock Cycle Time at CL = 1.5	not supported	00			
26	Access Time from Clock at CL = 1.5	not supported	00			
27	Minimum Row Precharge Time	20 ns	50			
28	Minimum Row Act. to Row Act. Delay t_{RRD}	15 ns	3C			
29	Minimum $\overline{RAS}$ to $\overline{CAS}$ Delay t_{RCD}	20 ns	50			
30	Minimum $\overline{RAS}$ Pulse Width t_{RAS}	50 ns	32			
31	Module Bank Density (per bank)	256MByte	40			
32	Addr. and Command Setup Time	1.1 ns	B0			
33	Addr. and Command Hold Time	1.1 ns	B0			
34	Data Input Setup Time	0.6 ns	60			
35	Data Input Hold Time	0.6 ns	60			
36-40	Superset Information	–	00			

Byte#	Description	SPD Entry Value	Hex			
			256MByte one bank x64	256 MByte one bank x72	512 MByte two banks x64	512 MBYte two banks x72
41	Minimum Core Cycle Time tRC	70 ns	46			
42	Min. Auto Refresh Cmd Cycle Time tRFC	80 ns	50			
43	Maximum Clock Cycle Time tck	12 ns	30			
44	Max. DQS-DQ Skew tDDSQ	0.6 ns	3C			
45	X-Factor tQHS	1.0 ns	A0			
46-61	Superset Information	-	00			
62	SPD Revision	Revision 0.0	00			
63	Checksum for Bytes 0 - 62	–	A7	B9	A8	BA
64	Manufacturers JEDEC ID Code	–	C1			
65-71	Manufacturer		INFINEO(N)			
72	Module Assembly Location					
73-90	Module Part Number					
91-92	Module Revision Code					
93-94	Module Manufacturing Date					
95-98	Module Serial Number					
99-127						
128-255	open for Customer use					

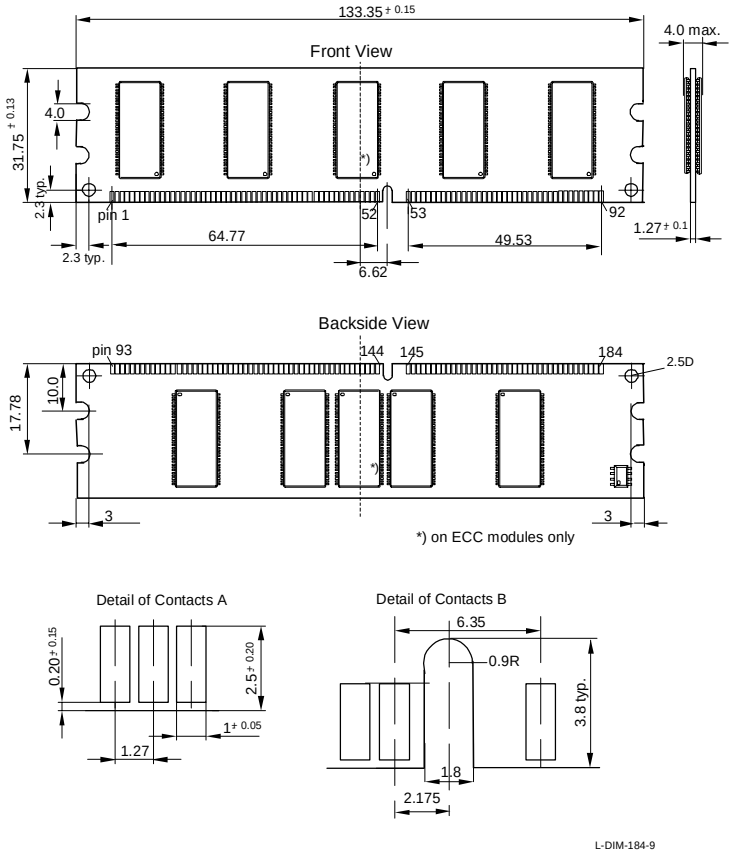
SPD Codes for PC2100 Modules "-7"

Byte#	Description	SPD Entry Value	Hex			
			256MByte one bank x64	256 MByte one bank x72	512 MByte two banks x64	512 MByte two banks x72
0	Number of SPD Bytes	128	80			
1	Total Bytes in Serial PD	256	08			
2	Memory Type	DDR-SDRAM	07			
3	Number of Row Addresses	12/13	0D			
4	Number of Column Addresses	10	0A			
5	Number of DIMM Banks	1 / 2	01	01	02	02
6	Module Data Width	x64 / x72	40	48	40	48
7	Module Data Width (cont'd)	0	00			
8	Module Interface Levels	SSTL_2.5	04			
9	SDRAM Cycle Time at CL = 2.5	7 ns	70			
10	Access Time from Clock at CL = 2.5	0.75 ns	75			
11	DIMM Config	non-ECC / ECC	00	02	00	02
12	Refresh Rate/Type	Self-Refresh, 7.8 µs	82			
13	SDRAM Width, Primary	x8	08			
14	Error Checking SDRAM Data Width	na / x8	00	08	00	08
15	Minimum Clock Delay for Back-to-Back Random Column Address	t_{CCD} = 1 CLK	01			
16	Burst Length Supported	2, 4 & 8	0E			
17	Number of SDRAM Banks	4	04			
18	Supported $\overline{CAS}$ Latencies	$\overline{CAS}$ latency = 2 & 2.5	0C			
19	$\overline{CS}$ Latencies	$\overline{CS}$ latency = 0	01			
20	$\overline{WE}$ Latencies	Write latency = 1	02			
21	SDRAM DIMM Module Attributes	unbuffered	20			
22	SDRAM Device Attributes: General		C0			
23	Min. Clock Cycle Time at $\overline{CAS}$ Latency = 2	7.5 ns	75			
24	Access Time from Clock for CL = 2	0.75 ns	75			
25	Minimum Clock Cycle Time at CL = 1.5	not supported	00			
26	Access Time from Clock at CL = 1.5	not supported	00			
27	Minimum Row Precharge Time	20 ns	50			
28	Minimum Row Act. to Row Ac. Delay t_{RRD}	15 ns	3C			
29	Minimum $\overline{RAS}$ to $\overline{CAS}$ Delay t_{RCD}	20 ns	50			
30	Minimum $\overline{RAS}$ Pulse Width t_{RAS}	45 ns	2D			
31	Module Bank Density (per bank)	256MByte	40			
32	Addr. and Command Setup Time	0.9 ns	90			
33	Addr. and Command Hold Time	0.9 ns	90			
34	Data Input Setup Time	0.5 ns	50			
35	Data Input Hold Time	0.5 ns	50			
36-40	Superset Information	–	00			

Byte#	Description	SPD Entry Value	Hex			
			256MByte one bank x64	256 MByte one bank x72	512 MByte two banks x64	512 MBYte two banks x72
41	Minimum Core Cycle Time tRC	65 ns	41			
42	Min. Auto Refresh Cmd Cycle Time tRFC	75 ns	4B			
43	Maximum Clock Cycle Time tck	12 ns	30			
44	Max. DQS-DQ Skew tDDSQ	0.5 ns	32			
45	X-Factor tQHS	0.75 ns	75			
46-61	Superset Information	-	00			
62	SPD Revision	Revision 0.0	00			
63	Checksum for Bytes 0 - 62	–	B2	C4	B3	C5
64	Manufacturers JEDEC ID Code	–	C1			
65-71	Manufacturer		INFINEO(N)			
72	Module Assembly Location					
73-90	Module Part Number					
91-92	Module Revision Code					
93-94	Module Manufacturing Date					
95-98	Module Serial Number					
99-127						
128-255	open for Customer use					

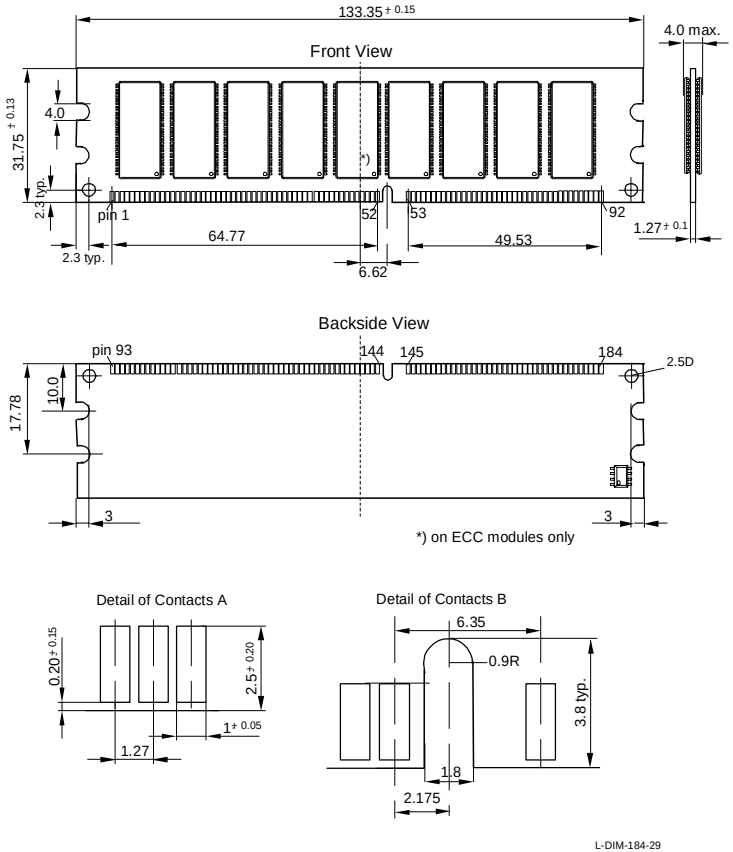
Package Outlines - Raw Card B1 (One Bank Modules)

DDR-SDRAM DIMM Module Package



Package Outlines -Raw Card A1 (One Bank Modules)

DDR-SDRAM DIMM Module Package



Package Outlines - Raw Card B1 (Two Bank Modules)

DDR-SDRAM DIMM Module Package

two bank modules