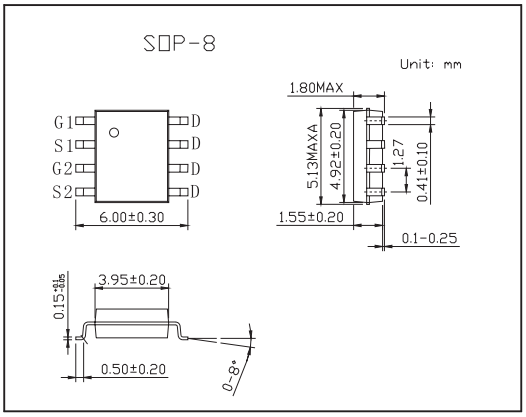
Complementary PowerTrench Half-Bridge MOSFET

KDS4501H



■ Features

- N-Channel

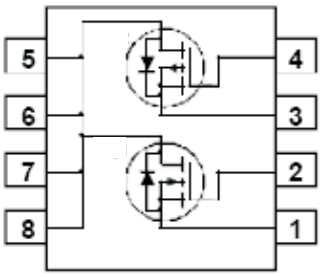
  9.3 A, 30 V $R_{DS(ON)}$ = 18mΩ @ V_{GS} = 10 V

  $R_{DS(ON)}$ = 23mΩ @ V_{GS} =4.5V

- P-Channel

  -5.6 A, -20 V $R_{DS(ON)}$ = 46 mΩ @ V_{GS} =- 4.5 V

  $R_{DS(ON)}$ = 63 mΩ @ V_{GS} =-2.5V



■ Absolute Maximum Ratings Ta = 25℃

Parameter	Symbol	N-Channel	P- Channel	Unit
Drain to Source Voltage	V_{DSS}	30	-20	V
Gate to Source Voltage	V_{GS}	±20	±8	V
Drain Current Continuous (Note 1a)	I_D	9.3	-5.6	A
Drain Current Pulsed		20	-20	A
Power Dissipation for Single Operation (Note 1a)	P_D	2.5		W
(Note 1b)		1.2		
(Note 1c)		1		
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150		℃
Thermal Resistance Junction to Ambient (Note 1a)	$R_{\theta JA}$	50		℃/W
Thermal Resistance Junction to Case (Note 1)	$R_{\theta JC}$	25		℃/W

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■ Electrical Characteristics Ta = 25℃

Parameter	Symbol	Testconditons		Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V, I_D = 250 μA	N-Ch	30			V
		V_{GS} = 0 V, I_D = -250 μA	P-Ch	-20			
Breakdown Voltage Temperature Coefficient	$\frac{\Delta BV_{DSS}}{\Delta T_J}$	I_D = 250 μA, Referenced to 25℃	N-Ch		24		mV/℃
		I_D = -250 μA, Referenced to 25℃	P-Ch		-13		
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 24V, V_{GS} = 0 V	N-Ch			1	μA
		V_{DS} = -16 V, V_{GS} = 0 V	P-Ch			-1	
Gate-Body Leakage	I_{GSS}	V_{GS} = ±20V, V_{DS} = 0 V	N-Ch			±100	nA
		V_{GS} = ±8 V, V_{DS} = 0 V	P-Ch			±100	
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	N-Ch	1	1.6	3	V
		V_{DS} = V_{GS}, I_D = -250 μA	P-Ch	-0.4	-0.7	-1.5	
Gate Threshold Voltage Temperature Coefficient	$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	I_D = 250 μA, Referenced to 25℃	N-Ch		-4		mV/℃
		I_D = -250 μA, Referenced to 25℃	P-Ch		3		
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D =9.3A	N-Ch		14	18	mΩ
		V_{GS} = 10 V, I_D = 9.3 A,T_J = 125℃			21	29	
		V_{GS} = 4.5 V, I_D =7.6 A			17	23	
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = -4.5 V, I_D =-5.6 A	P-Ch		36	46	
		V_{GS} = -4.5 V, I_D =-5.6 A,T_J = 125℃			49	80	
		V_{GS} = -2.5 V, I_D =-5.0A			47	63	
On-State Drain Current	$I_{D(on)}$	V_{GS} = 10 V, V_{DS} = 5V	N-Ch	20			A
		V_{GS} = -4.5 V, V_{DS} = -5V	P-Ch	-20			
Forward Transconductance	g_{FS}	V_{DS} = 5V, I_D = 9.3A	N-Ch		28		S
		V_{DS} = 5V, I_D = -5.6A	P-Ch		16		
Input Capacitance	C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V,f = 1.0 MHz	N-Ch		1958		pF
			P-Ch		1312		
Output Capacitance	C_{oss}		N-Ch		424		pF
			P-Ch		240		
Reverse Transfer Capacitance	C_{rss}		N-Ch		182		pF
			P-Ch		106		
Turn-On Delay Time	$t_{d(on)}$	N-Channel V_{DD} = 15 V, I_D = 1 A, V_{GS} = 10 V, R_{GEN} = 6 Ω (Note 2) P-Channel V_{DD} = -10 V, I_D = -1 A, V_{GS} = -4.5 V, R_{GEN} = 6 Ω (Note 2)	N-Ch		15	27	ns
			P-Ch		15	27	
Turn-On Rise Time	t_r		N-Ch		5	10	ns
			P-Ch		15	27	
Turn-Off Delay Time	$t_{d(off)}$		N-Ch		38	61	ns
			P-Ch		40	64	
Turn-Off Fall Time	t_f		N-Ch		10	20	ns
			P-Ch		25	40	
Total Gate Charge	Q_g	N-Channel V_{DS} =15V,I_D=9.3A,V_{GS}=4.5V(Note 2) P-Channel V_{DS}=-15V,I_D=-2.4A,V_{GS}=-4.5V(Note 2)	N-Ch		17	27	nC
			P-Ch		13	21	
Gate-Source Charge	Q_{gs}		N-Ch		4		nC
			P-Ch		2.5		
Gate-Drain Charge	Q_{gd}		N-Ch		5		nC
			P-Ch		2.0		

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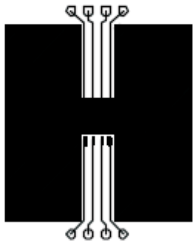
Parameter	Symbol	Testconditons		Min	Typ	Max	Unit
Maximum Continuous Drain-Source Diode Forward Current	Is		N-Ch			2.1	A
			P-Ch			-2.1	
Drain-Source Diode Forward Voltage	VSD	VGS = 0 V, Is = 2.1A (Not 2)	N-Ch			1.2	V
		VGS = 0 V, Is = -2.1A (Not 2)	P-Ch			-1.2	

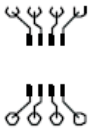
Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 50°C/W when mounted on a 1 in^2 pad of 2 oz copper

b) 105°C/W when mounted on a 0.04 in^2 pad of 2 oz copper



c) 125°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300us, Duty Cycle < 2.0%