L64720 Video Motion Estimation Processor (MEP)

Description

The MEP (Motion Estimation Processor) detects the relative motion between data blocks in two video frames. This operation makes it possible to transmit or store less information in a video compression system.

The data block (user selectable for either 16 x 16 or 8 x 8) in the current video frame is offset and compared with the reference image. The position of the best match, the minimum error and the zero offset error are returned by the processor. The error computed is the sum of absolute differences.

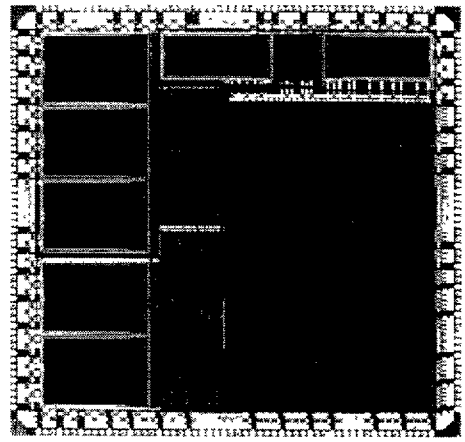
For the 16 x 16 data block size, errors are computed for offsets of -8 to +7 in both the X and Y dimensions. For the 8 x 8 data block size, errors are computed for offsets of -4 to +3 in both the X and Y dimensions.

In both cases, multiple devices can be used to increase the search window size.

The L64720-30 can process a 352 x 288 image at a 30 Hz frame rate with a 16 x 16 data block size. When operating with an 8 x 8 data block size, the L64720-30 can process broadcast quality images (600 x 480) at a 30 MHz frame rate.

All input and output data is double buffered to minimize the main memory bandwidth requirements. The search window and data blocks are loaded sequentially while the output values are randomly accessed.

The device is available in 68-pin Ceramic Pin Grid Arrays and 68-pin Plastic Leaded Chip Carriers .



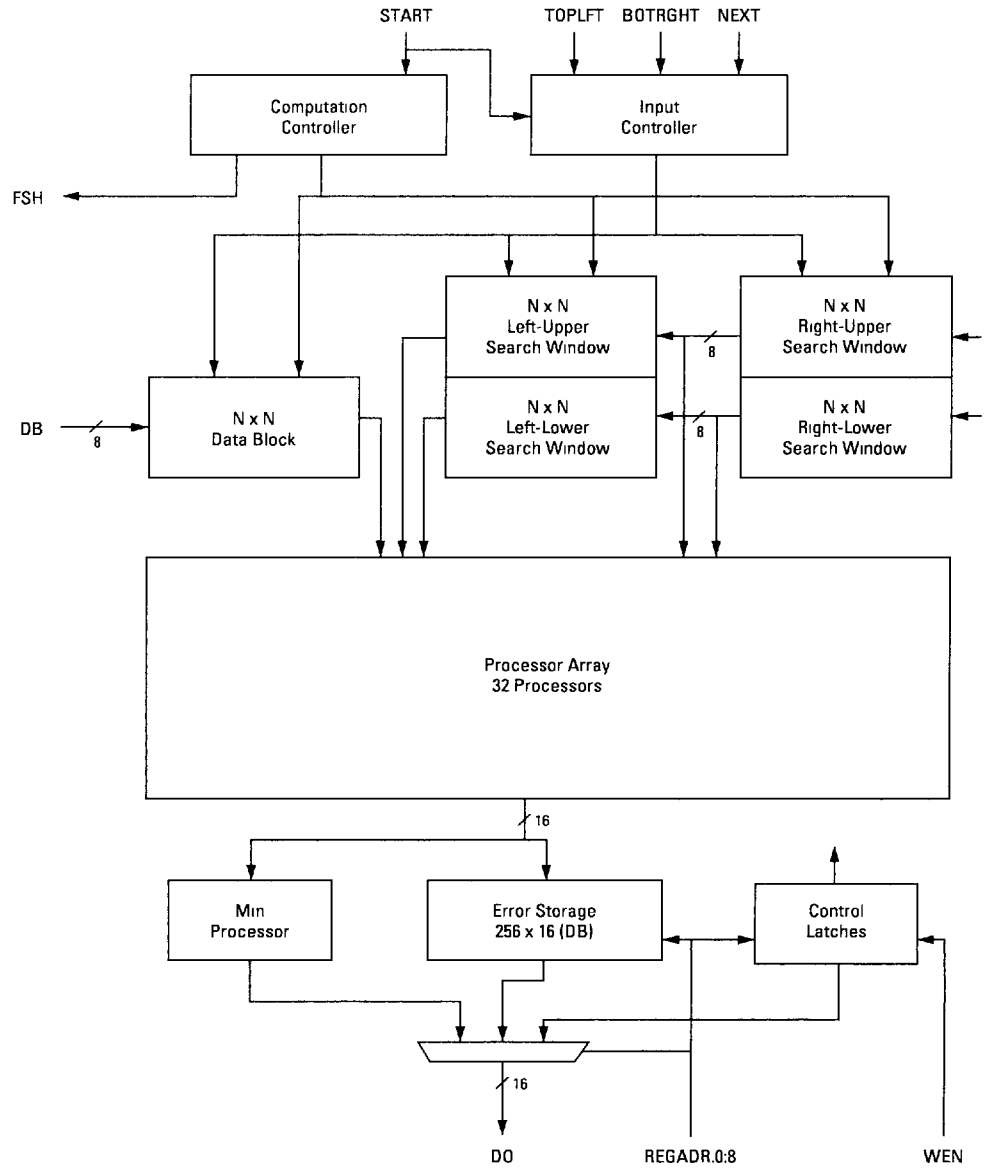
L64720 Chip

Features

- 16 x 16 or 8 x 8 data block
- 32 x 32 or 16 x 16 search window
- Search window can be increased with multiple devices
- Multiple devices can be used for increased performance
- Compatible with proposed ITU-TSS (formerly CCITT)
- 30/40 MHz clock rates
- Double buffered I/O
- Simple control
- 68-pin CPGA (Ceramic Pin Grid Array) or PLCC (Plastic Leaded Chip Carrier) package

 May 1994 Order Number I15013

Motion Estimation Processor Block Diagram



Pin Listing and Description

(SIGNAL.0 is always the LSB)

SW0.0-SW0.7
Eight-bit bus for loading the new right-upper N x N block of the search window. The format of the SW0 data is determined by the control bit UNSGN.

SW1.0-SW1.7
Eight-bit bus for loading the new right-lower N x N block of the search window. The format of the SW1 data is determined by the control bit UNSGN.

TOPLFT, BOTRGHT
Two-bit input flags which specify on which, if any, boundary of the image the data block touches. The data on these pins is only latched during the first two cycles in which NEXT is HIGH after START goes HIGH.

DB.0-DB.7
Eight-bit bus for loading the N x N data block. The format of the DB data is determined by the control bit UNSGN.

NEXT
One-bit input flag. When HIGH, indicates that the data on the SW0 , SW1 and DB buses should be latched. This pin should go HIGH for a single cycle each time a new set of inputs is available. NEXT must go LOW for at least one cycle after being HIGH.

START
One-bit input flag. When HIGH, causes a new computation to begin and the swapping of the double buffered input buffers. Should be HIGH for a single cycle only.

FSH
One-bit output flag. Goes HIGH for a single cycle to indicate that the computations have finished. The position of the minimum error, the minimum error and the zero offset error will be shifted out of the DO bus in the first six cycles after the rising edge FSH. The double buffered output buffers are swapped at this transition.

DO.0-DO.15
Sixteen-bit output bus. The minimum error, the position of the minimum and the zero offset error are automatically output on this bus when FSH goes HIGH. The randomly accessed errors versus position are read over this bus.

WEN
One-bit write enable input pin. When LOW and REGADR.8 and REGADR.7 are HIGH, the internal control latches are set.

OE
One-bit output enable input pin. When HIGH, data can be read from DO bus. When LOW, the DO bus floats.

REGADR.0-REGADR.8
Nine-bit address input. Selects which of the output parameters will be read over the DO bus. Also controls the latching of control bits. REGADR is ignored for the first six cycles after FSH goes HIGH.

CLK
System clock. Controls all system functions at LOW to HIGH transitions.

Pin Description Summary

Pin	No. of Pins	I/O	Description
SW0.0–SW0.7	8	I	Upper search window input
SW1.0–SW1.7	8	I	Lower search window input
DB.0–DB.7	8	I	Data input bus
TOPLFT	1	I	Top left boundary flag
BOTRGHT	1	I	Bottom right boundary flag
NEXT	1	I	New input flag
START	1	I	Start computation flag
FSH	1	O	Finish computation flag
REGADR.0–8	9	I	Address input
WEN	1	I	Active LOW write enable
DO.0–DO.15	16	O	Data output bus
OE	1	I	Active HIGH output enable
CLK	1	I	Clock

Architecture

The motion estimation processor consists of several major sections: the input buffers, the processor array, the controllers, control latches and the output buffers.

The input buffers store the N x N data block (N = 8, 16) and the 2N x 2N search window. All input buffers are double buffered in a manner transparent to the user. The writing of data via the SW0, SW1 and DB buses is controlled by the input controller while the reading of data for computation is controlled by the computation controller. Because the search windows overlap by N pixels as the window is moved from left to right, the data can be automatically transferred from the right to the left buffers without the need to access the external search window memory.

The bulk of the computations are performed in the processor array. The array must compute the following equation N x N times:

$$\text{for } \left(\frac{-N}{2} \le i < \frac{N}{2}, \frac{-N}{2} \le j < \frac{N}{2}\right):$$

$$\text{error}(i,j) = \sum_{y=0}^{N-1} \sum_{x=0}^{N-1} \text{abs}\left[SW(x+i, y+j) - DB(x,y)\right]$$

The device also computes the position, (I, J), and the value of the minimum error (m) in the min processor. These values are defined as follows:

$$m = \text{error}(I, J) = \min_{i,j}\left(\text{error}(i,j)\right)$$

In case of a tie, the offset whose distortion is computed later is chosen. Using the coordinate system defined on page 5, the distortions for the 256 different offsets are computed in the following order for N = 16 (N = 8 case is similar):

(-8, -8), (-8, -7), (-8, -6), ..., (-8, +7)
(-7, -8), (-7, -7), (-7, -6), ..., (-7, +7)

(+7, -8), (+7, -7), (+7,-6), ..., (+7, +7)

As the results are computed, they are stored in the output buffer. The outputs are double buffered, allowing the user to read the results in a random access manner during the following computation.

The control of the device is straight forward. When start is HIGH, the device is reset for a new computation and all input double buffers are swapped. When the computation has completed, the user is notified by FSH going HIGH for a single cycle. At this point, the double buffered output buffers are swapped and if all new data has been loaded into the device, a new computation can begin immediately. The input data is loaded sequentially into the buffers at a rate controlled by the NEXT signal. Each time NEXT goes HIGH, a new set of inputs is loaded into the inactive input buffers.

The search window and data block values are both eight bits wide. The user can select either unsigned or two's complement formats. The errors are computed to the full 16 bits, making overflow impossible. All 16 bits can be accessed by the user.

The control latches store the bits which determine the value of N, the format of the input data and whether the RAMS are active.

The performance of the device and the requirements for main memory access time (assuming no wait states) are given in Table 1. The times are for computing the N^2 errors for an N x N data block size.

Table 1. Performance of L64720

N	Clock Freq (MHz)	Cycles	Execution Time (μsec)	External RAM Access Time (ns)
8	30	229	7.56	99
8	40	229	5.73	75
16	30	2237	73.8	264
16	40	2237	55.9	200

Architecture
(continued)

Search Window Size
A single device computes N^2 errors for each offset of an N x N data block within a 2N x 2N search window. In general, (m – 1) x (k – 1) devices can be used to increase the search window to size mN x kN. Each device is provided with overlapping 2N x 2N subsections of the entire search window (see later example for m = k = 3). The N^2 errors computed by each device must be offset (by the user) by an amount corresponding to the relative position of the search windows used in each device. The user must also compute the true minimum error from the (m – 1) x (k – 1) local minimum errors that have been computed.

Edge Effects
Care must be taken for data blocks that are sufficiently close to one or more of the edges of the image frame such that the search window extends beyond the image frame. If the region outside the frame is considered to be undefined, then the motion vector should not point outside the frame. These edge effects should be handled in a case dependent way.

The first and most typical case (m = k = 2, EXPODD reset) is single processor operation, in which the search window extends N/2 pixels beyond the data block on each side. Hence, for blocks at the frame boundary, the search window will extend by N/2 pixels over one or more edges of the frame.

The signals TOPLFT and BOTRGHT are used to indicate which edges of the frame the search window extends beyond. When NEXT is HIGH for the first time after START goes HIGH, TOPLFT and BOTRGHT should be HIGH if the search window extends beyond the top and/or bottom edges of the frame, respectively. When NEXT is HIGH for the second time after START goes HIGH, TOPLFT and BOTRGHT should be HIGH if the search window extends beyond the left and/or right edges of the frame, respectively. Both should be LOW if the search window does not extend beyond any of the frame boundaries. It should be noted that in this mode, it is possible for the search window to extend beyond any combination of frame edges simultaneously.

An extension of the first case is all other multiprocessor configurations in which m, k are both even and the data block is centered within the overall search window. EXPODD, TOPLFT and BOTRGHT are controlled as described above.

The second case includes the most common multiprocessor configurations in which k and m are odd and the data block is centered within the overall search window. Under these conditions, the search window will extend by either 0 or N pixels beyond the edge of the frame. TOPLFT and BOTRGHT are used as described for case1 but EXPODD is set. However, for this case, the search window may extend beyond at most two edges of the frame simultaneously.

For both case 1 and 2, all of the device outputs are correct, including the optimum motion vector and the minimum error.

The third case is used to accommodate all other values of m and k (one even and one odd) and for data blocks not centered within the overall search window. For these cases, the search window may extend beyond the image frame edge by a number of pixels exceeding zero but not necessarily equal to N/2 or N, or there is unequal extention beyond two or more edges simultaneously. When the extension exceeds N pixels, none of the errors are valid because no motion vectors point within the frame and hence the entire output of the device should be ignored. When the extension is less than or equal to N pixels, the value of the minimum error and optimum motion vector may not be correct, but the errors computed for all motion vectors within the frame will be correct. For this case, EXPODD, TOPLFT and BOTRGHT should always be LOW.

Definition of Coordinate System

Figure 1 shows the way in which the coordinates are defined for the Search Window (SW) and the Data Block (DB) for the case of N = 16. The data block indices go from 0 to 15 and the SW indices go from -8 to 23. Note that the search window is twice the size of the data block in both dimensions.

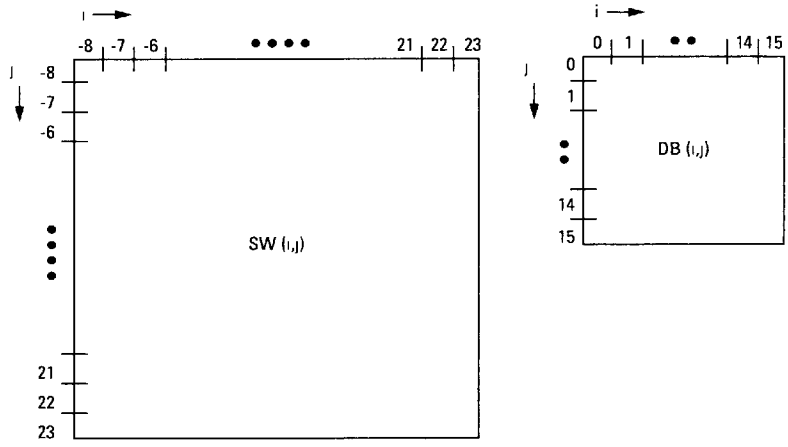


Figure 1. Coordinate Definition for N = 16

The processor will find the sum of absolute errors between the DB and the SW for N/2 offsets in each direction. This operation can be thought of as placing the DB at different positions within the SW and summing the magnitude of the errors between corresponding points. The position or offset is defined to be the coordinate within the search window that corresponds to the (0,0) point of the DB. An offset of (0,0) corresponds roughly to the DB centered within the search window.

In Figure 2, the offset is (-7,-6).

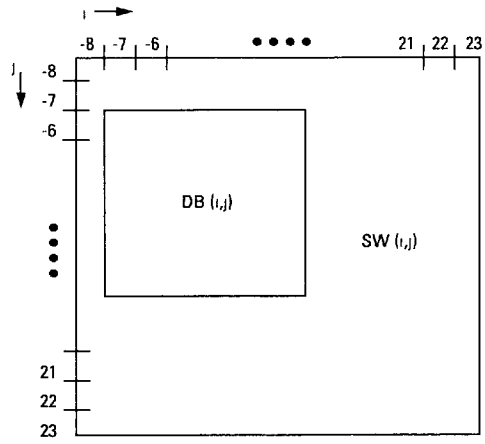


Figure 2. Example of Datablock Offset by (-7,-6) in Search Window

I/O Operations

Loading the Input Data (SW0, SW1, DB)

While all N^2 errors are being computed for different offsets between the data block and the search window, new input data should be loaded. Only the right half of the search window is normally updated with the upper and lower N x N blocks being loaded in parallel. At the same time, the N x N data block is also loaded. All three N x N blocks are loaded in a raster scan fashion, i.e., the loading proceeds row by row. The points in each row are loaded from left to right with the top row loaded first.

Setting START HIGH resets the input controller. Each time NEXT goes HIGH, the values on SW0, SW1, and DB are loaded into the internal RAMs.

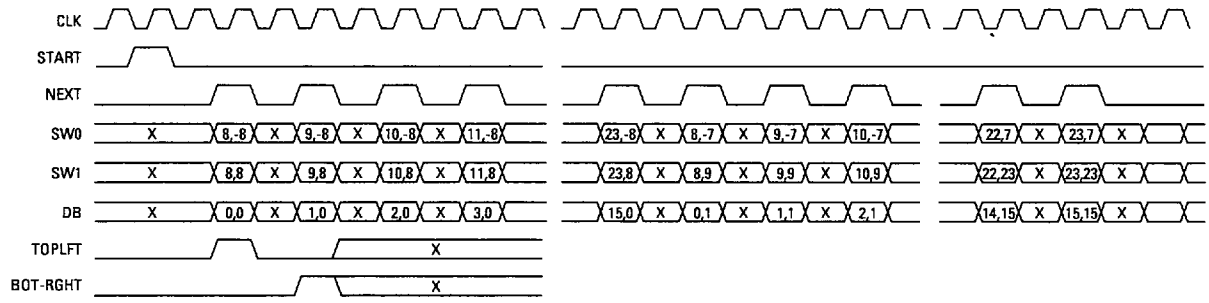


Figure 3. Loading Sequence for N = 16

Figure 3 shows the loading sequence for the N = 16 case. Although the data is shown being loaded once every two cycles, the rate is controlled by the user via the NEXT pin. TOPLFT and BOTRGHT indicate that the block is at the top right corner of the image frame.

In the case when it necessary to load both halves of the search window, the sequence shown above is simply performed twice without waiting for the FSH signal to go HIGH.

Reading the Results

The end of computation is shown in Figure 4. The FSH flag goes HIGH and the values of the minimum error, the offset corresponding to the minimum error and the zero offset error are output automatically. Note that a valid output can be latched at the rising edge of CLK in the first, third and fifth cycles after the rising edge of CLK that occurred when FSH was HIGH.

These values appear on the DO pins in the format shown in Table 2. Six cycles after FSH goes HIGH, all error(i,j) values can be randomly read from the RAM as shown in Figure 5. The offset is supplied on the REGADR bus and the error is returned on the DO bus. This operation can coincide with the loading of input data as described earlier.

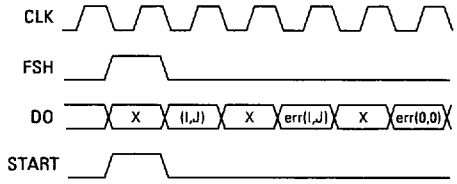


Figure 4. End of Computation Cycle

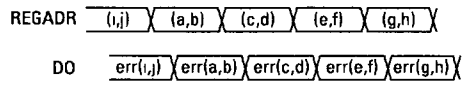


Figure 5. Reading Error Values from RAM

I/O Operations (Continued)

Tables 2 and 3 show the way in which the data is accessed from the internal double buffered storage. Note that i,j,I,J are two's complement numbers in the range from -N/2 to N/2 -1.

They can be converted to unsigned numbers by inverting the sign bit. The error values, e and m, are unsigned 16-bit numbers. The MSB of all numbers is the highest numbered bit.

The device will ignore the value on the REGADR pins when data is being automatically output during the six cycles after FSH goes HIGH. Therefore, the user should avoid reading the internally stored values during this period.

Table 2. Address Map for Error Values

REGADR									DO		Comment
8	7	6	5	4	3	2	1	0	15	0	
0	I_3	I_2	I_1	I_0	i_3	i_2	i_1	i_0	e_{15}	e_0	$e = error(i,j)$
1	0	x	x	x	x	x	x	0	m_{15} ...	m_0	$m = \min_{i,j}(error(i,j)) = error(I,J)$

Table 3. Address Map for Control Bits

REGADR									DO								Comment
8	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	
1	0	x	x	x	x	x	x	1	J_3	J_2	J_1	J_0	I_3	I_2	I_1	I_0	$error(I,J) = \min_{i,j}(error(i,j))$
1	1	x	x	x	x	x	x	x	x	x	TEST	RES	n = 16	UNSGN	PWDN	EXPODD	read control bits

Initialization

Before normal operation can begin, several operating parameters must be set. These control several LSI Logic test modes, the data format, the value of N and the power down mode of the internal RAMs.

Each bit can be set or reset by selecting the proper address on the REGADR bus and setting WEN LOW. If the internal random access error RAM is not used, the control bits can be hardwired without the need for a controller.

The function of each bit and the method by which it can be set and reset is given in Table 4.

Table 4. Function of Control Bits

REGADR.8:0	Control Bit	Function
111XXXXXX	Set TEST	LSI Logic RAM/PO TEST mode
110XXXXXX	Reset TEST	Normal operating mode
11X1XXXXX	Set RES	LSI Logic reset TEST mode
11X0XXXXX	Reset RES	Normal operating mode
11XX1XXXX	Set N = 16	16 x 16 data block size
11XX0XXXX	Reset N = 16	8 x 8 data block size
11XXX1XXX	Set UNSGN	DB, SW0, SW1 data are unsigned
11XXX0XXX	Reset UNSGN	DB, SW0, SW1 data are signed
11XXXX1XX	Set PWDN	RAMs are inactive (power down)
11XXXX0XX	Reset PWDN	RAMs are active (normal mode)
11XXXXX1X	Set EXPODD	Expanded search window operation (m, k both ODD)
11XXXXX0X	Reset EXPODD	Normal search window operation

All bits can be set with a single operation. For example, to put the device into a normal operation mode with 8 x 8 data blocks and unsigned data, the REGADR.8:0 bus would be set to 11000100X and WEN would be strobed LOW.

Increasing the Search Window Size (EXPODD Set)

In some applications it may be desired to accommodate greater degrees of motion. In this case, the error at more than N^2 offsets may be needed. To maintain the rate at which frames are processed, additional devices must be used.

Each device is loaded with a 2N x 2N sub-section of the desired search window. The sub-section must overlap by N points in each dimension to ensure that all offsets are computed. The same data block is loaded into all devices.

For example, a 48 x 48 search window and a 16 x 16 data block can be accommodated by four devices. Figure 6 shows how the search window for each device is obtained for three consecutive positions of the search window.

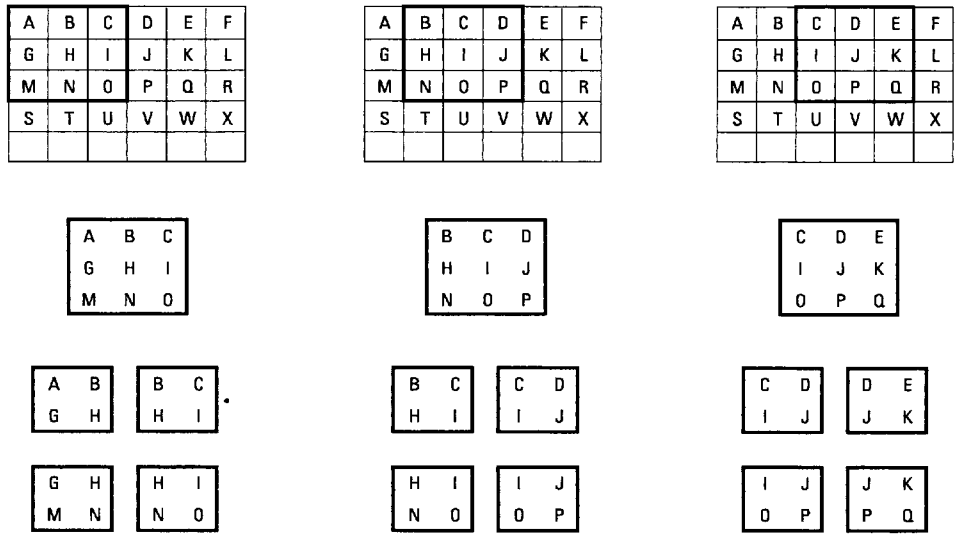


Figure 6. Increasing Search Window Size

The top of the diagram shows the search window frame divided into 16 x 16 blocks. For each data block, 9 blocks from the search window are used as indicated in the center of the diagram. These nine data blocks are further divided into four groups of four blocks. Each group as shown at the bottom of the diagram is loaded into one of the four devices. As in the single processor case, when the search window is moved one block to the right, only the right half of the search window in each device must be updated.

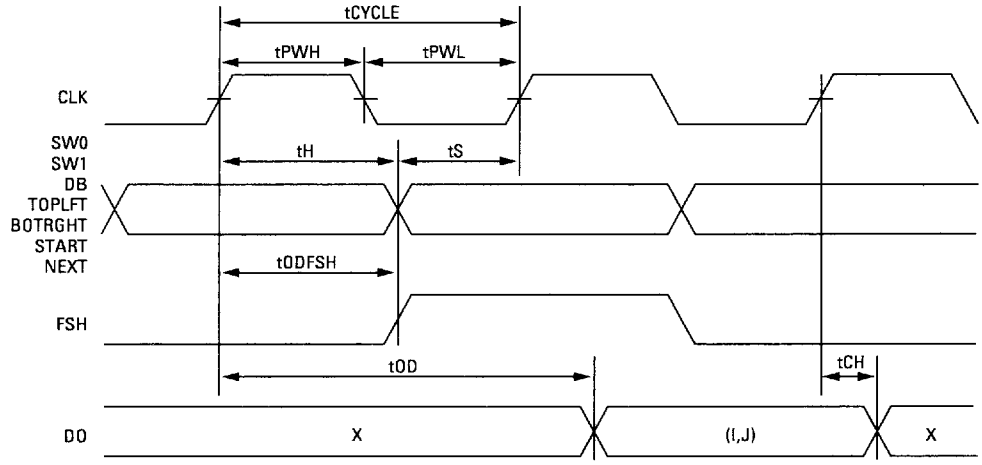
Each device will compute the N^2 errors with the offsets indicated in Table 5.

Table 5. Offsets for Multiprocessor Configuration

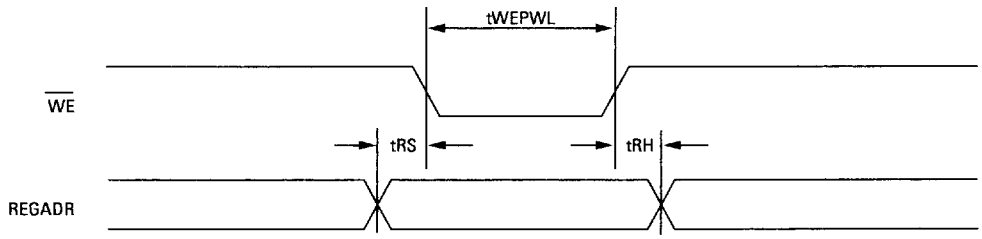
Device	Search Window Blocks	X Offsets	Y Offsets
1	Upper-left	-16 -1	-16:-1
2	Lower-left	-16:-1	0:15
3	Upper-right	0:15	-16:-1
4	Lower-right	0:15	0:15

AC Timing Waveforms

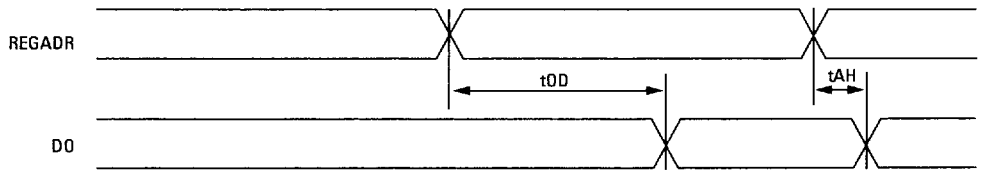
Normal Processing Mode and Loading Input Data



Setting and Resetting the Control Bits



Accessing the Error Storage RAM



AC Switching Characteristics: Commercial (TA = 0°C to 70°C, VDD = 4.75 V to 5.25 V)

Symbol	Parameter	L64720-40 Min	L64720-40 Max	L64720-30 Min	L64720-30 Max
tCYCLE	CLK cycle time	25		33	
tPWH	Min CLK pulse width, HIGH	11		15	
tPWL	Min CLK pulse width, LOW	11		15	
tS	Input setup time to CLK	7		7	
tH	Input hold time to CLK	3		4	
tODFSH	FSH output delay from CLK		18*		20*
tRS	REGADR setup time to WEN	10		15	
tRH	REGADR hold time to WEN	10		15	
tWEPWL	WEN pulse width, LOW	15		20	
tOD	DO output delay from CLK, REGADR		36*		40*
tAH	Output hold time from REGADR	0		0	
tCH	Output hold time from CLK	0		0	

Notes:
1. All times are in ns
2. * – Output loading = 50 pF.

Operating Characteristics

Absolute Maximum Ratings (Reference to GND)

Parameter	Symbol	Limits	Unit
DC supply voltage	VDD	-0.3 to +7	V
Input voltage	VIN	-0.3 to VDD +0.3	V
DC input current	IIN	±10	mA
Storage temperature range	TSTG	-65 to +150 ceramic -45 to +125 plastic	°C

Recommended Operating Conditions

Parameter	Symbol	Limits	Unit
DC supply voltage	VDD	+3 to +6	V
Commercial range	TA	0 to +70	°C

DC Characteristics: Specified at VDD = 5 V over the specified temperature and voltage ranges(1)

Symbol	Parameter	Condition	Min	Typ	Max	Units
VIL	Low level input voltage				0.8	V
VIH	High level input voltage	0°C ≤ TA ≤ 70°C	2.0			V
IIN	Input current	VIN = VDD	-150		200	µA
VOH	High level output voltage	IOH = -4 mA	2.4	4.5		V
VOL	Low level output voltage	IOL = 4 mA		0.2	0.4	V
IOS	Output short circuit current(2)	VDD = Max, VO = VDD	15		130	mA
		VDD = Max, VO = 0V	-5		-100	mA
IDDQ	Quiescent supply current	VIN = VDD or VSS			10	mA
IDD	Operating supply current(3)	tCYCLE = 25 ns		380		mA
CIN	Input capacitance	Any input		5		pF
COUT	Output capacitance	Any input		10		pF

Notes:
1. Commercial temperature range is 0°C to 70°C, ±5% power supply.
2. Not more than one output should be shorted at a time. Duration of short circuit test must not exceed one second.
3. For 40 MHz device.

L64720 Package Pin Information (68-Pin PGA, by Signal Name)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
E10	BOTRGHT	H11	DO.15	H1	REGADR.5	B7	SW1.4
B5	CLK	L4	DO.2	J2	REGADR.6	A5	SW1.5
E11	DB 0	K5	DO.3	J1	REGADR.7	B4	SW1.6
D10	DB 1	L6	DO.4	K1	REGADR.8	A4	SW1.7
D11	DB.2	K7	DO.5	G10	START	G11	TOPLFT
C10	DB.3	L7	DO.6	D1	SW0.0	B6	VDD
C11	DB.4	K8	DO.7	D2	SW0 1	E1	VDD
B11	DB.5	K9	DO.8	C1	SW0 2	F11	VDD
B10	DB.6	L9	DO.9	C2	SW0.3	J11	VDD
A10	DB.7	K2	FSH	B1	SW0 4	K6	VDD
L3	DO.0	A7	NEXT	B2	SW0.5	A6	VSS
K4	DO.1	L2	OE	A2	SW0.6	B3	VSS
L10	DO 10	E2	REGADR.0	A3	SW0.7	F10	VSS
K10	DO 11	F1	REGADR 1	B9	SW1.0	F2	VSS
K11	DO.12	G2	REGADR.2	A9	SW1 1	L5	VSS
J10	DO.13	G1	REGADR.3	B8	SW1.2	L8	VSS
H10	DO 14	H2	REGADR.4	A8	SW1.3	K3	WEN

L64720 Package Pin Information (68-Pin PGA, by Pin Name)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A2	SW0.6	B9	SW1.0	F10	VSS	K4	DO 1
A3	SW0 7	B10	DB 6	F11	VDD	K5	DO.3
A4	SW1.7	B11	DB.5	G1	REGADR.3	K6	VDD
A5	SW1.5	C1	SW0.2	G2	REGADR.2	K7	DO 5
A6	VSS	C2	SW0.3	G10	START	K8	DO.7
A7	NEXT	C10	DB.3	G11	TOPLFT	K9	DO 8
A8	SW1.3	C11	DB 4	H1	REGADR 5	K10	DO.11
A9	SW1.1	D1	SW0.0	H2	REGADR 4	K11	DO.12
A10	DB.7	D2	SW0.1	H10	DO.14	L2	OE
B1	SW0.4	D10	DB.1	H11	DO.15	L3	DO.0
B2	SW0 5	D11	DB.2	J1	REGADR.7	L4	DO.2
B3	VSS	E1	VDD	J2	REGADR.6	L5	VSS
B4	SW1 6	E2	REGADR.0	J10	DO.13	L6	DO 4
B5	CLK	E10	BOTRGHT	J11	VDD	L7	DO.6
B6	VDD	E11	DB.0	K1	REGADR.8	L8	VSS
B7	SW1.4	F1	REGADR 1	K2	FSH	L9	DO 9
B8	SW1.2	F2	VSS	K3	WEN	L10	DO.10

L64720 Package Pin Information (68-Pin PLCC, by Signal Name)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
54	BOTRGHT	49	DO.15	23	REGADR.5	67	SW1.4
3	CLK	32	DO.2	24	REGADR.6	4	SW1.5
55	DB.0	33	DO.3	25	REGADR.7	5	SW1.6
56	DB.1	36	DO.4	26	REGADR.8	6	SW1.7
57	DB.2	37	DO.5	50	START	51	TOPLFT
58	DB.3	38	DO.6	15	SW0.0	1	VDD
59	DB.4	39	DO.7	14	SW0.1	17	VDD
60	DB.5	41	DO.8	13	SW0.2	35	VDD
61	DB.6	42	DO.9	12	SW0.3	47	VDD
62	DB.7	27	FSH	11	SW0 4	53	VDD
30	DO.0	68	NEXT	10	SW0.5	18	VSS
31	DO.1	28	OE	9	SW0.6	2	VSS
43	DO.10	16	REGADR.0	8	SW0.7	34	VSS
44	DO.11	19	REGADR.1	63	SW1.0	40	VSS
45	DO.12	20	REGADR.2	64	SW1.1	52	VSS
46	DO.13	21	REGADR.3	65	SW1.2	7	VSS
48	DO 14	22	REGADR.4	66	SW1.3	29	WEN

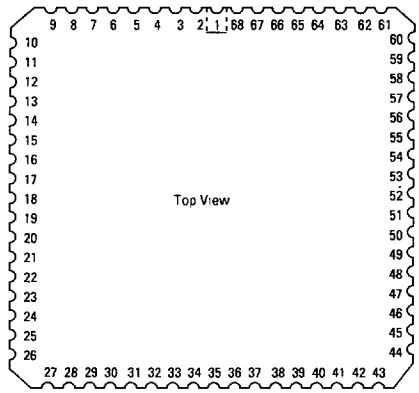
L64720 Package Pin Information (68-Pin PLCC, by Pin Name)

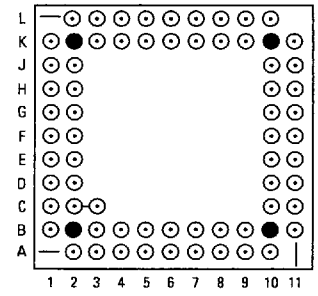
Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	VDD	18	VSS	35	VDD	52	VSS
2	VSS	19	REGADR.1	36	DO.4	53	VDD
3	CLK	20	REGADR.2	37	DO.5	54	BOTRGHT
4	SW1.5	21	REGADR.3	38	DO.6	55	DB.0
5	SW1.6	22	REGADR.4	39	DO.7	56	DB.1
6	SW1.7	23	REGADR.5	40	VSS	57	DB.2
7	VSS	24	REGADR.6	41	DO.8	58	DB.3
8	SW0.7	25	REGADR.7	42	DO.9	59	DB.4
9	SW0.6	26	REGADR.8	43	DO.10	60	DB.5
10	SW0.5	27	FSH	44	DO.11	61	DB.6
11	SW0.4	28	OE	45	DO.12	62	DB.7
12	SW0.3	29	WEN	46	DO.13	63	SW1.0
13	SW0.2	30	DO.0	47	VDD	64	SW1.1
14	SW0.1	31	DO.1	48	DO.14	65	SW1.2
15	SW0.0	32	DO.2	49	DO.15	66	SW1.3
16	REGADR.0	33	DO.3	50	START	67	SW1.4
17	VDD	34	VSS	51	TOPLFT	68	NEXT

LSI LOGIC

Pinout Diagram

68-Pin Plastic Leaded Chip Carrier (PLCC)





Note
Package viewed from underneath

Packaging

68-Pin Ceramic Pin Grid Array: See FB Package in Package Selector Guide
68-Pin Plastic Leaded Chip Carrier: See MC Package in Package Selector Guide

Ordering Information

L64720 G C -XX

- -XX: Speed MHz
- C: Temperature Range/Flow Option
  - C = Commercial (0°C to 70°C)
  - M = Military (-55°C to + 125°C)
    Processed to MIL-STD-883C Level B
- G: Package Code
  - G = 68-Pin Ceramic Grid Array
  - J = 68-Pin Plastic Leaded Chip Carrier
- L64720: Device Type
  Motion Estimation Processor