

OVERVIEW

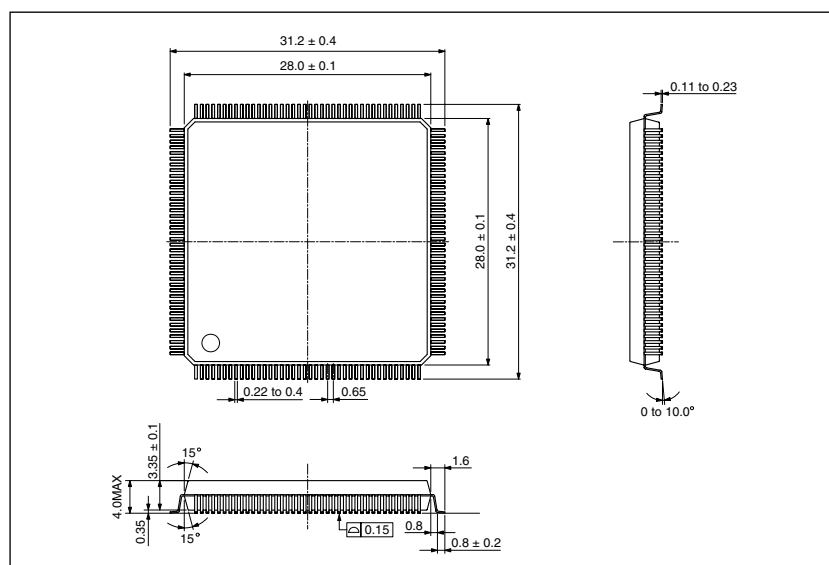
The SM5951A is an 8-channel DSD (Direct Stream Digital) editing system signal processor LSI. It takes 4 DSD input signals per channel, mixes them, and then converts the result back into 1-bit DSD data for output.

FEATURES

- DSD signal sampling rate: 5.6448MHz ($128 \times 44.1\text{kHz}$) and 2.8224MHz ($64 \times 44.1\text{kHz}$) supported
- 8-channel DSD signal mixing
 - 8-channel, 4 DSD signal inputs per channel mixing using arbitrary coefficients for each input
- Raw signal switching function (auto bypass)
 - Automatically switches to raw signal output with no switching noise and no signal degradation when mixing is not required, bypassing the mixing processing
- Input/output format
 - Normal input/output format where the data changes are synchronized to the bit clock cycle, and Manchester-type encoding input/output format where the data inverts during the bit clock cycle
- Monitor output: Simultaneous $64 \times 44.1\text{kHz}$ monitor data output when in $128 \times 44.1\text{kHz}$ sampling rate mode
- Microcontroller interface: Parallel bi-directional 8-bit/16-bit/32-bit data bus supported
- Master clock: 45.1584MHz ($1024 \times 44.1\text{kHz}$) or 56.448MHz ($1280 \times 44.1\text{kHz}$)
- 2 voltage supplies: 3.3V (3.0 to 3.6V) and 2.5V (2.3 to 2.7V)
- Operating temperature range: -20 to 70°C
- Package: 160-pin QFP

PACKAGE DIMENSIONS

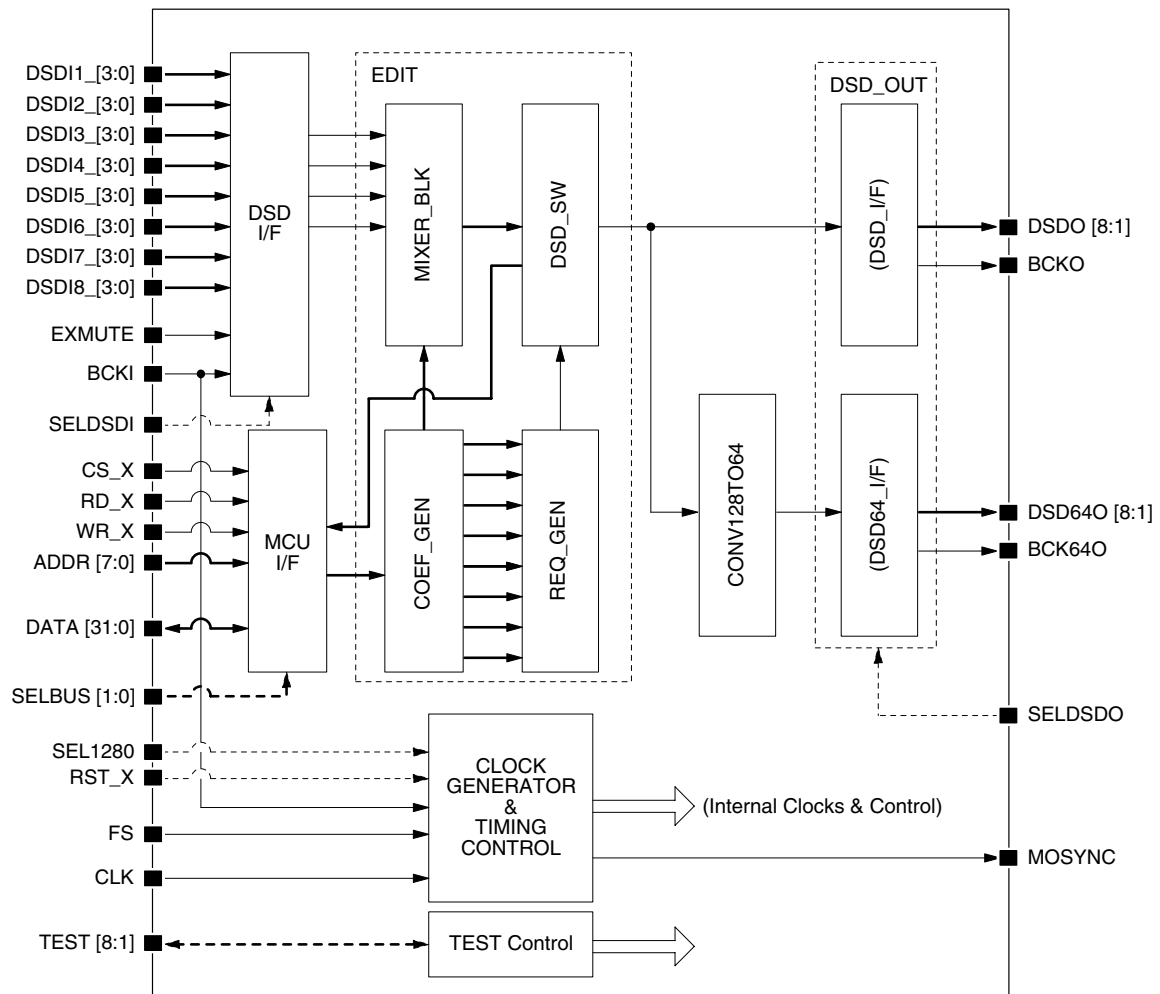
(Unit: mm)



ORDERING INFORMATION

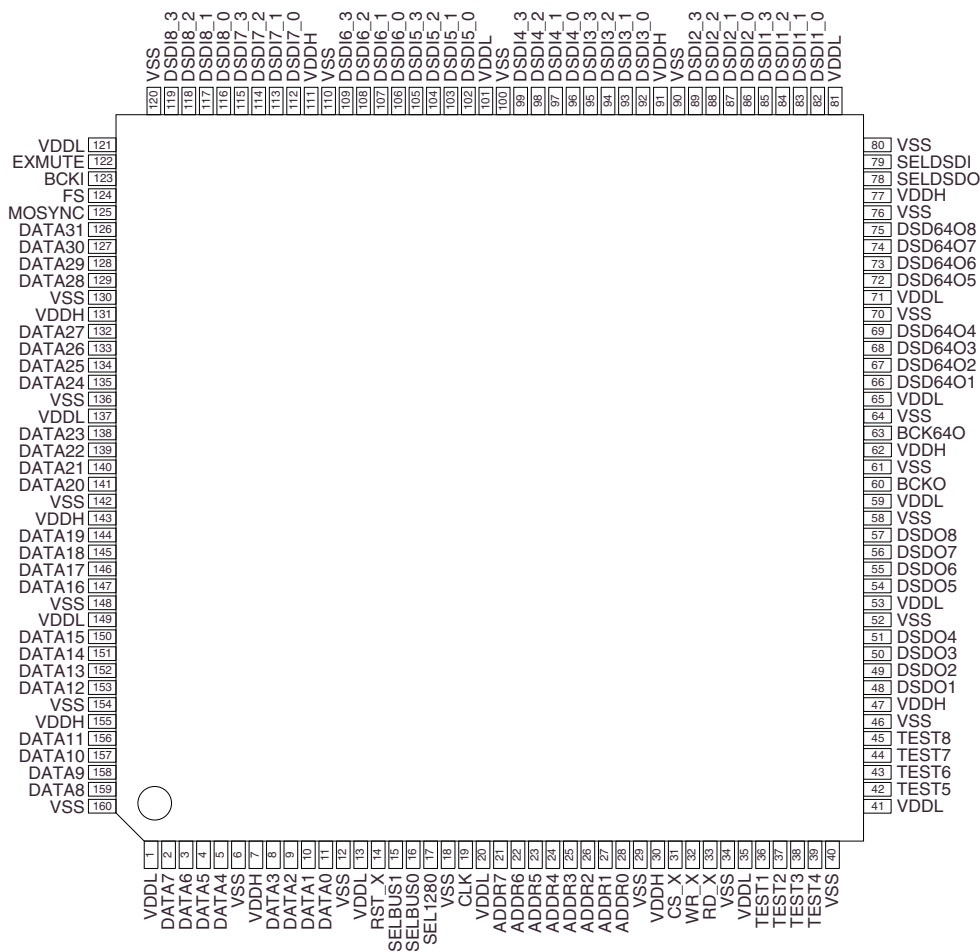
Device	Package
SM5951AF	160-pin QFP

BLOCK DIAGRAM



PINOUT

(Top view)



Pin Layout Table

No.	Name	I/O	No.	Name	I/O	No.	Name	I/O	No.	Name	I/O
1	VDDL	–	41	VDDL	–	81	VDDL	–	121	VDDL	–
2	DATA7	I/O	42	TEST5	I	82	DSDI1_0	I	122	EXMUTE	I
3	DATA6	I/O	43	TEST6	I	83	DSDI1_1	I	123	BCKI	I
4	DATA5	I/O	44	TEST7	I	84	DSDI1_2	I	124	FS	I
5	DATA4	I/O	45	TEST8	I	85	DSDI1_3	I	125	MOSYNC	O
6	VSS	–	46	VSS	–	86	DSDI2_0	I	126	DATA31	I/O
7	VDDH	–	47	VDDH	–	87	DSDI2_1	I	127	DATA30	I/O
8	DATA3	I/O	48	DSDO1	O	88	DSDI2_2	I	128	DATA29	I/O
9	DATA2	I/O	49	DSDO2	O	89	DSDI2_3	I	129	DATA28	I/O
10	DATA1	I/O	50	DSDO3	O	90	VSS	–	130	VSS	–
11	DATA0	I/O	51	DSDO4	O	91	VDDH	–	131	VDDH	–
12	VSS	–	52	VSS	–	92	DSDI3_0	I	132	DATA27	I/O
13	VDDL	–	53	VDDL	–	93	DSDI3_1	I	133	DATA26	I/O
14	RST_X	I	54	DSDO5	O	94	DSDI3_2	I	134	DATA25	I/O
15	SELBUS1	I	55	DSDO6	O	95	DSDI3_3	I	135	DATA24	I/O
16	SELBUS0	I	56	DSDO7	O	96	DSDI4_0	I	136	VSS	–
17	SEL1280	I	57	DSDO8	O	97	DSDI4_1	I	137	VDDL	–
18	VSS	–	58	VSS	–	98	DSDI4_2	I	138	DATA23	I/O
19	CLK	I	59	VDDL	–	99	DSDI4_3	I	139	DATA22	I/O
20	VDDL	–	60	BCKO	O	100	VSS	–	140	DATA21	I/O
21	ADDR7	I	61	VSS	–	101	VDDL	–	141	DATA20	I/O
22	ADDR6	I	62	VDDH	–	102	DSDI5_0	I	142	VSS	–
23	ADDR5	I	63	BCK64O	O	103	DSDI5_1	I	143	VDDH	–
24	ADDR4	I	64	VSS	–	104	DSDI5_2	I	144	DATA19	I/O
25	ADDR3	I	65	VDDL	–	105	DSDI5_3	I	145	DATA18	I/O
26	ADDR2	I	66	DSD64O1	O	106	DSDI6_0	I	146	DATA17	I/O
27	ADDR1	I	67	DSD64O2	O	107	DSDI6_1	I	147	DATA16	I/O
28	ADDR0	I	68	DSD64O3	O	108	DSDI6_2	I	148	VSS	–
29	VSS	–	69	DSD64O4	O	109	DSDI6_3	I	149	VDDL	–
30	VDDH	–	70	VSS	–	110	VSS	–	150	DATA15	I/O
31	CS_X	I	71	VDDL	–	111	VDDH	–	151	DATA14	I/O
32	WR_X	I	72	DSD64O5	O	112	DSDI7_0	I	152	DATA13	I/O
33	RD_X	I	73	DSD64O6	O	113	DSDI7_1	I	153	DATA12	I/O
34	VSS	–	74	DSD64O7	O	114	DSDI7_2	I	154	VSS	–
35	VDDL	–	75	DSD64O8	O	115	DSDI7_3	I	155	VDDH	–
36	TEST1	I	76	VSS	–	116	DSDI8_0	I	156	DATA11	I/O
37	TEST2	I	77	VDDH	–	117	DSDI8_1	I	157	DATA10	I/O
38	TEST3	I	78	SELDSDO	I	118	DSDI8_2	I	158	DATA9	I/O
39	TEST4	I	79	SELDSDI	I	119	DSDI8_3	I	159	DATA8	I/O
40	VSS	–	80	VSS	–	120	VSS	–	160	VSS	–

PIN DESCRIPTION

Number of Pins	Name	I/O	Polarity ¹	Voltage	Functional Description
1	RST_X	I	PU, S	3.3V	System Reset
1	FS	I	–	3.3V	1fs Clock (44.1kHz)
1	CLK	I	–	3.3V	Master Clock
1	SEL1280	I	PD, S	3.3V	Select Master Clock Rate [HIGH]: 1280 × 44.1kHz, [LOW]: 1024 × 44.1kHz
1	SELDSDI	I	PD, S	3.3V	Select DSD Input Format [HIGH]: Manchester Encoding, [LOW]: Normal
1	SELDSDO	I	PD, S	3.3V	Select DSD Output Format [HIGH]: Manchester Encoding, [LOW]: Normal
2	SELBUS [1:0]	I	PU, S	3.3V	Select MCU Data Bus Width [SELBUS1, SELBUS0] [LOW, LOW]: 8-bit [LOW, HIGH]: 16-bit [HIGH, × (LOW or HIGH)]: 32-bit
1	CS_X	I	PU	3.3V	MCU I/F: Chip Select
1	WR_X	I	PU, S	3.3V	MCU I/F: Write Enable
1	RD_X	I	PU, S	3.3V	MCU I/F: Read Enable
8	ADDR [7:0]	I	PU	3.3V	MCU I/F: Address Bus
32	DATA [31:0]	I/O	3mA	3.3V	MCU I/F: Data Bus
1	BCKI	I	S	3.3V	DSD Input: Bit Clock IN
4	DSDI1_[3:0]	I	–	3.3V	DSD Input: DSD CH1 Data (LINE0 to LINE3)
4	DSDI2_[3:0]	I	–	3.3V	DSD Input: DSD CH2 Data (LINE0 to LINE3)
4	DSDI3_[3:0]	I	–	3.3V	DSD Input: DSD CH3 Data (LINE0 to LINE3)
4	DSDI4_[3:0]	I	–	3.3V	DSD Input: DSD CH4 Data (LINE0 to LINE3)
4	DSDI5_[3:0]	I	–	3.3V	DSD Input: DSD CH5 Data (LINE0 to LINE3)
4	DSDI6_[3:0]	I	–	3.3V	DSD Input: DSD CH6 Data (LINE0 to LINE3)
4	DSDI7_[3:0]	I	–	3.3V	DSD Input: DSD CH7 Data (LINE0 to LINE3)
4	DSDI8_[3:0]	I	–	3.3V	DSD Input: DSD CH8 Data (LINE0 to LINE3)
1	EXMUTE	I	–	3.3V	DSD Input: External Mute Pattern
1	BCKO	O	6mA	3.3V	DSD Output: Bit Clock Out
8	DSDO [8:1]	O	3mA	3.3V	DSD Output: DSD Output DATA (CH1 to CH8)
1	BCK64O	O	6mA	3.3V	DSD 64fs Output: Bit Clock Out
8	DSD64O [8:1]	O	3mA	3.3V	DSD 64fs Output: DSD Output DATA (CH1 to CH8)
1	MOSYNC	O	3mA	3.3V	SYNC Monitor
8	TEST [8:1]	I	PD	3.3V	IOTEST_EN, SCAN_EN, ATPG_EN, FUNC_MODE etc.
10	VDDH	–	–	3.3V	Power Supply (I/O)
14	VDDL	–	–	2.5V	Power Supply (Core)
24	VSS	–	–	0V	Ground Level

1. Attributes: S = Schmitt type, PU = with pull-up resistor, PD = with pull-down resistor, mA = output current

SPECIFICATIONS

Absolute Maximum Ratings

$V_{SS} = 0V$

Parameter	Symbol	Rating	Unit
Supply voltage 1	V_{DDH}	- 0.3 to 4.0	V
Supply voltage 2	V_{DDL}	- 0.3 to 3.0	V
Input voltage (3.3V)	V_{IN}	- 0.3 to $V_{DDH} + 0.5$	V
Power dissipation	P_D	1.3	W
Storage temperature range	T_{STG}	- 55 to 125	°C

Recommended Operating Conditions

$V_{SS} = 0V$

Parameter	Symbol	Rating	Unit
Supply voltage 1	V_{DDH}	3.0 to 3.6	V
Supply voltage 2	V_{DDL}	2.3 to 2.7	V
Operating temperature	T_{OPR}	- 20 to 70	°C

Electrical Characteristics

DC Characteristics

$V_{DDH} = 3.0$ to $3.6V$, $V_{DDL} = 2.3$ to $2.7V$, $V_{SS} = 0V$, $T_{OPR} = - 20$ to $70^{\circ}C$, unless otherwise noted

Parameter	Pins	Symbol	Condition	Rating			Unit	
				min	typ	max		
Current consumption 1	V_{DDH}	I_{DDH}	All pins no load	-	-	8	mA	
Current consumption 2	V_{DDL}	I_{DDL}	All pins no load	-	-	550	mA	
Input voltage	HIGH-level	(*1)	V_{IH}	$V_{DDH} = 3.6V$	2.0	-	-	V
	LOW-level	(*1)	V_{IL}	$V_{DDH} = 3.0V$	-	-	0.8	V
Schmitt trigger voltage	Positive	(*2)	V_{T+}		1.1	-	2.4	V
	Negative	(*2)	V_{T-}		0.6	-	1.8	V
Hysteresis voltage	(*2)	V_H			0.1	-	-	V
Output voltage	HIGH-level	(*3)	V_{OH}	$I_{OH} = - 3mA$ (Type 1), $- 6mA$ (Type 2)	V_{DDH}	-	-	V
	LOW-level	(*3)	V_{OL}	$I_{OL} = 3mA$ (Type 1), $6mA$ (Type 2)	-	-	0.4	V
Input leakage current	(*1) (*2)	I_{LI}			- 5	-	5	μA
Pull-down resistance	(*4)	R_{PD}	$V_I = V_{DDH}$		60	120	288	$k\Omega$
Pull-up resistance	(*5)	R_{PU}	$V_I = V_{SS}$		60	120	288	$k\Omega$
HIGH-level holding current	(*6)	I_{BHH}	$V_{IN} = 2.0V$, $V_{DDH} = 3.0V$		-	-	- 20	μA
LOW-level holding current	(*6)	I_{BHL}	$V_{IN} = 0.8V$, $V_{DDH} = 3.0V$		-	-	17	μA
HIGH-level reverse current	(*6)	I_{BHHO}	$V_{IN} = 0.8V$, $V_{DDH} = 3.6V$		- 350	-	-	μA
LOW-level reverse current	(*6)	I_{BHLO}	$V_{IN} = 2.0V$, $V_{DDH} = 3.6V$		210	-	-	μA

Pin summary

(*1)	Input pins and bi-directional pins in input mode
(*2)	Schmitt-characteristic inputs and bi-directional pins in input mode
(*3)	Output pins and bi-directional pins in output mode
	Type 2: BCKO, BCK64O Type 1: All outputs excluding those above
(*4)	Inputs with pull-down resistor
(*5)	Inputs with pull-up resistor
(*6)	Input/outputs with bus hold circuit (DATA [31:0])

AC Characteristics

$V_{DDH} = 3.0$ to $3.6V$, $V_{DDL} = 2.3$ to $2.7V$, $V_{SS} = 0V$, $T_{OPR} = -20$ to $70^{\circ}C$ unless otherwise noted.

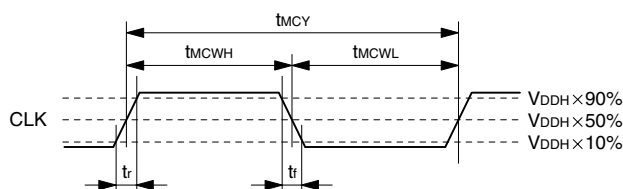
When $f_s = 44.1kHz$, the FS and BCKI clock inputs have the following frequency division relationship to the master clock input on CLK.

- When CLK = 1024fs:
 - (FS) cycle = $1024 \times CLK$ cycles
 - (BCKI) cycle [128fs mode] = $8 \times CLK$ cycles (128fs)
 - (BCKI) cycle [64fs mode] = $16 \times CLK$ cycles (64fs)
- When CLK = 1280fs:
 - (FS) cycle = $1280 \times CLK$ cycles
 - (BCKI) cycle [128fs mode] = $10 \times CLK$ cycles (128fs)
 - (BCKI) cycle [64fs mode] = $20 \times CLK$ cycles (64fs)

System clock input

- CLK pin

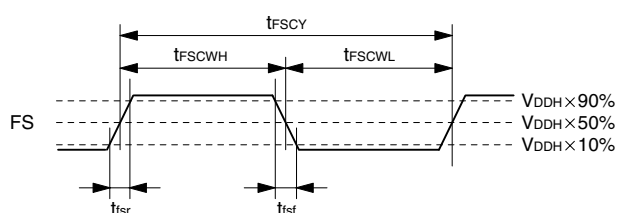
Parameter	Symbol	Rating			Unit
		min	typ	max	
HIGH-level pulsewidth	t_{MCWH}	7	11.07 (1024fs) 8.86 (1280fs)	—	ns
LOW-level pulsewidth	t_{MCWL}	7	11.07 (1024fs) 8.86 (1280fs)	—	ns
Pulse cycle	t_{MCY}	16	22.14 (1024fs) 17.72 (1280fs)	—	ns
Rise/Fall time	t_r, t_f	—	—	2	ns



1FS clock input

- FS pin (44.1kHz)

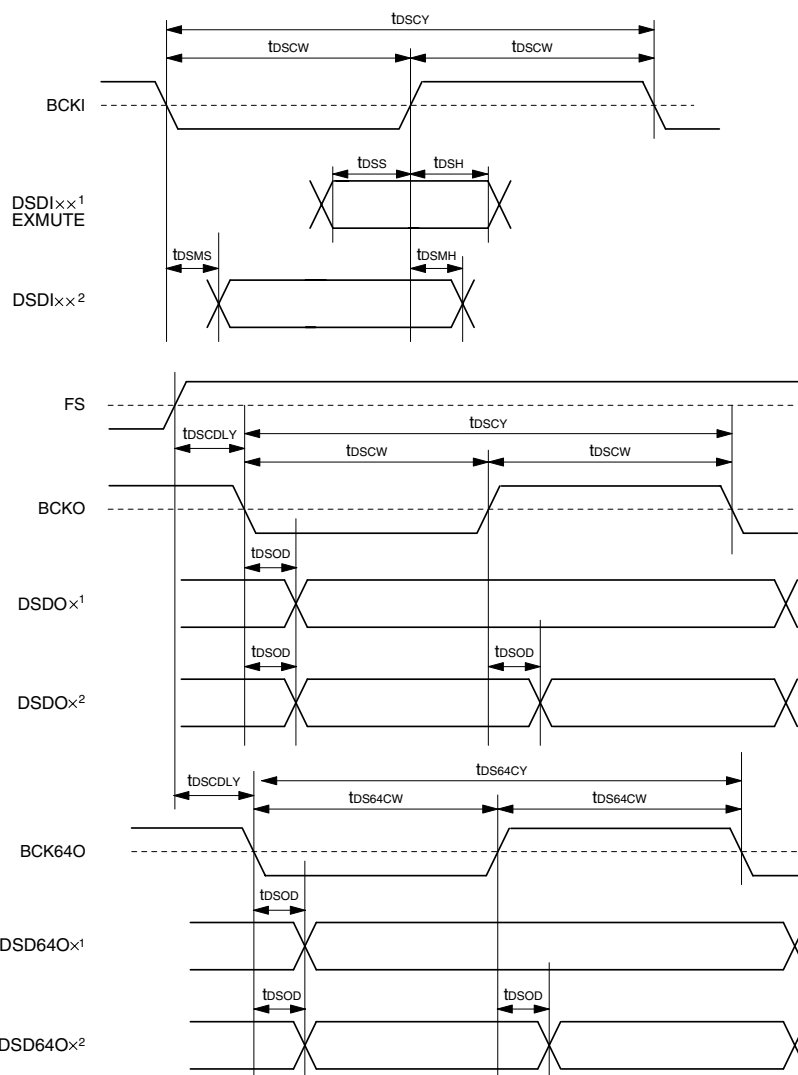
Parameter	Symbol	Rating			Unit
		min	typ	max	
HIGH-level pulsewidth	t_{FSCWH}	—	11.34	—	μs
LOW-level pulsewidth	t_{FSCWL}	—	11.34	—	μs
Pulse cycle	t_{FSCY}	—	22.68	—	μs
Rise/Fall time	t_{fsr}, t_{fsf}	—	—	10	ns



DSD input/output

FS, BCKI, DSDI $\times\times$, EXMUTE, BCKO, BCK64O, DSDO \times , DSD64O \times pins

Parameter	Symbol	Rating			Unit
		min	typ	max	
DSD bit clock pulsewidth	t_{DSCW}	80	177.16 (1/64fs) 88.58 (1/128fs)	—	ns
DSD bit clock pulse cycle	t_{DSCY}	—	354.31 (1/64fs) 177.16 (1/128fs)	—	ns
DSD 64fs bit clock output pulsewidth	t_{DS64CW}	—	177.16	—	ns
DSD 64fs clock output pulse cycle	t_{DS64CY}	—	354.31	—	ns
DSD data input setup time ¹	t_{DSS}	35	—	—	ns
DSD data input hold time ¹	t_{DSH}	35	—	—	ns
DSD data input setup time ²	t_{DSMS}	—	—	18	ns
DSD data input hold time ²	t_{DSMH}	0	—	—	ns
DSD data output delay time	t_{DSOD}	0	—	10	ns
DSD bit clock output delay time ³	t_{DSCDLY}	0	—	88	ns

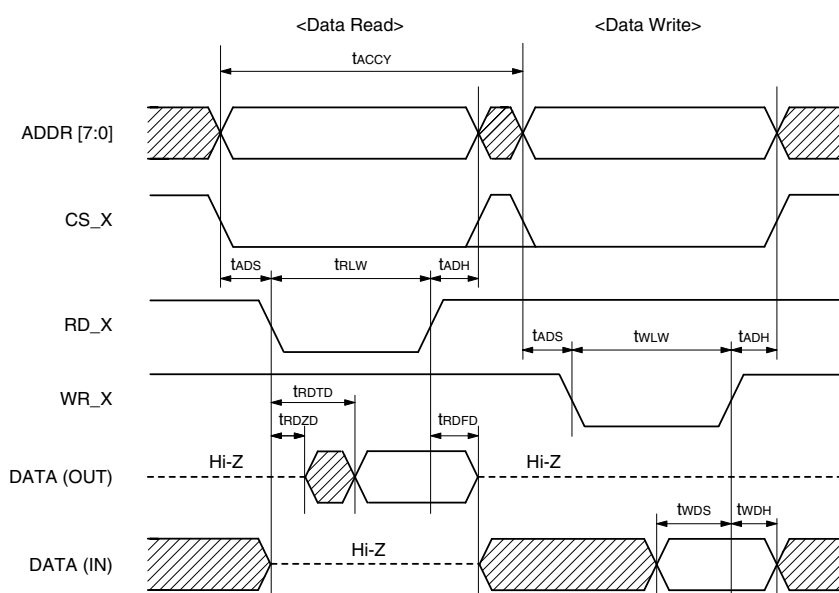


1. Normal mode rating (input data setup time is referenced to the BCKI rising edge)
2. Manchester-type mode rating (input data setup time is referenced to the BCKI falling edge)
3. The delay in the state of internal synchronization relative to the FS input edge

MCU interface

- ADDR [7:0], CS_X, RD_X, WR_X, DATA [31:0] pins

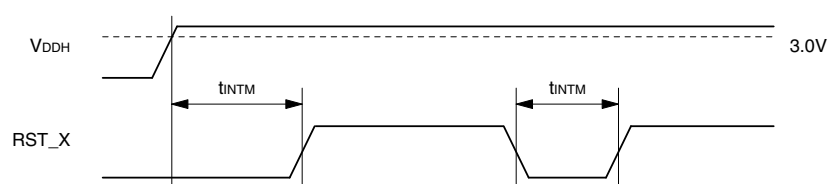
Parameter	Symbol	Rating			Unit
		min	typ	max	
Access cycle time	t_{ACCY}	150	–	–	ns
ADDR, CS_X setup time	t_{ADS}	10	–	–	ns
ADDR, CS_X hold time	t_{ADH}	10	–	–	ns
RD_X pulsewidth	t_{RLW}	100	–	–	ns
WR_X pulsewidth	t_{WLW}	100	–	–	ns
Read data output delay time	t_{RDZD}	0	–	20	ns
Read data defined delay time	t_{RDTD}	0	–	60	ns
Read data output floating delay time	t_{RDFD}	0	–	10	ns
Write data input setup time	t_{WDS}	20	–	–	ns
Write data input hold time	t_{WDH}	10	–	–	ns



Initialization

- RST_X pin

Parameter	Symbol	Rating			Unit
		min	typ	max	
Initialization time	t_{INTM}	$6 \times t_{\text{MCY}}$	–	–	ns



FUNCTIONAL DESCRIPTION

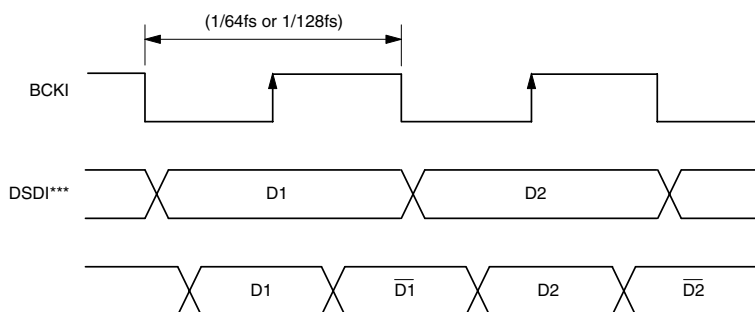
Data Input/Output Format

DSD input format

The DSD input format can be set to one of 2 types by the state of SELDSDI.

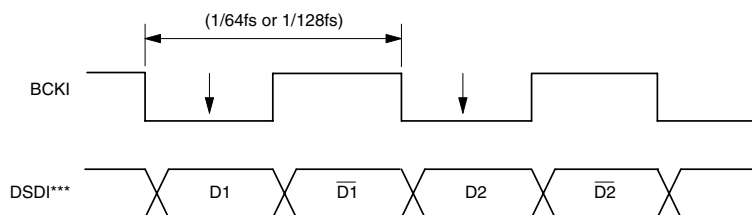
(1) Normal mode (SELDSDI = LOW)

DSD input data is read in close to the rising edge of the bit clock BCKI. Note that even if the input is phase modulated, the data is still read in close to the rising edge of BCKI if the data is defined.



(2) Manchester-type input (SELDSDI = HIGH)

DSD input data is read in during the LOW-level pulse of the bit clock BCKI.



Note. DSDI***: DSDI1_[3:0], DSDI2_[3:0], DSDI3_[3:0], DSDI4_[3:0], DSDI5_[3:0], DSDI6_[3:0], DSDI7_[3:0], DSDI8_[3:0] pins

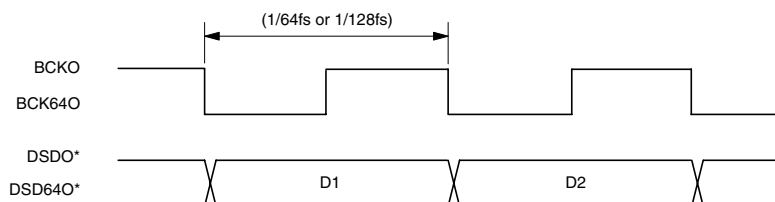
Note. When an external mute pattern is input on EXMUTE pin, data is read in normal mode format only, regardless of the state of SELDSDI.

DSD output format

The DSD output format can be set to one of 2 types by the state of SELDSDO.

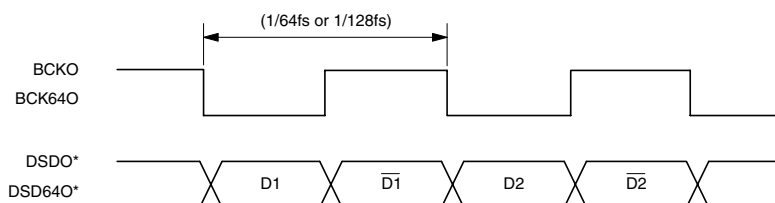
(1) Normal mode (SELDSDO = LOW)

DSD output data transitions occur on the falling edge of the bit clock BCKO.



(2) Manchester-type output (SELDSDO = HIGH)

DSD output data transitions occur on the falling edge of the bit clock BCKO and then inverts on the rising edge of the bit clock BCKO.



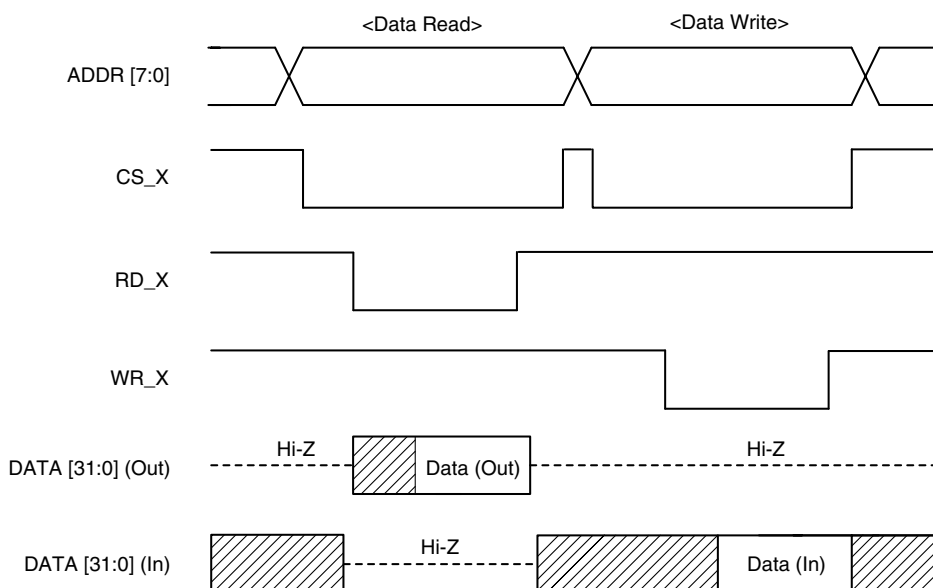
Note. DSDO*: DSDO [8:1] pins, DSD64O*: DSD64O [8:1] pins

MCU Interface

Bus access control

The internal mode and coefficients can be set using either 8/16/32-bit data bus, facilitating easy connection to various kinds of MCU bus.

The data bus control pins are active LOW. When the chip select (CS_X) is active, read/write control inputs are valid. When write control (WR_X) is active, data is written in on the rising edge. Data is read out when the read control (RD_X) is active.

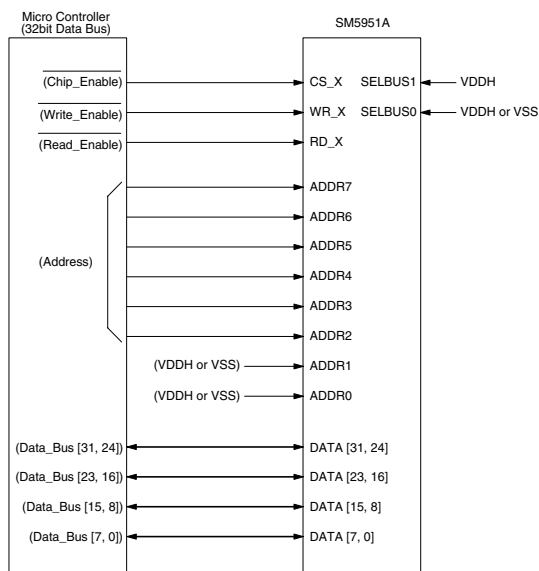


Note. DATA [31:0] pins have an additional bus hold circuit which holds the previous data even when the pin is in a high-impedance ("Hi-Z") state.

Data bus width selection

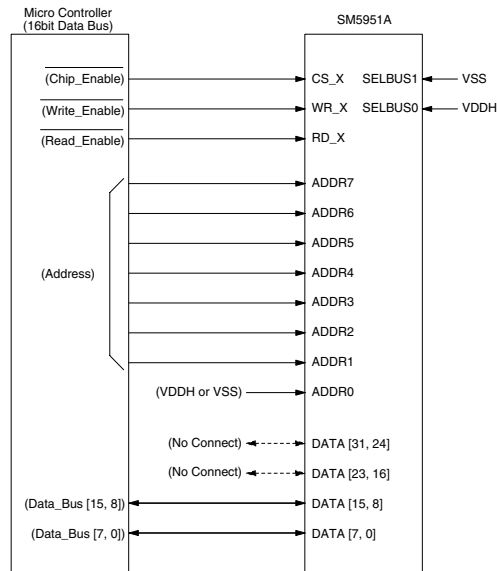
The width of the data bus for data access can be set to one of 3 types by the state of the SELBUS [1:0] pins.

(1) 32-bit bus: SELBUS [1:0] = (1, ×)



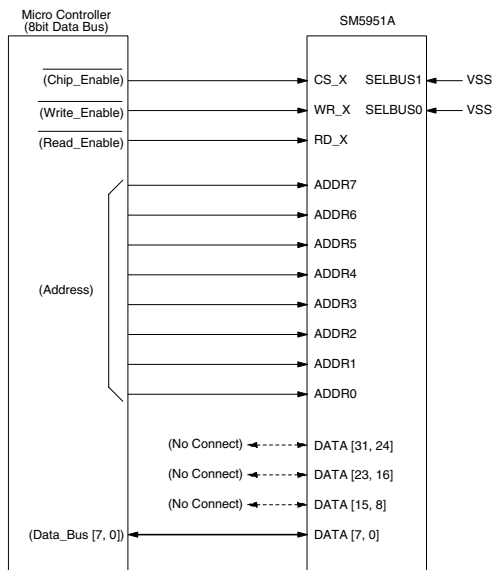
Note. ADDR [1:0] pins are not used.

(2) 16-bit bus: SELBUS [1:0] = (0, 1)



Note. ADDR0, DATA [31:16] pins are not used.

(3) 8-bit bus: SELBUS [1:0] = (0, 0)



Note. DATA [31:8] pins are not used.

Internally, parameter settings and data are handled in 32-bit units, while the memory area addresses are handled in 8-bit units. For 8-bit and 16-bit access bus widths, the 2 least significant address bits (ADDR [1:0]) are used to determine which internal data bits are accessed as shown in the following table.

Internal Data bit	32-bit Access		16-bit Access		8-bit Access	
	ADDR [1:0]	Data Pin	ADDR [1:0]	Data Pin	ADDR [1:0]	Data Pin
7-0 bit	(×, ×)	DATA [7:0]	(0, ×)	DATA [7:0]	(0, 0)	DATA [7:0]
15-8 bit	(×, ×)	DATA [15:8]	(0, ×)	DATA [15:8]	(0, 1)	DATA [7:0]
23-16 bit	(×, ×)	DATA [23:16]	(1, ×)	DATA [7:0]	(1, 0)	DATA [7:0]
31-24 bit	(×, ×)	DATA [31:24]	(1, ×)	DATA [15:8]	(1, 1)	DATA [7:0]

Note. "×" in the address column are don't care bits.

Address mapping

Address	Read/ Write	Initial Value	DATA Bit							
			31	24	23	16	15	8	7	0
03h-00h	R/W	xxxxxxxx8Bh						Control [7] = OFFPAT [6] = DCONVEN [5:4] = DITH [1:0] [3] = DITHEN [2] = MUTESEL [1] = DSD128 [0] = SRESET		
07h-04h	R	–	Switching Status [31:28] = STAT_CH8 [27:24] = STAT_CH7		[23:20] = STAT_CH6 [19:16] = STAT_CH5		[15:12] = STAT_CH4 [11:8] = STAT_CH3		[7:4] = STAT_CH2 [3:0] = STAT_CH1	
0Bh-08h	R/W	xx076543h			Pattern Match NO. [23:20] = (reserved) [19:16] = MATCH8		[15:12] = MATCH7 [11:8] = MATCH6		[7:4] = MATCH5 [3:0] = MATCH4	
0Fh-0Ch	R	–	Matching Status [31:28] = MATCH_CH8 [27:24] = MATCH_CH7		[23:20] = MATCH_CH6 [19:16] = MATCH_CH5		[15:12] = MATCH_CH4 [11:8] = MATCH_CH3		[7:4] = MATCH_CH2 [3:0] = MATCH_CH1	
13h-10h	R/W	xx152B6Bh			Delay Offset [23:21] = (reserved) [20:16] = DLY_DOWN		[15] = (reserved) [14:8] = DLY_64		[7] = (reserved) [6:0] = DLY_128	
7Fh-14h	–	–								
83h-80h	R/W	xx000000h			CH1 Coefficient [23:0] = CH1COEF1					
87h-84h	R/W	xx000000h			[23:0] = CH1COEF2					
8Bh-88h	R/W	xx000000h			[23:0] = CH1COEF3					
8Fh-8Ch	R/W	xx000000h			[23:0] = CH1COEF4					
93h-90h	R/W	xx000000h			CH2 Coefficient [23:0] = CH2COEF1					
97h-94h	R/W	xx000000h			[23:0] = CH2COEF2					
9Bh-98h	R/W	xx000000h			[23:0] = CH2COEF3					
9Fh-9Ch	R/W	xx000000h			[23:0] = CH2COEF4					
A3h-A0h	R/W	xx000000h			CH3 Coefficient [23:0] = CH3COEF1					
A7h-A4h	R/W	xx000000h			[23:0] = CH3COEF2					
ABh-A8h	R/W	xx000000h			[23:0] = CH3COEF3					
AFh-ACh	R/W	xx000000h			[23:0] = CH3COEF4					
B3h-B0h	R/W	xx000000h			CH4 Coefficient [23:0] = CH4COEF1					
B7h-B4h	R/W	xx000000h			[23:0] = CH4COEF2					
BBh-B8h	R/W	xx000000h			[23:0] = CH4COEF3					
BFh-BCh	R/W	xx000000h			[23:0] = CH4COEF4					
C3h-C0h	R/W	xx000000h			CH5 Coefficient [23:0] = CH5COEF1					
C7h-C4h	R/W	xx000000h			[23:0] = CH5COEF2					
CBh-C8h	R/W	xx000000h			[23:0] = CH5COEF3					
CFh-CCh	R/W	xx000000h			[23:0] = CH5COEF4					
D3h-D0h	R/W	xx000000h			CH6 Coefficient [23:0] = CH6COEF1					
D7h-D4h	R/W	xx000000h			[23:0] = CH6COEF2					
DBh-D8h	R/W	xx000000h			[23:0] = CH6COEF3					
DFh-DCh	R/W	xx000000h			[23:0] = CH6COEF4					
E3h-E0h	R/W	xx000000h			CH7 Coefficient [23:0] = CH7COEF1					
E7h-E4h	R/W	xx000000h			[23:0] = CH7COEF2					
EBh-E8h	R/W	xx000000h			[23:0] = CH7COEF3					
EFh-ECh	R/W	xx000000h			[23:0] = CH7COEF4					
F3h-F0h	R/W	xx000000h			CH8 Coefficient [23:0] = CH8COEF1					
F7h-F4h	R/W	xx000000h			[23:0] = CH8COEF2					
FBh-F8h	R/W	xx000000h			[23:0] = CH8COEF3					
FFh-FCh	R/W	xx000000h			[23:0] = CH8COEF4					

Switching status

The following addresses are used to monitor the switching status. This area of memory is read-only.

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
04h	STAT_CH2 [3:0]				STAT_CH1 [3:0]			
Address	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
05h	STAT_CH4 [3:0]				STAT_CH3 [3:0]			
Address	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
06h	STAT_CH6 [3:0]				STAT_CH5 [3:0]			
Address	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
07h	STAT_CH8 [3:0]				STAT_CH7 [3:0]			

The value of each address indicates the following operating status.

- 0 : Input DSD data is being passed directly to the output
- 1 : Switching from direct output (state 0) to internal computation output
- 4 : Internal DSM computation result signal is being output
- 7 to 9 : Switching from state 4 to state 0
- Other : Not used

Setting the number of pattern matching bits

The following addresses are used to set the minimum number of matching bits in each stage of the DSD input signal switching process during mixing.

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
08h	MATCH5 [3:0]				MATCH4 [3:0]			
Address	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
09h	MATCH7 [3:0]				MATCH6 [3:0]			
Address	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
0Ah	(reserved)				MATCH8 [3:0]			
Address	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
0Bh	(reserved)				(reserved)			

- MATCH8 [3:0] (Number of matching bits in 1st stage) – 1, (default = 7)
- MATCH7 [3:0] (Number of matching bits in 2nd stage) – 1, (default = 6)
- MATCH6 [3:0] (Number of matching bits in 3rd stage) – 1, (default = 5)
- MATCH5 [3:0] (Number of matching bits in 4th stage) – 1, (default = 4)
- MATCH4 [3:0] (Number of matching bits in 5th stage) – 1, (default = 3)

Reading the number of pattern matching bits

The following addresses are used to read out the number of matching bits in each stage of the DSD input signal switching process during mixing.

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Ch	MATCH_CH2 [3:0]				MATCH_CH1 [3:0]			
Address	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0Dh	MATCH_CH4 [3:0]				MATCH_CH3 [3:0]			
Address	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
0Eh	MATCH_CH6 [3:0]				MATCH_CH5 [3:0]			
Address	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
0Fh	MATCH_CH8 [3:0]				MATCH_CH7 [3:0]			

MATCH_CH1 [3:0]	(Number of channel 1 matching bits) – 1
MATCH_CH2 [3:0]	(Number of channel 2 matching bits) – 1
MATCH_CH3 [3:0]	(Number of channel 3 matching bits) – 1
MATCH_CH4 [3:0]	(Number of channel 4 matching bits) – 1
MATCH_CH5 [3:0]	(Number of channel 5 matching bits) – 1
MATCH_CH6 [3:0]	(Number of channel 6 matching bits) – 1
MATCH_CH7 [3:0]	(Number of channel 7 matching bits) – 1
MATCH_CH8 [3:0]	(Number of channel 8 matching bits) – 1

Output delay correction

These addresses are used to set the mixing delay correction for the DSD input. The setting adjusts the time from DSD input to DSD output by an internal delay in units of the DSD rate. The actual adjustment is the value written to memory + 1.

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
10h	(reserved)	DLY_128 [6:0]						
Address	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
11h	(reserved)	DLY_64 [6:0]						
Address	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
12h	(reserved)			DLY_DOWN [4:0]				
Address	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
13h	(reserved)							

DLY_128 [6:0]	(default = 107)	: Delay value when sample rate is 128fs
DLY_64 [6:0]	(default = 43)	: Delay value when sample rate is 64fs
DLY_DOWN [4:0]	(default = 21)	: Delay value when down sampling from DSDO (128fs) to DSD64O (64fs)

Coefficients

The address space 80h to FFh contains 32 coefficient registers, comprising independent mixing coefficients for the 4 DSD inputs for each of the 8 channels.

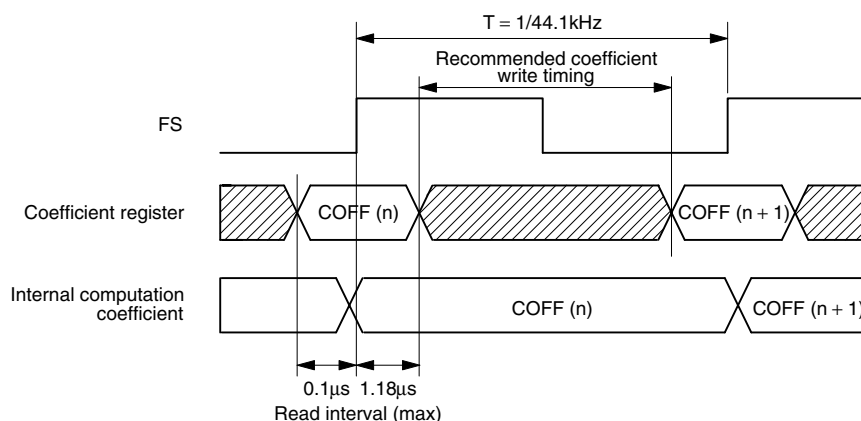
CHnCOEFm [23:0]: n-channel m-input coefficient (default = 0)

Coefficients are represented in linear, 2s-complement, 24-bit format. Minus coefficients have inverted polarity. Gain setting and positive/inverse (minus) polarity are represented as follows:

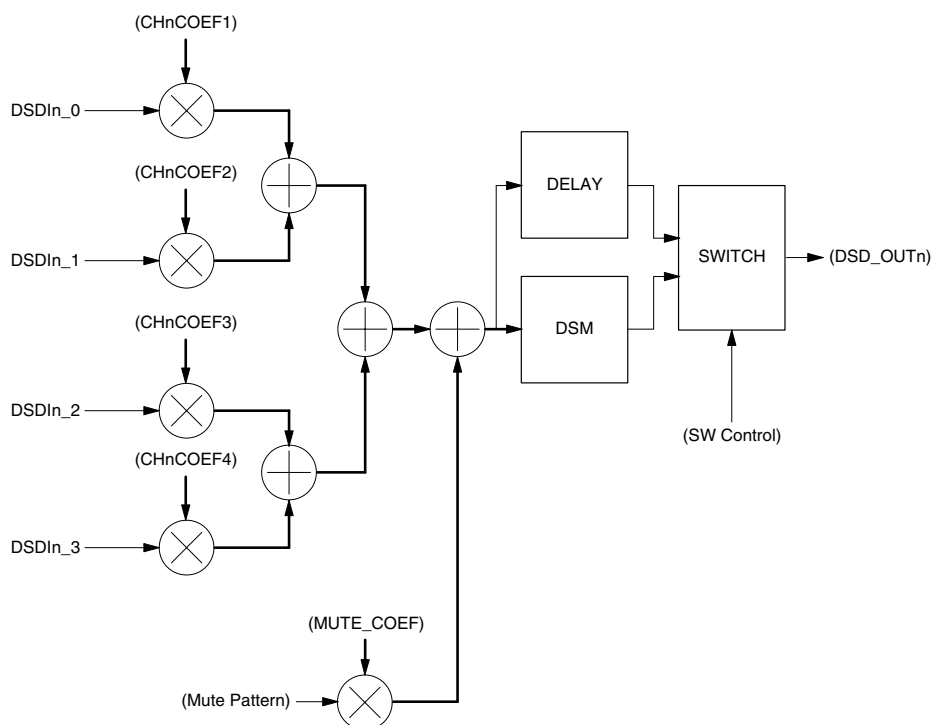
Positive: 0dB (input level \times 1.0) = 080000h Positive maximum: 7FFFFFFh (+ 24dB)
 Inverse : 0dB (input level \times - 1.0) = F80000h Inverse maximum : 800000h (+ 24dB)

Note 1: When the gain setting is $\geq +12$ dB, $\Delta\Sigma$ modulator saturation during requantization may cause noise to increase considerably.

Note 2: Coefficients are read in during an interval close to the rising edge of FS (44.1kHz). If coefficient data write timing starts and/or ends in this interval, computation using written-in data can be uncertain for an interval of $1f_s$ until it's certainly renewed at the next fetch timing. Hence, writing coefficient data during this interval should be avoided.



Mixing



Input signal mixing

This stage mixes the 4 DSD input signals on each channel. Each DSD signal is multiplied by its corresponding coefficient and then added, and the result is converted back into a 1-bit DSD signal by a $\Delta\Sigma$ modulator.

The DSD input signal represents + 1.0 when HIGH and - 1.0 when LOW.

If the mute pattern is selected during mixing, the muting coefficients are also multiplied and added.

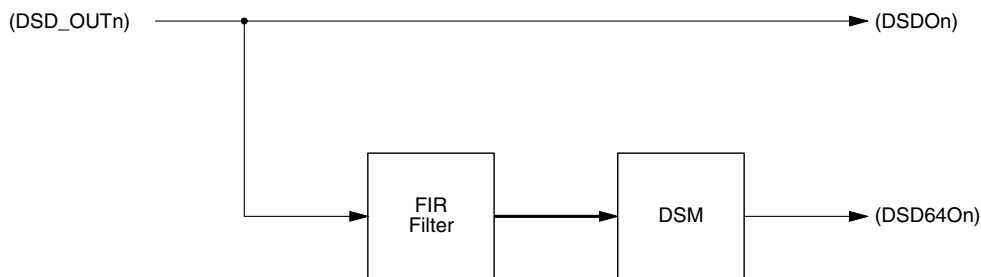
Coefficient interpolation and output switching

The mixing coefficients are read in every $1f_s$ cycle, and linearly interpolated for each DSD sample. The mute pattern coefficients are automatically calculated from the other input coefficients.

If one of the 4 DSD input coefficients is 1.0 or - 1.0 and the other 3 input coefficients are all 0, the corresponding DSD input is switched directly to the output through a delay circuit, avoiding any signal degradation caused by the $\Delta\Sigma$ modulator. If all 4 coefficients are 0, the mute pattern path is switched and output through the delay circuit.

The DSM ($\Delta\Sigma$ modulator) bypass condition is automatically calculated from the individual coefficients. The bypass switching occurs when the DSM output matches the delayed output pattern in order to minimize noise generation.

128fs → 64fs Down Conversion



The 128fs DSD output is passed through a 51-tap FIR filter that cuts high-frequency noise, then it is down-sampled to 64fs. The signal is reconverted by a $\Delta\Sigma$ modulator into a 64fs DSD signal for output on DSO64On.

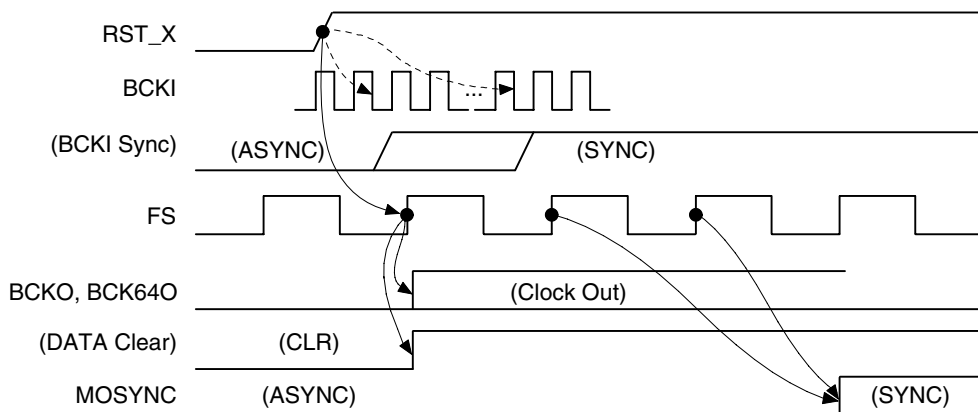
Synchronization

Input clock synchronization

The internal computation and interface operation timing are based on the internal word clock's word boundary signal (ENFS), regardless of the BCKI input state, so that they are always synchronized. They are synchronized on the first rising edge of the word clock input on FS after initialization by pin RST_X rising edge or writing to the SRESET bit (AD = 00h) of the control register. Also, BCKI is synchronized on the first falling edge after initialization.

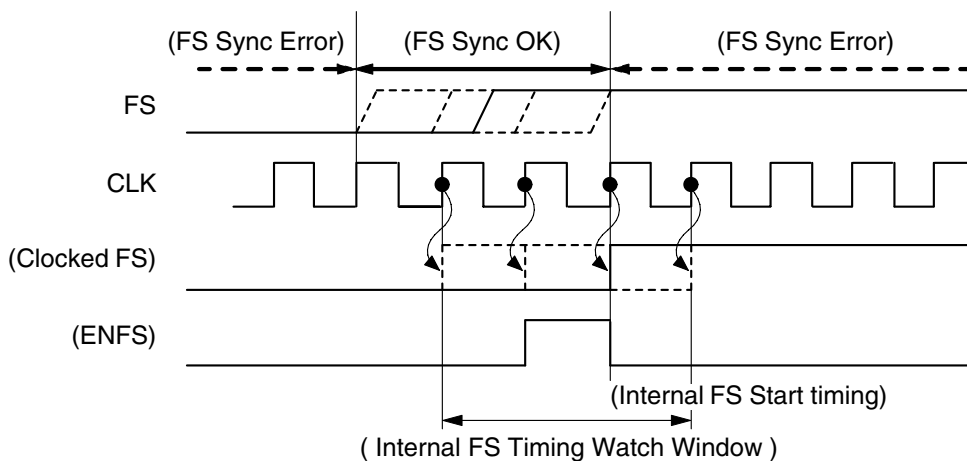
The internal synchronization status can be monitored on pin MOSYNC. The BCKI and FS synchronization status are checked at the beginning of the word clock cycle. If synchronization is maintained for 2 consecutive word clock cycles, MOSYNC goes HIGH, with the same timing as FS, to indicate successful synchronization.

MOSYNC immediately goes LOW whenever BCKI or FS lose synchronization, indicating resynchronization is required.



Monitoring word clock synchronization

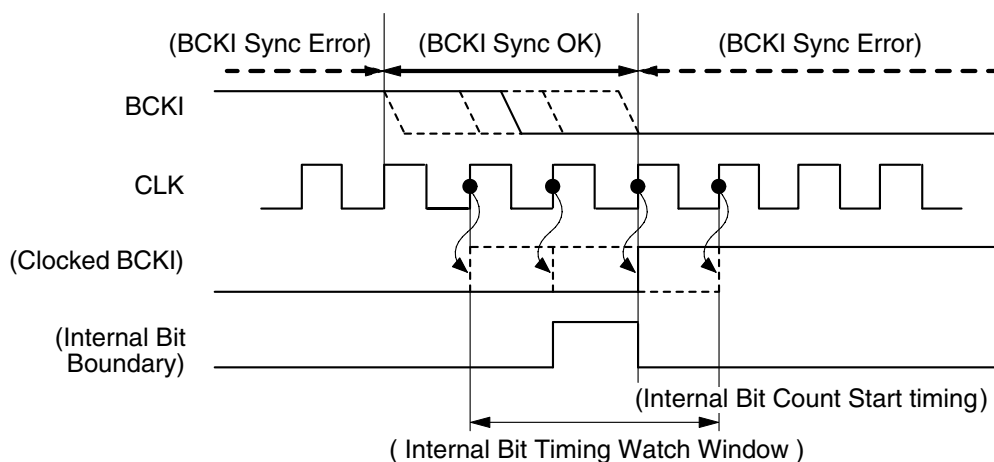
The FS input rising edge synchronization status is always monitored internally. It is monitored in a window -2 to $+1$ master clock cycles wide relative to the current synchronization timing. If the FS input rising edge occurs outside the window, an FS synchronization error occurs and resynchronization is required.



Word Boundary Timing

Monitoring input bit clock synchronization

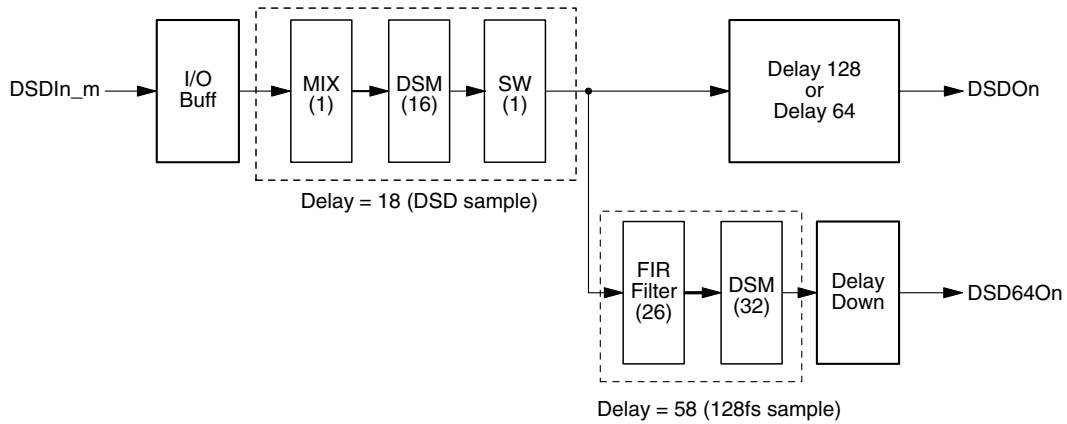
The BCKI input falling edge synchronization status is always monitored internally. It is monitored in a window -2 to $+1$ master clock cycles wide relative to the current synchronization timing. If the BCKI input falling edge occurs outside the window, a BCKI synchronization error occurs and resynchronization is required.



Bit Boundary Timing

DSD Signal Delay Information and Adjustment

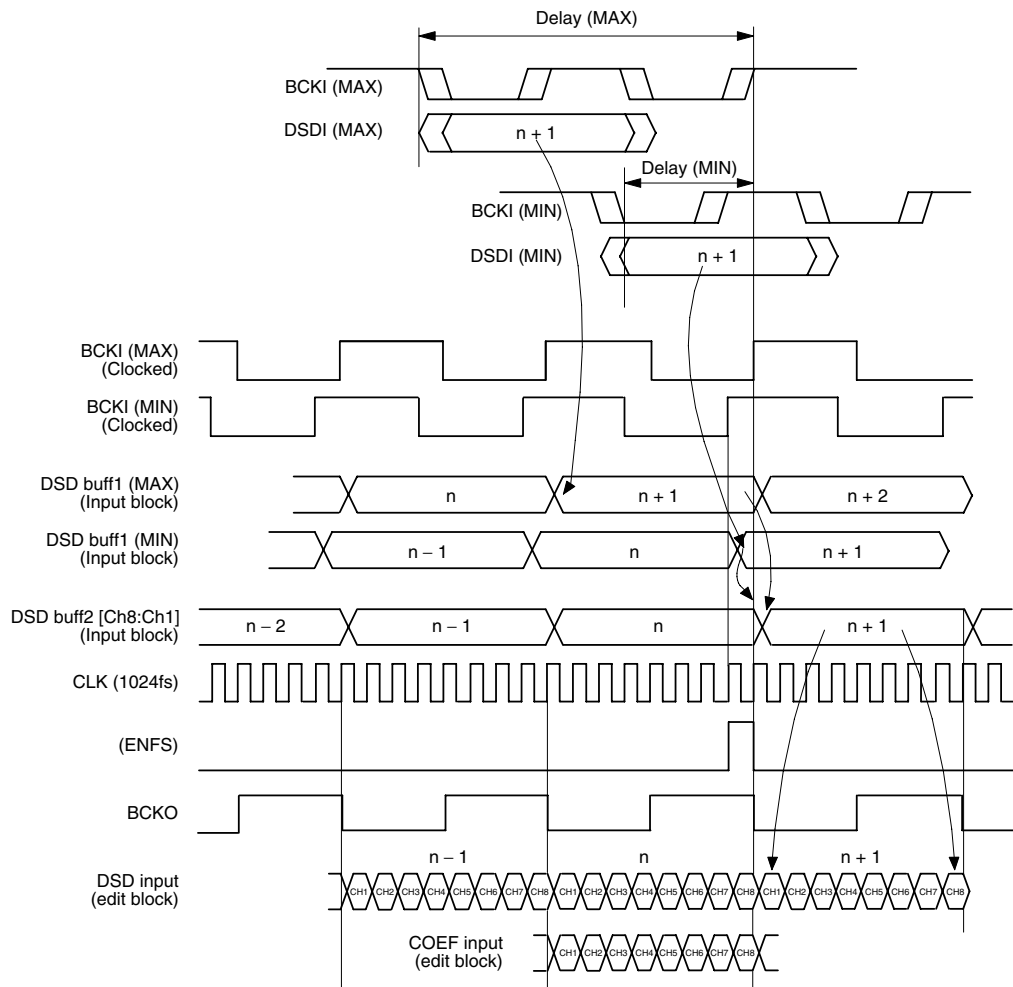
The DSD signal internal process flow is shown in the following diagram. Each stage of the process increases the data delay, and the delay is adjusted internally so that the delay is approximately 1FS cycle.



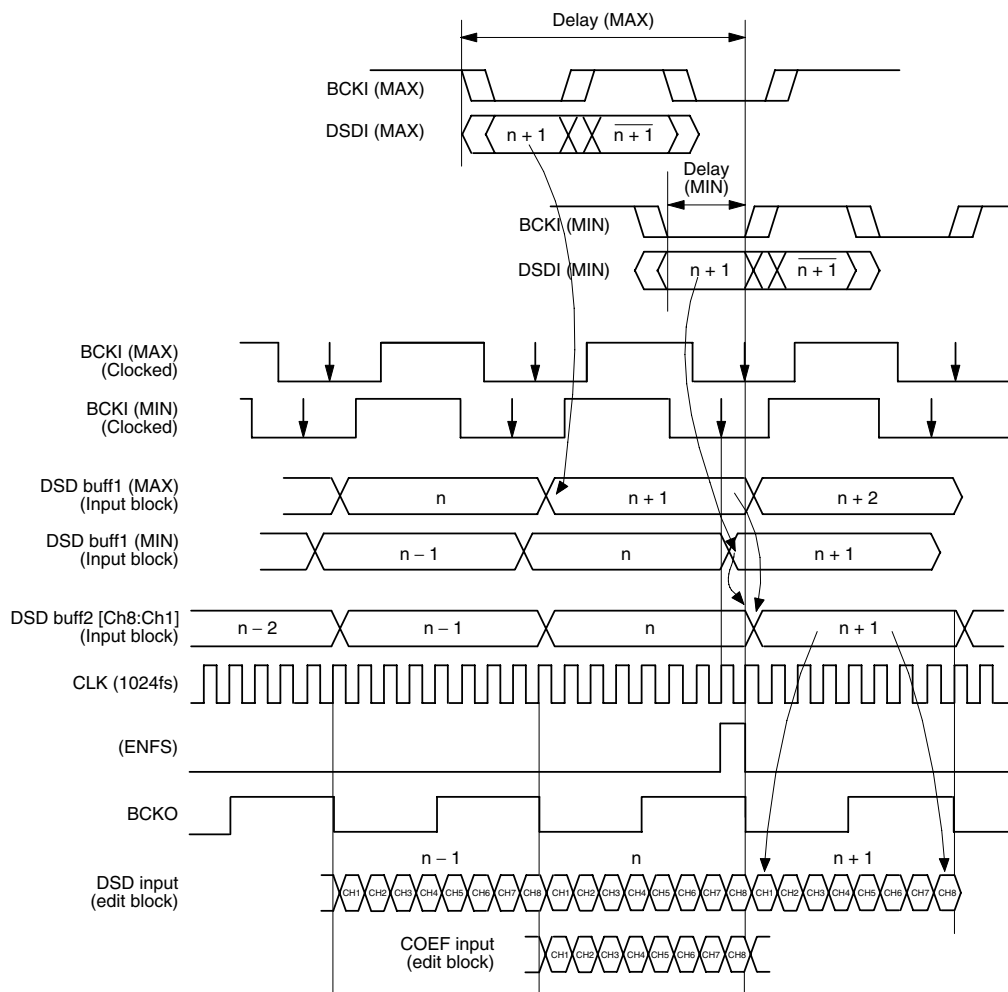
Input-stage delay (I/O buffer)

The input processing delay due to DSD input format status and the BCKI/FS phase relationship is approximately 0.5 to 1.5 samples in length.

(1) Normal mode timing example



(2) Manchester-type input mode timing example

**Internal computation delay**

The mixing process internal data delay is determined by the DSD sampling frequency and is 18 samples in length. The down-sampled 64fs output has an additional delay of 58 samples in length at 128fs rate.

Delay adjustment

The internal delay immediately before output can be adjusted in units of the sample rate. The delay adjustment can be set in the following internal registers.

- (1) DLY_128 [6:0] (Address = 10h) DSDOn delay in 128fs mode
- (2) DLY_64 [6:0] (Address = 11h) DSDOn delay in 64fs mode
- (3) DLY_DOWN [4:0] (Address = 12h) DSDOn → DSD64On delay

Initialization

After power is applied, RST_X must be held LOW for the rated time to initialize the device. During initialization, the data bus is in input mode. The output pins have the following state.

DSD data outputs: LOW
BCKO, BCK64O: LOW
MOSYNC : LOW

When RST_X goes HIGH, the synchronization adjustment takes place and internal operation commences.

When the initialization is performed by software reset in SRESET (Address = 0), the coefficient registers (Addresses = 80h to FFh) are cleared, but the internal state registers (Addresses = 00h to 7Fh) maintain their current setting.

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