

4-BIT SINGLE-CHIP MICROCONTROLLER
FOR INFRARED REMOTE CONTROL TRANSMISSION

DESCRIPTION

The μ PD66P04 is a microcontroller for infrared remote control transmitters which is provided with a one-time PROM as the program memory.

Because users can write programs for the μ PD66P04, it is ideal for program evaluation and small-scale production of the application systems using the μ PD6604.

When reading this document, also refer to the μ PD6604 Data Sheet (U11281E).

FEATURES

- Program memory (one-time PROM) : 2016 \times 10 bits
- Data memory (RAM) : 32 \times 4 bits
- Built-in carrier generation circuit for infrared remote control
- 9-bit programmable timer : 1 channel
- Command execution time : 16 μ s (when operating at $f_{osc} = 500$ kHz: RC oscillation)
- Stack level : 1 level (Stack RAM is for data memory RF as well.)
- I/O pins ($K_{I/O}$) : 8 units
- Input pins (K_i) : 4 units
- Sense input pin (S_o) : 1 unit
- S_1/\overline{LED} pin (I/O) : 1 unit (When in output mode, this is the remote control transmission display pin.)
- Power supply voltage : $V_{DD} = 2.2$ to 3.6 V
- Operating ambient temperature : $T_A = -20$ to $+70^\circ\text{C}$
- Oscillator frequency : $f_{osc} = 300$ kHz to 1 MHz
- POC circuit

APPLICATION

Infrared remote control transmitter (for AV and household electric appliances)

Because the μ PD66P04 uses an RC oscillation system clock, its accuracy and stability are lower than the models using ceramic oscillation.

In applications where the clock accuracy and stability pose a problem, use the μ PD61P34 (ceramic oscillation type).

The information in this document is subject to change without notice.

ORDERING INFORMATION

Part Number	Package
μPD66P04GS	20-pin plastic SOP (300 mil)
μPD66P04GS-GJG	20-pin plastic shrink SOP (300 mil)

PIN CONFIGURATION (TOP VIEW)

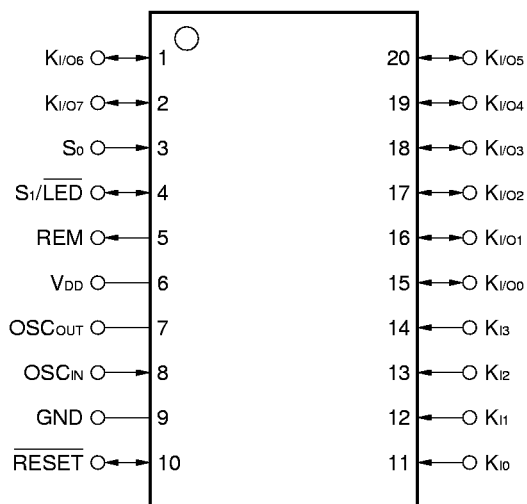
20-pin Plastic SOP (300 mil)

- μPD66P04GS

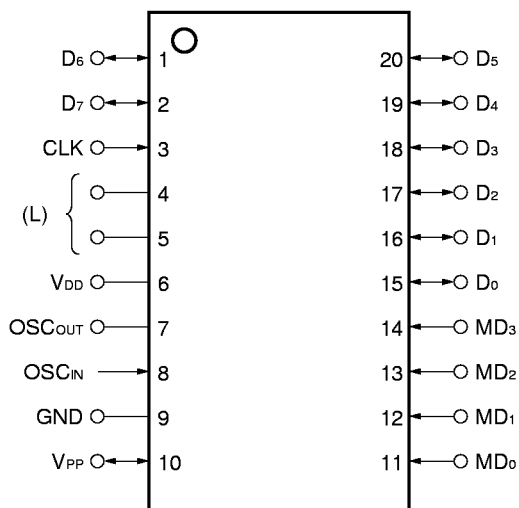
20-pin Plastic Shrink SOP (300 mil)

- μPD66P04GS-GJG

(1) Normal operating mode



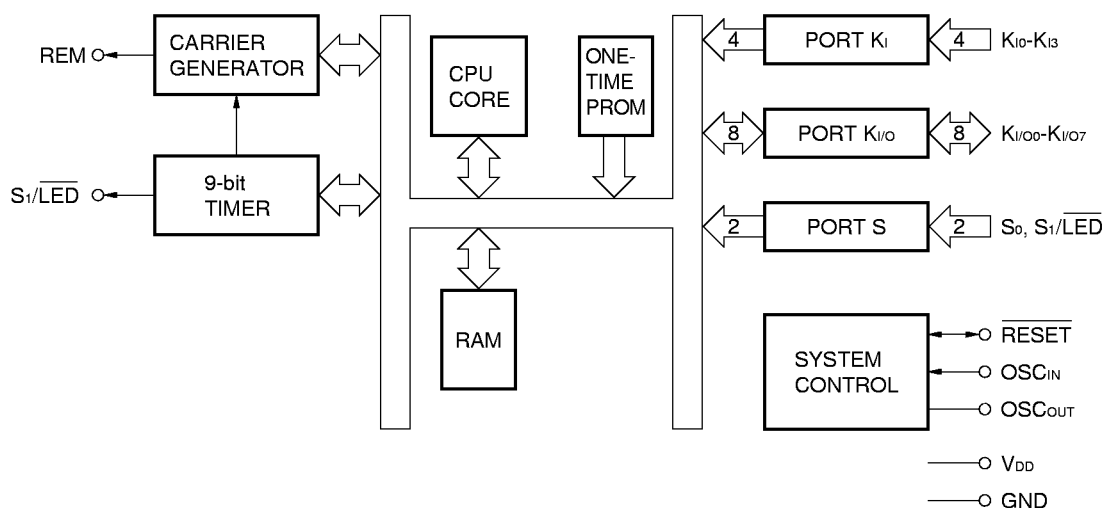
(2) PROM programming mode



Caution Round brackets () indicate the pins not used in the PROM programming mode.

L : Connect each of these pins to GND via a pull-down resistor.

BLOCK DIAGRAM



LIST OF FUNCTIONS

Item	μPD66P04
ROM capacity	2016 × 10 bits One-time PROM
RAM capacity	32 × 4 bits
Stack	1 level (shared with RF of RAM)
I/O pin	Key input (Ki) : 4 pins Key I/O (Ki/O) : 8 pins Key expansion input (So, S1) : 2 pins Remote control transmitter display output (LED) : 1 pin (shared with S1 pin)
Number of keys	32 keys 48 keys (when expanded by key expansion input) 96 keys (when expanded by key expansion input and diode)
Clock frequency	RC oscillation fosc = 300 to 500 kHz fosc = 500 kHz to 1 MHz ^{Note}
Instruction execution time	16 μs (at fosc = 500 kHz)
Carrier frequency	fosc, fosc/2, fosc/8, fosc/12, fosc/16, fosc/24, no carrier (high level)
Timer	9-bit programmable timer : 1 channel
POC circuit	Internal
Supply voltage	VDD = 2.2 to 3.6 V
Operating ambient temperature	TA = -20 to +70°C
Package	<ul style="list-style-type: none"> • 20-pin plastic SOP (300 mil) • 20-pin plastic shrink SOP (300 mil)

Note It is necessary to design the application circuit so that the RESET pin goes low at a supply voltage of less than 2.2 V.

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1. PIN FUNCTIONS

1.1 Normal Operating Mode

Pin No.	Symbol	Function	Output Format	When Reset
1 2 15-20	K _{I/O0} -K _{I/O7}	These pins refer to the 8-bit I/O ports. I/O switching can be made in 8-bit units. In INPUT mode, a pull-down resistor is added. In OUTPUT mode, they can be used as the key scan output of the key matrix.	CMOS push-pull ^{Note 1}	High-level output
3	S ₀	Refers to the input port. Can also be used as the key return input of the key matrix. In INPUT mode, the availability of the pull-down resistor of the S ₀ and S ₁ ports can be specified by software in terms in 2-bit units. If INPUT mode is canceled by software, this pin is placed in OFF mode and enters the high-impedance state.	—	High-impedance (OFF mode)
4	S ₁ /LED	Refers to the I/O port. In INPUT mode (S ₁), this pin can also be used as the key return input of the key matrix. The availability of the pull-down resistor of the S ₀ and S ₁ ports can be specified by software in 2-bit units. In OUTPUT mode (LED), it becomes the remote control transmission display output (active low). When the remote control carrier is output from the REM output, this pin outputs the low level from the LED output synchronously with the REM signal.	CMOS push-pull	High-level output (LED)
5	REM	Refers to the infrared remote control transmission output. The output is active high. Carrier frequency: f _x , f _x /8, f _x /12, high-level, f _x /2, f _x /16, f _x /24 (usable on software)	CMOS push-pull	Low-level output
6	V _{DD}	Refers to the power supply.	—	—
7 8	OSC _{OUT} OSC _{IN}	These pins are used for RC oscillation.	—	High-impedance (oscillation stopped) Low level (oscillation stopped)
9	GND	Refers to the ground.	—	—
10	RESET	Normally, this pin is a system reset input. By inputting a low level, the CPU can be reset. When resetting with the POC circuit a low level is output. A pull-up resistor is incorporated.	—	—
11-14	K _{I0} -K _{I3} ^{Note 2}	These pins refer to the 4-bit input ports. They can be used as the key return input of the key matrix. The use of the pull-down resistor can be specified by software in 4-bit units.	—	Input (low-level)

Notes 1. Be careful about this because the drive capability of the low-level output side is held low.

2. In order to prevent malfunction, be sure to input a low level to more than one of pins K_{I0} to K_{I3} when reset is released (when RESET pin changes from low level to high level, or POC is released due to supply voltage startup).

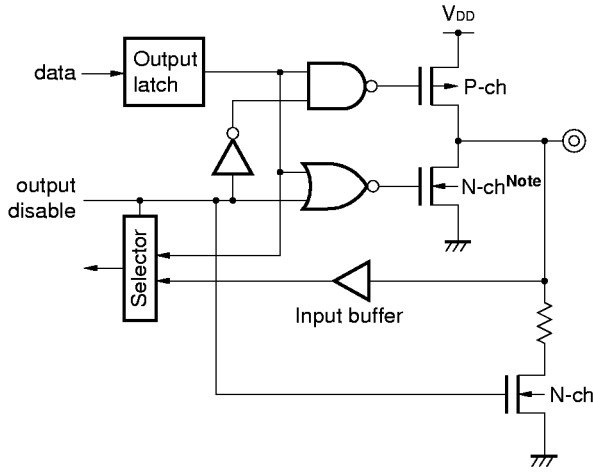
1.2 PROM Programming Mode

Pin No.	Symbol	Function	I/O
1, 2 15-20	D ₀ -D ₇	8-bit data input/output when writing/verifying program memory	I/O
3	CLK	Clock input for updating address when writing/verifying program memory	Input
6	V _{DD}	Power Supply. Supply +6 V to this pin when writing/verifying program memory.	–
7	OSC _{OUT}	Clock necessary for writing program memory. Connect a resistor (R = 47 k Ω) and a capacitor (C = 27 pF) to these pins.	–
8	OSC _{IN}		Input
9	GND	GND	–
10	V _{PP}	Supplies voltage for writing/verifying program memory. Apply +10 V to this pin.	–
11-14	MD ₀ -MD ₃	Input for selecting operation mode when writing/verifying program memory.	Input

1.3 INPUT/OUTPUT Circuits of Pins

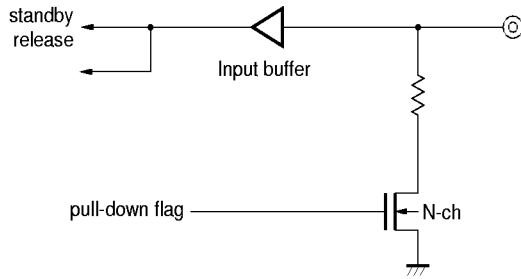
The input/output circuits of the μPD66P04 pins are shown in partially simplified forms below.

(1) K1/00-K1/07

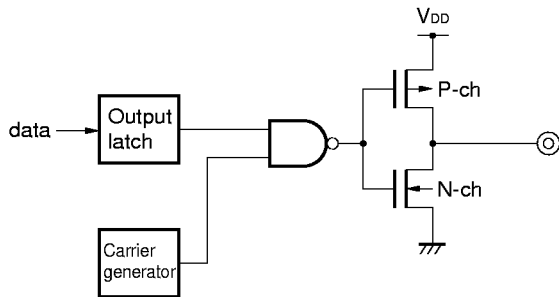


Note The drive capability is held low.

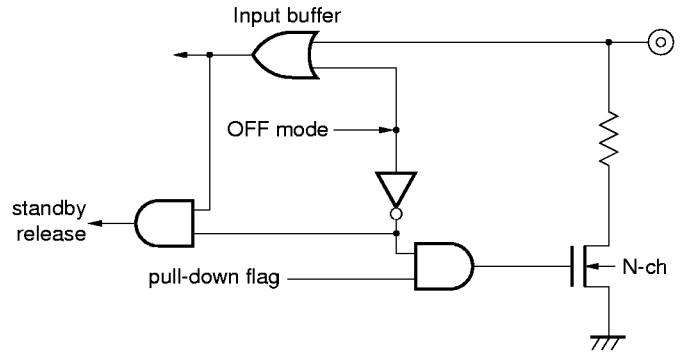
(2) K10-K13



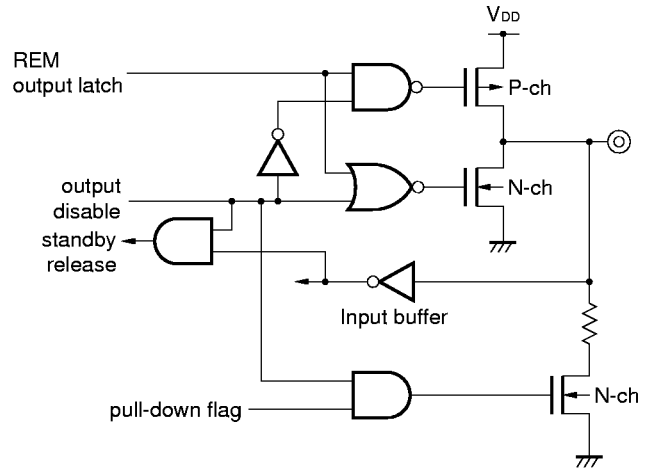
(3) REM



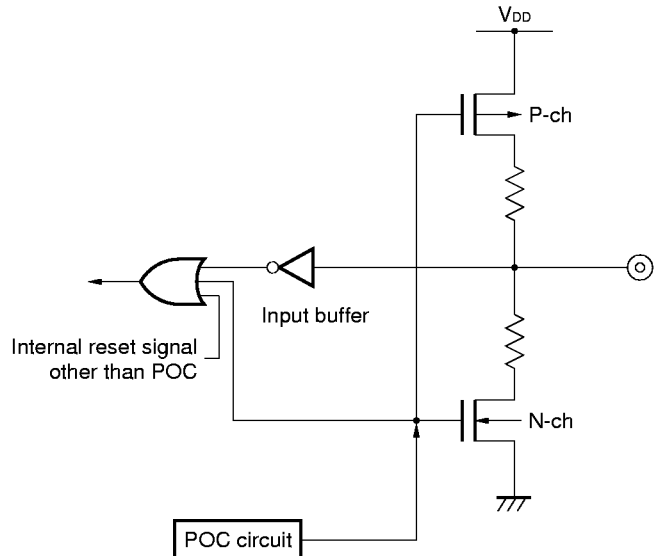
(4) S0



(5) S1/LED



(6) RESET



1.4 Dealing with Unused Pins

The following connections are recommended for unused pins in the normal operation mode.

Table 1-1. Connections for Unused Pins

Pin		Connection	
		Inside the microcontroller	Outside the microcontroller
K ₁₀	INPUT mode	—	Open
	OUTPUT mode	High-level output	
REM		—	
S ₁ /LED		OUTPUT mode (LED) setting	Directly connected to GND
S ₀		OFF mode setting	
K ₁		—	
RESET ^{Note}		Built-in POC circuit	Open

Note If the circuit is an applied one requiring high reliability, be sure to design it in such a manner that the $\overline{\text{RESET}}$ signal is entered externally.

Caution The I/O mode and the terminal output level are recommended to be fixed by setting them repeatedly in each loop of the program.

1.5 Notes on Using K₁ Pin at Reset

In order to prevent malfunction, be sure to input a low level to more than one of pins K₁₀ to K₁₃ when reset is released (when $\overline{\text{RESET}}$ pin changes from low level to high level, or POC is released due to supply voltage startup).

2. DIFFERENCES BETWEEN μPD6604 AND μPD66P04

Table 2-1 shows the differences between the μPD6604 and μPD66P04.

The only differences among these models are the program memory, supply voltage, system clock frequency, oscillation stabilization wait time, and POC circuit (mask option), and the CPU function and internal peripheral hardware are the same.

The electrical characteristics also differ slightly. For the electrical characteristics, refer to the Data Sheet of each model.

Table 2-1. Differences between μPD6604 and μPD66P04 (1/2)

(1) When POC circuit (mask option) is provided to μPD6604

Item	μPD66P04	μPD6604
ROM	One-time PROM	Mask ROM
	2016 × 10 bits (000H to 7DFH)	1002 × 10 bits (000H to 3E9H)
Program counter (PC)	11 bits	10 bits
Address stack register (ASR)		
Data pointer (DP)		
Oscillation stabilization wait time		
• On releasing STOP mode by release condition	260/fosc	36/fosc
• On releasing STOP or HALT mode by $\overline{\text{RESET}}$ input and at reset	284/fosc to 340/fosc	60/fosc to 116/fosc
V _{PP} pin and operating mode select pin	Provided	Not provided
Electrical characteristics	Some electrical characteristics, such as data retention voltage and current consumption, differ. For details, refer to Data Sheet of each model.	

Table 2-1. Differences between μ PD6604 and μ PD66P04 (2/2)(2) When POC circuit (mask option) is not provided to μ PD6604

Item	μ PD66P04	μ PD6604
ROM	One-time PROM	Mask ROM
	2016 \times 10 bits (000H to 7DFH)	1002 \times 10 bits (000H to 3E9H)
Program counter (PC)	11 bits	10 bits
Address stack register (ASR)		
Data pointer (DP)		
Oscillation stabilization wait time		
• On releasing STOP mode by release condition	260/fosc	36/fosc
• On releasing STOP or HALT mode by $\overline{\text{RESET}}$ input and at reset	284/fosc to 340/fosc	60/fosc to 116/fosc
V _{PP} pin and operating mode select pin	Provided	Not provided
POC circuit	Incorporated	Not provided
Supply voltage	V _{DD} = 2.2 to 3.6 V (T _A = -20 to +70°C)	V _{DD} = 1.8 to 3.6 V (T _A = -40 to +85°C)
System clock frequency	• fosc = 300 to 500 kHz • fosc = 500 kHz to 1MHz ^{Note}	• fosc = 300 to 500 kHz • fosc = 300 kHz to 1 MHz (V _{DD} = 2.2 to 3.6 V)
Electrical characteristics	Some electrical characteristics, such as data retention voltage and current consumption, differ. For details, refer to Data Sheet of each model.	

Note It is necessary to design the application circuit so that the $\overline{\text{RESET}}$ pin goes low when the supply voltage is less than 2.2 V.

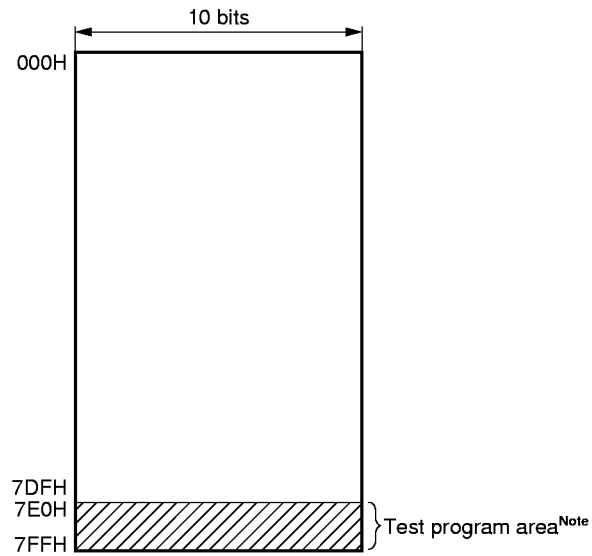
2.1 Program Memory (One-time PROM) ... 2016 steps × 10 bits

This one-time PROM is configured with 10 bits per step and is addressed by the program counter.

The program memory stores programs and table data.

The 32 steps from addresses 7E0H through 7FFH constitute a test program area and must not be used.

Figure 2-1. Program Memory Map

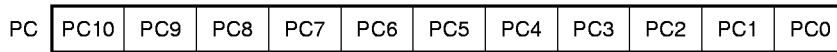


Note Even if execution jumps to the test program area by mistake, it returns to address 000H.

2.2 Program Counter (PC) ... 11 bits

The program counter is a binary counter that holds the address information of the program memory.

Figure 2-2. Program Counter Configuration



The program counter stores the address of the instruction to be executed next. Usually, each time an instruction has been executed, the contents of the PC are automatically incremented according to the length of the instruction (number of bytes).

If a jump instruction (JMP, JC, JNC, JF, or JNF) is executed, however, the jump destination address written as the operand is stored to the PC.

When a subroutine call instruction (CALL) is executed, the contents of the PC at that time are saved to the address stack register (ASR), and the call destination address written as the instruction operand is stored to the PC. If a return instruction (RET) is executed after the CALL instruction has been executed, the address saved to the ASR is restored to the PC.

At reset, the value of the PC is reset to "000H".

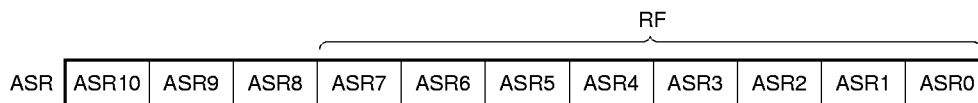
2.3 Address Stack Register (ASR (RF)) ... 11 bits

The address stack register saves an address to which program execution is to return after a subroutine call instruction has been executed. The low-order 8 bits of this register are located in the RF area of the data memory as a multiplexed RAM area. The value of ASR is retained even after the RET instruction has been executed.

At reset, the ASR holds the previous data (the value of the ASR is undefined on power application).

Caution The high-order 3 bits of the ASR are undefined if the RF is accessed as a data memory area.

Figure 2-3. Address Stack Register Configuration



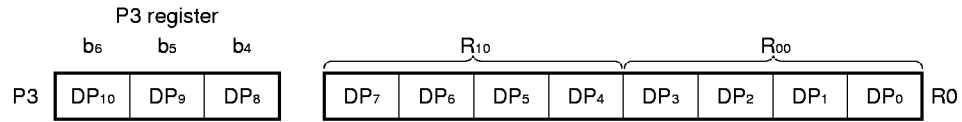
2.4 Data Pointer (DP) ... 11 Bits

The ROM data table can be referenced by setting the ROM address in the data pointer to call the ROM contents.

The low-order 8 bits of the ROM address are specified by R0 of the data memory, and the high-order 3 bits by bits 4, 5, and 6 of the P3 register.

When reset, the pointer contents become "000H".

Figure 2-4. Data Pointer Configuration



2.5 Control Register 0 (P3)

Control register 0 consists of 8 bits. This following bits of this register can be controlled.

At reset, the value of this register is set to 0000 0011B.

Table 2-2. Control Register 0 (P3)

Bit		b ₇	b ₆	b ₅	b ₄	b ₃	b ₂	b ₁	b ₀
Name		–	DP (data pointer)			TCTL	CARY	MOD ₁	MOD ₀
			DP ₁₀	DP ₉	DP ₈				
Set value	0	Fixed to	0	0	0	1/1	ON	Refer to Table 2-3.	
	1	"0"	1	1	1	1/2	OFF		
At reset		0	0	0	0	0	0	1	1

- b₀, b₁..... Specify the carrier frequency and duty factor of REM output.
- b₂ Specifies whether a carrier whose frequency is specified by b₀ and b₁ is used.
 "0" = ON (carrier), "1" = OFF (no carrier, high level)
- b₃ Changes the carrier frequency and division ratio of the timer clock.
 "0" = 1/1 (carrier frequency: value specified by b₀ and b₁, timer clock: fosc/8)
 "1" = 1/2 (carrier frequency: 1/2 of value specified by b₀ and b₁, timer clock: fosc/16)

Table 2-3. Setting of Timer Clock and Carrier Frequency

b ₃	b ₂	b ₁	b ₀	Timer Clock	Carrier Frequency (duty factor)
0	0	0	0	fosc/8	fosc (Duty 1/2)
		0	1		fosc/8 (Duty 1/2)
		1	0		fosc/12 (Duty 1/2)
		1	1		fosc/12 (Duty 1/3)
	1	x	x	No carrier (high level)	
1	0	0	0	fosc/16	fosc/2 (Duty 1/2)
		0	1		fosc/16 (Duty 1/2)
		1	0		fosc/24 (duty 1/2)
		1	1		fosc/24 (Duty 1/3)
	1	x	x	No carrier (high level)	

b₄, b₅, b₆... Specify the high-order 3 bits (DP₈, DP₉, and DP₁₀) of the data pointer of ROM.

Remark x: don't care

3. WRITING AND VERIFYING ONE-TIME PROM (PROGRAM MEMORY)

The program memory of the μPD66P04 is a one-time PROM of 2016 × 10 bits.

To write or verify this one-time PROM, the pins shown in Table 3-1 are used. Note that no address input pin is used. Instead, the address is updated by using the clock input from the CLK pin.

Table 3-1. Pins Used to Write/Verify Program Memory

Pin Name	Function
V _{PP}	Supplies voltage when writing/verifying program memory. Apply +10 V to this pin.
V _{DD}	Power supply. Supply +6 V to this pin when writing/verifying program memory.
CLK	Inputs clock to update address when writing/verifying program memory. By inputting pulse four times to CLK pin, address of program memory is updated.
MD ₀ -MD ₃	Input to select operation mode when writing/verifying program memory.
D ₀ -D ₇	Inputs/outputs 8-bit data when writing/verifying program memory.
OSC _{IN} , OSC _{OUT}	Clock necessary for writing program memory. Connect a resistor (R = 47 kΩ) and a capacitor (C = 27 pF) to these pins.

3.1 Operating Mode When Writing/Verifying Program Memory

The μPD66P04 is set in the program memory write/verify mode when +6 V is applied to the V_{DD} pin and +10 V is applied to the V_{PP} pin after the μPD66P04 has been in the reset status (V_{DD} = 5 V, V_{PP} = 0 V) for a specific time. In this mode, the operating modes shown in Table 3-2 can be set by setting the MD₀ through MD₃ pins. Connect all the pins other than those shown in Table 3-1 to GND via pull-down resistor.

Table 3-2. Setting Operation Mode

Setting of Operating Mode						Operation Mode
V _{PP}	V _{DD}	MD ₀	MD ₁	MD ₂	MD ₃	
+10V	+6V	H	L	H	L	Clear program address to 0
		L	H	H	H	Write mode
		L	L	H	H	Verify mode
		H	x	H	H	Program inhibit mode

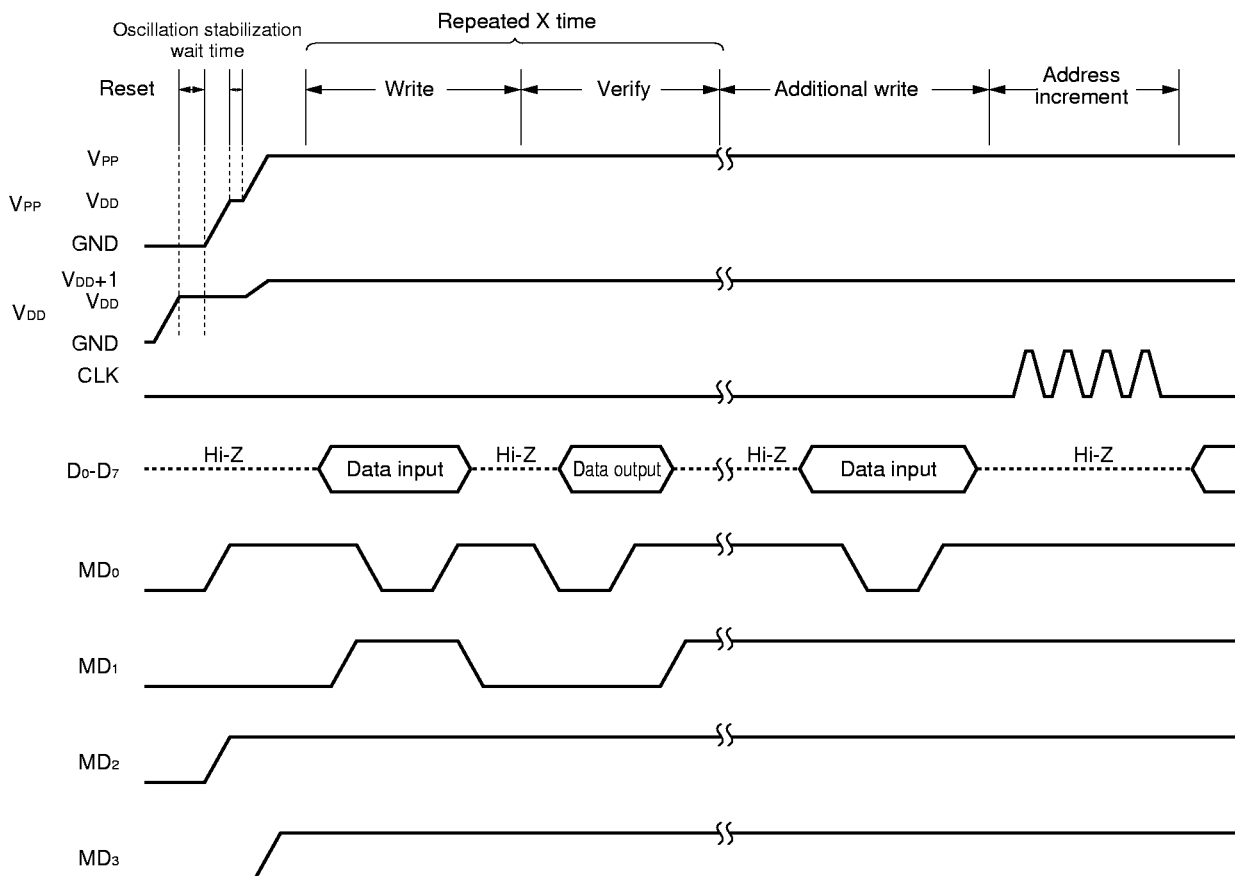
x: don't care (L or H)

3.2 Program Memory Writing Procedure

The program memory is written at high speed in the following procedure.

- (1) Pull down the pins not used to GND via resistor. Keep the CLK pin low.
- (2) Supply 5 V to the V_{DD} pin. Keep the V_{PP} pin low.
- (3) Supply 5 V to the V_{PP} pin after waiting for 10 μs.
- (4) Wait for 2 ms until oscillation of the clock connected across the OSC_{IN} and OSC_{OUT} pins stabilizes.
- (5) Set the program memory address 0 clear mode by using the mode setting pins.
- (6) Supply 6 V to V_{DD} and 10 V to V_{PP}.
- (7) Set the program inhibit mode.
- (8) Write data to the program memory in the 1-ms write mode.
- (9) Set the program inhibit mode.
- (10) Set the verify mode. If the data have been written to the program memory, proceed to (11). If not, repeat steps (8) through (10).
- (11) Additional writing of (number of times of writing in (8) through (10): X) × 1 ms.
- (12) Set the program inhibit mode.
- (13) Input a pulse to the CLK pin four times to update the program memory address (+1).
- (14) Repeat steps (8) through (13) up to the last address.
- (15) Set the 0 clear mode of the program memory address.
- (16) Change the voltages on the V_{DD} and V_{PP} pins to 5 V.
- (17) Turn off power.

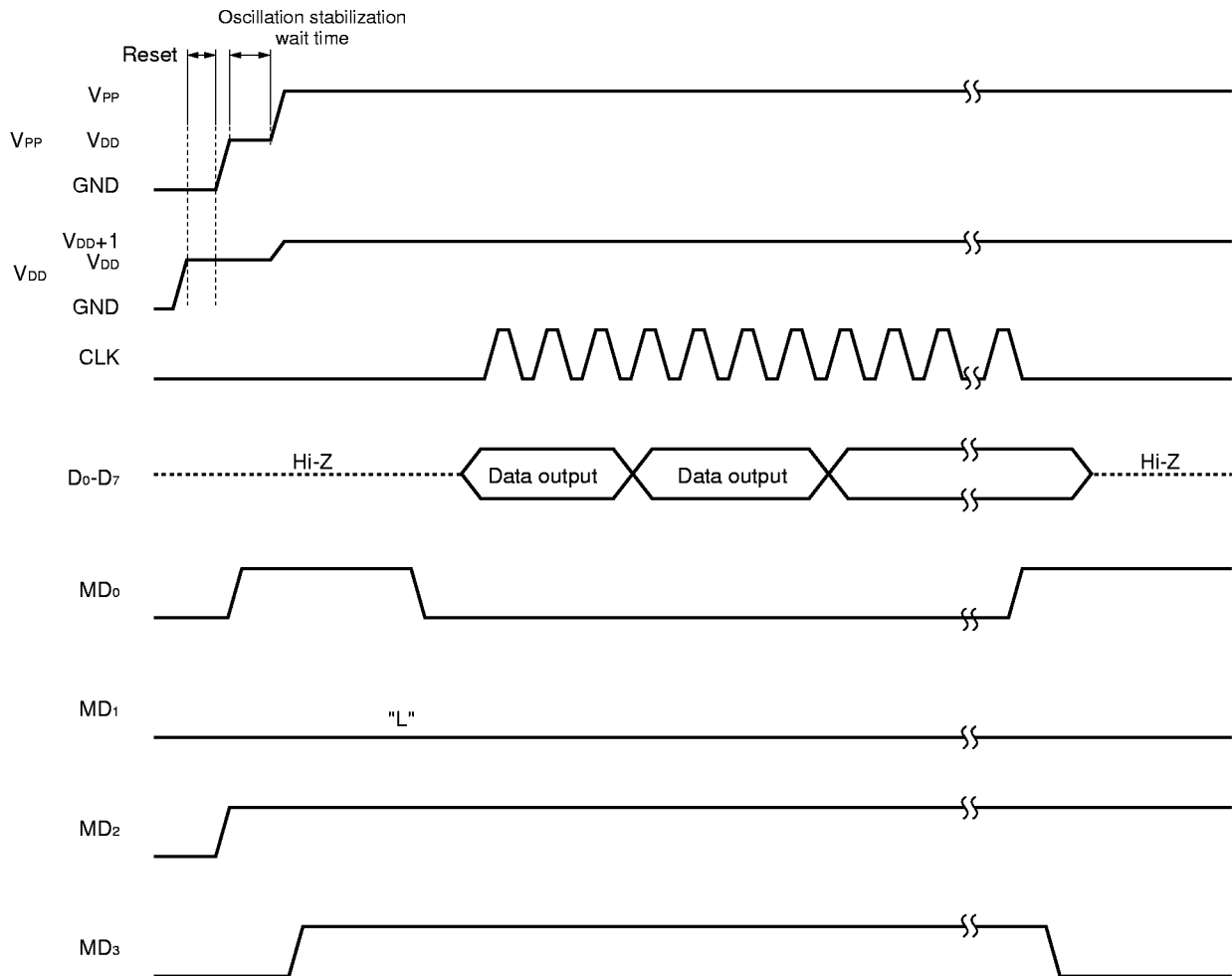
The following figure illustrates steps (2) through (13) above.



3.3 Program Memory Reading Procedure

- (1) Pull down the pins not used to GND via resistor. Keep the CLK pin low.
- (2) Supply 5 V to the V_{DD} pin. Keep the V_{PP} pin low.
- (3) Supply 5 V to the V_{PP} pin after waiting for 10 μs.
- (4) Wait for 2 ms until oscillation of the clock connected across the OSC_{IN} and OSC_{OUT} pins stabilizes.
- (5) Set the program memory address 0 clear mode by using the mode setting pins.
- (6) Supply 6 V to V_{DD} and 10 V to V_{PP}.
- (7) Set the program inhibit mode.
- (8) Set the verify mode. Data of each address is output sequentially each time the clock pulse is input to the CLK pin four times.
- (9) Set the program inhibit mode.
- (10) Set the program memory address 0 clear mode.
- (11) Change the voltage on the V_{DD} and V_{PP} pins to 5 V.
- (12) Turn off power.

The following figure illustrates steps (2) through (10) above.



4. ELECTRICAL SPECIFICATIONS (PRELIMINARY)

Absolute Maximum Ratings (T_A = +25 °C)

Parameter	Symbol	Test Conditions	Rating	Unit	
Power supply voltage	V _{DD}		-0.3 to +7.0	V	
	V _{PP}		-0.3 to +11	V	
Input voltage	V _I	K _{I/O} , K _I , S ₀ , S ₁ , $\overline{\text{RESET}}$	-0.3 to V _{DD} + 0.3	V	
Output voltage	V _O		-0.3 to V _{DD} + 0.3	V	
High-level output current	I _{OH} Note	REM	Peak value	-30	mA
			rms	-20	mA
		$\overline{\text{LED}}$	Peak value	-7.5	mA
			rms	-5	mA
		One K _{I/O} pin	Peak value	-13.5	mA
			rms	-9	mA
		Total of $\overline{\text{LED}}$ and K _{I/O} pins	Peak value	-18	mA
			rms	-12	mA
Low-level output current	I _{OL} Note	REM	Peak value	7.5	mA
			rms	5	mA
		$\overline{\text{LED}}$	Peak value	7.5	mA
			rms	5	mA
Operating ambient temperature	T _A		-20 to +70	°C	
Storage temperature	T _{stg}		-65 to +150	°C	

Note Work out the rms with: [rms] = [Peak value] × √Duty.

Caution Product quality may suffer if the absolute rating is exceeded for any parameter, even momentarily. In other words, an absolute maximum rating is a value at which the possibility of physical damage to the product cannot be ruled out. Care must therefore be taken to ensure that these ratings are not exceeded during use of the product.

Recommended Power Supply Voltage Range (T_A = -20 to + 70°C)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage	V _{DD}	f _{osc} = 300 to 500 kHz	2.2	3.0	3.6	V
		f _{osc} = 500 kHz to 1 MHz ^{Note}	2.2	3.0	3.6	V

Note It is necessary to design the application circuit so that the $\overline{\text{RESET}}$ pin goes low when the supply voltage is less than 2.2 V.

DC Characteristics (T_A = -20 to +70°C, V_{DD} = 2.2 to 3.6 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
High-level input voltage	V _{IH1}	$\overline{\text{RESET}}$		0.8 V _{DD}		V _{DD}	V
	V _{IH2}	K _{I/O}		0.65 V _{DD}		V _{DD}	V
	V _{IH3}	K _I , S ₀ , S ₁		0.65 V _{DD}		V _{DD}	V
Low-level input voltage	V _{IL1}	$\overline{\text{RESET}}$		0		0.2 V _{DD}	V
	V _{IL2}	K _{I/O}		0		0.3 V _{DD}	V
	V _{IL3}	K _I , S ₀ , S ₁		0		0.15 V _{DD}	V
High-level input leakage current	I _{LH1}	K _I V _I = V _{DD} , pull-down resistor not incorporated				3	μA
	I _{LH2}	S ₀ , S ₁ V _I = V _{DD} , pull-down resistor not incorporated				3	μA
Low-level input leakage current	I _{LUL1}	K _I V _I = 0 V				-3	μA
	I _{LUL2}	K _{I/O} V _I = 0 V				-3	μA
	I _{LUL3}	S ₀ , S ₁ V _I = 0 V				-3	μA
High-level output voltage	V _{OH1}	REM, $\overline{\text{LED}}$, K _{I/O}	I _{OH} = -0.3 mA	0.8 V _{DD}			V
Low-level output voltage	V _{OL1}	REM, $\overline{\text{LED}}$				0.3	V
	V _{OL2}	K _{I/O}				0.4	V
High-level output current	I _{OH1}	REM		V _{DD} = 3.0 V, V _{OH} = 1.0 V	-5	-9	mA
	I _{OH2}	K _{I/O}		V _{DD} = 3.0 V, V _{OH} = 2.2 V	-2.5	-5	mA
Low-level output current	I _{OL1}	K _{I/O}		V _{DD} = 3.0 V, V _{OL} = 0.4 V	30	70	μA
		K _{I/O}		V _{DD} = 3.0 V, V _{OL} = 2.2 V	100	220	μA
Built-in pull-up resistor	R ₁	$\overline{\text{RESET}}$		25	50	100	kΩ
Built-in pull-down resistor	R ₂	$\overline{\text{RESET}}$		2.5	5	15	kΩ
	R ₃	K _I , S ₀ , S ₁		75	150	300	kΩ
	R ₄	K _{I/O}		130	250	500	kΩ
Data hold power supply voltage	V _{DDOR}	In STOP mode		1.2		3.6	V
Supply current ^{Note}	I _{DD1}	Operating mode	f _{osc} = 1.0 MHz, V _{DD} = 3 V ± 10 %		0.6	1.2	mA
			f _{osc} = 455 kHz, V _{DD} = 3 V ± 10 %		0.5	1.0	mA
	I _{DD2}	HALT mode	f _{osc} = 1.0 MHz, V _{DD} = 3 V ± 10 %		0.5	1.0	mA
			f _{osc} = 455 kHz, V _{DD} = 3 V ± 10 %		0.4	0.8	mA
	I _{DD3}	STOP mode	V _{DD} = 3 V ± 10 %		1.0	8.0	μA
V _{DD} = 3 V ± 10 %, T _A = 25 °C				1.0	2.0	μA	

Note The POC circuit current and the current flowing in the built-in pull-up resistor are not included.

AC Characteristics (T_A = -20 to +70°C, V_{DD} = 2.2 to 3.6 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit	
Instruction execution time	t _{cy}		15.9		27	μs	
		Note 1	7.9		27	μs	
K _i , S ₀ , S ₁ high-level width	t _H		10			μs	
		When canceling standby mode	HALT mode	10			μs
			STOP mode	Note 2			μs
$\overline{\text{RESET}}$ low-level width	t _{RSL}		10			μs	

- Notes**
1. When using at f_{osc} = 500 kHz or higher, it is necessary to design the application circuit so that the $\overline{\text{RESET}}$ pin goes low when the supply voltage is less than 2.2 V.
 2. 10 + 260/f_{osc}

Remark t_{cy} = 8/f_{osc} (f_{osc}: System clock oscillator frequency)

POC Circuit^{Note 1} (T_A = -20 to +70°C)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
POC-detected voltage ^{Note 2}	V _{POC}		1.8	2.0	2.2	V
POC circuit current	I _{POC}			1.2	1.5	μA

- Notes**
1. Operates effectively under the conditions of V_{DD} = 2.2 to 3.6 V and f_{osc} = 300 to 500 kHz.
 2. Refers to the voltage with which the POC circuit cancels an internal reset. If V_{POC} < V_{DD}, the internal reset is canceled.
From the time of V_{POC} ≥ V_{DD} until the internal reset takes effect, lag of up to 1 ms occurs. When the period of V_{POC} ≥ V_{DD} lasts less than 1 ms, the internal reset may not take effect.

System Clock Oscillation Circuit Characteristics (T_A = -20 to +70°C, V_{DD} = 2.2 to 3.6 V)

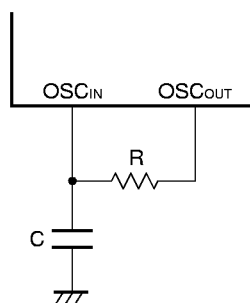
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Oscillator frequency	f _{osc}		300	455	500	kHz
		Note	300	455	1000	kHz

Note When using at f_{osc} = 500 kHz or higher, it is necessary to design the application circuit so that the $\overline{\text{RESET}}$ pin goes low when the supply voltage is less than 2.2 V.

Recommended Oscillation Circuit Constant (T_A = -20 to +70°C, V_{DD} = 2.2 to 3.6 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Capacity of oscillation capacitor	C		22	27	33	pF
Oscillation resistance	R			47		kΩ

An external circuit example



PROM Programming Mode

DC Programming Characteristics (T_A = 25°C, V_{DD} = 6.0±0.25 V, V_{PP} = 10.0±0.3 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
High-level input voltage	V _{IH1}	Other than CLK	0.7 V _{DD}		V _{DD}	V
	V _{IH2}	CLK	V _{DD} -0.5		V _{DD}	V
Low-level input voltage	V _{IL1}	Other than CLK	0		0.3 V _{DD}	V
	V _{IL2}	CLK	0		0.4	V
Input leakage current	I _{LI}	V _{IN} = V _{IL} or V _{IH}			10	μA
High-level output voltage	V _{OH}	I _{OH} = -1 mA	V _{DD} -1.0			V
Low-level output voltage	V _{OL}	I _{OL} = 1.6 mA			0.4	V
V _{DD} supply current	I _{DD}				30	mA
V _{PP} supply current	I _{PP}	MD0 = V _{IL} , MD1 = V _{IH}			30	mA

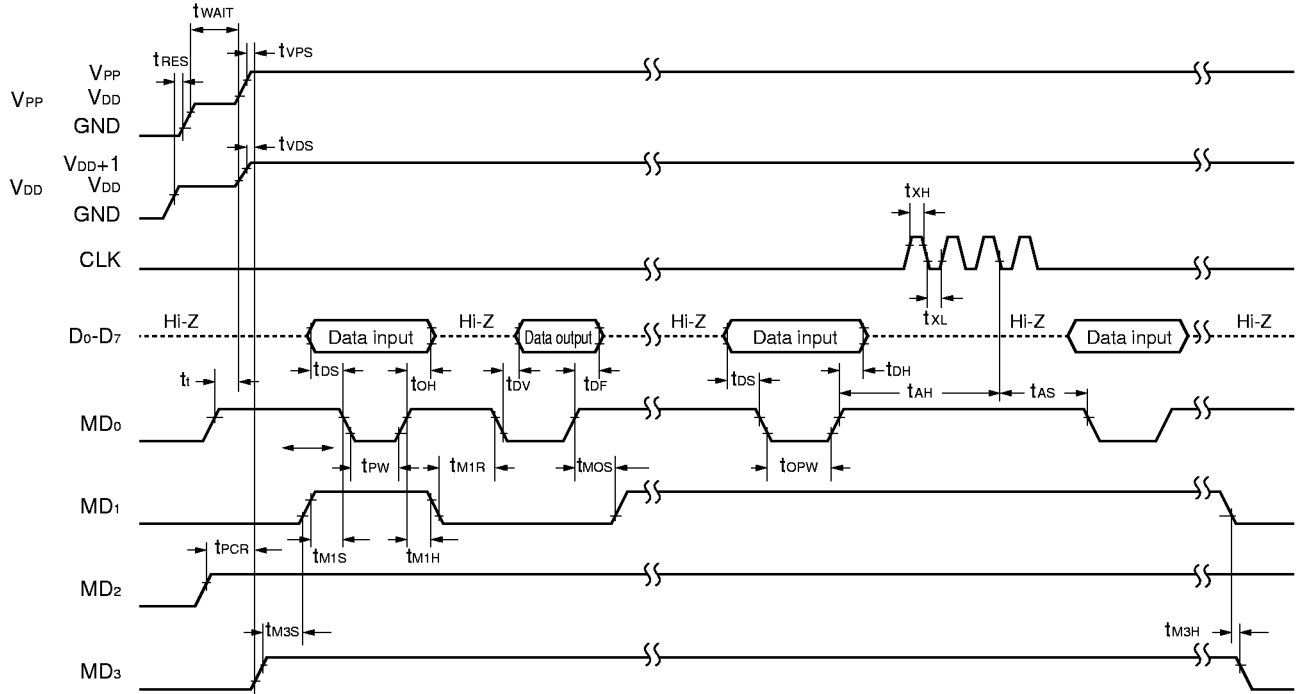
- Cautions**
1. Keep V_{PP} to within +11 V including overshoot.
 2. Apply V_{DD} before V_{PP} and turns it off after V_{PP}.

AC Programming Characteristics ($T_A = 25^\circ\text{C}$, $V_{DD} = 6.0 \pm 0.25 \text{ V}$, $V_{PP} = 10.0 \pm 0.3 \text{ V}$)

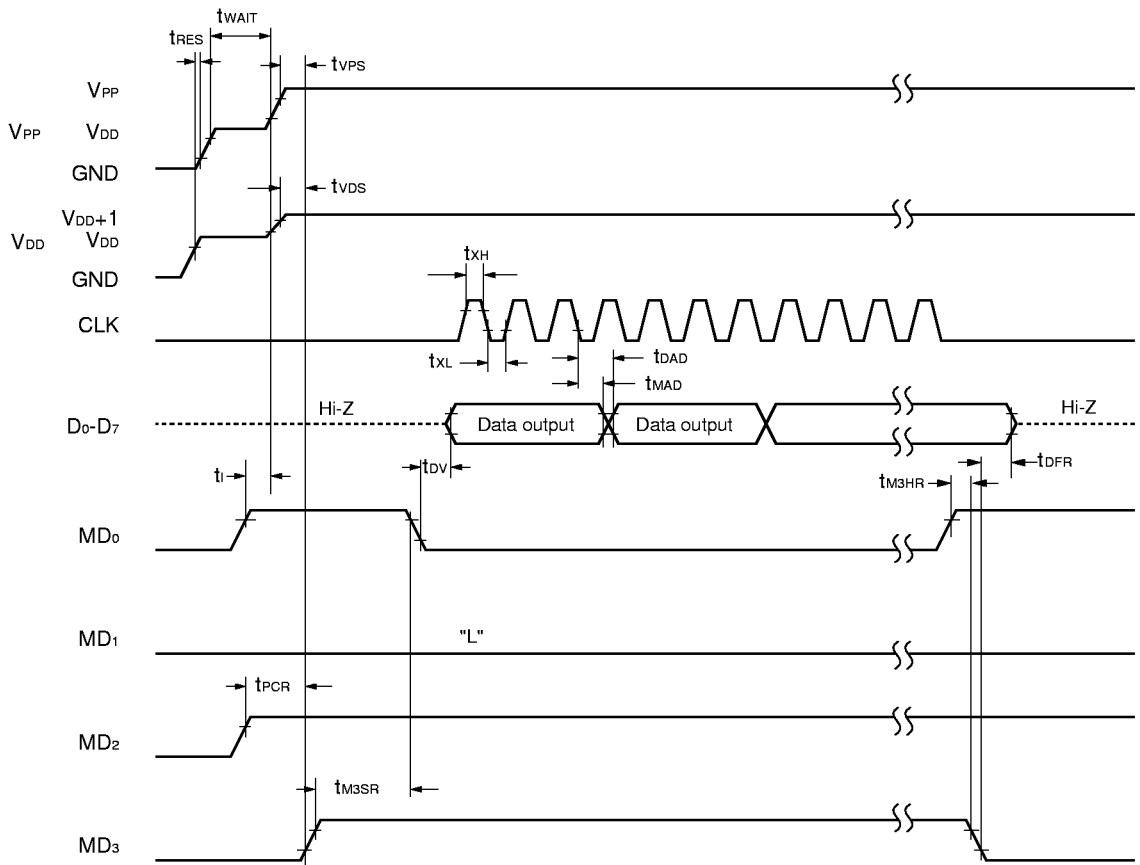
Parameter	Symbol	Note 1	Test Conditions	MIN.	TYP.	MAX.	Unit
Address setup time ^{Note 2} (vs. MD ₀ ↓)	t _{AS}	t _{AS}		2			μs
MD ₁ setup time (vs. MD ₀ ↓)	t _{M1S}	t _{oES}		2			μs
Data setup time (vs. MD ₀ ↓)	t _{DS}	t _{DS}		2			μs
Address hold time ^{Note 2} (vs. MD ₀ ↑)	t _{AH}	t _{AH}		2			μs
Data hold time (vs. MD ₀ ↑)	t _{DH}	t _{DH}		2			μs
MD ₀ ↑ → data output float delay time	t _{DF}	t _{DF}		0		130	ns
V _{PP} setup time (vs. MD ₃ ↑)	t _{VPS}	t _{VPS}		2			μs
V _{DD} setup time (vs. MD ₃ ↑)	t _{VDS}	t _{VCS}		2			μs
Initial program pulse width	t _{PW}	t _{PW}		0.95	1.0	1.05	ms
Additional program pulse width	t _{OPW}	t _{OPW}		0.95		21.0	ms
MD ₀ setup time (vs. MD ₁ ↑)	t _{MOS}	t _{CES}		2			μs
MD ₀ ↓ → data output delay time	t _{DV}	t _{DV}	MD ₀ = MD ₁ = V _{IL}			1	μs
MD ₁ hold time (vs. MD ₀ ↑)	t _{M1H}	t _{oEH}	t _{M1H} +t _{M1R} ≥ 50 μs	2			μs
MD ₁ recovery time (vs. MD ₀ ↓)	t _{M1R}	t _{oR}		2			μs
Program counter reset time	t _{PCR}	—		10			μs
CLK input high-, low-level width	t _{XH} , t _{XL}	—		0.125			μs
CLK input frequency	f _X	—				8	MHz
Initial mode set time	t _i	—		2			μs
MD ₃ setup time (vs. MD ₁ ↑)	t _{M3S}	—		2			μs
MD ₃ hold time (vs. MD ₁ ↓)	t _{M3H}	—		2			μs
MD ₃ setup time (vs. MD ₀ ↓)	t _{M3SR}	—	When program memory is read	2			μs
Address ^{Note 2} → data output delay time	t _{OAD}	t _{ACC}	When program memory is read			2	μs
Address ^{Note 2} → data output hold time	t _{HAD}	t _{OH}	When program memory is read	0		130	ns
MD ₃ hold time (vs. MD ₀ ↑)	t _{M3HR}	—	When program memory is read	2			μs
MD ₃ ↓ → data output float delay time	t _{DFR}	—	When program memory is read			2	μs
Reset setup time	t _{RES}	—		10			μs
Oscillation stabilization wait time ^{Note 3}	t _{WAIT}	—		2			ms

- Notes**
1. Equivalent symbol of the corresponding μ PD27C256A (The μ PD27C256A is a maintenance product.)
 2. The internal address signal is incremented at the falling edge of the third clock of CLK.
 3. Connect a resistor ($R = 47 \text{ k}\Omega$) and a capacitor ($C = 27 \text{ pF}$) between the OSC_{IN} and OSC_{OUT} pins.

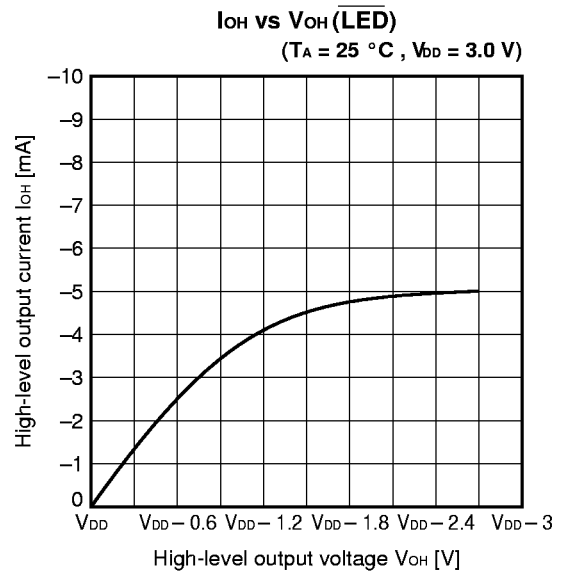
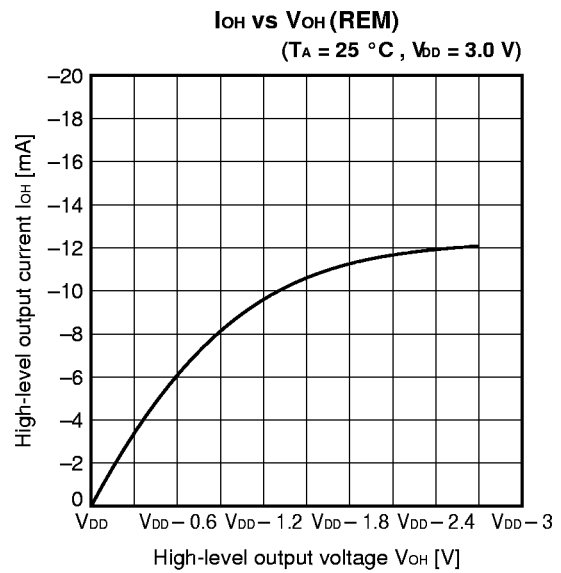
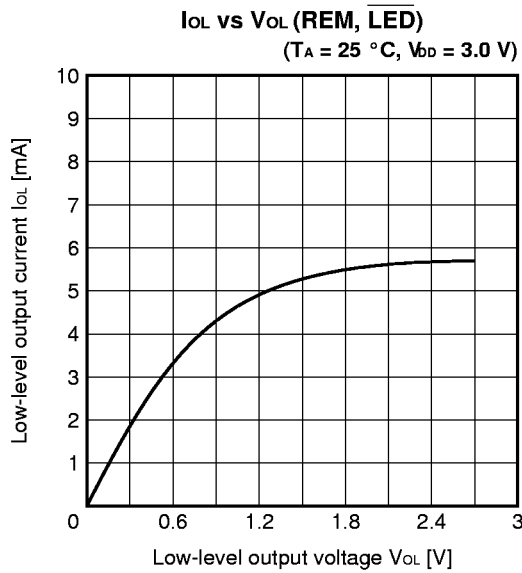
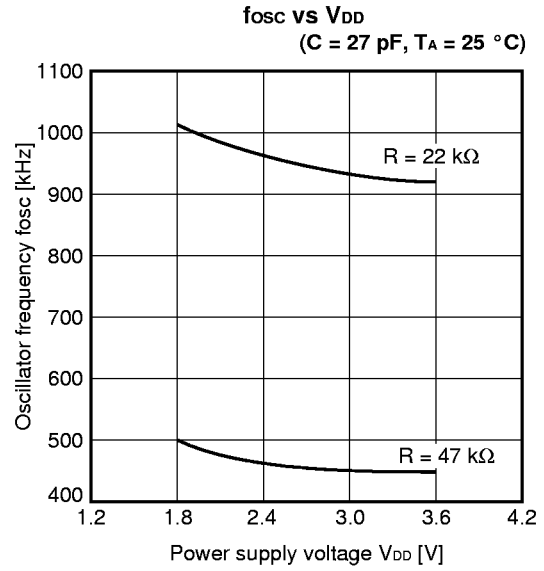
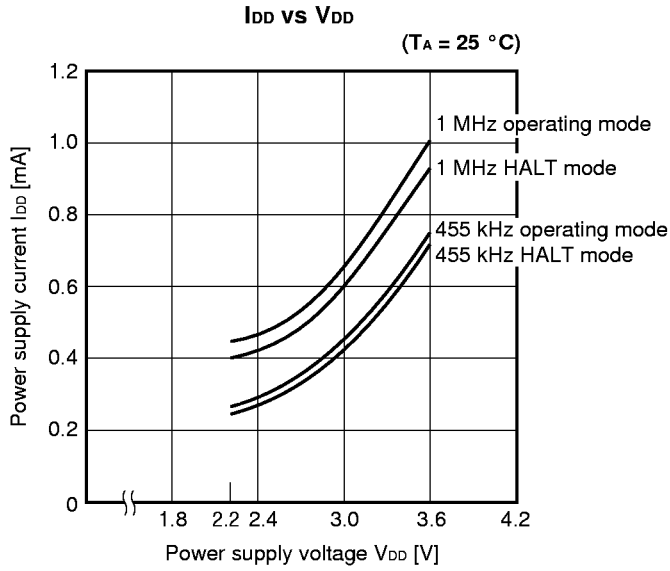
Program Memory Write Timing



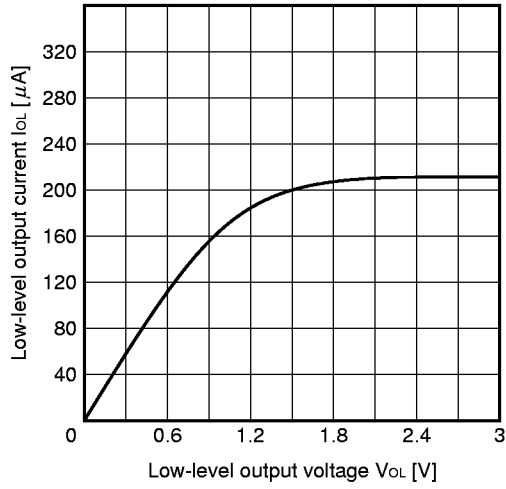
Program Memory Read Timing



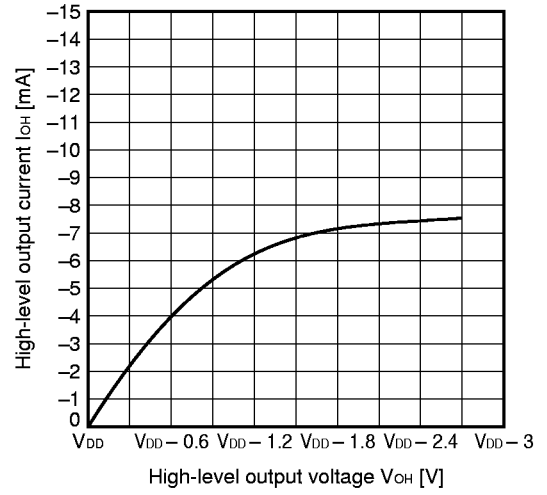
5. CHARACTERISTIC CURVE (REFERENCE VALUES)



I_{OL} vs V_{OL} (K_{I/O})
 (T_A = 25 °C, V_{DD} = 3.0 V)



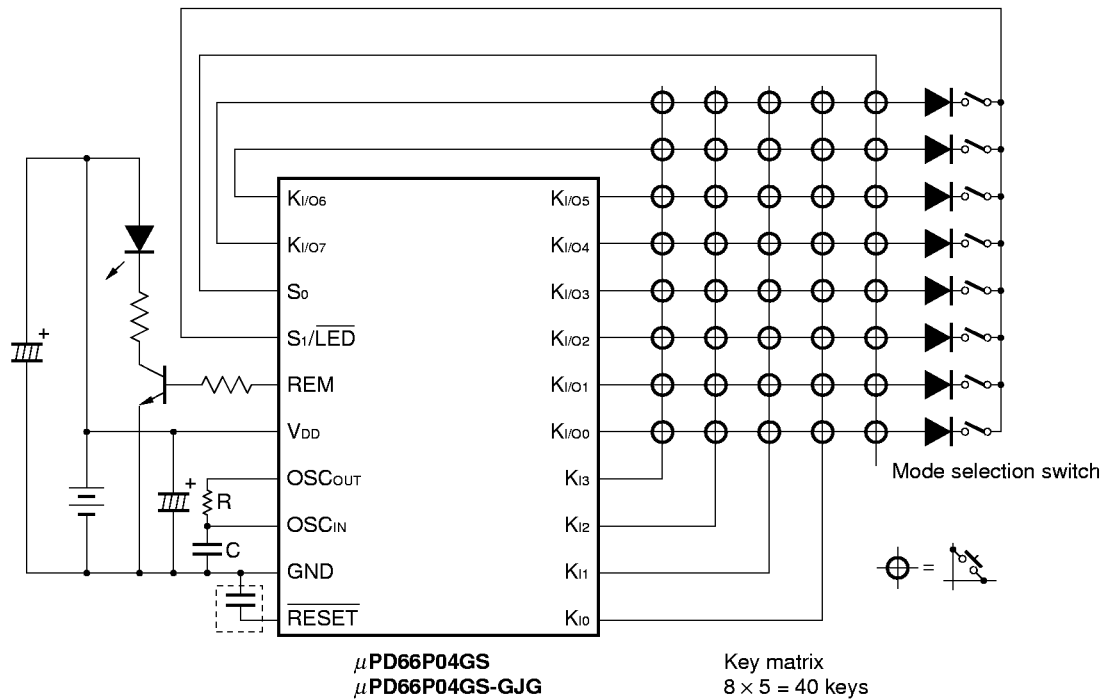
I_{OH} vs V_{OH} (K_{I/O})
 (T_A = 25 °C, V_{DD} = 3.0 V)



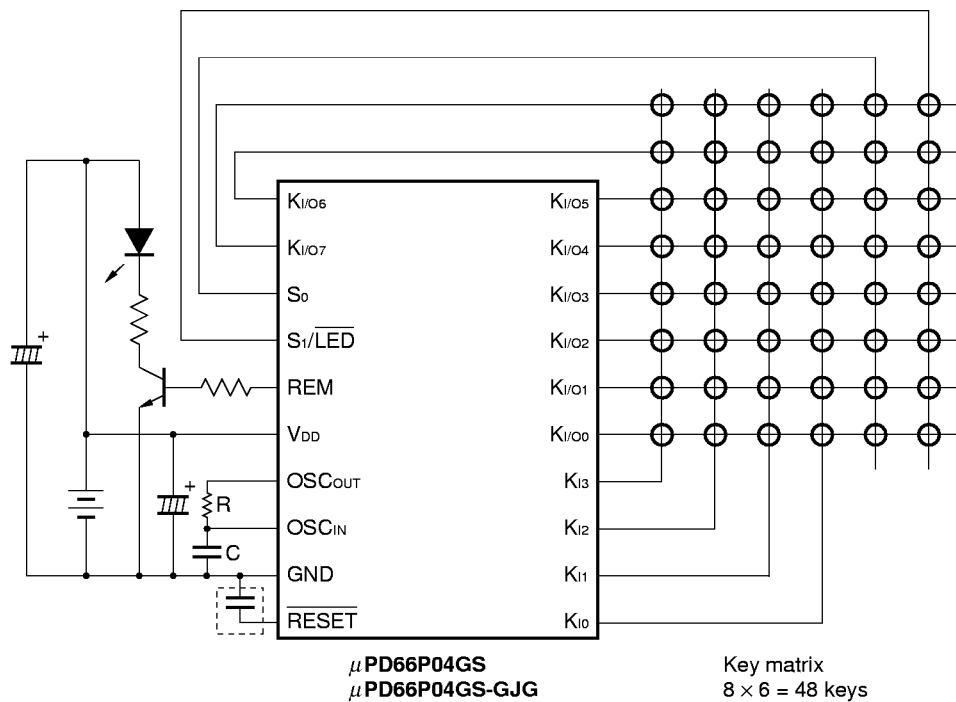
6. APPLIED CIRCUIT EXAMPLE

Example of Application to System

- Remote-control transmitter (40 keys; mode selection switch accommodated)



- Remote-control transmitter (48 keys accommodated)

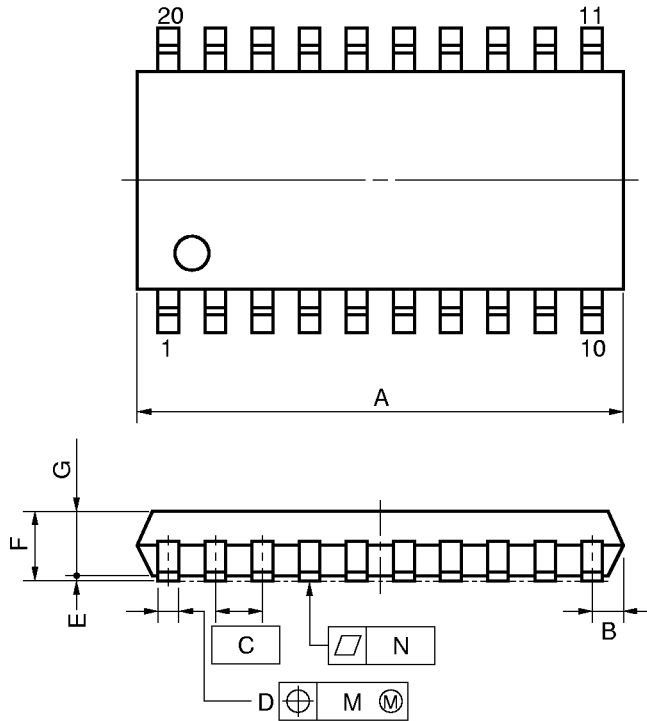


Remark When the POC circuit is used effectively, it is not necessary to connect the capacitor enclosed in the dotted lines.

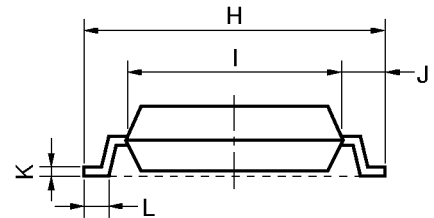
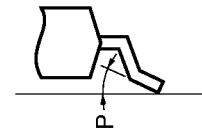
7. PACKAGE DRAWINGS

(1) μPD66P04GS

20 PIN PLASTIC SOP (300 mil)



detail of lead end



NOTE

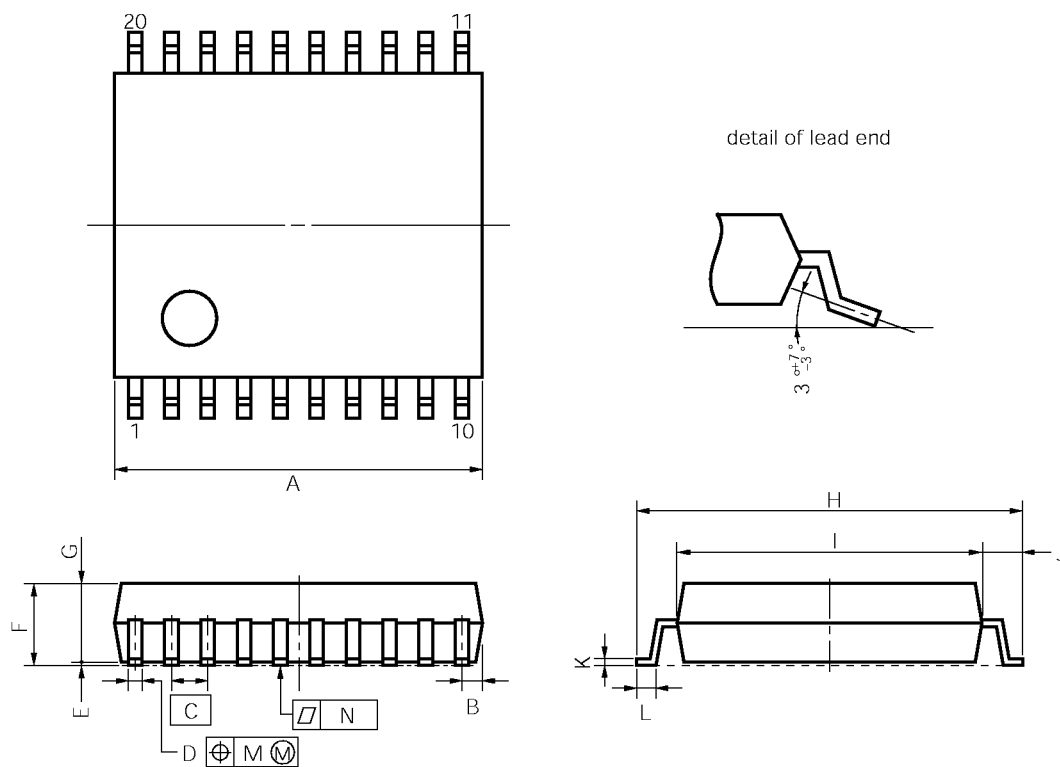
Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	13.00 MAX.	0.512 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	0.40 ^{+0.10} _{-0.05}	0.016 ^{+0.004} _{-0.003}
E	0.1±0.1	0.004±0.004
F	1.8 MAX.	0.071 MAX.
G	1.55	0.061
H	7.7±0.3	0.303±0.012
I	5.6	0.220
J	1.1	0.043
K	0.20 ^{+0.10} _{-0.05}	0.008 ^{+0.004} _{-0.002}
L	0.6±0.2	0.024 ^{+0.008} _{-0.009}
M	0.12	0.005
N	0.10	0.004
P	3°+7° -3°	3°+7° -3°

P20GM-50-300B, C-4

(2) μPD66P04GS-GJG

20 PIN PLASTIC SHRINK SOP (300 mil)



NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

P20GM-65-300B-2

ITEM	MILLIMETERS	INCHES
A	7.00 MAX.	0.276 MAX.
B	0.575 MAX.	0.023 MAX.
C	0.65 (T.P.)	0.026 (T.P.)
D	0.30±0.10	0.012 ^{+0.004} _{-0.005}
E	0.125±0.075	0.005±0.003
F	2.0 MAX.	0.079 MAX.
G	1.7	0.067
H	8.1±0.3	0.319±0.012
I	6.1±0.2	0.240±0.008
J	1.0±0.2	0.039 ^{+0.009} _{-0.008}
K	0.15 ^{+0.10} _{-0.05}	0.006 ^{+0.004} _{-0.002}
L	0.5±0.2	0.020 ^{+0.008} _{-0.009}
M	0.12	0.005
N	0.10	0.004

8. RECOMMENDED SOLDERING CONDITIONS

Carry out the soldered packaging of this product under the following recommended conditions.

For details of the soldering conditions, refer to information material **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than the recommended conditions, please consult one of our NEC sales representatives.

Table 8-1. Soldering Conditions for Surface-Mount Type

μPD66P04GS : 20-pin plastic SOP (300 mil)

μPD66P04-GJG: 20-pin plastic shrink SOP (300 mil)

Soldering Method	Soldering Condition	Recommended Condition Symbol
Partial heating	Pin temperature: 300 °C or less ; time: 3 secs or less (for each side of the device)	—

APPENDIX A. DEVELOPMENT TOOLS

This product uses no hardware in-circuit emulator, etc. Instead, the software simulator is used from designing to development and evaluation.

As a writing tools for the μ PD66P04, a PROM programmer and program adapter are provided.

Hardware

- **PROM programmer (AF-9704^{Note}, AF-9705^{Note}, AF-9706^{Note})**

This PROM programmer supports the μ PD66P04.

By connecting a program adapter to this PROM programmer, the μ PD66P04 can be programmed.

Note These are products of Ando Electric. For details, consult Ando Electric (03-3733-1163).

- **Program adapter (PA-61F34)**

It is used to program the μ PD66P04 in combination with AF-9704, AF-9705, or AF-9706.

Software

• **Software simulator (SM6133)**

- Refers to the software development tool of the remote-control transmitter.
- An assembler (AS6133) is added.

Caution The assembler alone cannot be purchased.

List of SM6133 Ordering Codes

Host Machine	OS		Supply Medium	Ordering Code
PC-9800 series (CPU: 80386 and up)	MS-DOS™	Windows™	3.5-inch 2HD	μSAA13SM6133
	PC DOS™		3.5-inch 2HC	μSBB13SM6133
IBM PC/AT™ and compatible	PC DOS™			

Remark The matching OS versions are as follows.

OS	Version
MS-DOS	Ver. 3.30 to Ver. 5.00
PC DOS	Ver. 3.1 to Ver. 5.0
Windows	Ver. 3.0 to Ver. 3.1

- CPU: 80386 and up (80486DX2 at 66 MHz or higher recommended); Windows environment (PC-9800 series; IBM PC/AT)
- Simulation run time: About 500 times of the actual device (when using CPU of 80486 at 16 MHz)
- Key matrix (KEY MAT) function : Capable of applications ranging from single pressing to continuous/multiple pressing, etc. (automatic patch)
: Direct input possible (serial communications mode available)
- Remote-control waveform data translation function: Translates data values to numeric values "0" and "1".

<Example> In the case of the NEC format:

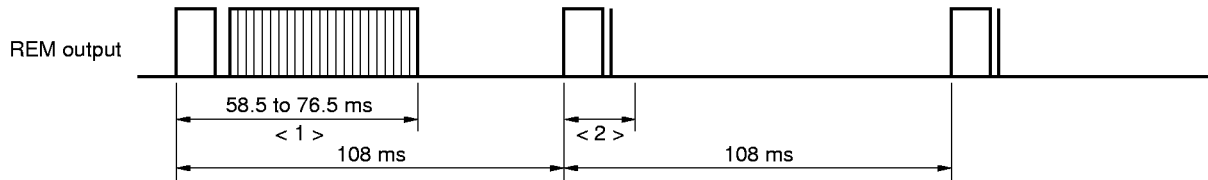
Header + customer code + data code + STOP bit + frame space
(P + 5A6C + 18E7 + H500μ + L2000μ)

- WAVE function: Edits and displays the I/O waveform and the key press waveform.
- MEMORY function: Displays all the memory values in real time.
- LISTING function: Capable of Run, Break, Continuous Exec/Step Exec operations.
- Editing function: Can correct and change the program on the simulator.
- TRIGGER function: Break conditions <program counter, memory register, stack level, run time>
<single, AND, OR, sequential>
- TRACE function: Can trace the program counter, the memory, and the register and measure their times.

APPENDIX B. EXAMPLE OF REMOTE-CONTROL TRANSMISSION FORMAT
 (in the case of NEC transmission format in command one-shot transmission mode)

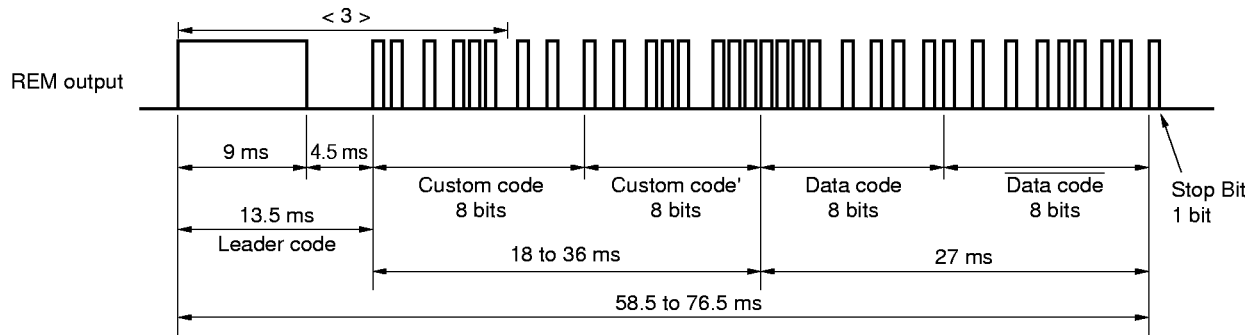
Caution When using the NEC transmission format, please apply for a custom code at NEC.

(1) REM output waveform (From <2> on, the output is made only when the key is kept pressed.)

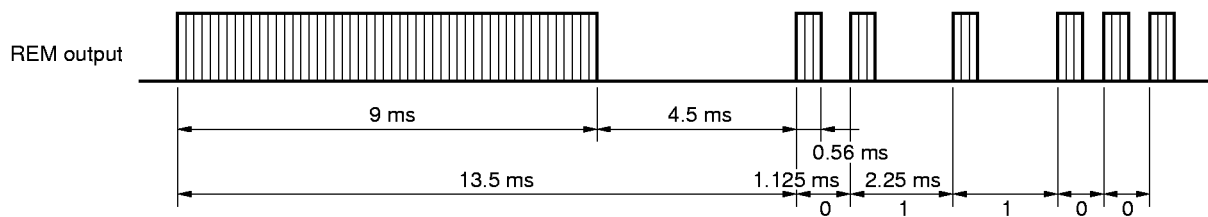


Remark If the key is repeatedly pressed, the power consumption of the infrared light-emitting diode (LED) can be reduced by sending the reader code and the stop bit from the second time.

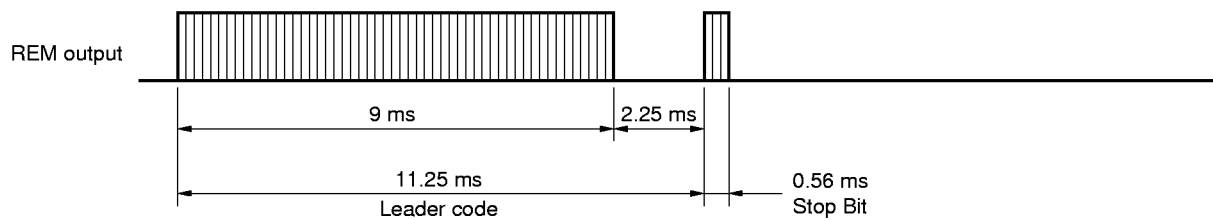
(2) Enlarged waveform of <1>



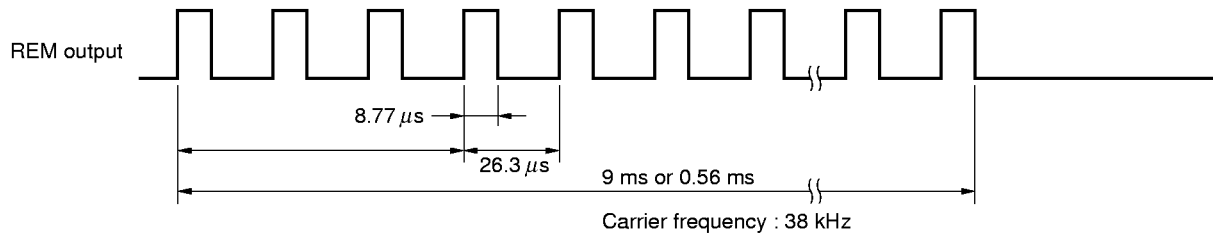
(3) Enlarged waveform of <3>



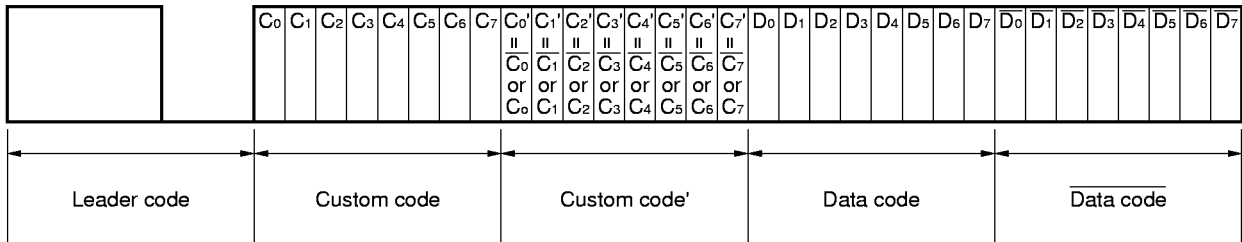
(4) Enlarged waveform of <2>



(5) Carrier waveform (Enlarged waveform of each code's high period)



(6) Bit array of each code



Caution To prevent malfunction with other systems when receiving data in the NEC transmission format, not only fully decode (make sure to check Data Code as well) the total 32 bits of the 16-bit custom codes (Custom Code, Custom Code') and the 16-bit data codes (Data Code, Data Code) but also check to make sure that no signals are present.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.