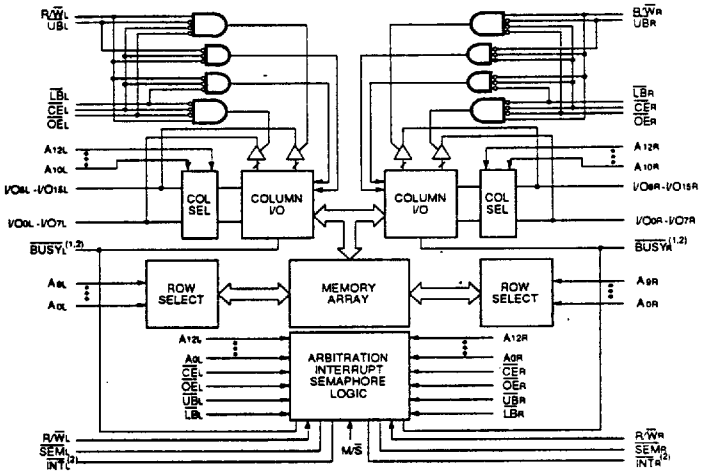
Radiation Hardened 7025RP

High - Speed 8K x 16 Dual - Port Static RAM

For Space Applications



SEI's 7025RP (RP for RAD-PAK®) high speed CMOS microcircuit features a minimum 100 kilorad (Si) total dose tolerance. Using SEI's radiation hardened RAD-PAK® packaging technology, the 7025RP combines Integrated Device Technology's advanced CMOS process and SEI's radiation hardened RAD-PAK® packaging. The 7025RP is designed to be used as a stand-alone 128K-bit Dual-Port RAM or as a combination MASTER/SLAVE Dual-Port RAM for 32-bit or more word systems. This design results in full-speed, error-free operation without the need for additional discrete logic. The 7025RP provides two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature controlled by $\overline{CE}$ permits the on-chip circuitry of each port to enter a very low standby power mode. The RAD-PAK® technology incorporates radiation shielding in the microcircuit package. It eliminates box shielding while providing life time in orbit. The 7025RP features the same system performance and architecture as the commercial counterparts. Capable of surviving in space environments, the 7025RP is ideal for satellite, spacecraft, and space probe missions. It is available in Class S packaging and screening.

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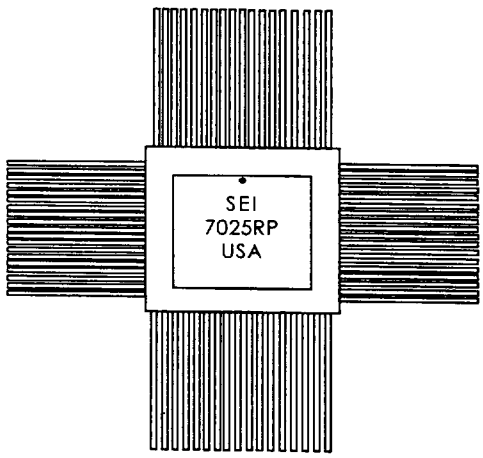
9011241 0000128 499

Radiation Hardened
7025RP

High Speed 8k x 16
Dual - Port Static RAM



PIN CONFIGURATION
TOP VIEW

Features

- 8k x 16 Dual Port Organization
- Pin Compatible with IDT7025
- RAD-PAK® Radiation Hardened Against Natural Space Radiation
- Total Dose Hardness >100 krad (Si)
- Package:
  - 84 Pin RAD-PAK® quad flat pack (650 mils x 650 mils)
  - Weight – 14 grams
- True Dual-Ported Memory Cells Which Allow Simultaneous Reads of the Same Memory Location
- High Speed Access Time:
  - 45/55 ns
- Expandable to 32 Bits or More Using Master/Slave Select When Cascading
- High Speed CEMOS Technology
  - Low Power Operation:
    - 750mW Active
    - 5mW Standby (typ)
  - TTL Compatible, Single +5V Power Supply
  - Interrupt Flag
  - On Chip Port Arbitration Logic
  - Asynchronous Operation From Either Port
- Screening per TM5004
- QCI per TM5005

TQM
Total Quality Management

Aug 1994

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7025RP ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage	V_{CC}	-0.5	7.0	V
Voltage on Any Pin, Relative to V_{SS}	V_T	-0.5	V_{CC}+0.5	V
Power Dissipation	P_D		1.0	W
Storage Temperature	T_S	-65	+150	°C
Operating Temperature	T_A	-55	+125	°C

7025RP RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage, Positive	V_{CC}	4.5	5.5	V
Supply Voltage, Negative	V_{SS}	0	0	V
Input High Voltage	V_{IH}	2.2	6.0	V
Input Low Voltage	V_{IL}	-0.5	0.8	V
Operating Temperature	T_A	-55	+125	°C

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7025RP DC ELECTRICAL CHARACTERISTICS[1]

PARAMETER	SYMBOL	MIN	MAX	UNIT	NOTES
Input Low Voltage	V_{IL}	-0.5	0.8	V	
Input High Voltage	V_{IH}	2.2	V_{cc}+0.3	V	
Output Low Voltage	V_{OL}		0.4	V	I_{OL}=4mA
Output High Voltage	V_{OH}	2.4		V	I_{OH}=-4mA
Input Leakage Current	I_{IN}		±10	uA	V_{CC}=5.5V, 0V<V_{IN}<5V
Output Leakage Current	I_{OL}		±10	uA	0V<V_{OUT}<5V CE\=5V
Dynamic Operating Supply Current, DC	I_{CC}		400	mA	f=f_{max}, CE\≤V_{IL}, SEM\≥V_{IH}
Standby Current, Both Ports, TTL Level In	I_{SB1}		85	mA	f=f_{max}, CE_R\=CE_L≥V_{IH}, SEM_R\=SEM_L\≥V_{IH}
Standby Current, One Port, TTL Level In	I_{SB2}		290	mA	f=f_{max}, CE_R\=CE_L≥V_{IH}, SEM_R\=SEM_L\≥V_{IH}
Full Standby Current, Both Ports, CMOS Level In	I_{SB3}		30	mA	f=0, Both ports CE_R\=CE_L≥V_{CC}-.2, SEM_R\=SEM_L\≥V_{CC}-.2
Full Standby Current, One Port, CMOS Level In	I_{SB4}		260	mA	f=f_{max}, One port CE_R\≥V_{CC}-.2, SEM_R\=SEM_L\≥V_{CC}-.2
Input Capacitance[2]	C_{IN}		12	pF	f=1MHz
Output Capacitance[2]	C_{OUT}		12	pF	f=1MHz

Notes: 1. V_{CC} = 4.5 to 5.5 volts; V_{SS} = 0 volts; T_A = -55 to +125 °C.
2. Guaranteed by design.

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7025RP AC ELECTRICAL CHARACTERISTICS - READ CYCLE[1]

PARAMETER	SYMBOL	MIN	MAX	UNITS
Read Cycle Time	t_{RC}			
7025ERPx-45		45		ns
7025ERPx-35		35		ns
Address Access Time	t_{AA}			
7025ERPx-45			45	ns
7025ERPx-35			35	ns
Chip Enable Access Time[2]	t_{ACE}			
7025ERPx-45			45	ns
7025ERPx-35			35	ns
Byte Enable Access Time[2]	t_{ABE}			
7025ERPx-45			45	ns
7025ERPx-35			35	ns
Output Enable to Output Valid	t_{AOE}			
7025ERPx-45			25	ns
7025ERPx-35			20	ns
Output Low Z Time[3,4]	t_{LZ}			
7025ERPx-45		5		ns
7025ERPx-35		3		ns
Output High Z Time[3,4]	t_{HZ}			
7025ERPx-45			20	ns
7025ERPx-35			15	ns
Chip Enable to Power Up Time[3]	t_{PU}	0		ns
Chip Disable to Power Up Time[3]	t_{PD}		50	ns
Semaphore Flag Update Pulse (OE\ or SEM\)	t_{SOP}	15		ns
Output Hold from Address Change	t_{OH}	3		ns

Notes:
1. V_{CC} = 4.5 to 5.5 volts; V_{SS} = 0 volts; T_A = -55 to +125 °C.
2. To access RAM, CE\ = L, UB\ or LB\ = L, SEM\ = H.
3. This parameter is guarenteed by design and is not tested.
4. Transition is measured ±500mV from low or high impedance voltage with load.

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7025RP AC ELECTRICAL CHARACTERISTICS - WRITE CYCLE[1]

PARAMETER	SYMBOL	MIN	MAX	UNITS
Write Cycle Time	t_{WC}			
Address Valid to End of Write	t_{AW}			
Chip Enable to End of Write[2]	t_{EW}			
Address Setup Time[2]	t_{AS}	0		ns
Write Pulse Width	t_{WP}			
Write Recovery Time	t_{WR}	0		ns
Data Valid to End of Write	t_{DW}	25		ns
Output High-Z Time[3,4]	t_{HZ}			
Data Hold Time[5]	t_{DH}	0		ns
Write Enable to Output in High-Z[3,4]	t_{WZ}			
Output Active from End of Write[3,4,5]	t_{OW}	0		ns
SEM\ Flag Write to Read Time	t_{SWRD}	10		ns
SEM\ Flag Contention Window	t_{SPS}	10		ns

Notes:

1. V_{CC} = 4.5 to 5.5 volts; V_{SS} = 0 volts; T_A = -55 to +125 °C.
2. To access RAM, CE\ = L, UB\ or LB\ = L, SEM\ = H. To access semaphore, CE\ = H and SEM\ = L. Either condition must be valid for the entire t_{EW} time.
3. This parameter is guarenteed by design and is not tested.
4. Transition is measured ±500mV from low or high impedance voltage with load.
5. The specification for t_{DH} must be met by the device supplying write data to the RAM under all operating conditions. Although t_{DH} and t_{OW} values will vary over voltage and temperature, the actual t_{DH} will always be smaller than the actual t_{OW}.

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7025RP AC ELECTRICAL CHARACTERISTICS - TIMING[1]

PARAMETER	SYMBOL	MIN	MAX	UNITS
BUSY\ Access Time from Address Match[2]	t_{BAA}		35	ns
BUSY\ Disable Time from Address Not Matched[2]	t_{BDA}		30	ns
BUSY\ Access Time from Chip Enable Low[2]	t_{BAC}		30	ns
BUSY\ Disable Time from Chip Enable High[2]	t_{BDC}		25	ns
Arbitration Priority Setup Time[2]	t_{APS}	5		ns
BUSY\ Disable to Valid Data[2,3]	t_{BDD}		0[2]	ns
BUSY\ Input to Write[4]	t_{WB}	0		ns
Write Hold after BUSY\[4,5]	t_{WH}	25		ns
Data Hold Time[5]	t_{DH}	0		ns
Write Pulse to Data Delay[6] 7025RPx-45 7025RPx-35	t_{WDD}		 70 60	 ns ns
Write Data Valid to Read Data Delay[6] 7025RPx-45 7025RPx-35	t_{DDD}		 55 45	 ns ns
Address Setup Time[7]	t_{AS}	0		ns
Write Recovery Time[7]	t_{WR}	0		ns
Interrupt Set Time[7] 7025RPx-45 7025RPx-35	t_{INS}		 35 30	 ns ns
Interrupt Reset Time[7] 7025RPx-45 7025RPx-35	t_{INR}		 35 30	 ns ns

Notes:
1. V_{CC} = 4.5 to 5.5 volts; V_{SS} = 0 volts; T_A = -55 to +125 °C.
2. BUSY timing, M/S\ = H.
3. t_{BDD} is a calculated parameter and is the greater of 0, t_{WDD} - t_{WP} (actual) or t_{DDD} - t_{DW} (actual).
4. BUSY timing, M/S\ = L.
5. To ensure that a write cycle is completed after contention.
6. Port to port timing delay through RAM cells from writing port to reading port.
7. Interrupt timing.

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7025RP TRUTH TABLES

INTERRUPT FLAG CONTROL[1]

LEFT PORTRIGHT PORT

R/W \L	CE\ L	OE\ L	A_{0L}-A_{12L}	INT \L	R/W\ R	CE\ R	OE\ R	A_{0R}-A_{12R}	INT\ R	FUNCTION
L	L	X	1FFF	X	X	X	X	X	L[2]	Set right INT\R flag
X	X	X	X	X	X	L	L	1FFF	H[3]	Reset right INT\R flag
X	X	X	X	L[3]	L	L	X	1FFE	X	Set left INT\L flag
X	L	L	1FFE	H[2]	X	X	X	X	X	Reset left INT\L flag

Notes:
1. Assumes BUSY\L = BUSY\R = H.
2. If BUSY\L = L, then no change.
3. If BUSY\R = L, then no change.

ADDRESS BUSY ARBITRATION [1]

INPUTS			OUTPUTS		
CE\L	CE\R	A_{0L}-A_{12L} A_{0R}-A_{12R}	BUSY\L[1]	BUSY\R[1]	FUNCTION
X	X	No Match	H	H	Normal
H	X	Match	H	H	Normal
X	H	Match	H	H	Normal
L	L	Match	(2)	(2)	Write Inhibit[3]

Notes:

1. Pins BUSY\L and BUSY\R are both outputs when the part is configured as a master. Both are inputs when configured as a slave. BUSY\X outputs on the 7025RP are push pull, not open drain outputs. On slaves the BUSY\X input internally inhibits writes.

2. L if the inputs to the opposite port were stable prior to the address and enable inputs of this port. H if the inputs to the opposite port became stable after the address and enable inputs of this port. If t_{APS} is not met, either BUSY\L or BUSY\R = Low will result. BUSY\L and BUSY\R outputs cannot be low simultaneously.

3. Writes to the left port are internally ignored when BUSY\L outputs are driving low regardless of actual logic level on the pin. Writes to the right port are internally ignored when BUSY|R outputs are driving low regardless of actual logic level on the pin.

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7025RP TRUTH TABLES

NON-CONTENTION READ/WRITE CONTROL

CE\	R/W\	OE\	UB\	LB\	SEM\	I/O_{8-15}	I/O_{0-7}	MODE
H	X	X	X	X	H	Hi-Z	Hi-Z	Deselected:Power Down
X	X	X	H	H	H	Hi-Z	Hi-Z	Both bytes deselected;Power Down
L	L	X	L	H	H	$DATA_{in}$	Hi-Z	Write to upper byte only
L	L	X	H	L	H	Hi-Z	$DATA_{in}$	Write to lower byte only
L	L	X	L	L	H	$DATA_{in}$	$DATA_{in}$	Write to both bytes
L	H	L	L	H	H	$DATA_{out}$	Hi-Z	Read upper byte only
L	H	L	H	L	H	Hi-Z	$DATA_{out}$	Read lower byte only
L	H	L	L	L	H	$DATA_{out}$	$DATA_{out}$	Read both bytes
X	X	H	X	X	X	Hi-Z	Hi-Z	Outputs disabled

SEMAPHORE READ/WRITE CONTROL

CE\	R/W\	OE\	UB\	LB\	SEM\	I/O_{8-15}	I/O_{0-7}	MODE
H	H	L	X	X	L	$DATA_{out}$	$DATA_{out}$	Read data in semaphore flag
X	H	L	H	H	L	$DATA_{out}$	$DATA_{out}$	Read data in semaphore flag
H	/	X	X	X	L	$DATA_{in}$	$DATA_{in}$	Write Din0 into semaphore flag
X	/	X	H	H	L	$DATA_{in}$	$DATA_{in}$	Write Din0 into semaphore flag
L	X	X	L	X	L	--	--	Not allowed
L	X	X	X	L	L	--	--	Not allowed

7025RP Package Ordering Guide

Package Style	Case Outline 1/	Description
Q	Q-84	84 Pin Quad Flat Package

Note:

1/ For outline information, see Appendix A (Package Information - Outline Dimension)

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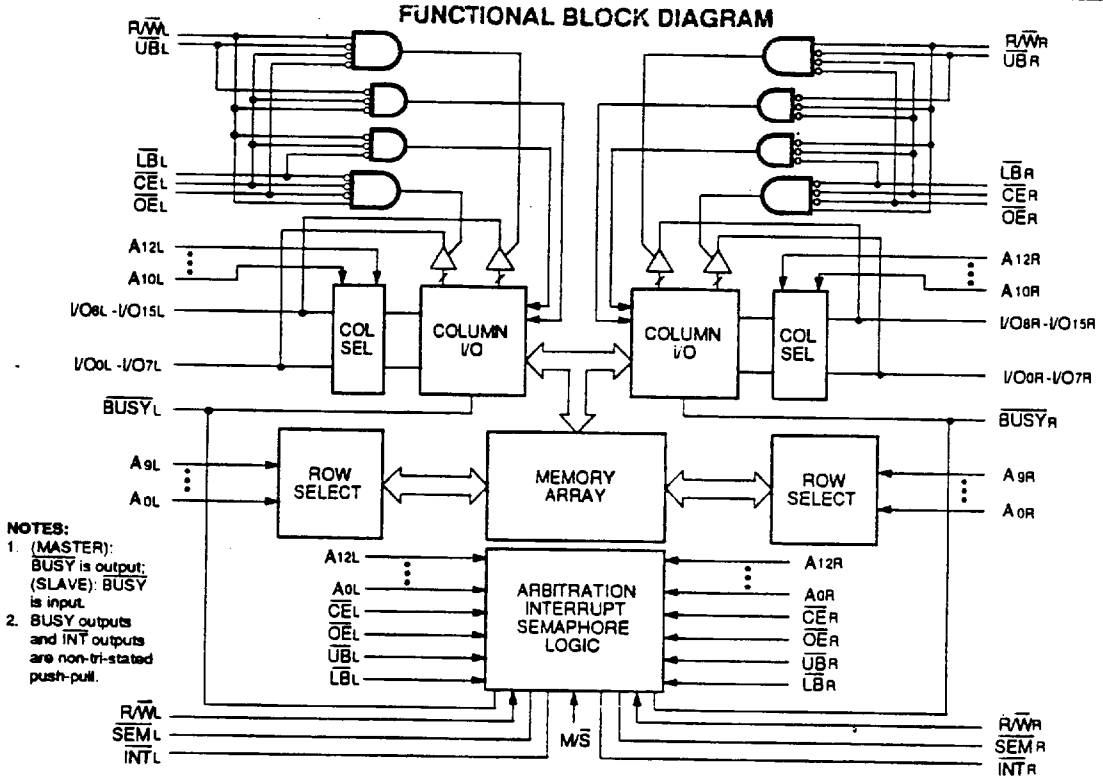
FUNCTIONAL BLOCK DIAGRAM



NOTES:
1. (MASTER): BUSY is output; (SLAVE): BUSY is input.
2. BUSY outputs and INT outputs are non-tri-stated push-pull.

7025 Dual Port RAM Pinout

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	I/O 8L	22	I/O 9R	43	A 6R	64	A 8L
2	I/O 9L	23	I/O 10R	44	A 5R	65	A 9L
3	I/O 10L	24	I/O 11R	45	A 4R	66	A 10L
4	I/O 11L	25	I/O 12R	46	A 3R	67	A 11L
5	I/O 12L	26	I/O 13R	47	A 2R	68	A 12L
6	I/O 13L	27	I/O 14R	48	A 1R	69	LB\ L
7	GND	28	GND	49	A 0R	70	UB\ L
8	I/O 14L	29	I/O 15R	50	INT\ R	71	CE\ L
9	I/O 15L	30	OE\ R	51	BUSY\ R	72	SEM\ L
10	Vcc	31	R/W\ R	52	M/S\	73	R/W\ L
11	GND	32	GND	53	GND	74	Vcc
12	I/O 0R	33	SEM\ R	54	BUSY\ L	75	OE\ L
13	I/O 1R	34	CE\ R	55	INT\ L	76	I/O 0L
14	I/O 2R	35	UB\ R	56	A 0L	77	I/O 1L
15	Vcc	36	LB\ R	57	A 1L	78	GND
16	I/O 3R	37	A 12R	58	A 2L	79	I/O 2L
17	I/O 4R	38	A 11R	59	A 3L	80	I/O 3L
18	I/O 5R	39	A 10R	60	A 4L	81	I/O 4L
19	I/O 6R	40	A 9R	61	A 5L	82	I/O 5L
20	I/O 7R	41	A 8R	62	A 6L	83	I/O 6L
21	I/O 85	42	A 7R	63	A 7L	84	I/O 7L

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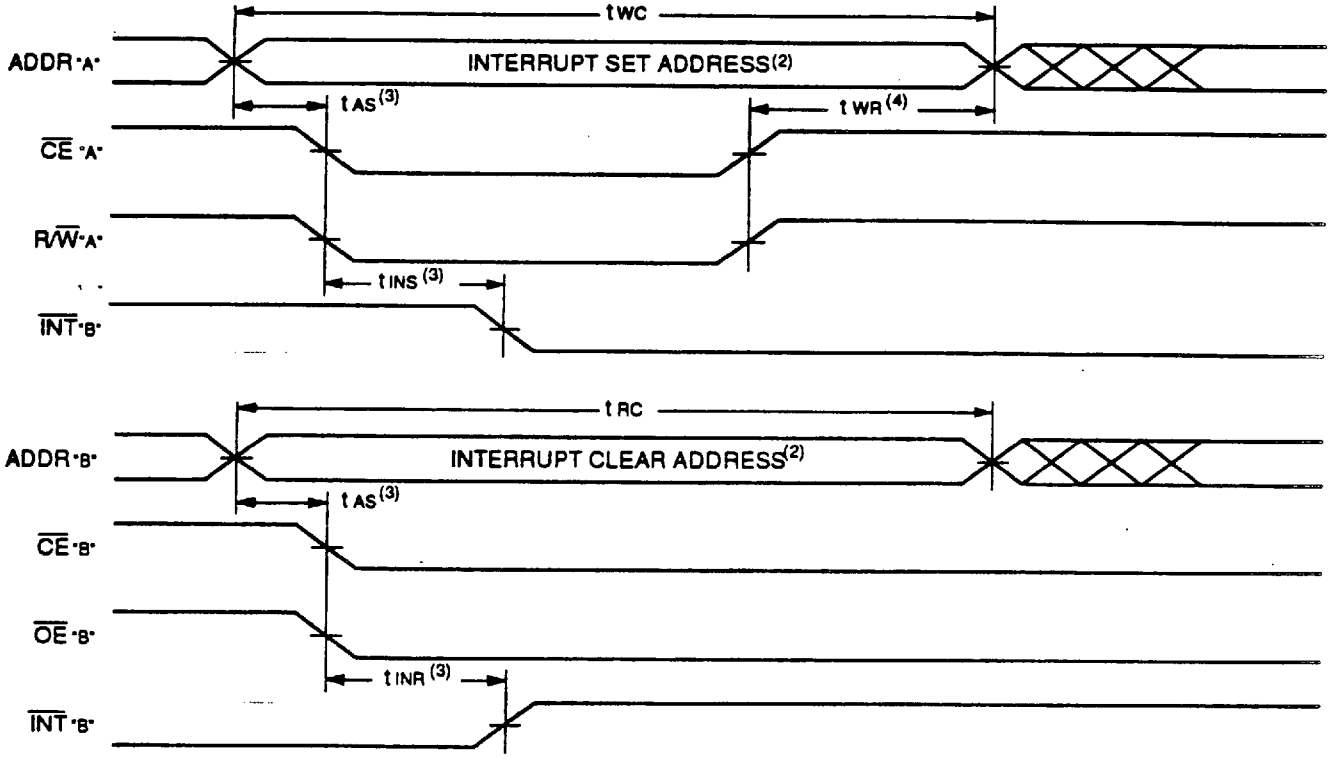
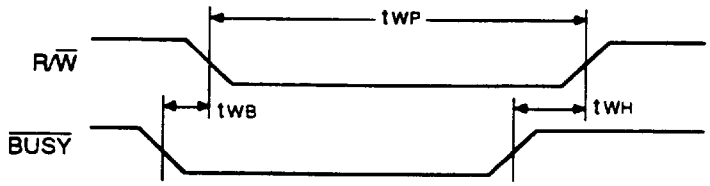
WAVEFORM OF INTERRUPT TIMING[1]

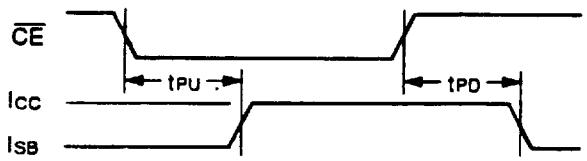


NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from "A".
2. See interrupt truth table.
3. Timing depends on which enable signal is asserted last.
4. Timing depends on which enable signal is de-asserted first.

TIMING WAVEFORM OF SLAVE WRITE (M/$\overline{S}$ = L)



TIMING OF POWER-UP POWER-DOWN



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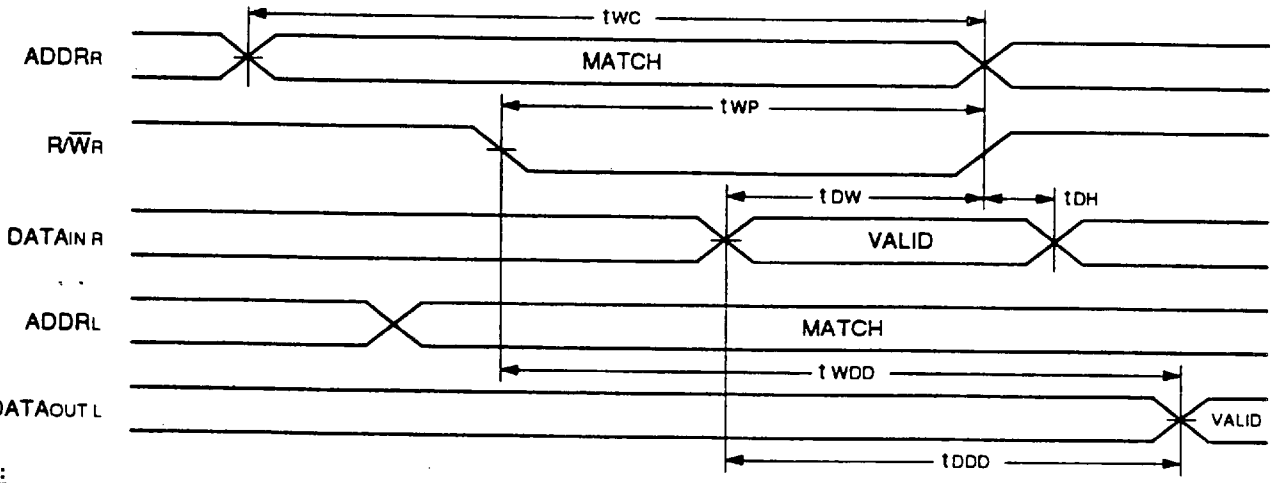
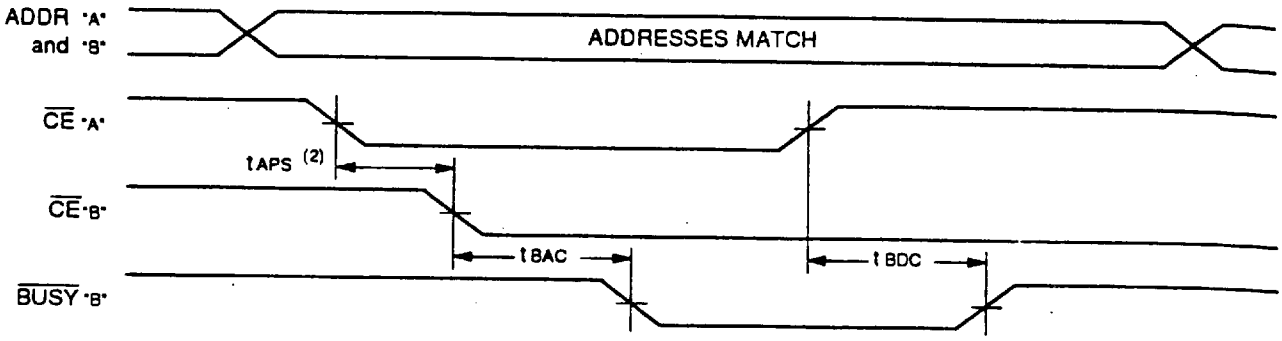
TIMING WAVEFORM OF WRITE WITH PORT-TO-PORT DELAY[1,2] (M/$\overline{S}$ = L)

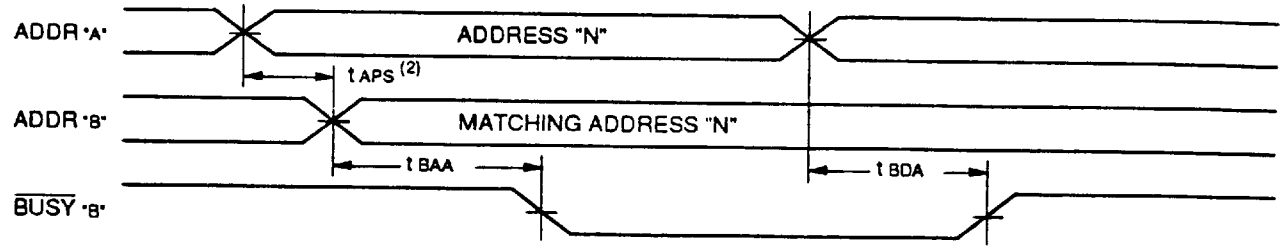


NOTES:
1. $\overline{BUSY}$ input equals H for the writing port.
2. $\overline{CE}_L$ = $\overline{CE}_R$ = L

WAVEFORM OF BUSY ARBITRATION CONTROLLED BY $\overline{CE}$ TIMING[1] (M/$\overline{S}$ = H)



WAVEFORM OF BUSY ARBITRATION CYCLE CONTROLLED BY ADDRESS MATCH TIMING[1](M/$\overline{S}$ = H)



NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from "A".
2. If tAPS is violated, the busy signal will be asserted on one side or another but there is no guarantee on which side busy will be asserted.

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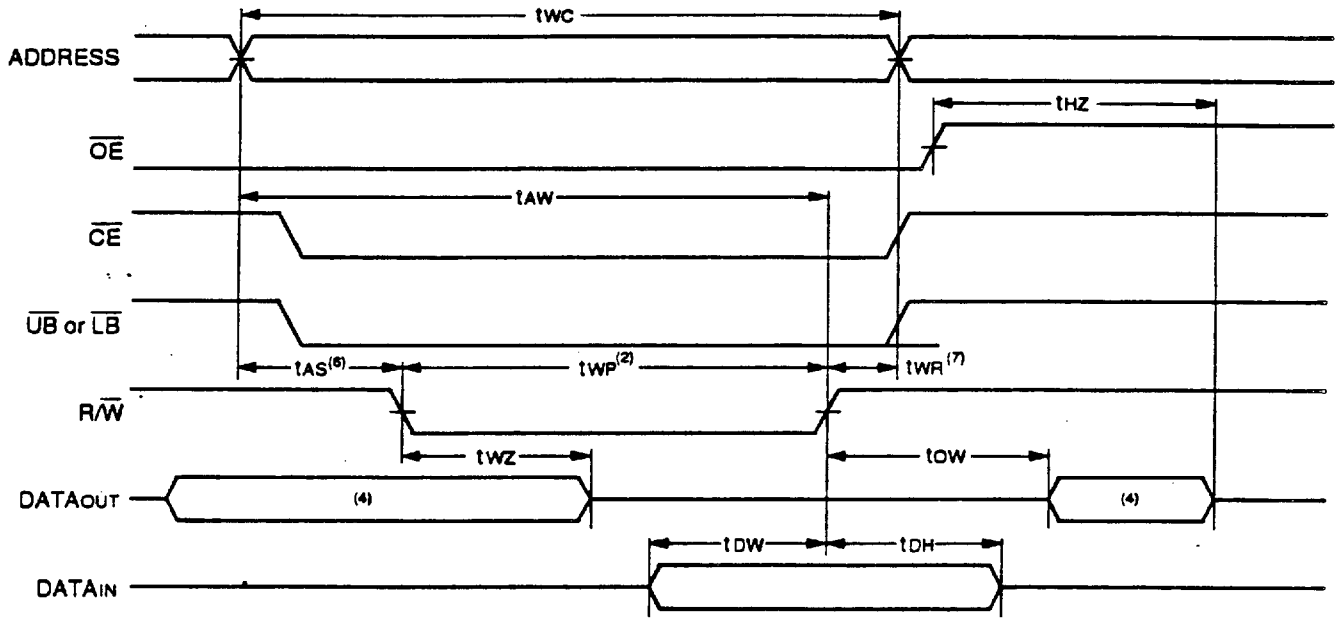
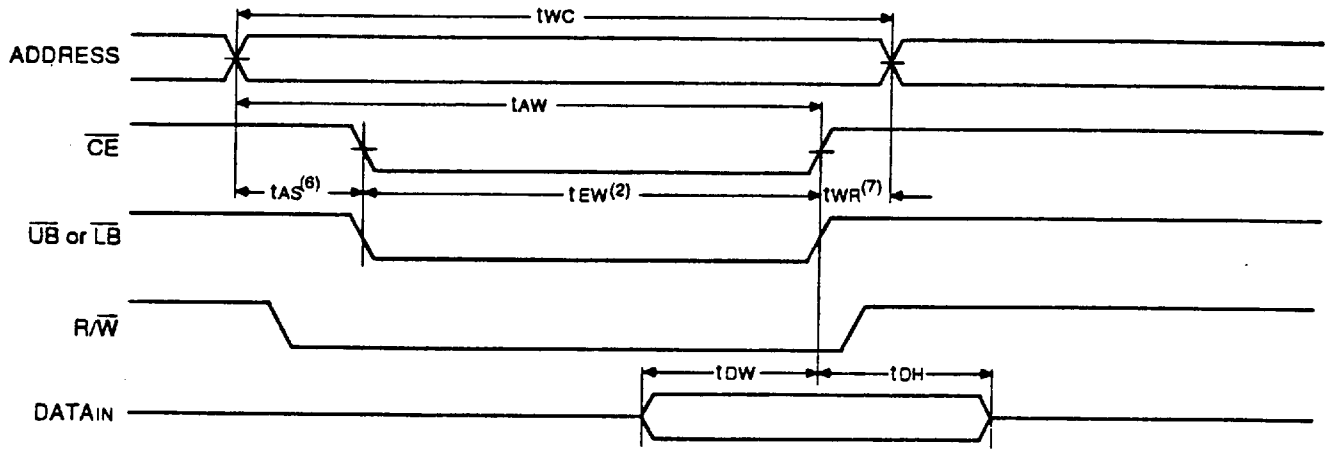
TIMING WAVEFORM OF WRITE CYCLE NO. 1, R/$\overline{W}$ CONTROLLED TIMING(1,3,5,8)



TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CE}$, $\overline{UB}$, $\overline{LB}$ CONTROLLED TIMING(1,3,5,8)



NOTES:

1. R/$\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a low $\overline{UB}$ or $\overline{LB}$ and a low $\overline{CE}$ and a low R/$\overline{W}$ for memory array writing cycle.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ (or $\overline{SEM}$ or R/$\overline{W}$) going high to the end of write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ or $\overline{SEM}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Timing depends on which enable signal is asserted last, $\overline{CE}$, R/$\overline{W}$ or byte control.
7. Timing depends on which enable signal is de-asserted first, $\overline{CE}$, R/$\overline{W}$ or byte control.
8. If $\overline{OE}$ is low during R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

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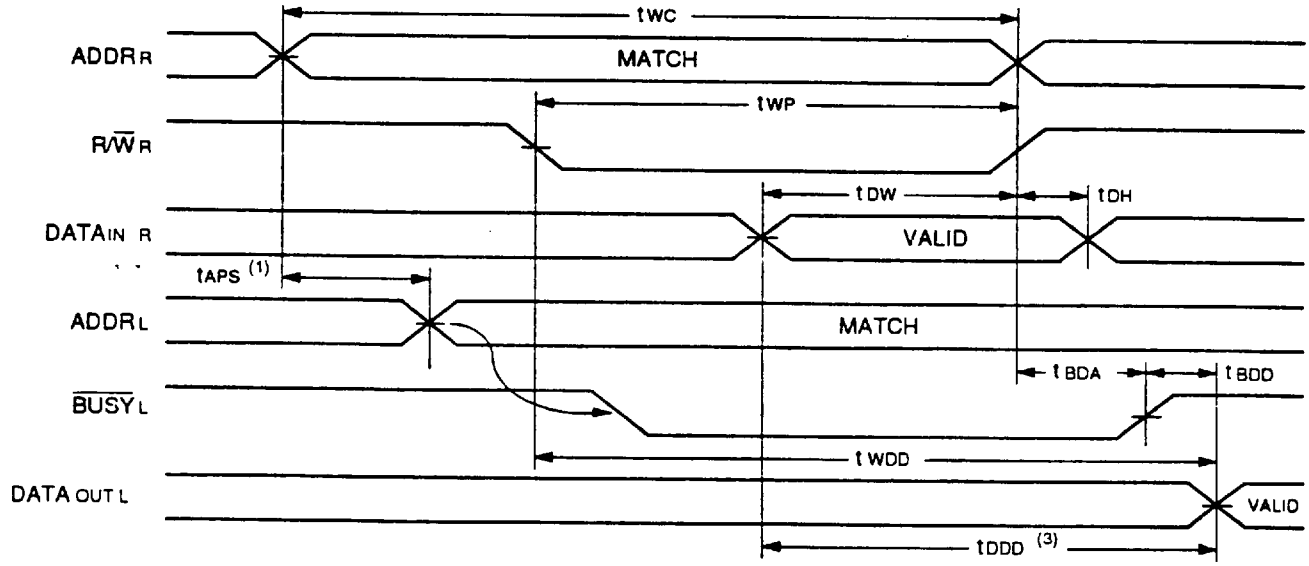
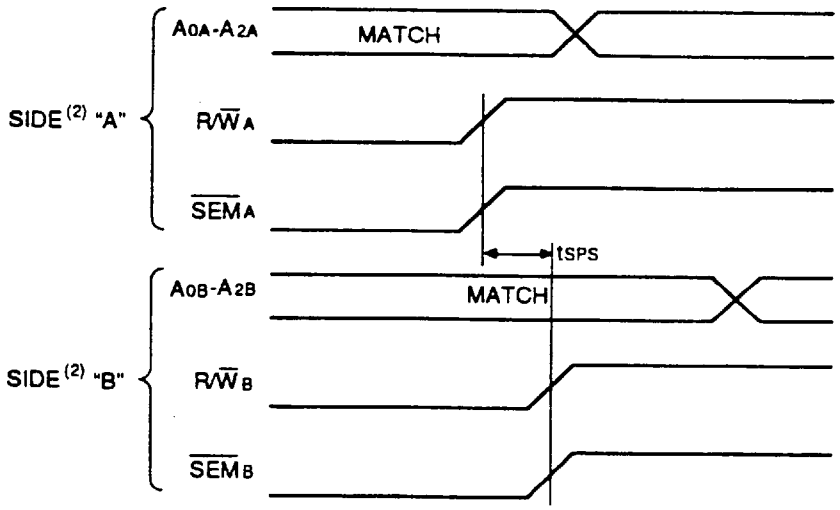
TIMING WAVEFORM OF READ WITH $\overline{BUSY}$(2) (M/$\overline{S}$ = H)



NOTES:
1. To ensure that the earlier of the two ports wins.
2. $\overline{CE}_L$ = $\overline{CE}_R$ = L
3. $\overline{OE}$ = L for the reading port.

TIMING WAVEFORM OF SEMAPHORE WRITE CONTENTION(1,3,4)



NOTES:
1. D_{OR} = D_{OL} = L, $\overline{CE}_R$ = $\overline{CE}_L$ = H, Semaphore Flag is released from both sides (reads as ones from both sides) at cycle start.
2. "A" may be either left or right port. "B" is the opposite port from "A".
3. This parameter is measured from R/$\overline{W}_A$ or $\overline{SEM}_A$ going high to R/$\overline{W}_B$ or $\overline{SEM}_B$ going high.
4. If t_{SPS} is violated, the semaphore will fall positively to one side or the other, but there is not guarantee which side will obtain the flag.

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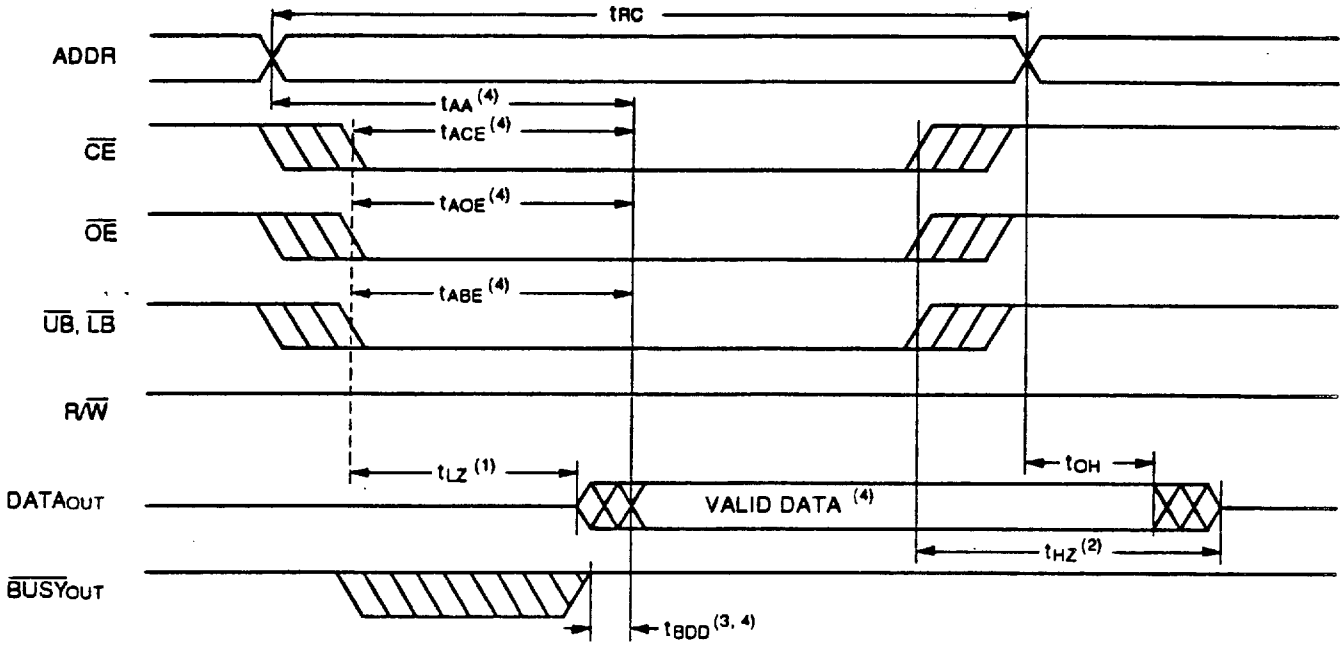
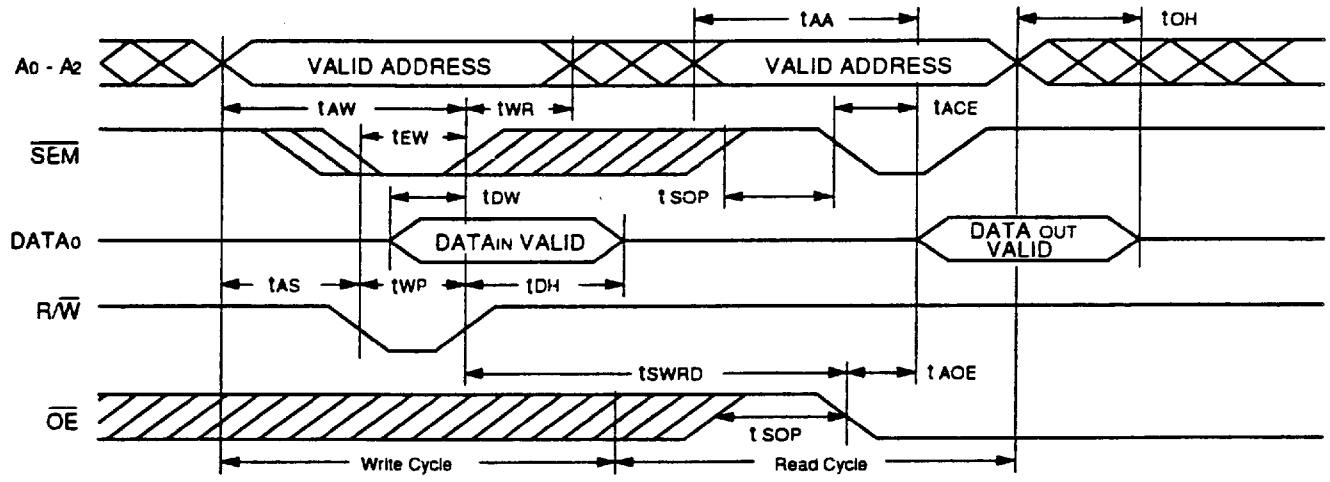
WAVEFORM OF READ CYCLES[5]



NOTES:
1. Timing depends on which signal is asserted last, $\overline{OE}$, $\overline{CE}$, $\overline{LB}$, or $\overline{UB}$.
2. Timing depends on which signal is de-asserted first $\overline{CE}$, $\overline{OE}$, $\overline{LB}$, or $\overline{UB}$.
3. tBDD delay i s required only in case where opposite port is completing a write operation to the same address location for simultaneous read operations $\overline{BUSY}$ has no relation to valid output data.
4. Start of valid data depends on which timing becomes effective last tABE, tAOE, tACE, tAA or tBDD.
5. $\overline{SEM}$ = H.

TIMING WAVEFORM OF SEMAPHORE READ AFTER WRITE TIMING, EITHER SIDE[1]



NOTE:
1. $\overline{CE}$ = H for the duration of the above timing (both write and read cycle).

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7025RP PINOUT DESCRIPTION

PIN	SIGNAL	DESCRIPTION	PIN	SIGNAL	DESCRIPTION
1	Vcc	Power	43	GND	Ground
2	OEl\	Output Enable (Left Port)	44	SEMR\	Semaphore Enable (Right Port)
3	I/O0l	Data Input/Output (Left Port)	45	CER\	Chip Enable (Right Port)
4	I/O1l	Data Input/Output (Left Port)	46	UBR\	Upper Byte Select (Right Port)
5	GND	Ground	47	LBR\	Lower Byte Select (Right Port)
6	I/O2l	Data Input/Output (Left Port)	48	A12r	Address (Right Port)
7	I/O3l	Data Input/Output (Left Port)	49	A11r	Address (Right Port)
8	I/O4l	Data Input/Output (Left Port)	50	A10r	Address (Right Port)
9	I/O5l	Data Input/Output (Left Port)	51	A9r	Address (Right Port)
10	I/O6l	Data Input/Output (Left Port)	52	A8r	Address (Right Port)
11	I/O7l	Data Input/Output (Left Port)	53	A7r	Address (Right Port)
12	I/O8l	Data Input/Output (Left Port)	54	A6r	Address (Right Port)
13	I/O9l	Data Input/Output (Left Port)	55	A5r	Address (Right Port)
14	I/O10l	Data Input/Output (Left Port)	56	A4r	Address (Right Port)
15	I/O11l	Data Input/Output (Left Port)	57	A3r	Address (Right Port)
16	I/O12l	Data Input/Output (Left Port)	58	A2r	Address (Right Port)
17	I/O13l	Data Input/Output (Left Port)	59	A1r	Address (Right Port)
18	GND	Ground	60	A0r	Address (Right Port)
19	I/O14l	Data Input/Output (Left Port)	61	INTR\	Interrupt Flag (Right Port)
20	I/O15l	Data Input/Output (Left Port)	62	BUSYR\	Busy Flag (Right Port)
21	Vcc	Power	63	M/S\	Master or Slave Select
22	GND	Ground	64	GND	Ground
23	I/O0r	Data Input/Output (Right Port)	65	BUSYL\	Busy Flag (Left Port)
24	I/O1r	Data Input/Output (Right Port)	66	INTL\	Interrupt Flag (Left Port)
25	I/O2r	Data Input/Output (Right Port)	67	A0l	Address (Left Port)
26	Vcc	Power	68	A1l	Address (Left Port)
27	I/O3r	Data Input/Output (Right Port)	69	A2l	Address (Left Port)
28	I/O4r	Data Input/Output (Right Port)	70	A3l	Address (Left Port)
29	I/O5r	Data Input/Output (Right Port)	71	A4l	Address (Left Port)
30	I/O6r	Data Input/Output (Right Port)	72	A5l	Address (Left Port)
31	I/O7r	Data Input/Output (Right Port)	73	A6l	Address (Left Port)
32	I/O8r	Data Input/Output (Right Port)	74	A7l	Address (Left Port)
33	I/O9r	Data Input/Output (Right Port)	75	A8l	Address (Left Port)
34	I/O10r	Data Input/Output (Right Port)	76	A9l	Address (Left Port)
35	I/O11r	Data Input/Output (Right Port)	77	A10l	Address (Left Port)
36	I/O12r	Data Input/Output (Right Port)	78	A11l	Address (Left Port)
37	I/O13r	Data Input/Output (Right Port)	79	A12l	Address (Left Port)
38	I/O14r	Data Input/Output (Right Port)	80	LBL\	Lower Byte Select (Left Port)
39	GND	Ground	81	UBL\	Upper Byte Select (Left Port)
40	I/O15r	Data Input/Output (Right Port)	82	CEL\	Chip Enable (Left Port)
41	OER\	Output Enable (Right Port)	83	SEML\	Semaphore Enable (Left Port)
42	R/WR\	Read/Write Enable (Right Port)	84	R/WL\	Read/Write Enable (Left Port)

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