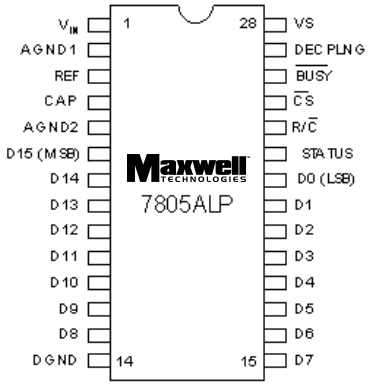
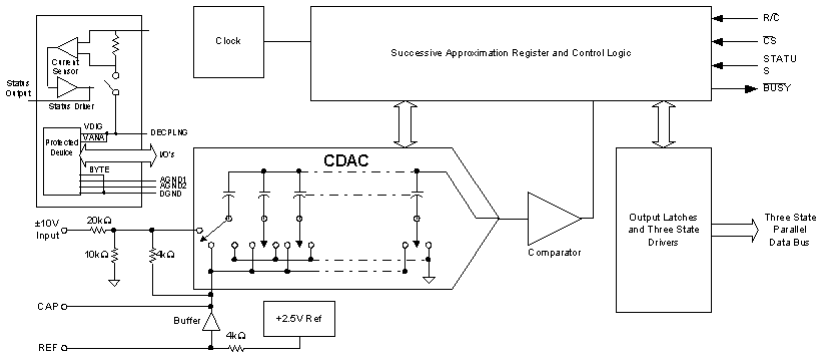
7805ALP
16-Bit Latchup Protected ADC





Logic Diagram

FEATURES:

- 16-bit organization
- Latchup Protection Technology™
- RAD-PAK® radiation-hardened against natural space radiation
- Total dose hardness:
  - > 50 krads(Si), depending upon space mission
- Latchup converted to reset.
  - Rate based on cross section and mission.
- Package:
  - 28 pin RAD-PAK® flat pack
  - 28 pin RAD-PAK® DIP
- 100 kHz min sampling rate
- Standard ± 10V input range
- Advance CMOS technology
  - 86 dB min SINAD with 20 kHz input
  - Single 5V supply operation
  - Utilizes internal or external reference
  - Full parallel data output
  - Power dissipation: 132 mW max

DESCRIPTION:

Maxwell Technologies' 7805ALP high-speed analog-to-digital converter features a greater than 50 krad (Si) total dose tolerance, depending upon space mission. Using Mawell's radiation-hardened RAD-PAK® packaging technology, the 7805ALP incorporates the commercial ADS7805 from Burr Brown. This device is latchup protected by Maxwell Technologies' LPT™ technology. The 7805ALP, 16-bit sampling CMOS A/D . The device contains a complete 16-bit capacitor-based SAR A/D with S/H, reference, clock, interface for microprocessor use, and three-state output drivers. The 7805ALP is specified at a 100 kHz sampling rate, and guaranteed over the full temperature range. Laser-trimmed scaling resistors provide an industry-standard ± 10V input range, while the innovative design allows operation from a single 5V supply, with power dissipation of under 132 mW.

Maxwell Technologies' patented RAD-PAK® packaging technology incorporates radiation shielding in the microcircuit package. It eliminates the need for box shielding while providing the required radiation shielding for a lifetime in orbit or space mission. In a GEO orbit, RAD-PAK® provides greater than 50 krad (Si) radiation dose tolerance. This product is available with screening up to Maxwell Technologies self-defiened Class K.

(858) 503-3300 Fax: (858) 503-3301- www.maxwell.com

TABLE 1. 7805ALP PINOUT DESCRIPTION

PIN NUMBER	NAME	DIGITAL I/O	DESCRIPTION
1	V_{IN}		Analog input.
2	AGND1		Analog ground. Used internally as ground reference point.
3	REF		Reference input/output. 2.2 µF tantalum capacitor to ground
4	CAP		Reference buffer capacitor. 2.2 µF tantalum capacitor to ground.
5	AGND2		Analog ground.
6	D15 (MSB)	0	Data bit 15. Most Significant Bit (MSB) of conversion results. When STATUS is HIGH*, D15 must not be driven high.
7	D14	0	Data bit 14. When STATUS is HIGH*, D14 must not be driven high.
8	D13	0	Data bit 13. When STATUS is HIGH*, D13 must not be driven high.
9	D12	0	Data bit 12. When STATUS is HIGH*, D12 must not be driven high.
10	D11	0	Data bit 11. When STATUS is HIGH*, D11 must not be driven high.
11	D10	0	Data bit 10. When STATUS is HIGH*, D10 must not be driven high.
12	D9	0	Data bit 9. When STATUS is HIGH*, D9 must not be driven high.
13	D8	0	Data bit 8. When STATUS is HIGH*, D8 must not be driven high.
14	DGND		Digital Ground
15	D7	0	Data bit 7. When STATUS is HIGH*, D7 must not be driven high.
16	D6	0	Data bit 6. When STATUS is HIGH*, D6 must not be driven high.
17	D5	0	Data bit 5. When STATUS is HIGH*, D5 must not be driven high.
18	D4	0	Data bit 4. When STATUS is HIGH*, D4 must not be driven high.
19	D3	0	Data bit 3. When STATUS is HIGH*, D3 must not be driven high.
20	D2	0	Data bit 2. When STATUS is HIGH*, D2 must not be driven high.
21	D1	0	Data bit 1. When STATUS is HIGH*, D1 must not be driven high.
22	D0 (LSB)	0	Data bit 0. Least Significant Bit (LSB) of conversion results. When STATUS is HIGH*, D0 must not be driven high.
23	STATUS*	0	STATUS when HIGH indicates latchup protection is active and output data is invalid. Capacitive loading should not exceed 1000 pF.
24	R/$\overline{C}$	I	With $\overline{CS}$ LOW and $\overline{BUSY}$ HIGH, a falling edge of R/$\overline{C}$ initiates a new conversion. When STATUS is HIGH*, $\overline{CS}$ and R/$\overline{C}$ must not be driven high.
25	$\overline{CS}$	I	Internally OR'd with R/$\overline{C}$. If R/$\overline{C}$ LOW, a falling edge on $\overline{CS}$ initiates a new conversion. When STATUS is HIGH*, $\overline{CS}$ and R/$\overline{C}$ must not be driven high.
26	$\overline{BUSY}$	0	At the start of a conversion, $\overline{BUSY}$ goes LOW and stays LOW until the conversion is completed and the digital outputs have been updated.
27	DECPLNG		Supply voltage high speed decoupling pin. Decouple to ground with 1.0 µF ceramic capacitor.
28	V_S		Supply input. Nominally 5V. Decouple to ground with 10 µF tantalum capacitor.

TABLE 2. 7805ALP ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Analog Inputs	V_{IN} CAP REF	-25 V_S 9	-- -- --	25 AGND2 - 0.3 --	V
Ground Voltage Difference	DGND AGND1 AGND2	-0.3 -0.3 -0.3	-- -- --	0.3 0.3 0.3	V
Supply Input	V_S	--	7		V
Digital Inputs		-0.3	--	VS + 0.3	V
Thermal Impedance	Θ_{JC}			11	˚C/W
Internal Power Dissipation		--	--	825	mW
Maximum Junction Temperature	T_J	--	--	165	˚C

TABLE 3. 7805ALP DC ACCURACY SPECIFICATIONS

(V_S = 5V, T_A = -40 TO +85˚C UNLESS OTHERWISE SPECIFIED)

PARAMETER	CONDITIONS	SUBGROUPS	MIN	TYP	MAX	UNIT
Integral Linearity Error			--	--	±3	LSB
Differential Linearity Error			--	--	4, -1	LSB
No Missing Codes [1]			15	--	--	Bits
Transition Noise [2]			--	1.3	--	LSB
Full Scale Error [3,4]			--	--	±0.5	%
Full Scale Error Drift			--	±7	--	ppm/˚C
Bipolar Zero Error [3]			--	--	±10	mV
Bipolar Zero Error Drift			--	±2	--	ppm/˚C
Power Supply Sensitivity	4.8V < V_S < 5.25V		--	--	±8	LSB

1. Guaranteed by design
2. Typical rms noise at worst case transitions and temperatures.
3. Measured with various fixed resistors.
4. Full scale error is worst case - Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and included the effect of offset error.

TABLE 4. 7805ALP DIGITAL INPUTS

(V_S = 5V, T_A = -40 TO +85˚C UNLESS OTHERWISE SPECIFIED)

PARAMETER	SUBGROUPS	MIN	TYP	MAX	UNIT
V_{IL}	1, 2, 3	-0.3	--	0.8	V
V_{IH}		2.0	--	V_S +0.3	V

TABLE 4. 7805ALP DIGITAL INPUTS

(V_S = 5V, T_A = -40 TO +85˚C UNLESS OTHERWISE SPECIFIED)

PARAMETER	SUBGROUPS	MIN	TYP	MAX	UNIT
I_{IL}, I_{IH}	1, 2, 3	--	--	±10	µA

TABLE 5. 7805ALP ANALOG INPUTS

(V_S = 5V, T_A = -40 TO +85˚C UNLESS OTHERWISE SPECIFIED)

PARAMETER	SUBGROUPS	MIN	TYP	MAX	UNIT
Voltage Ranges [1]	1, 2, 3	-10	±10	10	V
Impedance	1, 2, 3	--	23	--	kΩ
Capacitance[2]	--	--	35	--	pF

1. Tested by application of signal.
2. Guarenteed by design

TABLE 6. 7805ALP THROUGHPUT SPEED

(V_S = 5V, T_A = -40 TO +85˚C UNLESS OTHERWISE SPECIFIED)

PARAMETER	SUBGROUPS	MIN	TYP	MAX	UNIT
Conversion Time	9, 10, 11	--	7.6	8	µs
Complete Cycle (Acquire and Convert)	9, 10, 11	--	--	10	µs
Throughput Rate [1]		100	--	--	kHz

1. Guaranteed by design

TABLE 7. 7805ALP AC ACCURACY SPECIFICATIONS

(V_S = 5V, T_A = -40 TO +85˚C UNLESS OTHERWISE SPECIFIED)

PARAMETER	TEST CONDITIONS	SUBGROUPS	MIN	TYP	MAX	UNIT
Spurious-Free Dynamic Range [1,2]	f_{IN} = 45 kHz	4, 5, 6	90	--	--	dB
Total Harmonic Distortion [1,2]	f_{IN} = 45 kHz	4, 5, 6	--	--	-90	dB
Signal-to-(Noise + Distortion) [1,2]	f_{IN} = 45 kHz	4, 5, 6	83	--	--	dB
	-60dB Input	4, 5, 6	--	30	--	
Signal-to-Noise [1,2]	f_{IN} = 45 kHz	4, 5, 6	83	--	--	dB
Full-Power Bandwidth [3]		4, 5, 6	--	250	--	kHz

1. All specifications in dB are referred to a full-scale 10V input.
2. Guaranteed by design.
3. Full-power bandwidth defined as full-scale input frequency at which signal-to-(noise + distortion) degrades to 60 dB or 10 bits of accuracy.

TABLE 8. 7805ALP SAMPLING DYNAMICS

(V_S = 5V, T_A = -40 TO +85˚C UNLESS OTHERWISE SPECIFIED)

PARAMETER	TEST CONDITIONS	SUBGROUPS	MIN	TYP	MAX	UNIT
Aperture Delay		9, 10, 11	--	40	--	nS
Transient Response	FS Step	9, 10, 11	--	2	--	µS
Overvoltage Recovery [1]		9, 10, 11	--	150	--	nS

1. Recovers to specified performance after 2 x f_S input overvoltage.

TABLE 9. 7805ALP REFERENCE

TABLE 10. (V_S = 5V, T_A = -40 TO +85˚C UNLESS OTHERWISE SPECIFIED)

PARAMETER	SUBGROUPS	MIN	TYP	MAX	UNIT
Internal Reference Voltage	1, 2, 3	2.48	2.5	2.52	V
Internal Reference Source Current (Must use external buffer)	1, 2, 3	--	1	--	µA
Internal Reference Drift	1, 2, 3	--	8	--	ppm/˚C
External Reference Voltage Range for Specified Linearity [1]	1, 2, 3	--	2.5	--	V
External Reference Current Drain [2]	--	--	--	100	µA

1. Tested by application of signal.
2. Guaranteed by design

TABLE 11. 7805ALP DIGITAL OUTPUTS

(V_S = 5V, T_A = -40 TO +85˚C UNLESS OTHERWISE SPECIFIED)

PARAMETER	TEST CONDITIONS	SUBGROUPS	MIN	TYP	MAX	UNIT
Data Formatting			(Parallel 16-bits Binary Two's Complement)			
Data Coding			Binary Two's Complement			
V_{OL}	(I_{SINK} = 1.6mA) 4.0	1, 2, 3	--	--	0.4	V
V_{OH}	(I_{SOURCE} = -400 µA)	1, 2, 3	4.0	--	--	V
Leakage Current	High-Z State, V_{OUT} = 0V to V_S	1, 2, 3	--	--	±5	µA
Output Capacitance[1]	High-Z State	--	--	10	--	pF

1. Guarenteed by design

TABLE 12. 7805ALP POWER SUPPLIES

(V_S = 5V, T_A = -40 TO +85˚C UNLESS OTHERWISE SPECIFIED)

PARAMETER	TEST CONDITIONS	SUBGROUPS	MIN	TYP	MAX	UNIT
V_S		--	4.8	5	5.25	V
I_S		1, 2, 3	--	20.3	--	mA
Power Dissipation	f_S = 100 kHz	1, 2, 3	--	102	132.0	mW

TABLE 13. 7805ALP DIGITAL TIMING

(V_S = 5V, T_A = -40 TO +85˚C UNLESS OTHERWISE SPECIFIED)

PARAMETER	SUBGROUPS	MIN	TYP	MAX	UNIT
Bus Access Time	9, 10, 11	--	--	83	nS
Bus Relinquish Time	9, 10, 11	--	--	83	nS

TABLE 14. 7805ALP TEMPERATURE

PARAMETER	MIN	TYP	MAX	UNIT
Specified Performance	-40	--	85	˚C
Derated Performance [1]	-55	--	125	˚C
Storage	-65	--	150	˚C

1. Tested by application of signal.

TABLE 15. 7805ALP CONVERSION TIMING[1]

(V_S = 5V, T_A = -40 TO +85˚C UNLESS OTHERWISE SPECIFIED)

DESCRIPTION	SYMBOL	SUBGROUPS	MIN	TYP	MAX	UNIT
Convert pulse width	t_1	9, 10, 11	40	--	7000	ns
Data valid delay after R/$\overline{C}$ low	t_2	9, 10, 11	--	--	8	µs
$\overline{BUSY}$ delay from R/$\overline{C}$ low	t_3	9, 10, 11	--	--	85	ns
$\overline{BUSY}$ low	t_4	9, 10, 11	--	--	8	µs
$\overline{BUSY}$ delay after end-of-conversion	t_5	9, 10, 11	--	220	--	ns
Aperture time	t_6	9, 10, 11	--	40	--	ns
Conversion time	t_7	9, 10, 11	--	7.6	8	µs
Acquisition time	t_8	9, 10, 11	--	--	2	µs
Throughput time	$t_7 + t_8$	9, 10, 11	--	9	10	µs
Bus relinquish time	t_9	9, 10, 11	10	35	83	ns

TABLE 15. 7805ALP CONVERSION TIMING[1]

(V_S = 5V, T_A = -40 TO +85°C UNLESS OTHERWISE SPECIFIED)

DESCRIPTION	SYMBOL	SUBGROUPS	MIN	TYP	MAX	UNIT
$\overline{BUSY}$ delay after data valid	t_{10}	9, 10, 11	50	200	--	ns
Previous data valid delay after R/$\overline{C}$ low	t_{11}	9, 10, 11	--	7.4	--	µs
R/$\overline{C}$ to $\overline{CS}$ setup time	t_{12}	9, 10, 11	10	--	--	ns
Time between conversions	t_{13}	9, 10, 11	10	--	--	µs
Bus access time	t_{14}	9, 10, 11	10	--	83	ns

1. Tested by application of signal.

TABLE 16. 7805ALP CONTROL LINE FUNCTION FOR READ AND CONVERT

$\overline{CS}$	R/$\overline{C}$	$\overline{BUSY}$	OPERATION
1	X	X	None. Databus is in Hi-Z state.
↓	0	1	Initiates conversion "n". Databus remains in Hi-Z state.
0	↓	1	Initiates conversion "n". Databus enters Hi-Z state.
0	1	↑	Conversion "n" completed. Valid data from conversion "n" on the databus.
↓	1	1	Enables databus with valid data from conversion "n".
↓	1	0	Enables databus with valid data from conversion "n-1". Conversion "n" in progress.
0	↑	0	Enables databus with valid data from conversion "n-1". Conversion "n" in progress."
0	0	↑	New conversion initiated without acquisition of a new signal. Data will be invalid. $\overline{CS}$ and/or R/$\overline{C}$ must be HIGH when $\overline{BUSY}$ goes HIGH.
X	X	0	New convert commands ignored. Conversion "n" in progress.

FIGURE 1. CONVERSION TIMING WITH OUTPUTS ENABLED AFTER CONVERSION ($\overline{CS}$ TIED LOW)

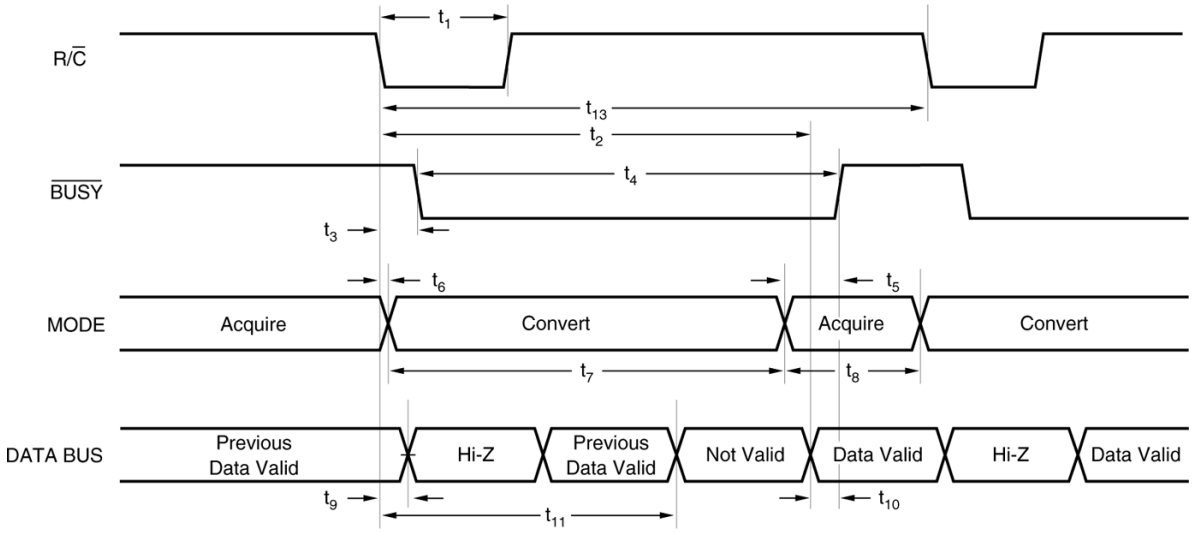
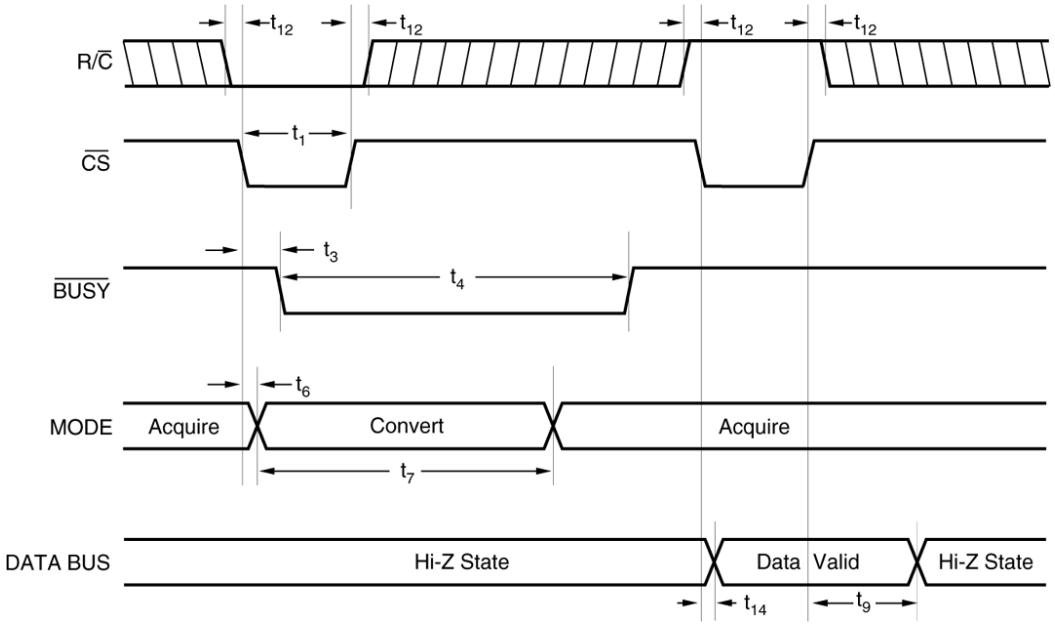


FIGURE 2. USING CS TO CONTROL CONVERSION AND READ TIMING



LPT™ Operation

Latchup Protection Technology (LPT™) automatically detects an increase in the supply current of the 7805ALP converter due to a single event effect and internally cycles the power to the converter off, then on, which restores the

steady state operation of the device. A simplified block diagram of the 7805ALP circuitry is shown in Figure 1. The circuitry consists of a protected device, the ADS7805 die, a current sensor, a power switch, and a status output driver.

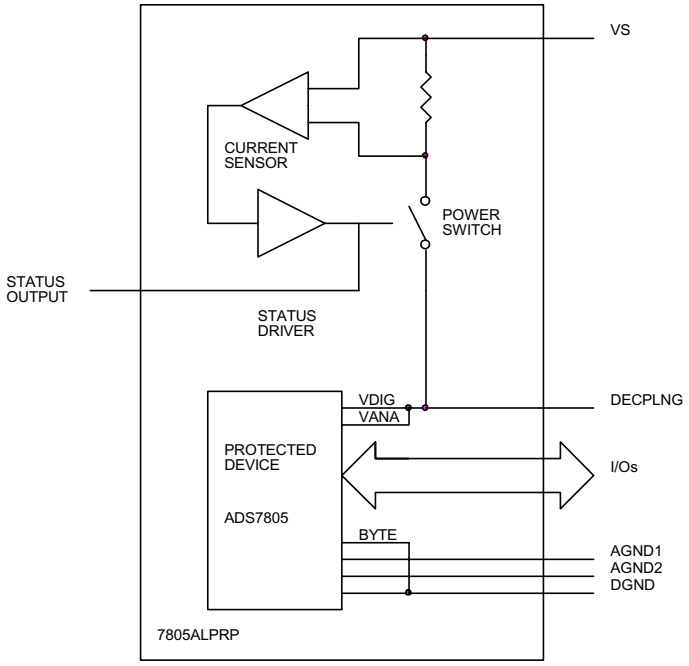


FIGURE 3. LATCHUP PROTECTION DIAGRAM

Differences Between the7805A and the ADS7805

Because the 7805A uses the ADS7805 die to perform the analog to digital conversion function its operation and performance is very similar to the ADS7805 packaged part from Burr-Brown. In general the operation and application will be the same for both parts. There are two primary differences: the operation of the supply pins and the operation of the BYTE and STATUS pins.

The ADS7805 provides separate analog and digital supply pins. The 7805A provides a single supply input V_S pin in place of the V_{DIG} pin which powers both the analog and digital circuitry through the LPT™ current sensor and power switch. The V_S power supply should be treated as an analog supply and isolated from noise on the system digital power supply. The low side of the power switch connects to the ADS7805 die power pads and to the package DECPLNG pin which replaces the VANA pin. The DECPLNG pin allows low ESR ceramic capacitors to directly decouple the ADS7805 die. CAUTION: The DECPLNG pin must not be connected to the power supply since this will defeat the LPT™ power switch and could result in latchup of the device during operation in a radiation environment. Electrolytic capacitors should not be connected to the DECPLNG pin because the large capacitance will increase the recovery time of the 7805A.

The primary functional difference between the ADS7805 and the 7805A is that the BYTE signal of the ADS7805 is internally grounded and the pin function is replaced by the STATUS output. Grounding the BYTE signal permanently assigns the data output signal bits 15:0 as shown in the 7805A pinout diagram where bit15 is the MSB and bit 0 is the LSB.

A high level STATUS signal indicates that a single event induced latchup current was detected by the LPT™ circuitry causing power to be removed from the protected device. **CAUTION:** During the time that power is removed from the protected device, it is critical that external circuitry driving the device I/O pins does not backdrive the device supply. Backdriving the supply could contribute to an extended or even a permanent latchup condition.

In order to prevent backdriving the supply, the STATUS signal should be used in the system to tri-state or gate external I/O drive circuits to a low state. Similarly, if the data outputs are connected to a bus with other bus driver circuits, all external data bus drivers must be tri-stated and individual pull up resistors to the supply voltage (if used on the data bus) must not be less than 10 KΩ typical to assure proper single event effect recovery. Tri-stating of inputs should occur within 100 nsec after the rise of the status pin. The BYTE signal can be made available in place of the STATUS signal at customer request.

STATUS can also be used to generate an input to the system data processor indicating that an LPT™ cycle has occurred, and the protected device output accuracy may not be met until after the respective recovery time to the event. The STATUS signal is generated from an advanced CMOS logic gate output. This output may not exhibit a monotonic falltime and may even oscillate briefly while power is being restored to the protected device and the decoupling capacitance is charged. Loading on the STATUS output should be minimized because this signal is used internally by the 7805A. It is recommended that load current not exceed 2 mA and load capacitance be kept well below 1000 pF.

A summary of the pin differences between the ADS7805 and 7805A is provided below.

TABLE 16. PIN DIFFERENCES

PIN NUMBER	ADS7805	7805A	PIN DIFFERENCE DESCRIPTION
23	BYTE	STATUS	A high level STATUS signal indicates that power is removed from the ADS7805 die. I/O pins must not be driven high while this signal is active. The BYTE signal of the ADS7805 die is internally grounded but can also be made available in place of the STATUS pin at customer request.
27	VANA	DECPLNG	The ADS7805 VANA and V_{DIG} die pads are connected together and are available at the DECPLNG pin. This pin allows external ceramic capacitors to directly decouple the power inputs to the ADS7805 die-to-analog ground. Decoupling capacitance should not exceed 0.2 uF typical. This pin must not be connected to a power supply directly since this will defeat the latchup protection circuitry. Electrolytic filter capacitors should not be connected to this pin but should be connected between the V_S pin and ground.
28	V_{DIG}	V_S	This is the power supply input for the LPT circuitry and the protected ADS7805 die. This supply should be treated as an analog supply with filtering and/or isolation from the noisy system digital power supply. The LPT latchup current sense and power switch circuitry is located between this pin and the DECPLNG pin.

Example Circuits for Using the 7805A

Figure 2 shows a typical application circuit for using the 7805A as an input to a digital data processor. This circuit shows the use of the STATUS pin to tri-state the control inputs when the latchup protection circuit cycles the power to the protected ADS7805 die.

Figure 3 shows a typical application circuit for connecting the 7805A to a 16-bit data bus with multiple drivers on the bus. Tri-state buffers are used to isolate the 7805A data outputs from the data bus. Figure 4 shows the typical application circuit for connecting the 7805A to an 8-bit data bus.

FIGURE 4. TYPICAL 7805A APPLICATION CIRCUIT

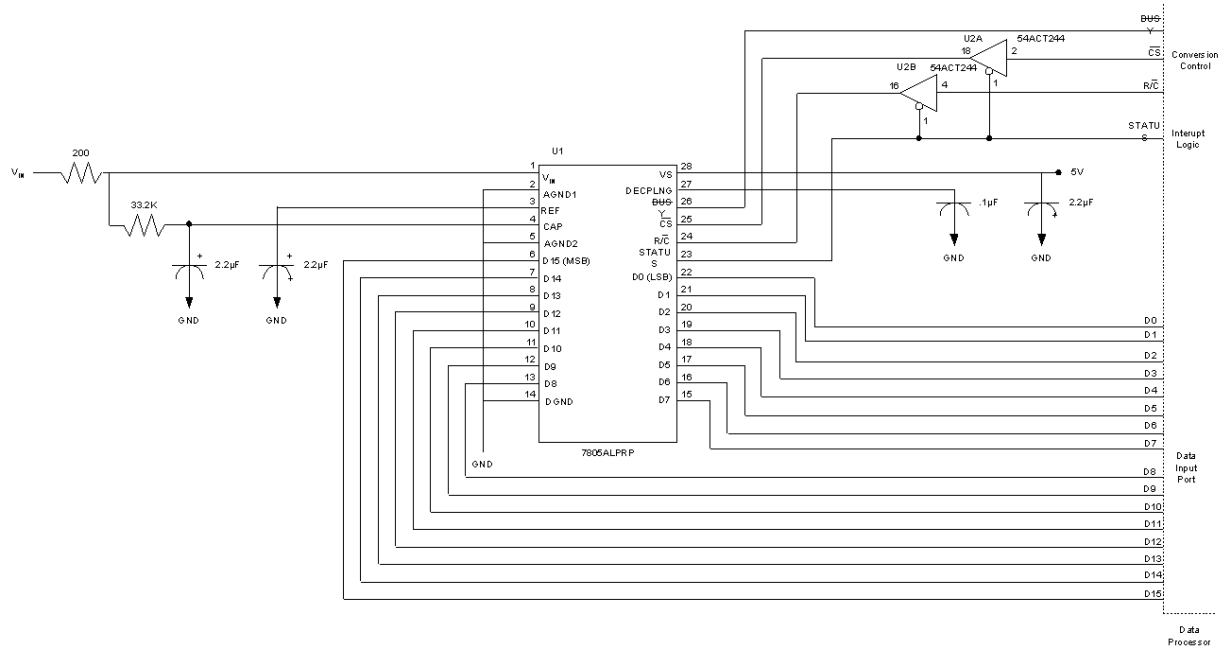


FIGURE 5. TYPICAL 7805A CIRCUIT WITH 16-BIT BUS INTERFACE

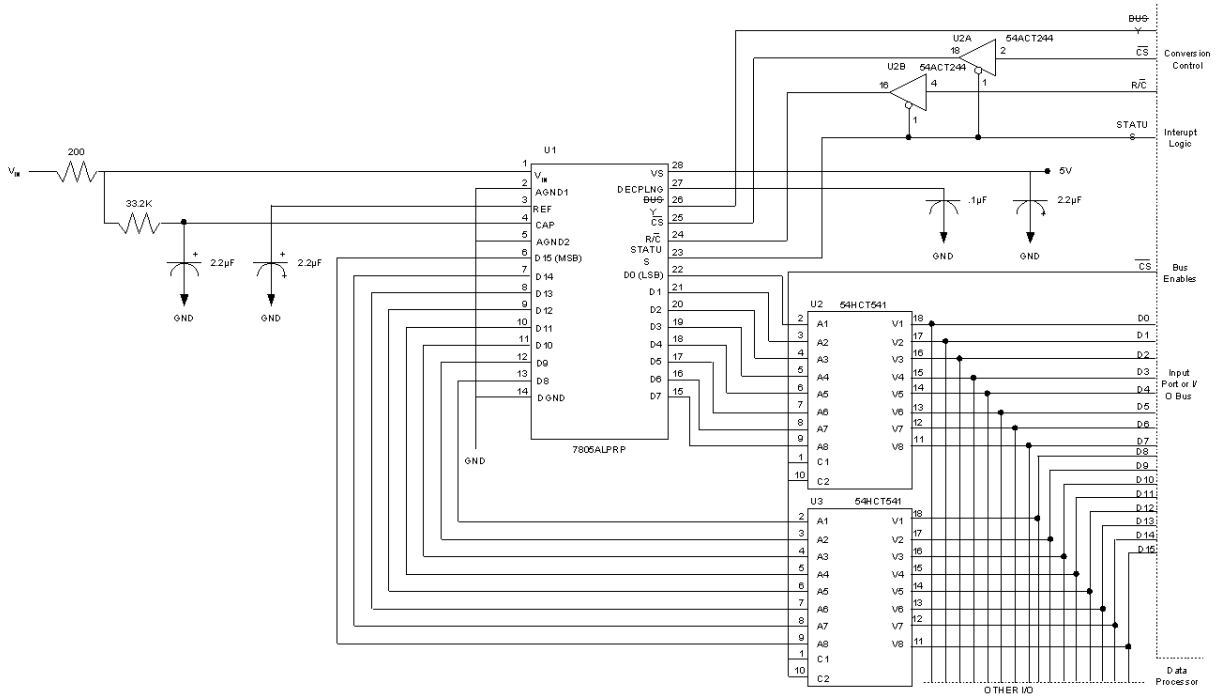
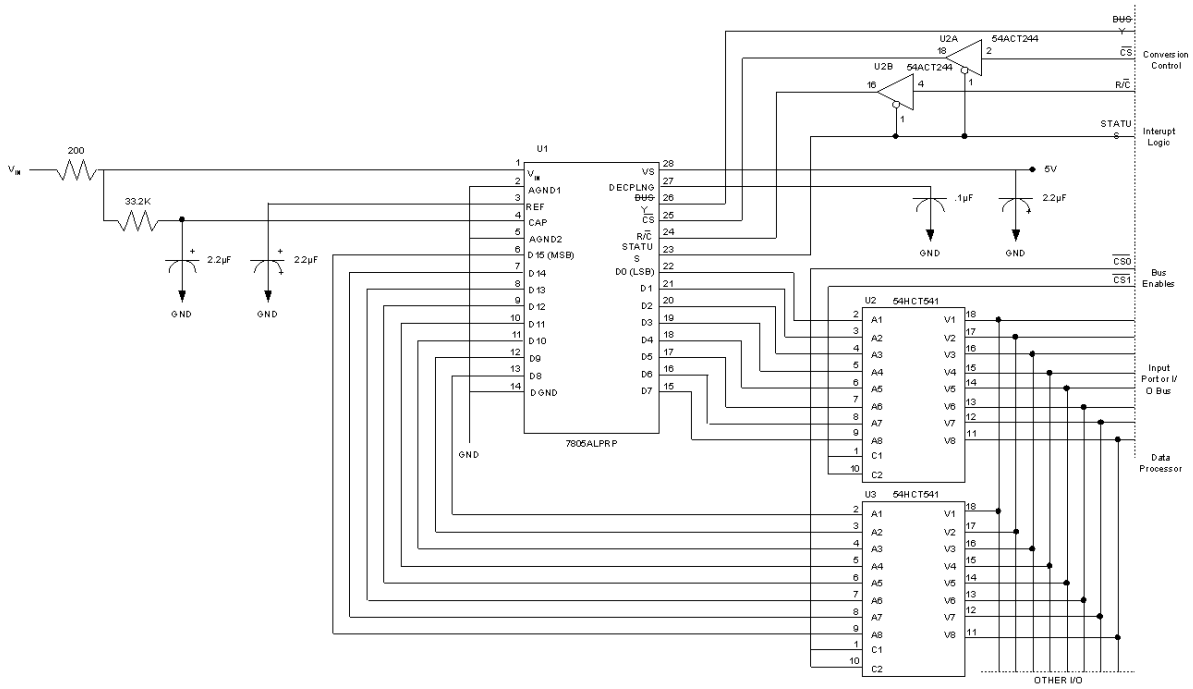


FIGURE 6. TYPICAL 7805A CIRCUIT WITH 8-BIT BUS INTERFACE



Testing the 7805A Latchup Protection Circuitry

The DECPLNG pin provides direct access to the 7805ALP converter supply pins for attaching external decoupling capacitor(s) to ground. This pin can also be used to test the LPT™ operation by sinking a pulsed current load to ground as shown in the test circuit in Figure 5 and as described in the LPT Operating Characteristics Table (Table 17) and LPT Timing diagram (Figure 7). This test approximates the operation of the 7805A in response to a single event latchup and recovery.

During the time that the power is cycled, output signals and data from the 7805A are invalid. The STATUS signal HIGH indicates that power is removed from the ADS7805 die. All input pins must be driven low or tri-stated. When this signal is low, power is applied to the ADS7805 die. The STATUS signal can be used to measure the supply recovery time. The status signal can exhibit multiple transitions when power is re-applied and the decoupling capacitors are charged. The duration and number of transitions is dependent on the amount of capacitance used. The supply recovery time interval starts when the supply current rises (causing STATUS to go high) and ends when the STATUS signal stabilizes low again.

Within the functional recovery time interval (typically 25 µsec after the LPT circuit reapplies power), the normal functional operation of the converter is restored with less than 5% full scale error. Additional settling time is then required to return to full accurate operation. Defined recovery time intervals indicate that time to recover first is within 8-bit accuracy, then within 12 bit accuracy, and finally full 16-bit accuracy. These recovery times are primarily due to the single event and power cycling effects on the reference circuits and the settling times of their respective filter capacitors.

TABLE 17. LPT™ OPERATING CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNITS
Supply threshold current - ITHR	56	77	99	mA
Protection time (IS Peak = .2A) - TPT	--	1	--	µsec
Input tri-state time - TIOFF	--	--	100	nsec

TABLE 17. LPT™ OPERATING CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNITS
Status instability time - TINST	--	--	10	µsec
Supply recovery time (IS Peak = .2A) - TSR	25	50	100	µsec
Functional recovery time (IS Peak = .2A) - TFR	--	TSR + 25	--	µsec
8-Bit accuracy recovery time (IS Peak = .2A) - T8R	--	75	--	msec
12-Bit accuracy recovery time (IS Peak = .2A) - T12R	--	250	--	msec
Full accuracy recovery time (IS Peak - .2A) - TFAR	--	425	--	msec

FIGURE 7. LPT™ TEST CIRCUIT

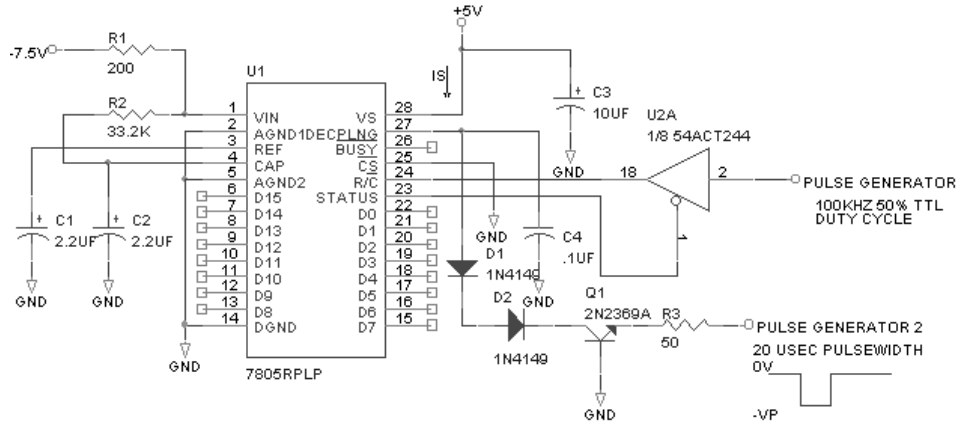


FIGURE 8.

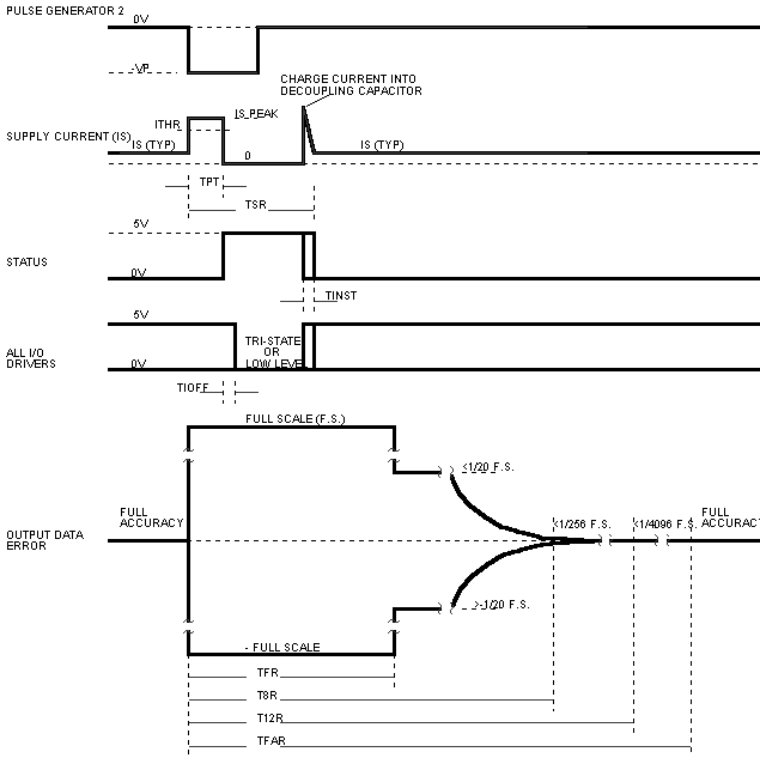
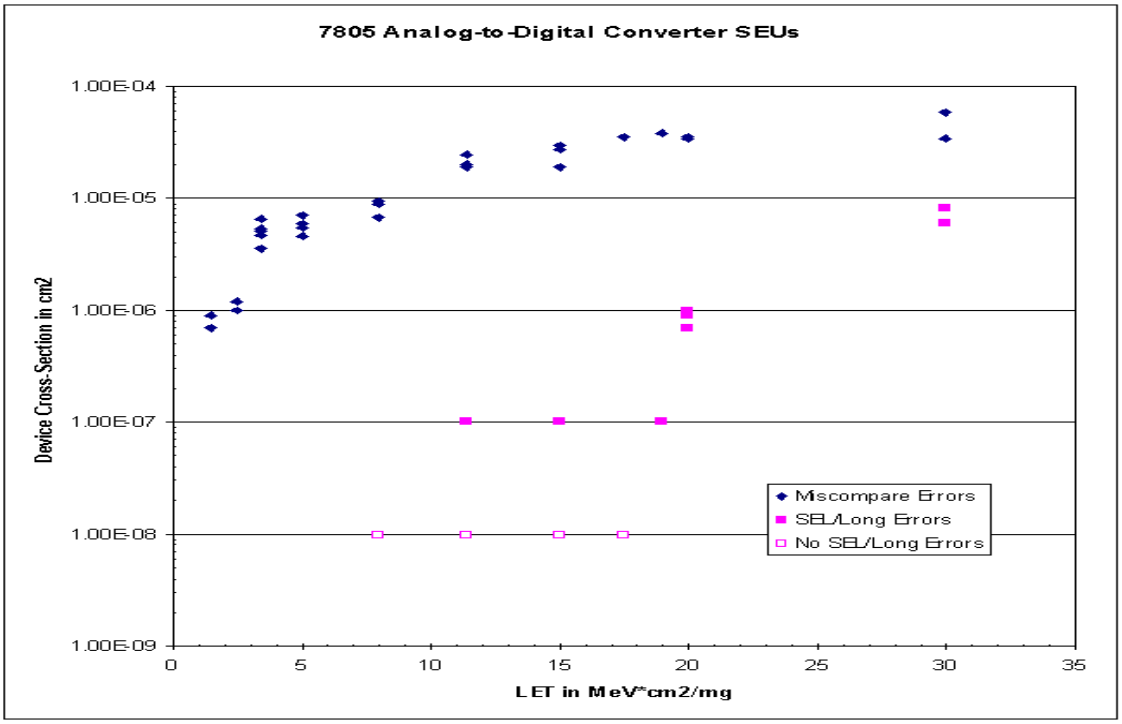
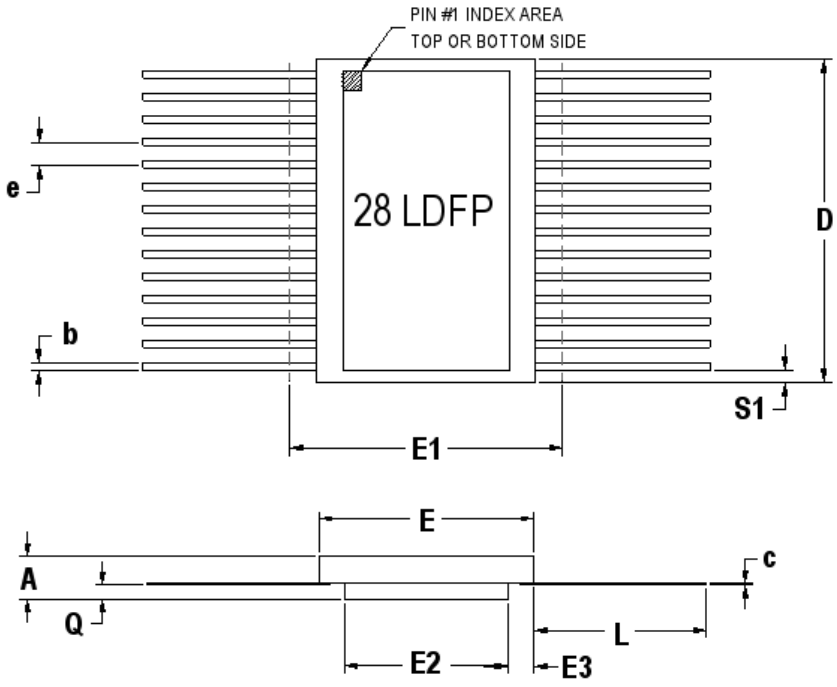


FIGURE 9. SEU AND SEL CROSS SECTION

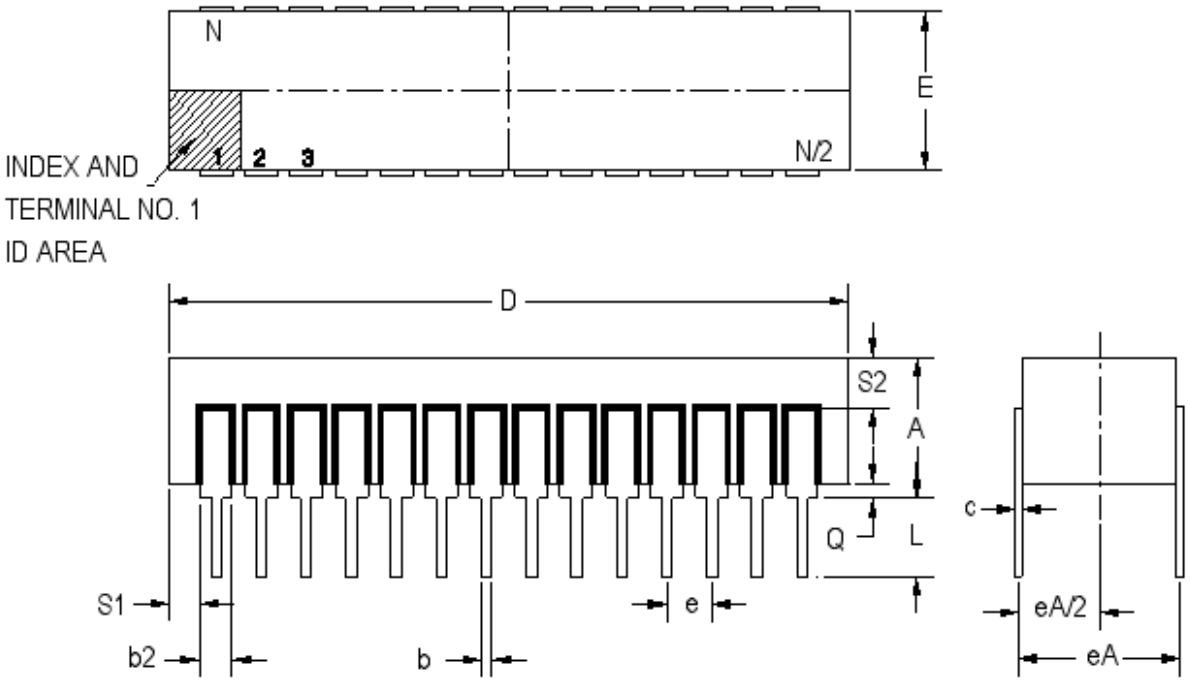




28 PIN RAD-PAK® FLAT PACKAGE

SYMBOL	DIMENSION		
	MIN	NOM	MAX
A	0.177	0.192	0.207
b	0.015	0.017	0.022
c	0.004	0.005	0.009
D	--	0.800	0.808
E	0.400	0.410	0.420
E1	--	--	0.440
E2	0.295	0.300	--
E3	0.000	0.055	--
e	0.050 BSC		
L	0.390	0.400	0.410
Q	0.028	0.032	0.036
S1	0.000	0.067	--
N	28		

Note: All dimensions in inches



28-PIN RAD-PAK® DUAL IN LINE PACKAGE

SYMBOL	DIMENSION		
	MIN	NOM	MAX
A	--	0.185	0.225
b	0.014	0.018	0.026
b2	0.045	0.050	0.065
c	0.008	0.010	0.018
D	--	1.600	1.616
E	0.585	0.595	0.605
eA	0.600 BSC		
eA/2	0.300 BSC		
e	0.100 BSC		
L	0.165	0.175	0.185
Q	0.015	0.030	0.075
S1	0.005	0.125	--
S2	0.005	--	--
N	28		

Note: All dimensions in inches

Important Notice:

These data sheets are created using the chip manufacturer's published specifications. Maxwell Technologies verifies functionality by testing key parameters either by 100% testing, sample testing or characterization.

The specifications presented within these data sheets represent the latest and most accurate information available to date. However, these specifications are subject to change without notice and Maxwell Technologies assumes no responsibility for the use of this information.

Maxwell Technologies' products are not authorized for use as critical components in life support devices or systems without express written approval from Maxwell Technologies.

Any claim against Maxwell Technologies must be made within 90 days from the date of shipment from Maxwell Technologies. Maxwell Technologies' liability shall be limited to replacement of defective parts.