



93CX56/93CX66

2,048/4,096-Bit CMOS Serial EEPROM

with extended-voltage operation (2.5V to 6.5V)

Features

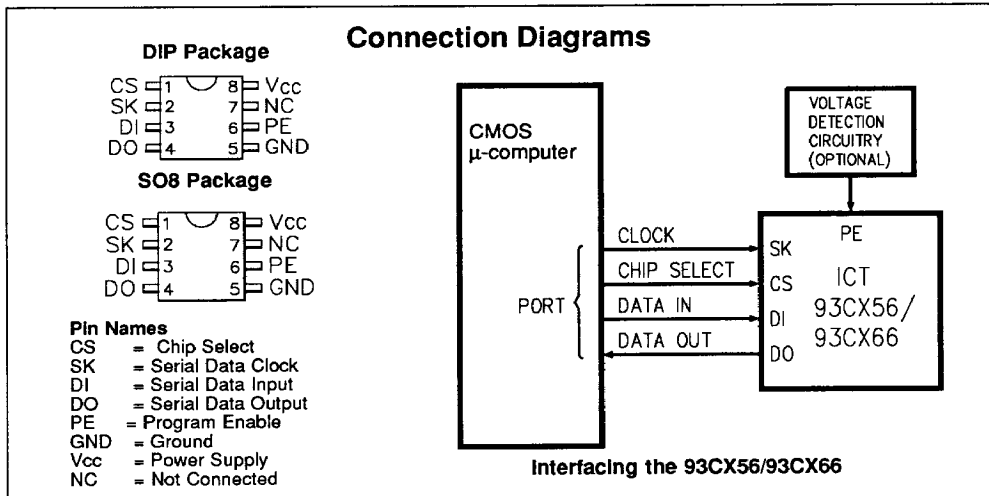
- **Advanced CMOS EEPROM Technology**
- **Read/Write Non-volatile Memory**
 - Single supply operation (2.5V to 6.0V)
 - 2,048 bits: 128 x 16 organization
 - 4,096 bits: 256 x 16 organization
 - Versatile easy-to-use serial data interface
- **Low Power Consumption**
 - 4mA max Active
 - 50µA max Standby, CMOS interface
- **Special Features**
 - Automatic-erase write instruction
 - Ready/Busy status signal
 - Software and hardware controlled write protection
- **Ideal For Low-density Data Storage**
 - Low-cost, space-saving 8-pin package
 - Commercial, industrial, & military versions
 - Interfaces with popular CMOS micro controllers- (ie., COP4XX, uPD75XX, HMCS-400, Series-40, M5-Series, 80CXX families)
- **Application Versatility**
 - Extended-voltage operation is ideal for battery-powered applications
 - Alarms, Electronic Locks, Appliances, Terminals, Smart Cards, Robotics, Meters, Telephones, Tuners, etc.

2

General Description

The ICT 93CX56/CX66 is a 2,048/4,096-bit, non-volatile memory device fabricated using an advanced CMOS EEPROM technology. It is possible to read or write data with Vcc ranging from 2.5V to 6.0V. The 2,048/4,096 bits of memory are organized into 128/256 registers of 16 bits each. Each register is individually addressable for serial read (or write) operations through the DI (or DO) pin. A versatile serial interface consisting of chip select, clock, data-in and data-out, can easily be controlled by popular CMOS microcontrollers (ie., COP4XX, uPD75XX, HMCS-400, Series-40, M5-Series, 80CXX families) or standard microprocessors.

Low power consumption, low cost, and space efficiency make the ICT 93CX56/CX66 an ideal candidate for high-volume, low-density data-storage applications. Special features of the 93CX56/CX66 include: automatic write time-out, ready/busy status signal, software-controlled write-protection, and an ultra-low-power standby mode (when deselected) that is ideal for battery-powered applications. Additionally, the 93CX56/CX66 offers functional compatibility with existing NMOS and CMOS serial EEPROMs. The 93CX56/CX66 is designed for applications requiring up to 10,000 erase/write cycles per register and 40 years of data retention.





Function Description

Device Operation ¹

The ICT 93CX56/CX66 are serial 2,048/4,096-bit non-volatile memory devices organized as 128/256 registers by 16 bits. Each register is independently addressable for read, write, or erase operations. Five, 11-bit instructions control the operation of the device. The 93CX56/CX66 operates on a single supply voltage, which may range from 2.5 Volts to 6.0 Volts, and will generate, on chip, the high voltage required for any programming operation.

The 93CX56/CX66 provides two methods of protecting data from being accidentally disturbed. The Write-Disable (WDS) instruction will disable all programming functions until a Write-Enable (WEN) instruction is executed. A hardware control is also available in the form of the PE (program enable) control pin. To perform any programming instruction, PE must be held high while loading the instruction into the 93CX56/CX66. The PE control can be used to ensure that no data is accidentally disturbed by erratic switching of the microcontroller's outputs during power-up or power-down. Voltage detection circuitry can be implemented to disable PE when the supply voltage drops below a user-specified voltage level. Note that the PE control pin is tied to an internal pull-up so that the pin may be left unconnected if the PE control feature is not to be used.

Instructions, address, and write data are clocked into the DI pin on the rising edge of the clock (SK). The instructions include: read; write; write enable; write disable; and write all. The format of each eleven-bit instruction, starting with the most significant bit, is as follows: start bit (logical "1"); a two-bit op code; and an eight-bit address (one "Don't Care" bit and seven address bits for the 93CX56). The DO pin is normally in a high-impedance state, except when reading data from the device, or when checking the BUSY/READY status after a programming operation. The BUSY/READY status can be determined after a programming operation by selecting the device (CS high) and polling the DO pin. DO low indicates that the programming operation is not completed (BUSY), while DO high indicates that the device is ready for the next operation (READY). DO will return to the high-impedance state when the next instruction is initiated.

Read (READ)

The read (READ) instruction outputs serial data on the DO pin. After a read instruction is received, the instruction and the address are decoded. Then data is transferred from the selected memory register to a 16-bit shift register and DO comes out of the high-impedance state. After sending a dummy bit (logi-

cal "0"), the 16-bit data string is shifted out of the device. The DO transitions occur on the rising edge of the clock and the data is stable after the specified delay t_{P0} or t_{PD1} .

Write Enable/Disable ² (WEN /WDS)

The 93CX56/CX66 powers up in the programming-disable state. Any programming after power-up, or following a write disable (WDS) instruction, must first be preceded by a write enable (WEN) instruction. The PE pin (if used) **MUST** be held high while loading the programming enable instruction. Once enabled, programming remains enabled until a write disable (WDS) instruction is executed or power is removed from the device. The write disable instruction disables all programming functions of the 93CX56/CX66 and can be used to prevent accidentally disturbing data in the device. Data can be read from the 93CX56/CX66 regardless of the programming enable/disable status.

Write (WRITE) ²

The 93CX56/CX66 initiates an autoerase cycle when executing a write (WRITE) instruction, eliminating the need of an erase (ERASE) command. The write instruction (opcode plus address) is followed by 16 bits of data to be written into the specified address. After the last bit of data (Do) has been clocked into the DI pin, the CS (chip select) must be brought low before the next rising edge of the SK clock and held low for the minimum period specified by t_{cs} . The falling edge of CS initiates the self-timed programming cycle. The PE pin (if used) **MUST** be held high while loading the write instruction. However, after loading the write instruction the PE pin becomes a "don't care". It is not necessary to clock the SK pin after initiating the self-timed write mode. The BUSY/READY status of the device can be determined by selecting the device and polling the DO pin.

Write All (WRAL) ²

The write-all (WRAL) instruction simultaneously programs all registers with the data pattern specified in the instruction. After receiving the write-all instruction and 16 bits of data, CS is brought low before the next rising edge of the SK clock and held low for a minimum period specified by t_{cs} . The falling edge of CS initiates the self-timed write cycle. The PE pin (if used) **MUST** be held high while loading the write-all instruction. It is not necessary to clock the SK pin after initiating the self-timed write-all mode. The BUSY/READY status of the device can be determined by selecting the device and polling the DO pin.



Absolute Maximum Ratings

Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permanent damage

Symbol	Parameter	Conditions	Rating	Unit
V _{CC}	Supply Voltage	Relative to GND	- 0.6 to +7.5	V
V _{IO}	Voltage Applied to Any Pin	Relative to GND	- 0.6 to V _{CC} + 0.6	V
T _{ST}	Storage Temperature		- 65 to + 150	°C
T _{LT}	Lead Temperature	Soldering 10 seconds	+ 300	°C

Operating Ranges

Symbol	Parameter	Commercial		Industrial (I)		Military (M)		Unit
		93CX56/93CX66		93CX56/93CX66		93CX56/93CX66		
		Min	Max	Min	Max	Min	Max	
V _{CC}	Supply Voltage	2.5	6.0	2.5	6.0	2.5	6.0	V
T _A	Ambient Temperature ³	0	+ 70	- 40	+ 85	- 55	+ 125	°C

DC and AC Electrical Characteristics

Over the operating range

Symbol	Parameter	Conditions	Commercial		Industrial		Military		Unit
			Min	Max	Min	Max	Min	Max	
I _{CC}	Power Supply Current, Active, TTL/CMOS Interface	V _{CC} = 6.0V, CS=SK=V _{IH} DO = Open, f = 1.0MHz		4		6		8	mA
I _{CCSB1}	Supply Current, Standby, TTL Interface	V _{CC} = 6.0V, CS = V _{IL} DO = Open		100		150		250	µA
I _{CCSB2}	Supply Current, Standby, CMOS Interface	V _{CC} = 6.0V, CS = V _{IL} DO = Open		50		100		200	µA
V _{IH}	Input HIGH Level ⁴		V _{CC} -2	V _{CC} +1	V _{CC} -2	V _{CC} +1	V _{CC} -2	V _{CC} +1	V
V _{IL}	Input LOW Level ⁴		- 0.1	0.8	- 0.1	0.8	- 0.1	0.8	V
V _{OH}	Output HIGH Voltage ⁴	I _{OH} = - 0.4mA	2.2		2.2		2.2		V
V _{OL}	Output LOW Voltage ⁴	I _{OL} = 2.1mA		0.4		0.4		0.4	V
I _{LI}	Input Leakage Current	V _{IN} = 6.0V		±10		±10		±10	µA
I _{LO}	Output Leakage Current	V _O =6.0V, CS=0, V _{CC} ≤ 6.0V		±10		±10		±10	µA
t _{SKP}	SK Period		1		1		2		µs
t _{SKW}	SK Pulse Width	High or Low	400		400		800		ns
t _{CSS}	CS High to SK High Delay		100		100		200		ns
t _{CSH}	SK Low to CS Low Delay		0		0		0		ns
t _{DIS}	Data Setup Time (Write)		200		200		200		ns
t _{DIH}	Data Hold Time (Write)		200		200		200		ns
t _{PD1}	Serial Clock to Output Delay	C _L = 100pF, V _{OL} = 0.8V, V _{OH} = 2.0V, V _{IL} = 0.45V, V _{IH} = 2.4V		250		250		500	ns
t _{PD0}									
t _{EW}	Self-timed Program Cycle			20		20		40	ms
t _{CS}	Min CS Low Time		250		250		250		ns
t _{SV}	CS to Status Valid	CL = 100pF		500		500		1000	ns
t _{OH} , t _{IH}	Falling Edge of CS to DO High Impedence			100		100		200	ns



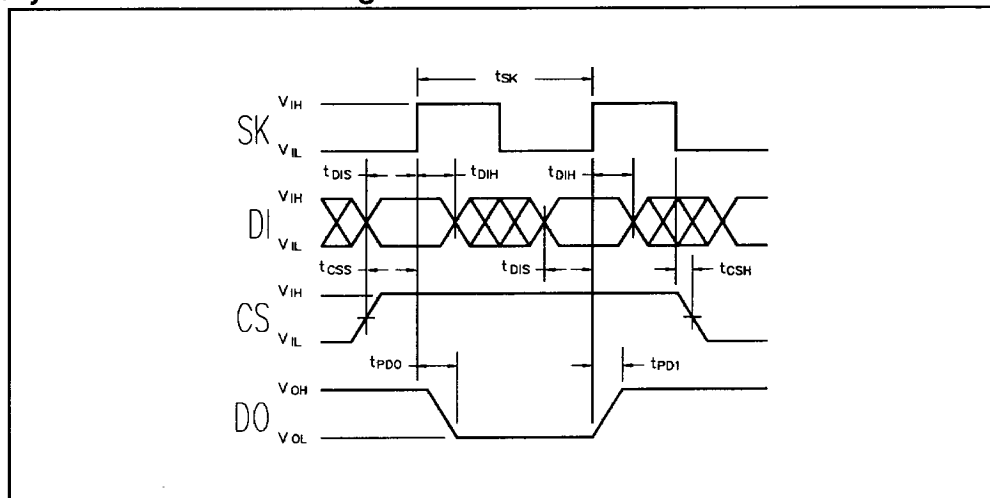
Notes

- Note 1.** If the power is removed or the CS pin is brought low during an instruction cycle, the device's instruction registers will be reset. Note that a power-down will totally reset the device. This means that the write-enable instruction (WEN) will need to be executed prior to any programming.
- Note 2.** If the PE pin is brought to low during the loading of the instruction, this instruction (WEN, WDS, WRITE, and WRAL) may not be executed reliably.
- Note 3.** ICT's E² devices are designed to endure 10,000 Erase/Write cycles and to retain data for at least forty years while operating at 55°C. ICT's standard test flow verifies at least ten years of data retention for Commercial and Industrial temperature devices and at least two years data retention for Military temperature devices. Data retention verification is performed on 100% of the units being shipped. Cycling endurance is verified by lot-sample testing.
- Note 4.** The 93CX56/CX66 is designed to operate with TTL interface only when $4.5V \leq V_{CC} \leq 5.5V$.
- Note 5.** Although the 93CX56/CX66 self-timed program cycle allows software delay loops to be used to achieve the necessary Erase/Write delay, using the Ready/Busy feature is recommended instead. Using the Ready/Busy feature allows faster response time since $t_{E/W}$ will typically be less than the maximum specification.
- Note 6.** A7 is a "Don't Care" bit for addressing the 93CX56.

Instruction set for the 93CX56/93CX66

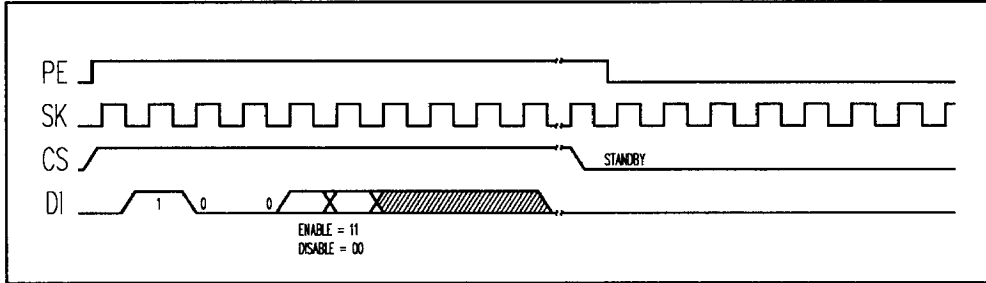
Instruction	Start Bit	Opcode	Address ⁶	Data	Comments
READ	1	10	A7A6A5A4A3A2A1A0		Read address
WRITE	1	01	A7A6A5A4A3A2A1A0	D15 - D0	Write to address
WEN	1	00	1 1 X X X X X X		Write enable
WDS	1	00	0 0 X X X X X X		Write disable
WRAL	1	00	0 1 X X X X X X	D15 - D0	Write all addresses

Synchronous Data Timing Waveforms



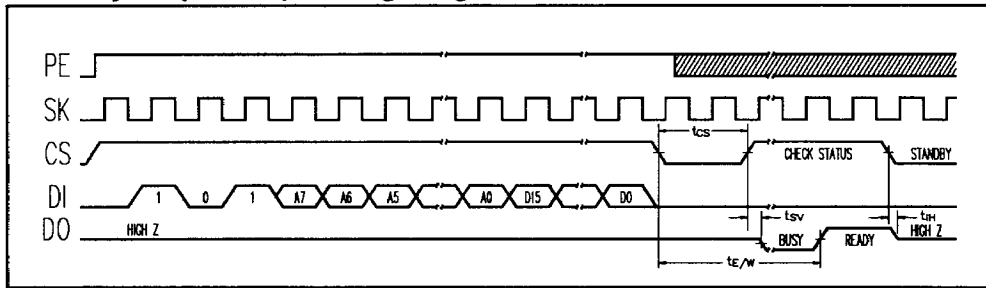


Write Enable (WEN)/Write Disable (WDS) Timing Diagram

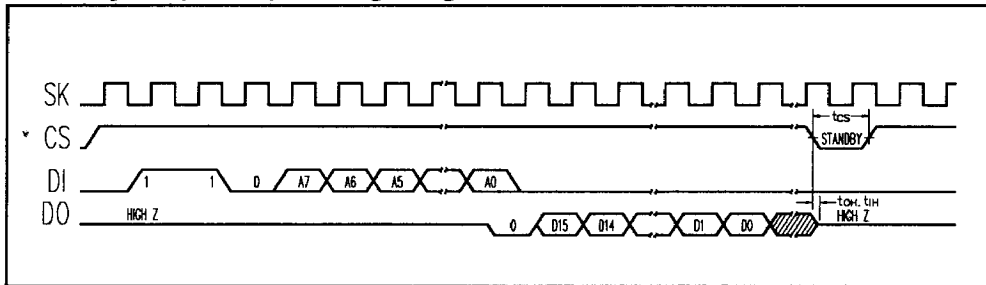


2

Write Cycle (WRITE) Timing Diagram



Read Cycle (READ) Timing Diagram



Write All (WRAL) Timing Diagram

