1 GSPS Direct Digital Synthesizer w/ 14-bit DAC

Preliminary Technical Data

AD9912

FEATURES

1 GSPS internal clock speed (up to 400 MHz out directly)
Integrated 1 GSPS 14-bit DAC
48-bit frequency tuning word
Differential HSTL Comparator
Flexible System Clock Input accepts either crystal or external reference clock.
On-chip Low-Noise PLL REFCLK Multiplier
2 Spur Reduction Channels
Low Jitter clock doubler for frequencies up to 750 MHz
Single-ended CMOS Comparator; frequencies < 50MHz
Programmable output divider for CMOS output
Serial I/O control
Excellent Dynamic Performance
Software controlled power-down
64-lead LFCSP package
Phase Noise @ 95MHz using Vectron VCC6 87.5MHz Oscillator:
100 Hz Offset: -103 dBc/Hz
10 kHz Offset: -133 dBc/Hz
1 MHz Offset: -136 dBc/Hz

APPLICATIONS

Agile LO frequency synthesis
Low jitter, fine tune clock generation
Test and measurement equipment
Wireless Base Stations, Controllers
Secure Communications
Fast frequency hopping

GENERAL DESCRIPTION

The AD9912 is a direct digital synthesizer (DDS) featuring an integrated 14-bit DAC. The AD9912 features a 48–bit frequency tuning word (FTW) which can synthesize frequencies in step sizes no larger than 4 uHz. Absolute frequency accuracy can be achieved by adjusting the DAC system clock.

The AD9912 also features an integrated system clock PLL, which allows reference clocks as low as 25 MHz.

The AD9912 operates over an industrial temperature range, spanning -40°C to +85°C.

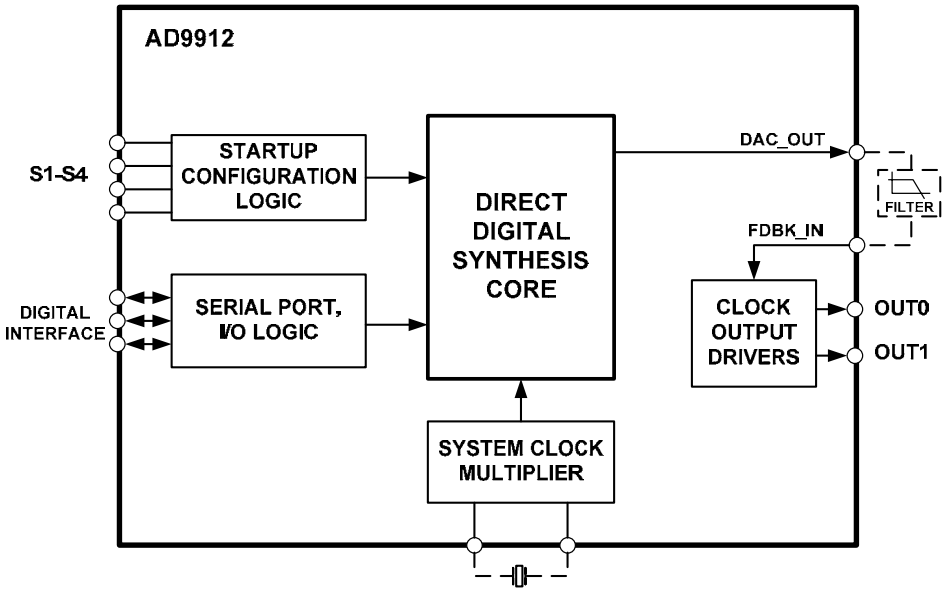

Figure 1: Basic Block Diagram

Rev. PrB

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PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

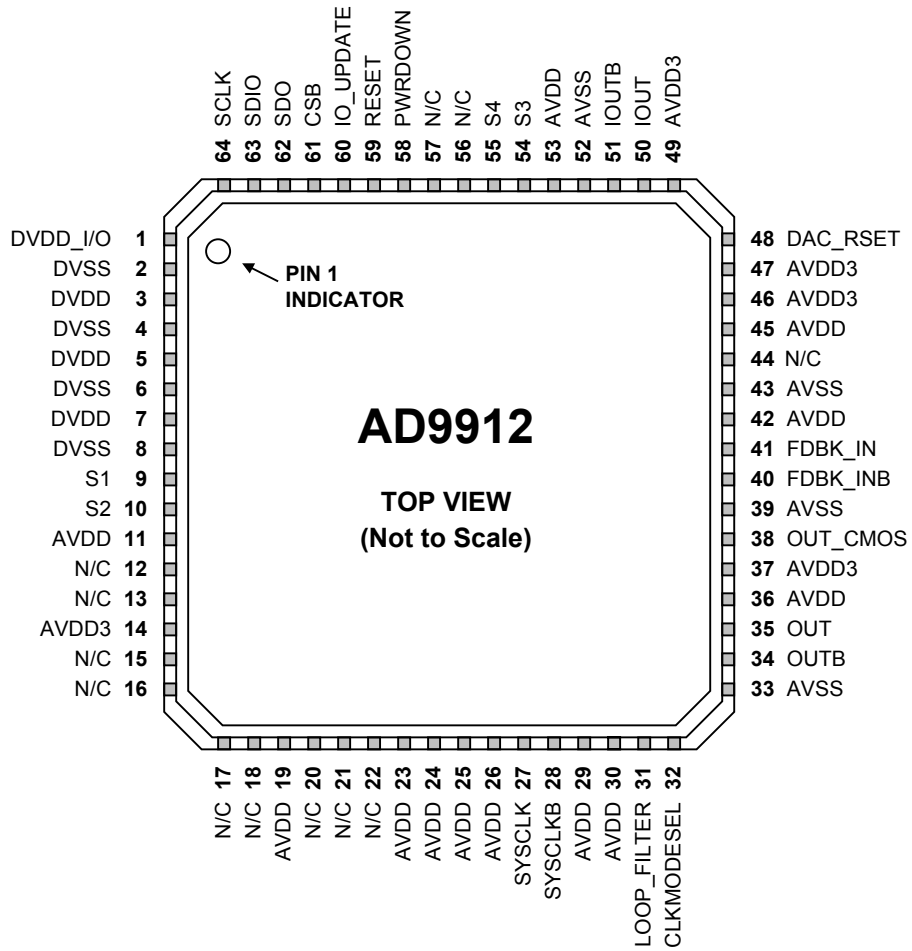

Figure 2: 64-Lead LFCSP Pin Configuration

Table 2: Pin Function Descriptions

Pin No.	Input/ Output	Pin Type	Mnemonic	Description
1	I	Power	DVDD_I/O	3.3V I/O Digital Supply
2, 4, 6, 8	I	Power	DVSS	Digital Ground: Connect to Ground
3, 5, 7	I	Power	DVDD	1.8V Digital Supply
9, 10, 54, 55	I/O	3.3V CMOS	S1, S2, S3, S4	Configurable startup strapping pins: These pins are configured under program control (see "Default Power-up Frequency Options for 1 GHz System Clock" on Page 21. After power-up, these pins become outputs.
11, 19, 23-26, 29, 30, 36, 42, 45, 53	I	Power	AVDD	Analog Supply: Connect to a nominal 1.8V Supply

12, 13, 15-18, 20, 21, 22, 44		N/C	No Connect	No Connect: These excess, unused pins should be left floating.
14, 37, 46, 47, 49	I	Power	AVDD3	Analog Supply: Connect to a nominal 3.3V supply
27	I		SYSCLK	System Clock Input. Can be LVPECL or Crystal input, depending on CLKMODESEL pin.
28	I		SYSCLKB	Complementary System Clock: Complementary signal to the input provided on pin 27
31			LOOP_FILTER	System Clock Multiplier Loop Filter: When using the frequency multiplier to drive the System Clock, an external loop filter must be constructed and attached to this pin.
32	I	1.8V CMOS	CLKMODESEL	Clock Mode Select. Set to GND when using a crystal. Pull up to 1.8V when using either an oscillator or external clock source. (See the *SysClk Inputs* section for details on the use of this pin).
33, 39, 43, 52	I	GND	AVSS	Analog Ground: Connect to Ground. NOTE: Pin 43 is a ground shield connection.
34	O	1.8V HSTL	OUTB	Complementary HSTL Output: See spec table and the OUTPUT DRIVERS AND MULTIPLIER section, under sub heading Primary (Differential) Driver, for details
35	O	1.8V HSTL	OUT	HSTL Output: See specification table and the CLOCK DRIVERS section
38	O	3.3V CMOS	OUT_CMOS	CMOS Output: See specification table and the CLOCK DRIVERS section
40	I		FDBK_INB	Complementary Feedback input: In standard operating mode, this pin is connected to the filtered IOUTB output . This internally biased input is typically AC-coupled, and when configured as such, can accept any differential signal.
41	I		FDBK_IN	Feedback Input: In standard operating mode, this pin is connected to the filtered IOUT output
48	O		DAC_RSET	DAC output current setting resistor. Connect a resistor from this pin to GND . See the "*DAC Output"* section.
50	O		IOUT	DAC output: Output signal should be filtered and sent back on chip through FDBK_INB input
51	O		IOUTB	Complimentary DAC output: Output signal should be filtered and sent back on chip through FDBK_IN input
56, 57			No Connect	No Connect: These should be left floating.
58	I	3.3V CMOS	PWRDOWN	Power Down: When this active high pin is asserted, the device goes into full power down mode.
59	I	3.3V CMOS	RESET	Chip Reset: When this active high pin is asserted, the chip goes into reset. Note: upon power up, a 10 us reset pulse is automatically generated when the power supplies reach a threshold and stabilize.
60	I	3.3V CMOS	IO_UPDATE	I/O Update: A logic transition from 0 to 1 on this pin transfers data from the I/O port registers to the control registers (see the *Write* subsection of the *General Operation of Serial Control Port* section).
61	I	3.3V CMOS	CSB	Chip Select: Active low. When programming a device, this pin must be held low. In systems where more than one AD9549 is present this enables individual programming of each AD9549
62	O	3.3V CMOS	SDO	Serial Data Output: When the device is in three wire mode, data is read on this pin
63	I/O	3.3V CMOS	SDIO	Serial Data Input/Output: When the device is in three-wire mode, data is written via this pin. In 2 wire mode, data reads and writes both occur on this pin
64	O	3.3V CMOS	SCLK	Serial Programming Clock: data clock for serial programming.