

# **AMD Athlon™ MP Processor Model 10 Data Sheet for Multiprocessor Platforms**



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## Revision History

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Date	Rev	Description
October 2003	C	Public revision C of the <i>AMD Athlon™ MP Processor Model 10 Data Sheet for Multiprocessor Platforms</i> includes the following changes: <ul style="list-style-type: none"><li data-bbox="435 506 1485 573">■ In Chapter 6, revised Table 1, “Electrical and Thermal Specifications for the AMD Athlon™ MP Processor Model 10,” on page 23.</li><li data-bbox="435 583 1485 646">■ In Chapter 11, revised Figure 16, “OPN Example for the AMD Athlon™ MP Processor Model 10,” on page 77.</li></ul>
May 2003	B	Initial public release of the <i>AMD Athlon™ MP Processor Model 10 Data Sheet for Multiprocessor Platforms</i>



# 1 Overview

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**The AMD Athlon™ MP processor model 10 powers the next generation in computing platforms, delivering compelling performance for cutting-edge applications and an unprecedented computing experience.**

The AMD Athlon™ MP processor model 10, based on leading-edge 0.13 micron technology and increased on-chip cache, integrates the innovative design and manufacturing expertise of AMD to deliver improved performance, while maintaining the stable and compatible Socket A infrastructure of the AMD Athlon MP processor. The AMD Athlon MP processor model 10 continues to deliver breakthrough performance in the multiprocessing server and workstation markets. This processor is designed to meet the reliability and computation-intensive requirements of cutting-edge software applications required by workstations and servers.

Delivered in an OPGA package, the AMD Athlon MP processor model 10 delivers the integer, floating-point, and 3D multimedia performance for enterprise applications running on x86 system platforms. The AMD Athlon MP processor model 10 offers compelling performance for productivity software, including workstation-class digital content creation (DCC), electronic design automation (EDA), and computer-aided design (CAD), as well as infrastructure and collaborative server applications. It also offers the scalability and reliability that IT managers and business users require for mission-critical computing.

The AMD Athlon MP processor model 10 features the seventh-generation microarchitecture, including a high-speed execution core that includes multiple x86 instruction decoders, a dual-ported, 128-Kbyte, split level-one (L1) cache, a 512-Kbyte on-chip L2 cache, three independent integer pipelines, three address calculation pipelines, and a superscalar, fully pipelined, out-of-order, three-way floating-point engine. The integrated L2 cache supports the growing processor and system bandwidth requirements of emerging software, graphics, I/O, and memory technologies. The processor also features the advanced modified owner exclusive shared invalid (MOESI) cache coherency protocol to ensure efficient cache integrity in a multiprocessing environment. The floating-point engine is capable of delivering excellent performance on the numerically complex applications typical of servers and workstations.

The key features of the AMD Athlon MP processor model 10 include QuantiSpeed™ architecture, 640 Kbytes of total, high-performance, full-speed, on-chip cache, an advanced 266 front-side bus (FSB), a 2.1-Gigabyte per second system bus, 3DNow!™ Professional technology, and fully featured logic implementation for the multiprocessor configuration.

The AMD Athlon system bus combines the latest technological advances, such as point-to-point topology, source-synchronous packet-based transfers, and low-voltage signaling. The point-to-point front-side bus architecture provides a more efficient, higher bandwidth bus that allows each processor, in a multiprocessor configuration, to communicate to the system chipset through two, full-speed, independent buses rather than through a common, shared bus. Combined with the AMD-760™ MPX chipset, the processor and the system bus interface with double-data rate (DDR) memory subsystems, providing scalable headroom for bandwidth-hungry applications such as large databases, CAD/CAM modeling, and simulation engines.

The front-side bus of the AMD Athlon MP processor model 10 also provides multiple-bit error detection and single-bit error correction with 8-bit error correction code (ECC). The front-side bus with 8-bit ECC delivers the high reliability and consistency demanded by mission-critical applications.

The AMD Athlon MP processor model 10 is binary-compatible with existing x86 software and backwards compatible with applications optimized for MMX™ and 3DNow! technologies. Using a data format and single-instruction multiple-data (SIMD) operations based on the MMX instruction model, the AMD Athlon MP processor model 10 can produce as many as four, 32-bit, single-precision floating-point results per clock cycle. The 3DNow! Professional technology implemented in the AMD Athlon MP processor model 10 includes new integer multimedia instructions and software-directed data movement instructions for optimizing such applications as digital content creation and streaming video for the internet, as well as new instructions for digital signal processing (DSP)/communications applications.

## 1.1 AMD Athlon™ MP Processor Model 10 Key Microarchitecture Summary

The following features summarize the AMD Athlon MP processor model 10 microarchitecture:

- **QuantiSpeed architecture:**
  - An advanced nine-issue, superpipelined, superscalar x86 processor microarchitecture designed for increased instructions per clock cycle (IPC) and high clock frequencies
  - Fully pipelined floating-point unit that executes all x87 (floating-point), MMX and 3DNow! professional instructions
  - Hardware data pre-fetch that increases and optimizes performance on high-end software applications that utilize high-bandwidth system capability
  - Advanced two-level translation look-aside buffer (TLB) structures for enhanced data and instruction address translation. The AMD Athlon MP processor with QuantiSpeed architecture incorporates three TLB optimizations: the L1 DTLB increases from 32 to 40 entries, the L2 ITLB and L2 DTLB both use exclusive architecture, and the TLB entries can be speculatively loaded.
- 3DNow! Professional technology with new instructions to enable improved integer-math calculations for speech or video encoding and improved data movement for internet plug-ins and other streaming applications
- A 266-MHz AMD Athlon system bus enabling leading-edge system bandwidth for data movement-intensive applications
- Point-to-point front-side bus architecture allowing each processor in a multi-processor configuration to communicate to the system chipsets through two, full speed, independent buses
- High-performance cache architecture featuring an integrated 128-Kbyte L1 cache and a 16-way, 256-Kbyte on-chip L2 cache for a total of 640 Kbytes of on-chip cache
- Multiple-bit error detection and single-bit error correction with 8-bit error correction code (ECC)
- Full-featured MP Local APIC implementation





## 2 Interface Signals

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The AMD Athlon system bus architecture is designed to deliver superior data movement bandwidth for next-generation x86 platforms as well as the high-performance required by enterprise-class application software. The system bus architecture consists of three high-speed channels (a unidirectional processor request channel, a unidirectional probe channel, and a 72-bit bidirectional data channel, including 8-bit error correction code [ECC] protection), source-synchronous clocking, and a packet-based protocol. In addition, the system bus supports several control, clock, and legacy signals. The interface signals use an impedance controlled push-pull, low-voltage, swing-signaling technology contained within the Socket A socket.

For more information, see “AMD Athlon™ System Bus Signals” on page 6, Chapter 10, “Pin Descriptions” on page 51, and the *AMD Athlon™ and AMD Duron™ System Bus Specification*, order# 21902.

### 2.1 Signaling Technology

The AMD Athlon system bus uses a low-voltage, swing-signaling technology, that has been enhanced to provide larger noise margins, reduced ringing, and variable voltage levels. The signals are push-pull and impedance compensated. The signal inputs use differential receivers that require a reference voltage ( $V_{REF}$ ). The reference signal is used by the receivers to determine if a signal is asserted or deasserted by the source. Termination resistors are not needed because the driver is impedance-matched to the motherboard and a high impedance reflection is used at the receiver to bring the signal past the input threshold.

For more information about pins and signals, see Chapter 10, “Pin Descriptions” on page 51.

## 2.2 Push-Pull (PP) Drivers

The AMD Athlon MP processor model 10 supports push-pull (PP) drivers. The system logic configures the processor with the configuration parameter called SysPushPull (1=PP). The impedance of the PP drivers is set to match the impedance of the motherboard by two external resistors connected to the ZN and ZP pins.

See “ZN and ZP Pins” on page 76 for more information.

## 2.3 AMD Athlon™ System Bus Signals

The AMD Athlon system bus is a clock-forwarded, point-to-point interface with the following three point-to-point channels:

- A 13-bit unidirectional output address/command channel
- A 13-bit unidirectional input address/command channel
- A 72-bit bidirectional data channel

For more information, see Chapter 7, “Electrical Data” on page 25 and the *AMD Athlon™ and AMD Duron™ System Bus Specification*, order# 21902.

### 3 Logic Symbol Diagram

Figure 1 is the logic symbol diagram of the processor. This diagram shows the logical grouping of the input and output signals.

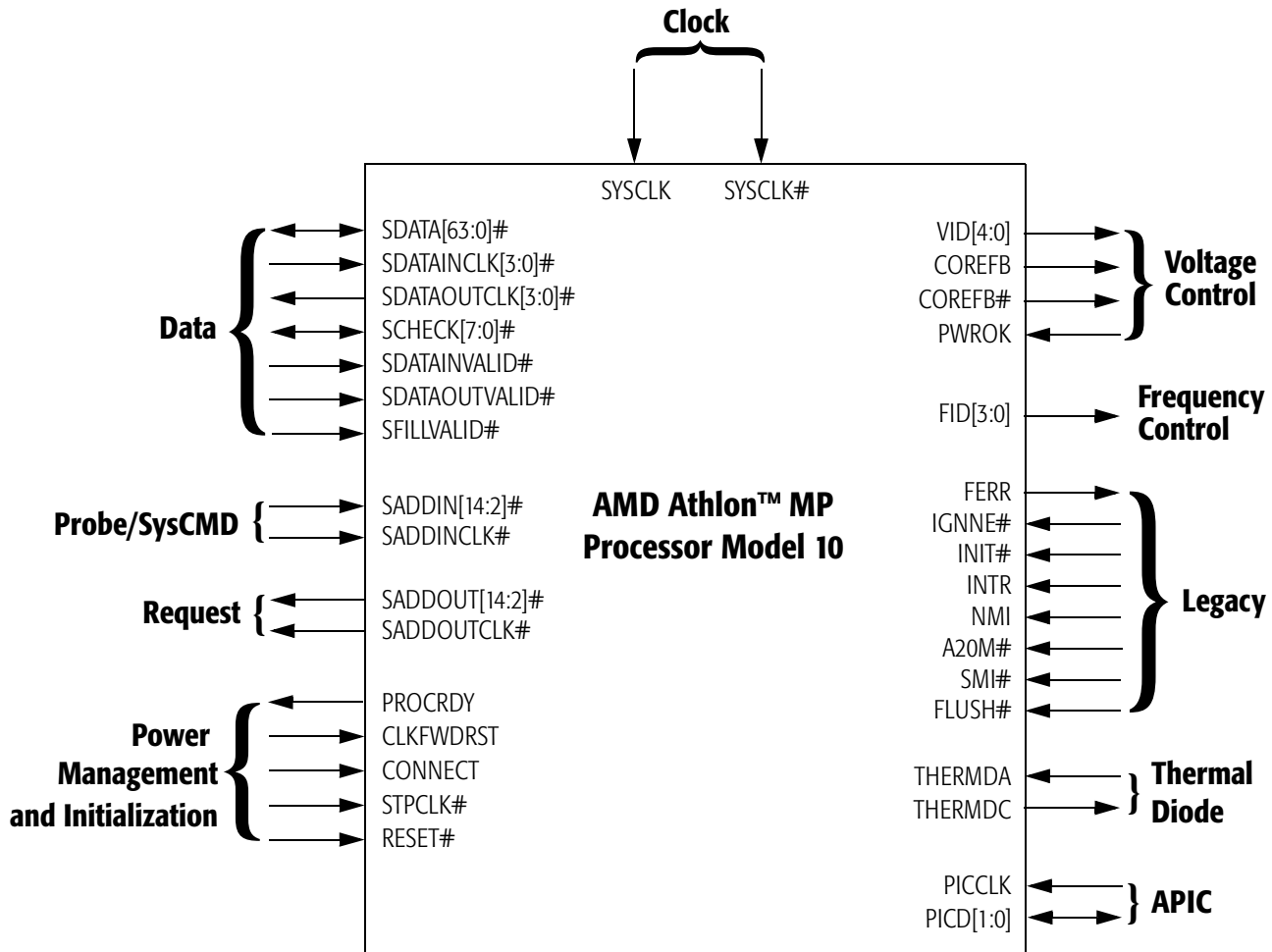


Figure 1. Logic Symbol Diagram



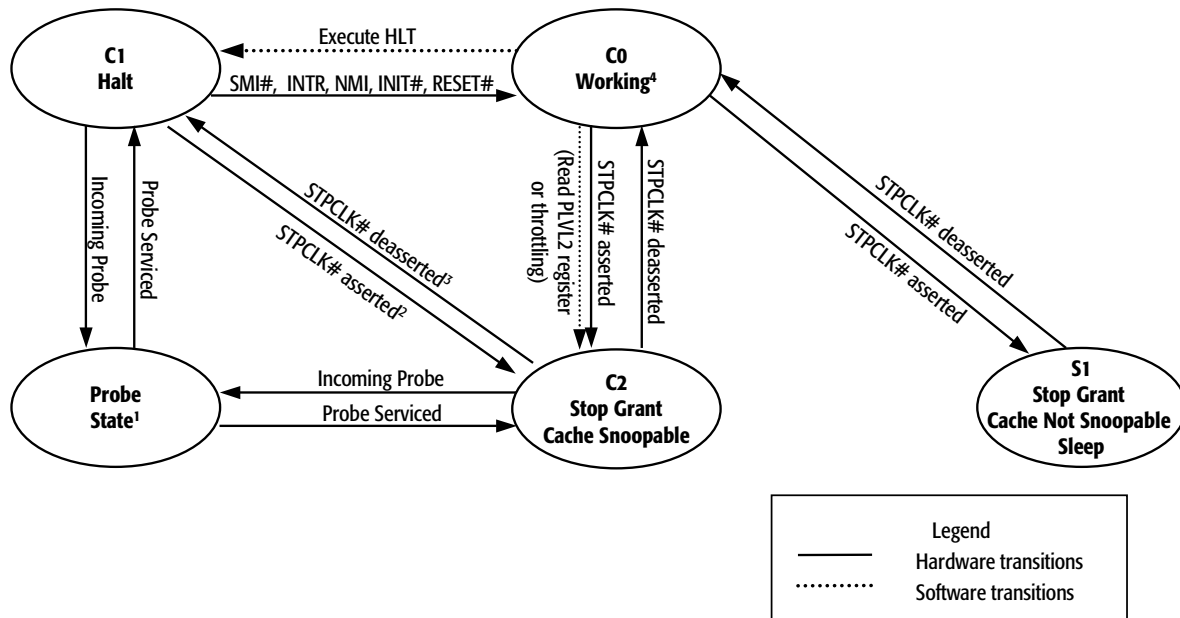
## 4 Power Management

This chapter describes the power management control system of the AMD Athlon™ MP processor model 10. The power management features of the processor are compliant with the ACPI 1.0b and ACPI 2.0 specifications.

### 4.1 Power Management States

The AMD Athlon MP processor model 10 supports low-power Halt and Stop Grant states. These states are used by advanced configuration and power interface (ACPI) enabled operating systems for processor power management.

Figure 2 shows the power management states of the processor. The figure includes the ACPI “Cx” naming convention for these states.



Note: The AMD Athlon™ System Bus is connected during the following states:

- 1) The Probe state
- 2) During transitions between the Halt state and the C2 Stop Grant state
- 3) During transitions between the C2 Stop Grant state and the Halt state
- 4) C0 Working state

Figure 2. AMD Athlon™ MP Processor Model 10 Power Management States

The following sections provide an overview of the power management states. For more details, refer to the *AMD Athlon™ and AMD Duron™ System Bus Specification*, order# 21902.

**Note:** *In all power management states that the processor is powered, the system must not stop the system clock (SYSCLK/SYSCLK#) to the processor.*

**Working State**

The Working state is the state in which the processor is executing instructions.

**Halt State**

When the processor executes the HLT instruction, the processor enters the Halt state and issues a Halt special cycle to the AMD Athlon system bus. The processor only enters the low power state dictated by the CLK\_Ctl MSR if the system controller (Northbridge) disconnects the AMD Athlon system bus in response to the Halt special cycle.

If STPCLK# is asserted, the processor will exit the Halt state and enter the Stop Grant state. The processor will initiate a system bus connect, if it is disconnected, then issue a Stop Grant special cycle. When STPCLK# is deasserted, the processor will exit the Stop Grant state and re-enter the Halt state. The processor will issue a Halt special cycle when re-entering the Halt state.

The Halt state is exited when the processor detects the assertion of INIT#, RESET#, SMI#, or an interrupt via the INTR or NMI pins, or via a local APIC interrupt message. When the Halt state is exited, the processor will initiate an AMD Athlon system bus connect if it is disconnected.

**Stop Grant States**

The processor enters the Stop Grant state upon recognition of assertion of STPCLK# input. After entering the Stop Grant state, the processor issues a Stop Grant special bus cycle on the AMD Athlon system bus. The processor is not in a low-power state at this time, because the AMD Athlon system bus is still connected. After the Northbridge disconnects the AMD Athlon system bus in response to the Stop Grant special bus cycle, the processor enters a low-power state dictated by the CLK\_Ctl MSR. If the Northbridge needs to probe the processor during the Stop Grant state while the system bus is disconnected, it

must first connect the system bus. Connecting the system bus places the processor into the higher power probe state. After the Northbridge has completed all probes of the processor, the Northbridge must disconnect the AMD Athlon system bus again so that the processor can return to the low-power state. During the Stop Grant states, the processor latches INIT#, INTR, NMI, SMI#, or a local APIC interrupt message, if they are asserted.

The Stop Grant state is exited upon the deassertion of STPCLK# or the assertion of RESET#. When STPCLK# is deasserted, the processor initiates a connect of the AMD Athlon system bus if it is disconnected. After the processor enters the Working state, any pending interrupts are recognized and serviced and the processor resumes execution at the instruction boundary where STPCLK# was initially recognized. If RESET# is sampled asserted during the Stop Grant state, the processor exits the Stop Grant state and the reset process begins.

There are two mechanisms for asserting STPCLK#—hardware and software.

The Southbridge can force STPCLK# assertion for throttling to protect the processor from exceeding its maximum case temperature. This is accomplished by asserting the THERM# input to the Southbridge. Throttling asserts STPCLK# for a percentage of a predefined throttling period: STPCLK# is repetitively asserted and deasserted until THERM# is deasserted.

Software can force the processor into the Stop Grant state by accessing ACPI-defined registers typically located in the Southbridge.

The operating system places the processor into the C2 Stop Grant state by reading the P\_LVL2 register in the Southbridge.

If an ACPI Thermal Zone is defined for the processor, the operating system can initiate throttling with STPCLK# using the ACPI defined P\_CNT register in the Southbridge. The Northbridge connects the AMD Athlon system bus, and the processor enters the Probe state to service cache snoops during Stop Grant for C2 or throttling.

In C2, probes are allowed, as shown in Figure 2 on page 9

The Stop Grant state is also entered for the S1, Powered On Suspend, system sleep state based on a write to the SLP\_TYP and SLP\_EN fields in the ACPI-defined Power Management 1 control register in the Southbridge. During the S1 sleep state, system software ensures no bus master or probe activity occurs. The Southbridge deasserts STPCLK# and brings the processor out of the S1 Stop Grant state when any enabled resume event occurs.

### **Probe State**

The Probe state is entered when the Northbridge connects the AMD Athlon system bus to probe the processor (for example, to snoop the processor caches) when the processor is in the Halt or Stop Grant state. When in the Probe state, the processor responds to a probe cycle in the same manner as when it is in the Working state. When the probe has been serviced, the processor returns to the same state as when it entered the Probe state (Halt or Stop Grant state). When probe activity is completed the processor only returns to a low-power state after the Northbridge disconnects the AMD Athlon system bus again.



## 4.2 Connect and Disconnect Protocol

Significant power savings of the processor only occur if the processor is disconnected from the system bus by the Northbridge while in the Halt or Stop Grant state. The Northbridge can optionally initiate a bus disconnect upon the receipt of a Halt or Stop Grant special cycle. The option of disconnecting is controlled by an enable bit in the Northbridge. If the Northbridge requires the processor to service a probe after the system bus has been disconnected, it must first initiate a system bus connect.

### Connect Protocol

In addition to the legacy STPCLK# signal and the Halt and Stop Grant special cycles, the AMD Athlon system bus connect protocol includes the CONNECT, PROCRDY, and CLKFWDRST signals and a Connect special cycle.

AMD Athlon system bus disconnects are initiated by the Northbridge in response to the receipt of a Halt or Stop Grant. Reconnect is initiated by the processor in response to an interrupt for Halt or STPCLK# deassertion. Reconnect is initiated by the Northbridge to probe the processor.

The Northbridge contains BIOS programmable registers to enable the system bus disconnect in response to Halt and Stop Grant special cycles. When the Northbridge receives the Halt or Stop Grant special cycle from the processor and, if there are no outstanding probes or data movements, the Northbridge deasserts CONNECT a minimum of eight SYSCLK periods after the last command sent to the processor. The processor detects the deassertion of CONNECT on a rising edge of SYSCLK and deasserts PROCRDY to the Northbridge. In return, the Northbridge asserts CLKFWDRST in anticipation of reestablishing a connection at some later point.

**Note:** *The Northbridge must disconnect the processor from the AMD Athlon system bus before issuing the Stop Grant special cycle to the PCI bus or passing the Stop Grant special cycle to the Southbridge for systems that connect to the Southbridge with HyperTransport™ technology.*

*This note applies to current chipset implementation—alternate chipset implementations that do not require this are possible.*

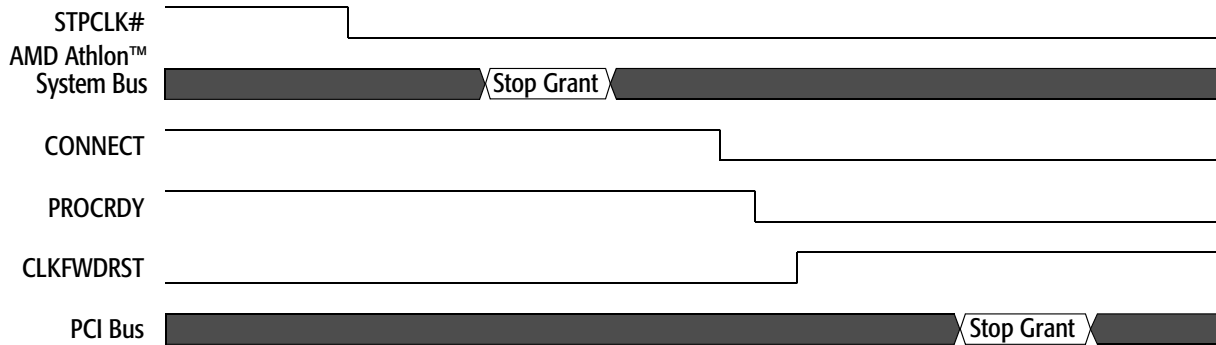
**Note:** *In response to Halt special cycles, the Northbridge passes the Halt special cycle to the PCI bus or Southbridge immediately.*

The processor can receive an interrupt after it sends a Halt special cycle, or STPCLK# deassertion after it sends a Stop Grant special cycle to the Northbridge but before the disconnect actually occurs. In this case, the processor sends the Connect special cycle to the Northbridge, rather than continuing with the disconnect sequence. In response to the Connect special cycle, the Northbridge cancels the disconnect request.

The system is required to assert the CONNECT signal before returning the C-bit for the connect special cycle (assuming CONNECT has been deasserted).

For more information, see the *AMD Athlon™ and AMD Duron™ System Bus Specification*, order# 21902 for the definition of the C-bit and the Connect special cycle.

Figure 3 shows STPCLK# assertion resulting in the processor in the Stop Grant state and the AMD Athlon system bus disconnected.

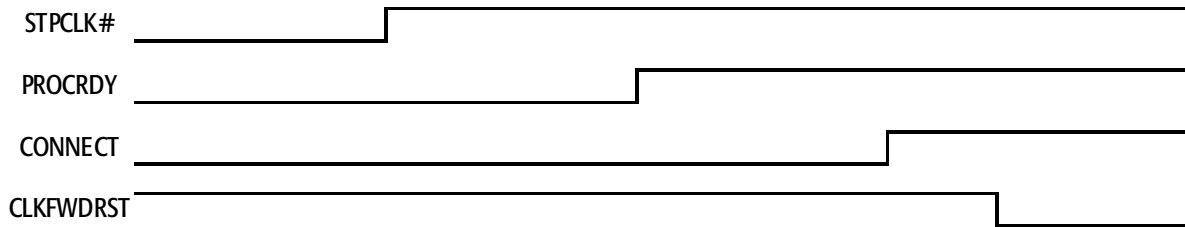


**Figure 3. AMD Athlon™ System Bus Disconnect Sequence in the Stop Grant State**

An example of the AMD Athlon system bus disconnect sequence is as follows:

1. The peripheral controller (Southbridge) asserts STPCLK# to place the processor in the Stop Grant state.
2. When the processor recognizes STPCLK# asserted, it enters the Stop Grant state and then issues a Stop Grant special cycle.
3. When the special cycle is received by the Northbridge, it deasserts CONNECT, assuming no probes are pending, initiating a bus disconnect to the processor.
4. The processor responds to the Northbridge by deasserting PROCRDY.
5. The Northbridge asserts CLKFWRST to complete the bus disconnect sequence.
6. After the processor is disconnected from the bus, the processor enters a low-power state. The Northbridge passes the Stop Grant special cycle along to the Southbridge.

Figure 4 shows the signal sequence of events that takes the processor out of the Stop Grant state, connects the processor to the AMD Athlon system bus, and puts the processor into the Working state.



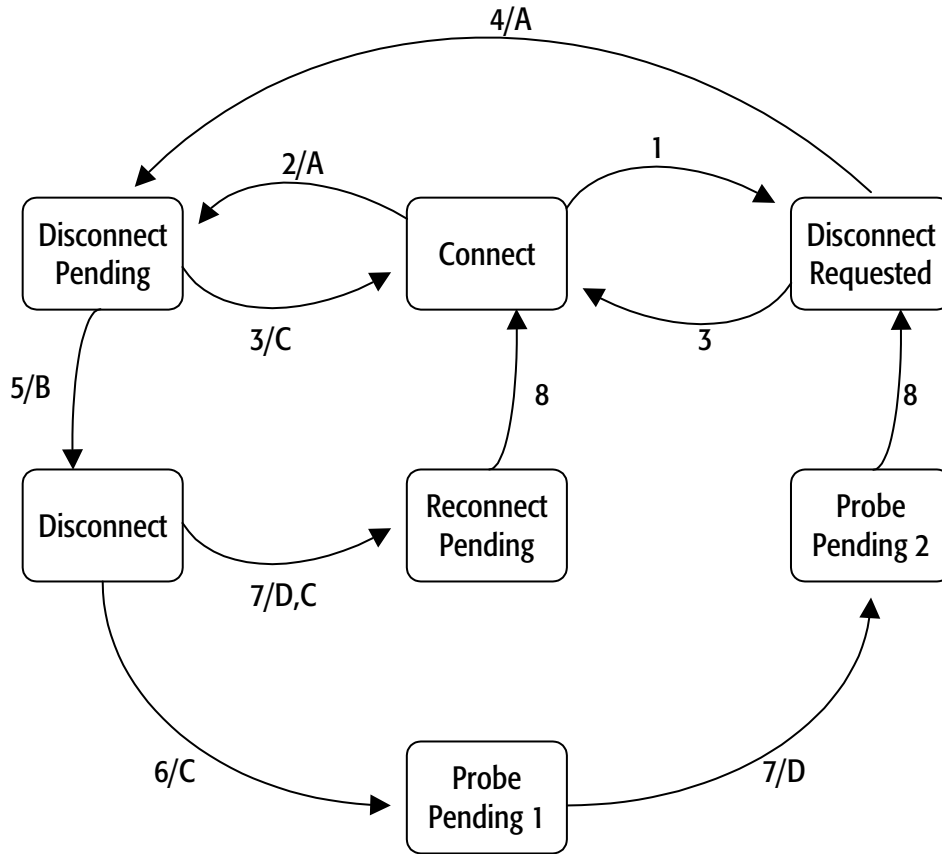
**Figure 4. Exiting the Stop Grant State and Bus Connect Sequence**

The following sequence of events removes the processor from the Stop Grant state and connects it to the system bus:

1. The Southbridge deasserts STPCLK#, informing the processor of a wake event.
2. When the processor recognizes STPCLK# deassertion, it exits the low-power state and asserts PROCRDY, notifying the Northbridge to connect to the bus.
3. The Northbridge asserts CONNECT.
4. The Northbridge deasserts CLKFWRST, synchronizing the forwarded clocks between the processor and the Northbridge.
5. The processor issues a Connect special cycle on the system bus and resumes operating system and application code execution.

**Connect State Diagram**

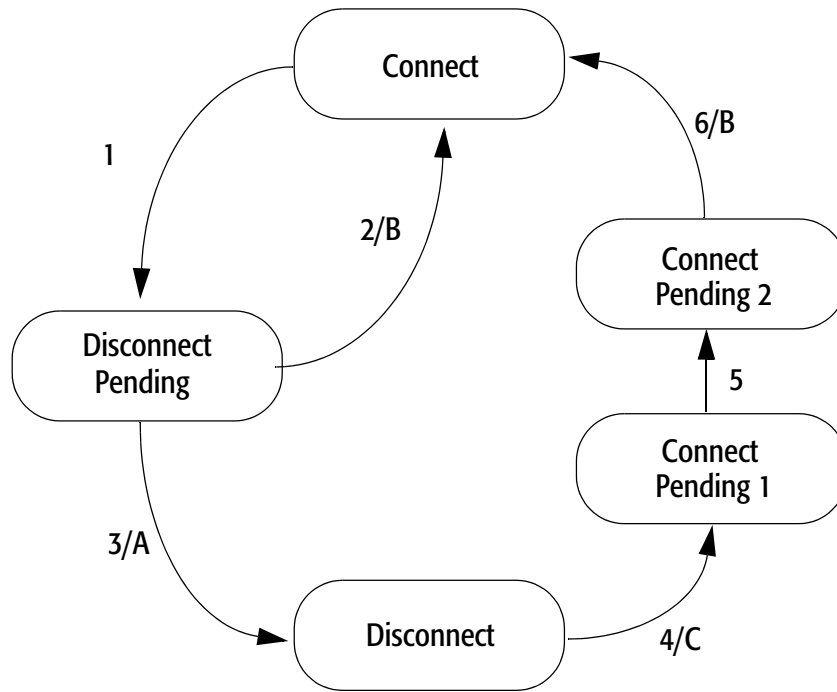
Figure 5 below and Figure 6 on page 18 show the Northbridge and processor connect state diagrams, respectively.



Condition	
1	A disconnect is requested and probes are still pending.
2	A disconnect is requested and no probes are pending.
3	A Connect special cycle from the processor.
4	No probes are pending.
5	PROCRDY is deasserted.
6	A probe needs service.
7	PROCRDY is asserted.
8	Three SYSCLK periods after CLKFWRST is deasserted. <i>Although reconnected to the system interface, the Northbridge must not issue any non-NOP SysDC commands for a minimum of four SYSCLK periods after deasserting CLKFWRST.</i>

Action	
A	Deassert CONNECT eight SYSCLK periods after last SysDC sent.
B	Assert CLKFWRST.
C	Assert CONNECT.
D	Deassert CLKFWRST.

**Figure 5. Northbridge Connect State Diagram**



Condition		Action	
1	CONNECT is deasserted by the Northbridge (for a previously sent Halt or Stop Grant special cycle).	A	CLKFWRST is asserted by the Northbridge.
2	Processor receives a wake-up event and must cancel the disconnect request.	B	Issue a Connect special cycle.*
3	Deassert PROCRDY and slow down internal clocks.	C	Return internal clocks to full speed and assert PROCRDY.
4	Processor wake-up event or CONNECT asserted by Northbridge.	<b>Note:</b> * The Connect special cycle is only issued after a processor wake-up event (interrupt or STPCLK# deassertion) occurs. If the AMD Athlon™ system bus is connected so the Northbridge can probe the processor, a Connect special cycle is not issued at that time (it is only issued after a subsequent processor wake-up event).	
5	CLKFWRST is deasserted by the Northbridge.		
6	Forward clocks start three SYSClk periods after CLKFWRST is deasserted.		

Figure 6. Processor Connect State Diagram

### 4.3 Clock Control

The processor implements a Clock Control (CLK\_Ctl) MSR (address C001\_001Bh) that determines the internal clock divisor when the AMD Athlon system bus is disconnected.

Refer to the *AMD Athlon™ and AMD Duron™ Processors BIOS, Software, and Debug Developers Guide*, order# 21656, for more details on the CLK\_Ctl register.





## 5 CPUID Support

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AMD Athlon™ MP processor model 10 version and feature set recognition can be performed through the use of the CPUID instruction, that provides complete information about the processor—vendor, type, name, etc., and its capabilities. Software can make use of this information to accurately tune the system for maximum performance and benefit to users.

For information on the use of the CPUID instruction see the following documents:

- *AMD Processor Recognition Application Note*, order# 20734
- *AMD Athlon™ Processor Recognition Application Note Addendum*, order# 21922
- *AMD Athlon™ and AMD Duron™ Processors BIOS, Software, and Debug Developers Guide*, order# 21656



## 6 Electrical and Thermal Specifications for the AMD Athlon™ MP Processor Model 10

This chapter provides the electrical and thermal specifications for the AMD Athlon™ MP processor model 10.

Table 1 shows the electrical and thermal specifications in the C0 Working state and the S1 Stop Grant state for the AMD Athlon MP processor model 10.

**Table 1. Electrical and Thermal Specifications for the AMD Athlon™ MP Processor Model 10**

Frequency in MHz (Model Number)	V <sub>CC_CORE</sub> (Core Voltage)	I <sub>CC</sub> (Processor Current)				Thermal Power <sup>5</sup>		Maximum Die Temperature
		Working State C0		Stop Grant S1 <sup>1, 2, 3, 4</sup>		Maximum	Typical	
		Maximum	Typical	Maximum	Typical			
2000 (2600+)	1.60 V	37.5 A	29.5 A	8.75 A	6.88 A	60.0 W	47.2 W	90°C
2133 (2800+)								

**Notes:**

1. See Figure 2, "AMD Athlon™ MP Processor Model 10 Power Management States" on page 9.
2. The maximum Stop Grant currents are absolute worst case currents for parts that may yield from the worst case corner of the process and are not representative of the typical Stop Grant current that is currently about one-third of the maximum specified current.
3. These currents occur when the AMD Athlon™ system bus is disconnected and a low power ratio of 1/64 is applied to the core clock grid of the processor as dictated by a value of 2003\_D22Fh programmed into the Clock Control (CLK\_Ctl) MSR. For more information, refer to the AMD Athlon™ and AMD Duron™ Processors BIOS, Software, and Debug Developers Guide, order# 21656.
4. The Stop Grant current consumption is characterized at 50°C and not tested.
5. Thermal design power represents the maximum sustained power dissipated while executing publicly-available software or instruction sequences under normal system operation at nominal V<sub>CC\_CORE</sub>. Thermal solutions must monitor the temperature of the processor to prevent the processor from exceeding its maximum die temperature.



## 7 Electrical Data

This chapter describes the electrical characteristics that apply to the AMD Athlon™ MP processor model 10.

### 7.1 Conventions

The conventions used in this chapter are as follows:

- Current specified as being sourced by the processor is *negative*.
- Current specified as being sunk by the processor is *positive*.

### 7.2 Interface Signal Groupings

The electrical data in this chapter is presented separately for each signal group.

Table 2 defines each group and the signals contained in each group.

**Table 2. Interface Signal Groupings**

Signal Group	Signals	Notes
Power	VID[4:0], VCCA, V <sub>CC_CORE</sub> , COREFB, COREFB#	See , "Voltage Identification (VID[4:0])" on page 26, "" on page 75, "VCCA AC and DC Characteristics" on page 27, "VCCA Pin" on page 75, "V <sub>CC_CORE</sub> Characteristics" on page 28, and "COREFB and COREFB# Pins" on page 71.
Frequency	FID[3:0]	See "Frequency Identification (FID[3:0])" on page 27 and "FID[3:0] Pins" on page 71.
System Clocks	SYSCLK, SYSCLK# (Tied to CLKIN/CLKIN# and RSTCLK/RSTCLK#), PLLBYPASSCLK#, PLLBYPASSCLK	See Table 8, "SYSCLK and SYSCLK# DC Characteristics," on page 31, Table 9, "SYSCLK and SYSCLK# AC Characteristics," on page 32, "SYSCLK and SYSCLK#" on page 75, and "PLL Bypass and Test Pins" on page 74.
AMD Athlon™ System Bus	SADDIN[14:2]#, SADDOUT[14:2]#, SADDINCLK#, SADDOUTCLK#, SFILLVAL#, SDATAINVAL#, SDATAOUTVAL#, SDATA[63:0]#, SDATAINCLK[3:0]#, SDATAOUTCLK[3:0]#, CLKFWDRST, PROCRDY, CONNECT	See "AMD Athlon™ System Bus AC and DC Characteristics" on page 33, and "CLKFWDRST Pin" on page 70.

**Table 2. Interface Signal Groupings (Continued)**

Signal Group	Signals	Notes
Southbridge	RESET#, INTR, NMI, SMI#, INIT#, A20M#, FERR, IGNNE#, STPCLK#, FLUSH#	See "General AC and DC Characteristics" on page 35, "INTR Pin" on page 73, "NMI Pin" on page 74, "SMI# Pin" on page 75, "INIT# Pin" on page 73, "A20M# Pin" on page 70, "FERR Pin" on page 71, "IGNNE# Pin" on page 73, "SYSCLK and SYSCLK#" on page 75, and "FLUSH# Pin" on page 73.
JTAG	TMS, TCK, TRST#, TDI, TDO	See "General AC and DC Characteristics" on page 35.
Test	PLLBYPASS#, PLLTEST#, PLLMON1, PLLMON2, SCANCLK1, SCANCLK2, SCANSHIFTEN, SCANINTEVAL, ANALOG	See "General AC and DC Characteristics" on page 35, "PLL Bypass and Test Pins" on page 74, "Scan Pins" on page 74, "Analog Pin" on page 70.
Miscellaneous	DBREQ#, DBRDY, PWROK	See "General AC and DC Characteristics" on page 35, "DBRDY and DBREQ# Pins" on page 71, "PWROK Pin" on page 74.
APIC	PICD[1:0]#, PICCLK	See "APIC Pins AC and DC Characteristics" on page 40, and "APIC Pins, PICCLK, PICD[1:0]#" on page 70.
Thermal	THERMDA, THERMDC	See Table 13, "Thermal Diode Electrical Characteristics," on page 38, and "THERMDA and THERMDC Pins" on page 75.

### 7.3 Voltage Identification (VID[4:0])

Table 3 shows the VID[4:0] DC Characteristics. For more information on VID[4:0] DC Characteristics, see " " on page 75.

**Table 3. VID[4:0] DC Characteristics**

Parameter	Description	Min	Max
I <sub>OL</sub>	Output Current Low	6 mA	
V <sub>OH</sub>	Output High Voltage	–	5.25 V *
<b>Note:</b>			
* The VID pins are either open circuit or pulled to ground. It is recommended that these pins are not pulled above 5.25 V, which is 5.0 V + 5%.			

## 7.4 Frequency Identification (FID[3:0])

Table 4 shows the FID[3:0] DC characteristics. For more information, see “FID[3:0] Pins” on page 71.

**Table 4. FID[3:0] DC Characteristics**

Parameter	Description	Min	Max
$I_{OL}$	Output Current Low	6 mA	
$V_{OH}$	Output High Voltage	-	2.625 V <sup>1</sup>
			$ V_{OH} - V_{CC\_CORE}  \leq 1.60 V^2$

**Note:**

1. The FID pins must not be pulled above 2.625 V, which is equal to 2.5 V plus a maximum of five percent.
2. Refer to “VCC\_2.5V Generation Circuit” found in the section, “Motherboard Required Circuits,” of the AMD Athlon™ Processor-Based Motherboard Design Guide, order# 24363.

## 7.5 VCCA AC and DC Characteristics

Table 5 shows the AC and DC characteristics for VCCA. For more information, see “VCCA Pin” on page 75.

**Table 5. VCCA AC and DC Characteristics**

Symbol	Parameter	Min	Nominal	Max	Units	Notes
$V_{VCCA}$	VCCA Pin Voltage	2.25	2.5	2.75	V	1
				$ V_{VCCA} - V_{CC\_CORE}  \leq 1.60 V$	-	2
$I_{VCCA}$	VCCA Pin Current	0		50	mA/GHz	3

**Notes:**

1. Minimum and Maximum voltages are absolute. No transients below minimum nor above maximum voltages are permitted.
2. For more information, refer to the AMD Athlon™ Processor-Based Motherboard Design Guide, order# 24363.
3. Measured at 2.5 V.

## 7.6 Decoupling

See the AMD Athlon™ Processor-Based Motherboard Design Guide, order# 24363, or contact your local AMD office for information about the decoupling required on the motherboard for use with the AMD Athlon MP processor model 10.

## 7.7 $V_{CC\_CORE}$ Characteristics

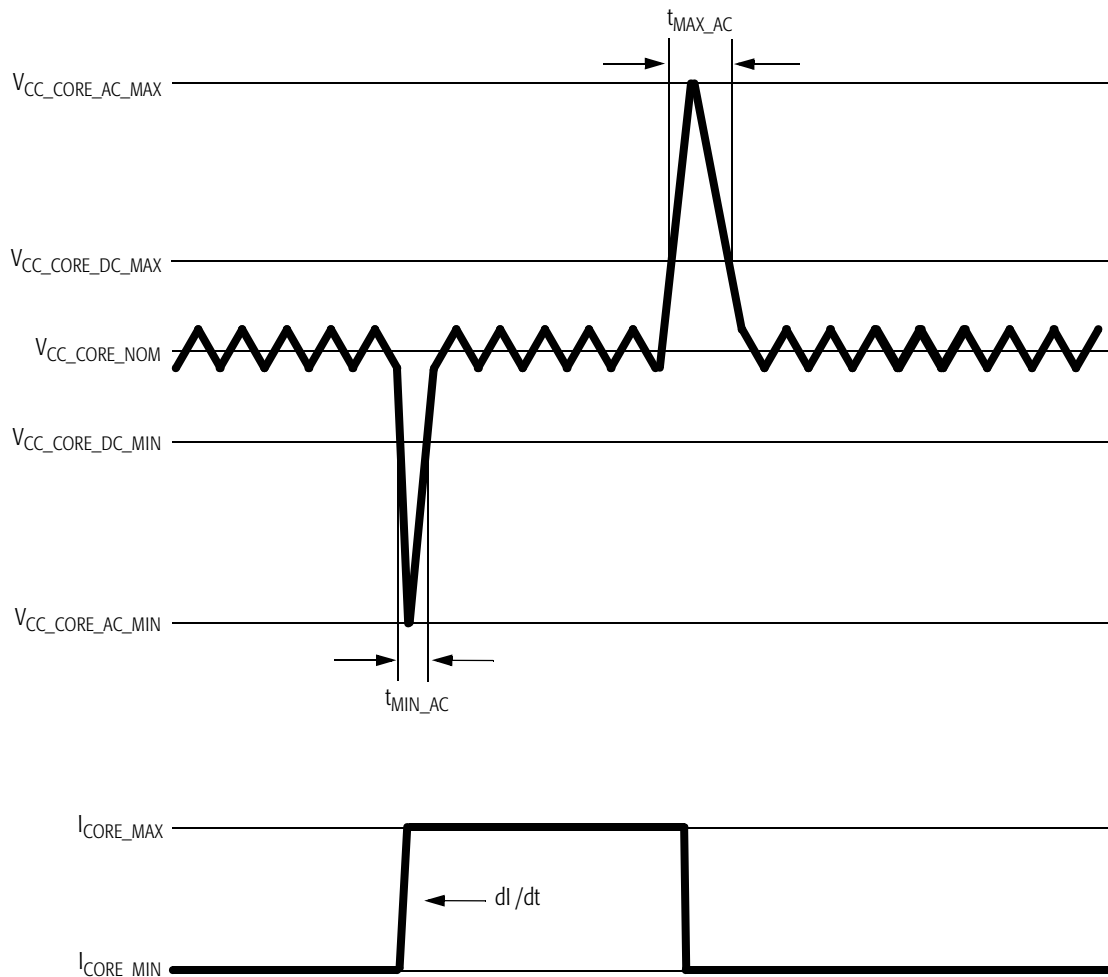
Table 6 shows the AC and DC characteristics for  $V_{CC\_CORE}$ . See Figure 7 on page 29 for a graphical representation of the  $V_{CC\_CORE}$  waveform.

**Table 6.  $V_{CC\_CORE}$  AC and DC Characteristics**

Symbol	Parameter	Limit in Working State	Units
$V_{CC\_CORE\_DC\_MAX}$	Maximum static voltage above $V_{CC\_CORE\_NOM}$ *	50	mV
$V_{CC\_CORE\_DC\_MIN}$	Maximum static voltage below $V_{CC\_CORE\_NOM}$ *	-50	mV
$V_{CC\_CORE\_AC\_MAX}$	Maximum excursion above $V_{CC\_CORE\_NOM}$ *	150	mV
$V_{CC\_CORE\_AC\_MIN}$	Maximum excursion below $V_{CC\_CORE\_NOM}$ *	-100	mV
$t_{MAX\_AC}$	Maximum excursion time for AC transients	10	$\mu$ s
$t_{MIN\_AC}$	Negative excursion time for AC transients	5	$\mu$ s
<b>Note:</b> * All voltage measurements are taken differentially at the COREFB/COREFB# pins.			



Figure 7 shows the processor core voltage ( $V_{CC\_CORE}$ ) waveform response to perturbation. The  $t_{MIN\_AC}$  (negative AC transient excursion time) and  $t_{MAX\_AC}$  (positive AC transient excursion time) represent the maximum allowable time below or above the DC tolerance thresholds.



**Figure 7.  $V_{CC\_CORE}$  Voltage Waveform**

## 7.8 Absolute Ratings

The AMD Athlon MP processor model 10 should not be subjected to conditions exceeding the absolute ratings, as such conditions can adversely affect long-term reliability or result in functional damage.

Table 7 lists the maximum absolute ratings of operation for the AMD Athlon MP processor model 10.

**Table 7. Absolute Ratings**

Parameter	Description	Min	Max
V <sub>CC_CORE</sub>	Processor core voltage supply	-0.5 V	V <sub>CC_CORE</sub> Max + 0.5 V
V <sub>CCA</sub>	Processor PLL voltage supply	-0.5 V	V <sub>CCA</sub> Max + 0.5 V
V <sub>PIN</sub>	Voltage on any signal pin	-0.5 V	V <sub>CC_CORE</sub> Max + 0.5 V
T <sub>STORAGE</sub>	Storage temperature of processor	-40°C	100°C

## 7.9 SYSCLK and SYSCLK# AC and DC Characteristics

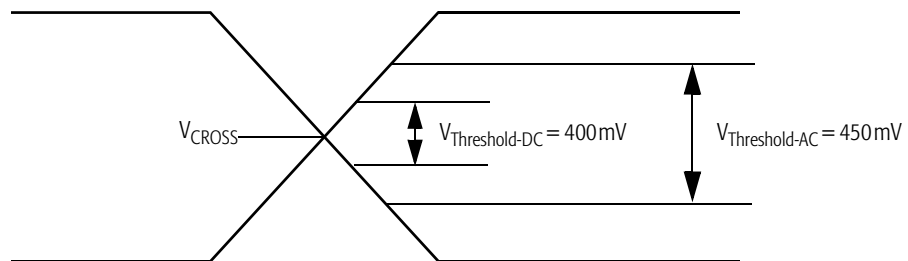
Table 8 shows the DC characteristics of the SYSCLK and SYSCLK# differential clocks. The SYSCLK signal represents CLKIN and RSTCLK tied together while the SYSCLK# signal represents CLKIN# and RSTCLK# tied together.

**Table 8. SYSCLK and SYSCLK# DC Characteristics**

Symbol	Description	Min	Max	Units
$V_{\text{Threshold-DC}}$	Crossing before transition is detected (DC)	400		mV
$V_{\text{Threshold-AC}}$	Crossing before transition is detected (AC)	450		mV
$I_{\text{LEAK\_P}}$	Leakage current through P-channel pullup to $V_{\text{CC\_CORE}}$	-1		mA
$I_{\text{LEAK\_N}}$	Leakage current through N-channel pulldown to VSS (Ground)		1	mA
$V_{\text{CROSS}}$	Differential signal crossover		$V_{\text{CC\_CORE}}/2 \pm 100$	mV
$C_{\text{PIN}}$	Capacitance *	4	25 *	pF

**Note:**  
 \* The following processor inputs have twice the listed capacitance because they connect to two input pads—SYSCLK and SYSCLK#. SYSCLK connects to CLKIN/RSTCLK. SYSCLK# connects to CLKIN#/RSTCLK#.

Figure 8 shows the DC characteristics of the SYSCLK and SYSCLK# signals.



**Figure 8. SYSCLK and SYSCLK# Differential Clock Signals**

Table 9 shows the SYSCLK/SYSCLK# differential clock AC characteristics of the AMD Athlon MP processor model 10.

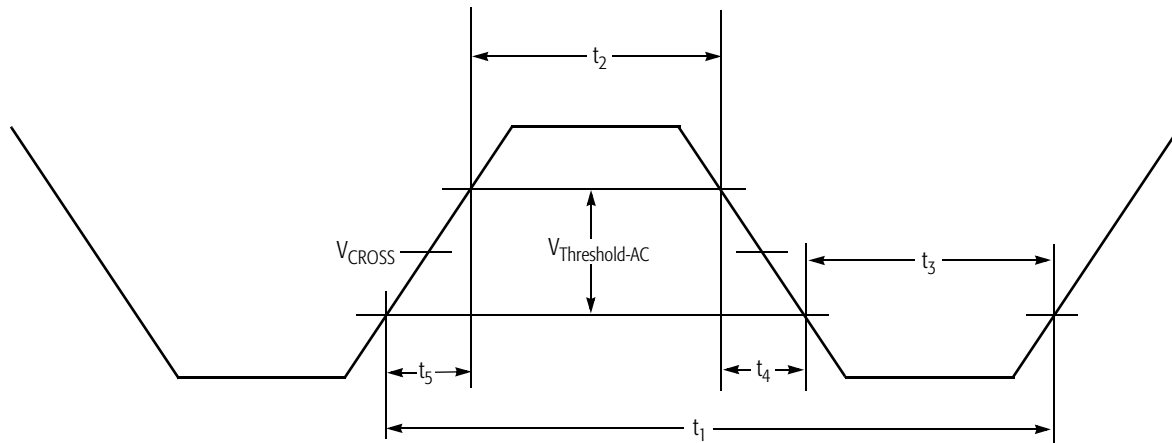
**Table 9. SYSCLK and SYSCLK# AC Characteristics**

Symbol	Parameter Description	Minimum	Maximum	Units	Notes
	Clock Frequency	50	133	MHz	1
	Duty Cycle	30%	70%		
$t_1$	Period	7.5		ns	2, 3
$t_2$	High Time	1.05		ns	
$t_3$	Low Time	1.05		ns	
$t_4$	Fall Time		2	ns	
$t_5$	Rise Time		2	ns	
	Period Stability		$\pm 300$	ps	

**Notes:**

1. The AMD Athlon™ system bus operates at twice the front-side bus (FSB) frequency shown here.
2. Circuitry driving the AMD Athlon system bus clock inputs must exhibit a suitably low closed-loop jitter bandwidth to allow the PLL to track the jitter. The  $-20\text{dB}$  attenuation point, as measured into a 20- or 30-pF load must be less than 500 kHz.
3. Circuitry driving the AMD Athlon system bus clock inputs may purposely alter the AMD Athlon system bus clock frequency (spread spectrum clock generators). In no cases can the AMD Athlon system bus period violate the minimum specification above. AMD Athlon system bus clock inputs can vary from 100% of the specified frequency to 99% of the specified frequency at a maximum rate of 100 kHz.

Figure 9 shows a sample waveform of the SYSCLK signal.



**Figure 9. SYSCLK Waveform**

## 7.10 AMD Athlon™ System Bus AC and DC Characteristics

Table 10 shows the DC characteristics of the AMD Athlon system bus used by the AMD Athlon MP processor model 10. See Table 6, “ $V_{CC\_CORE}$  AC and DC Characteristics,” on page 28 for information on  $T_{DIE}$  and  $V_{CC\_CORE}$ . For information about SYSCLK and SYSCLK#, see “SYSCLK and SYSCLK#” on page 75 and Table 19, “Pin Name Abbreviations,” on page 54.

**Table 10. AMD Athlon™ System Bus DC Characteristics**

Symbol	Parameter	Condition	Min	Max	Units	Notes
$V_{REF}$	DC Input Reference Voltage		$(0.5 \times V_{CC\_CORE})$ -50	$(0.5 \times V_{CC\_CORE})$ +50	mV	1
$I_{VREF\_LEAK\_P}$	$V_{REF}$ Tristate Leakage Pullup	$V_{IN} = V_{REF}$ Nominal	-100		$\mu$ A	
$I_{VREF\_LEAK\_N}$	$V_{REF}$ Tristate Leakage Pulldown	$V_{IN} = V_{REF}$ Nominal		100	$\mu$ A	
$V_{IH}$	Input High Voltage		$V_{REF} + 200$	$V_{CC\_CORE} + 500$	mV	
$V_{IL}$	Input Low Voltage		-500	$V_{REF} - 200$	mV	
$I_{LEAK\_P}$	Tristate Leakage Pullup	$V_{IN} = V_{SS}$ (Ground)	-1		mA	
$I_{LEAK\_N}$	Tristate Leakage Pulldown	$V_{IN} = V_{CC\_CORE}$ Nominal		1	mA	
$C_{IN}$	Input Pin Capacitance		4	7	pF	
$R_{ON}$	Output Resistance		$0.90 \times R_{setN,P}$	$1.1 \times R_{setN,P}$	$\Omega$	2
$R_{setP}$	Impedance Set Point, P Channel		40	70	$\Omega$	2
$R_{setN}$	Impedance Set Point, N Channel		40	70	$\Omega$	2

**Notes:**

- $V_{REF}$  is nominally set to 50% of  $V_{CC\_CORE}$  with actual values that are specific to motherboard design implementation.  $V_{REF}$  must be created with a sufficiently accurate DC source and a sufficiently quiet AC response to adhere to the  $\pm 50$  mV specification listed above.
- Measured at  $V_{CC\_CORE} / 2$ .

The AC characteristics of the AMD Athlon system bus are shown in Table 11 on page 34. The parameters are grouped based on the source or destination of the signals involved.

**Table 11. AMD Athlon™ System Bus AC Characteristics**

Group	Symbol	Parameter	Min	Max	Units	Notes
All Signals	$T_{RISE}$	Output Rise Slew Rate	1	3	V/ns	1
	$T_{FALL}$	Output Fall Slew Rate	1	3	V/ns	1
Forward Clocks	$T_{SKEW-SAMEEDGE}$	Output skew with respect to the same clock edge	–	385	ps	2
	$T_{SKEW-DIFFEDGE}$	Output skew with respect to a different clock edge	–	770	ps	2
	$T_{SU}$	Input Data Setup Time	300		ps	3
	$T_{HD}$	Input Data Hold Time	300		ps	3
	$C_{IN}$	Capacitance on input clocks	4	25	pF	
	$C_{OUT}$	Capacitance on output clocks	4	12	pF	
Sync	$T_{VAL}$	RSTCLK to Output Valid	250	2000	ps	4, 5
	$T_{SU}$	Setup to RSTCLK	500		ps	4, 6
	$T_{HD}$	Hold from RSTCLK	1000		ps	4, 6

**Notes:**

1. Rise and fall time ranges are guidelines over which the I/O has been characterized.
2.  $T_{SKEW-SAMEEDGE}$  is the maximum skew within a clock forwarded group between any two signals or between any signal and its forward clock, as measured at the package, with respect to the same clock edge.  
 $T_{SKEW-DIFFEDGE}$  is the maximum skew within a clock forwarded group between any two signals or between any signal and its forward clock, as measured at the package, with respect to different clock edges.
3. Input SU and HD times are with respect to the appropriate Clock Forward Group input clock.
4. The synchronous signals include PROCRDY, CONNECT, and CLKFWRDST.
5.  $T_{VAL}$  is RSTCLK rising edge to output valid for PROCRDY. Test Load is 25 pF.
6.  $T_{SU}$  is setup of CONNECT/CLKFWRDST to rising edge of RSTCLK.  $T_{HD}$  is hold of CONNECT/CLKFWRDST from rising edge of RSTCLK.

## 7.11 General AC and DC Characteristics

Table 12 shows the AMD Athlon MP processor model 10 AC and DC characteristics of the Southbridge, JTAG, test, and miscellaneous pins.

**Table 12. General AC and DC Characteristics**

Symbol	Parameter Description	Condition	Min	Max	Units	Notes
V <sub>IH</sub>	Input High Voltage		(V <sub>CC_CORE</sub> /2) + 200 mV	V <sub>CC_CORE</sub> + 300 mV	V	1, 2
V <sub>IL</sub>	Input Low Voltage		-300	350	mV	1, 2
V <sub>OH</sub>	Output High Voltage		V <sub>CC_CORE</sub> - 400	V <sub>CC_CORE</sub> + 300	mV	
V <sub>OL</sub>	Output Low Voltage		-300	400	mV	
I <sub>LEAK_P</sub>	Tristate Leakage Pullup	V <sub>IN</sub> = VSS (Ground)	-1		mA	
I <sub>LEAK_N</sub>	Tristate Leakage Pulldown	V <sub>IN</sub> = V <sub>CC_CORE</sub> Nominal		600	μA	
I <sub>OH</sub>	Output High Current			-6	mA	3
I <sub>OL</sub>	Output Low Current		6		mA	3
T <sub>SU</sub>	Sync Input Setup Time		2.0		ns	4, 5
T <sub>HD</sub>	Sync Input Hold Time		0.0		ps	4, 5

**Notes:**

1. Characterized across DC supply voltage range.
2. Values specified at nominal V<sub>CC\_CORE</sub>. Scale parameters between V<sub>CC\_CORE</sub> minimum and V<sub>CC\_CORE</sub> maximum.
3. I<sub>OL</sub> and I<sub>OH</sub> are measured at V<sub>OL</sub> maximum and V<sub>OH</sub> minimum, respectively.
4. Synchronous inputs/outputs are specified with respect to RSTCLK and RSTCK# at the pins.
5. These are aggregate numbers.
6. Edge rates indicate the range over which inputs were characterized.
7. In asynchronous operation, the signal must persist for this time to enable capture.
8. This value assumes RSTCLK period is 10 ns ⇒ TBIT = 2\*fRST.
9. The approximate value for standard case in normal mode operation.
10. This value is dependent on RSTCLK frequency, divisors, Low Power mode, and core frequency.
11. Reassertions of the signal within this time are not guaranteed to be seen by the core.
12. This value assumes that the skew between RSTCLK and K7CLKOUT is much less than one phase.
13. This value assumes RSTCLK and K7CLKOUT are running at the same frequency, though the processor is capable of other configurations.
14. Time to valid is for any open-drain pins. See requirements 7 and 8 in the "Power-Up Timing Requirements" chapter for more information.

Table 12. General AC and DC Characteristics (Continued)

Symbol	Parameter Description	Condition	Min	Max	Units	Notes
T <sub>DELAY</sub>	Output Delay with respect to RSTCLK		0.0	6.1	ns	5
T <sub>BIT</sub>	Input Time to Acquire		20.0		ns	7, 8
T <sub>RPT</sub>	Input Time to Reacquire		40.0		ns	9–13
T <sub>RISE</sub>	Signal Rise Time		1.0	3.0	V/ns	6
T <sub>FALL</sub>	Signal Fall Time		1.0	3.0	V/ns	6
C <sub>PIN</sub>	Pin Capacitance		4	12	pF	
T <sub>VALID</sub>	Time to data valid			100	ns	14

**Notes:**

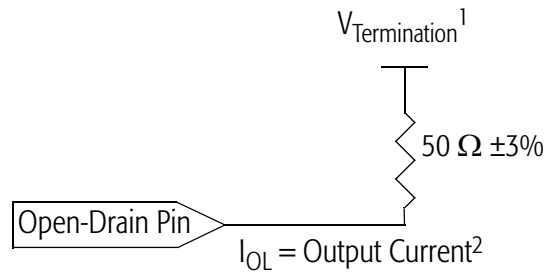
1. Characterized across DC supply voltage range.
2. Values specified at nominal V<sub>CC\_CORE</sub>. Scale parameters between V<sub>CC\_CORE</sub> minimum and V<sub>CC\_CORE</sub> maximum.
3. I<sub>OL</sub> and I<sub>OH</sub> are measured at V<sub>OL</sub> maximum and V<sub>OH</sub> minimum, respectively.
4. Synchronous inputs/outputs are specified with respect to RSTCLK and RSTCK# at the pins.
5. These are aggregate numbers.
6. Edge rates indicate the range over which inputs were characterized.
7. In asynchronous operation, the signal must persist for this time to enable capture.
8. This value assumes RSTCLK period is 10 ns ⇒ T<sub>BIT</sub> = 2\*f<sub>RST</sub>.
9. The approximate value for standard case in normal mode operation.
10. This value is dependent on RSTCLK frequency, divisors, Low Power mode, and core frequency.
11. Reassertions of the signal within this time are not guaranteed to be seen by the core.
12. This value assumes that the skew between RSTCLK and K7CLKOUT is much less than one phase.
13. This value assumes RSTCLK and K7CLKOUT are running at the same frequency, though the processor is capable of other configurations.
14. Time to valid is for any open-drain pins. See requirements 7 and 8 in the "Power-Up Timing Requirements" chapter for more information.



## 7.12 Open Drain Test Circuit

Figure 10 is a test circuit that may be used on automated test equipment (ATE) to test for validity on open drain pins.

Refer to Table 12, “General AC and DC Characteristics,” on page 35 for timing requirements.



Notes:

1.  $V_{Termination} = 1.2\text{ V}$  for VID and FID pins  
 $V_{Termination} = 1.0\text{ V}$  for APIC pins
2.  $I_{OL} = -6\text{ mA}$  for VID and FID pins  
 $I_{OL} = -9\text{ mA}$  for APIC pins

**Figure 10. General ATE Open-Drain Test Circuit**

## 7.13 Thermal Diode Characteristics

The AMD Athlon MP processor model 10 provides a diode that can be used in conjunction with an external temperature sensor to determine the die temperature of the processor. The diode anode (THERMDA) and cathode (THERMDC) are available as pins on the processor, as described in “THERMDA and THERMDC Pins” on page 75.

For information about thermal design for the AMD Athlon MP processor model 10, including layout and airflow considerations, see the *AMD Processor Thermal, Mechanical, and Chassis Cooling Design Guide*, order# 23794, and the cooling guidelines on <http://www.amd.com>.

### Thermal Diode Electrical Characteristics

Table 13 shows the AMD Athlon MP processor model 10 characteristics of the on-board thermal diode. For information about calculations for the ideal diode equation and temperature offset correction, see Appendix A, “Thermal Diode Calculations” on page 79.

**Table 13. Thermal Diode Electrical Characteristics**

Symbol	Parameter Description	Min	Nom	Max	Units	Notes
I	Sourcing current	5		300	μA	1
$\eta_f$ , lumped	Lumped ideality factor	1.00000	1.00374	1.00900		2, 3, 4
$\eta_f$ , actual	Actual ideality factor		1.00261			3, 4
$R_T$	Series Resistance		0.93		Ω	3, 4
<b>Notes:</b> <ol style="list-style-type: none"> <li>1. The sourcing current should always be used in forward bias only.</li> <li>2. Characterized at 95°C with a forward bias current pair of 10 μA and 100 μA. AMD recommends using a minimum of two sourcing currents to accurately measure the temperature of the thermal diode.</li> <li>3. Not 100% tested. Specified by design and limited characterization.</li> <li>4. The lumped ideality factor adds the effect of the series resistance term to the actual ideality factor. The series resistance term indicates the resistance from the pins of the processor to the on-die thermal diode. The value of the lumped ideality factor depends on the sourcing current pair used.</li> </ol>						

### Thermal Protection Characterization

The following section describes parameters relating to thermal protection. The implementation of thermal control circuitry to control processor temperature is left to the manufacturer to determine how to implement.

Thermal limits in motherboard design are necessary to protect the processor from thermal damage.  $T_{\text{SHUTDOWN}}$  is the temperature for thermal protection circuitry to initiate shutdown of the processor.  $T_{\text{SD\_DELAY}}$  is the maximum time allowed from the detection of the over-temperature condition to processor shutdown to prevent thermal damage to the processor.

Systems that do not implement thermal protection circuitry or that do not react within the time specified by  $T_{\text{SD\_DELAY}}$  can cause thermal damage to the processor during a fan failure or if the processor is powered up without a heat-sink. The processor relies on thermal circuitry on the motherboard to turn off the regulated core voltage to the processor in response to a thermal shutdown event.

Thermal protection circuitry reference designs and thermal solution guidelines are found in the following documents:

- *AMD Athlon™ Processor-Based Motherboard Design Guide*, order# 24363
- *AMD Thermal, Mechanical, and Chassis Cooling Design Guide*, order# 23794
- <http://www1.amd.com/products/athlon/thermals>

Table 14 shows the  $T_{\text{SHUTDOWN}}$  and  $T_{\text{SD\_DELAY}}$  specifications for circuitry in motherboard design necessary for thermal protection of the processor.

**Table 14. Guidelines for Platform Thermal Protection of the Processor**

Symbol	Parameter Description	Max	Units	Notes
$T_{\text{SHUTDOWN}}$	Thermal diode shutdown temperature for processor protection	125	°C	1, 2, 3
$T_{\text{SD\_DELAY}}$	Maximum allowed time from $T_{\text{SHUTDOWN}}$ detection to processor shutdown	500	ms	1, 3
<p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>1. The thermal diode is not 100% tested, it is specified by design and limited characterization.</li> <li>2. The thermal diode is capable of responding to thermal events of 40°C/s or faster.</li> <li>3. The AMD Athlon™ MP processor model 10 provides a thermal diode for measuring die temperature of the processor. The processor relies on thermal circuitry on the motherboard to turn off the regulated core voltage to the processor in response to a thermal shutdown event. Refer to AMD Athlon™ Processor-Based Motherboard Design Guide, order# 24363, for thermal protection circuitry designs.</li> </ol>				

## 7.14 APIC Pins AC and DC Characteristics

Table 15 shows the AMD Athlon MP processor model 10 AC and DC characteristics of the APIC pins.

**Table 15. APIC Pin AC and DC Characteristics**

Symbol	Parameter Description	Condition	Min	Max	Units	Notes
V <sub>IH</sub>	Input High Voltage		1.7	2.625	V	1, 2
		V <sub>CC_CORE</sub> < V <sub>CC_CORE_MAX</sub>		V <sub>IH</sub> - V <sub>CC_CORE</sub>   ≤ 1.60 V	V	3
V <sub>IL</sub>	Input Low Voltage		-300	700	mV	1
V <sub>OH</sub>	Output High Voltage			2.625	V	2
		V <sub>CC_CORE</sub> < V <sub>CC_CORE_MAX</sub>		V <sub>OH</sub> - V <sub>CC_CORE</sub>   ≤ 1.60 V	V	3
V <sub>OL</sub>	Output Low Voltage		-300	400	mV	
I <sub>LEAK_P</sub>	Tristate Leakage Pullup	V <sub>IN</sub> = VSS (Ground)	-1		mA	
I <sub>LEAK_N</sub>	Tristate Leakage Pulldown	V <sub>IN</sub> = 2.5 V		1	mA	
I <sub>OL</sub>	Output Low Current	V <sub>OL</sub> Max	9		mA	
T <sub>RISE</sub>	Signal Rise Time		1.0	3.0	V/ns	3
T <sub>FALL</sub>	Signal Fall Time		1.0	3.0	V/ns	3
T <sub>SU</sub>	Setup Time		1		ns	
T <sub>HD</sub>	Hold Time		1		ns	
C <sub>PIN</sub>	Pin Capacitance		4	12	pF	

**Notes:**

1. Characterized across DC supply voltage range.
2. The 2.625-V value is equal to 2.5 V plus a maximum of five percent.
3. Refer to "VCC\_2.5V Generation Circuit" found in the section, "Motherboard Required Circuits," of the AMD Athlon™ Processor-Based Motherboard Design Guide, order# 24363.
4. Edge rates indicate the range for characterizing the inputs.

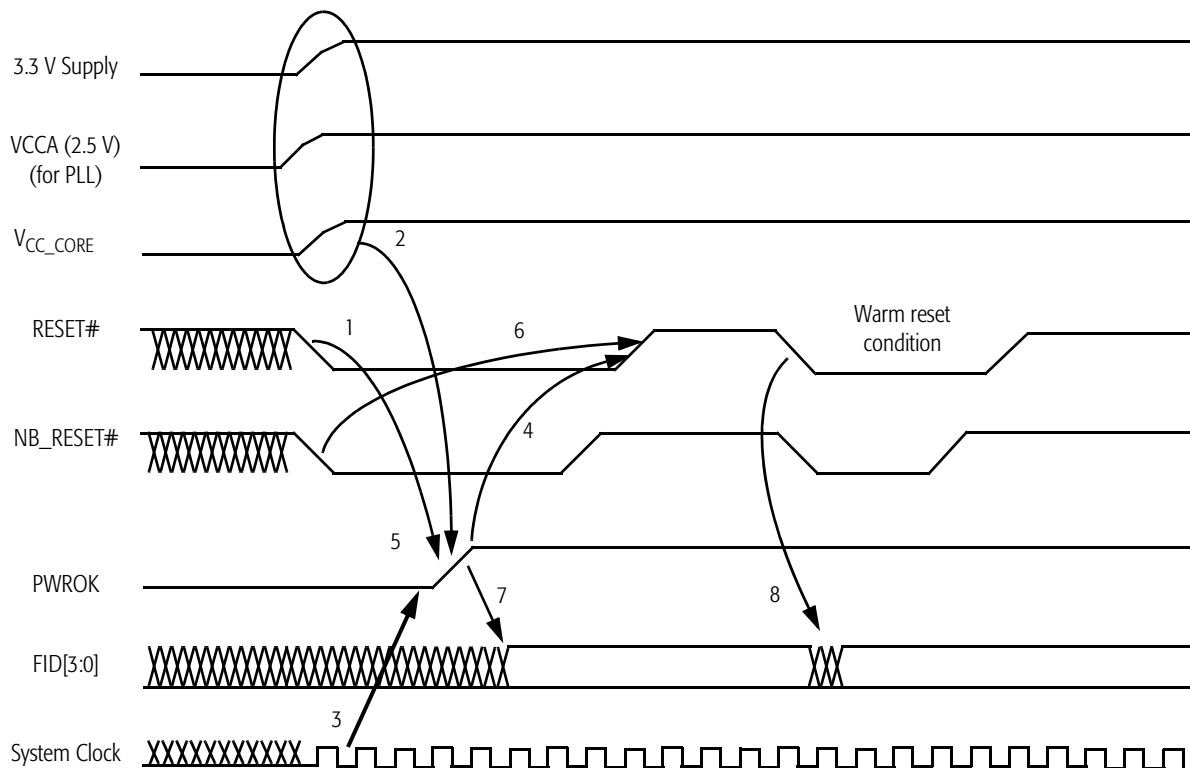
## 8 Signal and Power-Up Requirements

The AMD Athlon™ MP processor model 10 is designed to provide functional operation if the voltage and temperature parameters are within the limits of normal operating ranges.

### 8.1 Power-Up Requirements

#### Signal Sequence and Timing Description

Figure 11 shows the relationship between key signals in the system during a power-up sequence. This figure details the requirements of the processor.



**Figure 11. Signal Relationship Requirements During Power-Up Sequence**

- Notes:**
- Figure 11 represents several signals generically by using names not necessarily consistent with any pin lists or schematics.
  - Requirements 1–8 in Figure 11 are described in “Power-Up Timing Requirements” on page 42.

**Power-Up Timing Requirements.** The signal timing requirements are as follows:

1. RESET# must be asserted before PWROK is asserted.

The AMD Athlon MP processor model 10 does not set the correct clock multiplier if PWROK is asserted prior to a RESET# assertion. It is recommended that RESET# be asserted at least **10 nanoseconds** prior to the assertion of PWROK.

In practice, a Southbridge asserts RESET# milliseconds before PWROK is asserted.

2. All motherboard voltage planes must be within specification before PWROK is asserted.

PWROK is an output of the voltage regulation circuit on the motherboard. PWROK indicates that  $V_{CC\_CORE}$  and all other voltage planes in the system are within specification.

The motherboard is required to delay PWROK assertion for a minimum of three milliseconds from the 3.3 V supply being within specification. This delay ensures that the system clock (SYSCLK/SYSCLK#) is operating within specification when PWROK is asserted.

The processor core voltage,  $V_{CC\_CORE}$ , must be within specification as dictated by the VID[4:0] pins driven by the processor before PWROK is asserted. Before PWROK assertion, the AMD Athlon MP processor is clocked by a ring oscillator.

The processor PLL is powered by VCCA. The processor PLL does not lock if VCCA is not high enough for the processor logic to switch for some period before PWROK is asserted. VCCA must be within specification at least five microseconds before PWROK is asserted.

In practice VCCA,  $V_{CC\_CORE}$ , and all other voltage planes must be within specification for several milliseconds before PWROK is asserted.

After PWROK is asserted, the processor PLL locks to its operational frequency.

3. The system clock (SYSCLK/SYSCLK#) must be running before PWROK is asserted.

When PWROK is asserted, the processor switches from driving the internal processor clock grid from the ring oscillator to driving from the PLL. The reference system

clock must be valid at this time. The system clocks are designed to be running after 3.3 V has been within specification for three milliseconds.

4. PWROK assertion to deassertion of RESET#

The duration of RESET# assertion during cold boots is intended to satisfy the time it takes for the PLL to lock with a less than 1 ns phase error. The processor PLL begins to run after PWROK is asserted and the internal clock grid is switched from the ring oscillator to the PLL. The PLL lock time may take from hundreds of nanoseconds to tens of microseconds. It is recommended that the minimum time between PWROK assertion to the deassertion of RESET# be at least **1.0 milliseconds**. Southbridges enforce a delay of 1.5 to 2.0 milliseconds between PWRGD (Southbridge version of PWROK) assertion and NB\_RESET# deassertion.

5. PWROK must be monotonic and meet the timing requirements as defined in Table 12, “General AC and DC Characteristics,” on page 35. The processor should not switch between the ring oscillator and the PLL after the initial assertion of PWROK.

6. NB\_RESET# must be asserted (causing CONNECT to also assert) before RESET# is deasserted. In practice all Southbridges enforce this requirement.

If NB\_RESET# does not assert until after RESET# has deasserted, the processor misinterprets the CONNECT assertion (due to NB\_RESET# being asserted) as the beginning of the SIP transfer. There must be sufficient overlap in the resets to ensure that CONNECT is sampled asserted by the processor before RESET# is deasserted.

7. The FID[3:0] signals are valid within 100 ns after PWROK is asserted. The chipset must not sample the FID[3:0] signals until they become valid. Refer to the *AMD Athlon™ Processor-Based Motherboard Design Guide*, order# 24363, for the specific implementation and additional circuitry required.

8. The FID[3:0] signals become valid within 100 ns after RESET# is asserted. Refer to the *AMD Athlon™ Processor-Based Motherboard Design Guide*, order# 24363, for the specific implementation and additional circuitry required.

**Clock Multiplier Selection (FID[3:0])**

The chipset samples the FID[3:0] signals in a chipset-specific manner from the processor and uses this information to determine the correct serial initialization packet (SIP). The chipset then sends the SIP information to the processor for configuration of the AMD Athlon system bus for the clock multiplier that determines the processor frequency indicated by the FID[3:0] code. The SIP is sent to the processor using the SIP protocol. This protocol uses the PROCRDY, CONNECT, and CLKFWDRST signals, that are synchronous to SYSCLK.

For more information about FID[3:0], see “FID[3:0] Pins” on page 71.

**Serial Initialization Packet (SIP) Protocol.** Refer to *AMD Athlon™ and AMD Duron™ System Bus Specification*, order# 21902 for details of the SIP protocol.

## 8.2 Processor Warm Reset Requirements

**Northbridge Reset Pins**

RESET# cannot be asserted to the processor without also being asserted to the Northbridge. RESET# to the Northbridge is the same as PCI RESET#. The minimum assertion for PCI RESET# is one millisecond. Southbridges enforce a minimum assertion of RESET# for the processor, Northbridge, and PCI of 1.5 to 2.0 milliseconds.



## 9 Mechanical Data

The AMD Athlon™ MP processor model 10 connects to the motherboard through a Pin Grid Array (PGA) socket named Socket A. This processor utilizes the Organic Pin Grid Array (OPGA) package type described in this chapter. For more information, see the *AMD Athlon™ Processor-Based Motherboard Design Guide*, order# 24363.

### 9.1 Die Loading

The processor die on the OPGA package is exposed at the top of the package. This feature facilitates heat transfer from the die to an approved heat sink. Any heat sink design should avoid loads on corners and edges of die. The OPGA package has compliant pads that serve to bring surfaces in planar contact. Tool-assisted zero insertion force sockets should be designed so that no load is placed on the ceramic substrate of the package.

Table 16 shows the mechanical loading specifications for the processor die. It is critical that the mechanical loading of the heat sink does not exceed the limits shown in Table 16.

**Table 16. Mechanical Loading**

Location	Dynamic (MAX)	Static (MAX)	Units	Note
Die Surface	100	30	lbf	1
Die Edge	10	10	lbf	2
<b>Notes:</b>				
1. Load specified for coplanar contact to die surface.				
2. Load defined for a surface at no more than a two-degree angle of inclination to die surface.				

## 9.2 AMD Athlon™ MP Processor Model 10 Part Number 27488 OPGA Package Dimensions

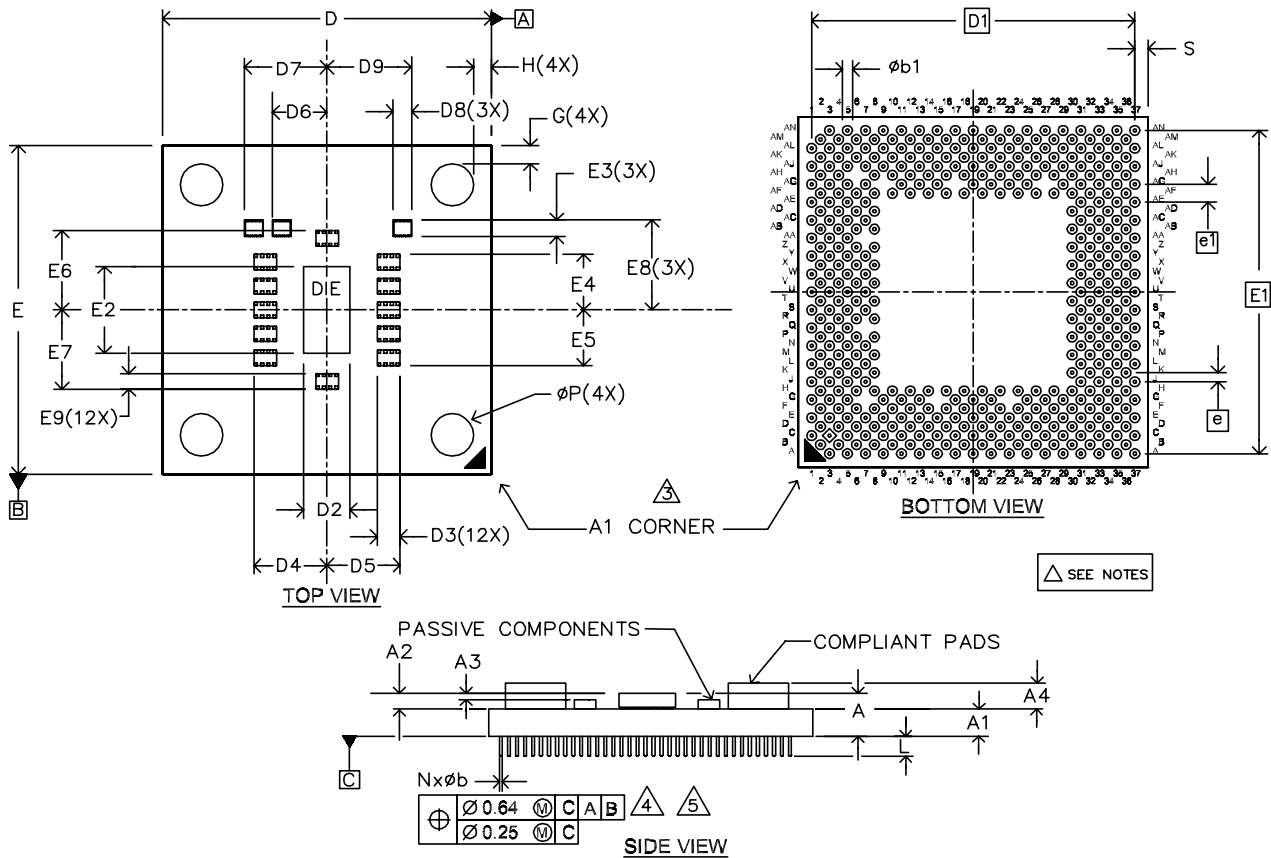
Table 17 shows the part number 27488 OPGA package dimensions in millimeters assigned to the letters and symbols used in the 27488 package diagram, Figure 12 on page 47.

**Table 17. Dimensions for the AMD Athlon™ MP Processor Model 10 Part Number 27488 OPGA Package**

Letter or Symbol	Minimum Dimension <sup>1</sup>	Maximum Dimension <sup>1</sup>	Letter or Symbol	Minimum Dimension <sup>1</sup>	Maximum Dimension <sup>1</sup>
D/E	49.27	49.78	E9	1.66	1.96
D1/E1	45.72 BSC		G/H	–	4.50
D2	7.42 REF		A	1.942 REF	
D3	3.30	3.60	A1	1.00	1.20
D4	10.78	11.33	A2	0.80	0.88
D5	10.78	11.33	A3	0.116	–
D6	8.13	8.68	A4	–	1.90
D7	12.33	12.88	φP	–	6.60
D8	3.05	3.35	φb	0.43	0.50
D9	12.71	13.26	φb1	1.40 REF	
E2	13.61 REF		S	1.435	2.375
E3	2.35	2.65	L	3.05	3.31
E4	7.87	8.42	M	37	
E5	7.87	8.42	N	453	
E6	11.41	11.96	e	1.27 BSC	
E7	11.41	11.96	e1	2.54 BSC	
E8	13.28	13.83	Mass <sup>2</sup>	11.0 g REF	

**Note:**

1. Dimensions are given in millimeters.
2. The mass consists of the completed package, including processor, surface mounted parts and pins.



GENERAL NOTES

1. All dimensions are specified in millimeters (mm).
2. Dimensioning and tolerancing per ASME-Y14.5M-1994.
3. This corner is marked with a triangle on both sides of the package to identify the pin A1 corner for orientation purposes.
4. Symbol "M" determines pin matrix size and "N" is number of pins.
5. Dimension "b" is measured at maximum solder pin diameter on a plane parallel to datum C.

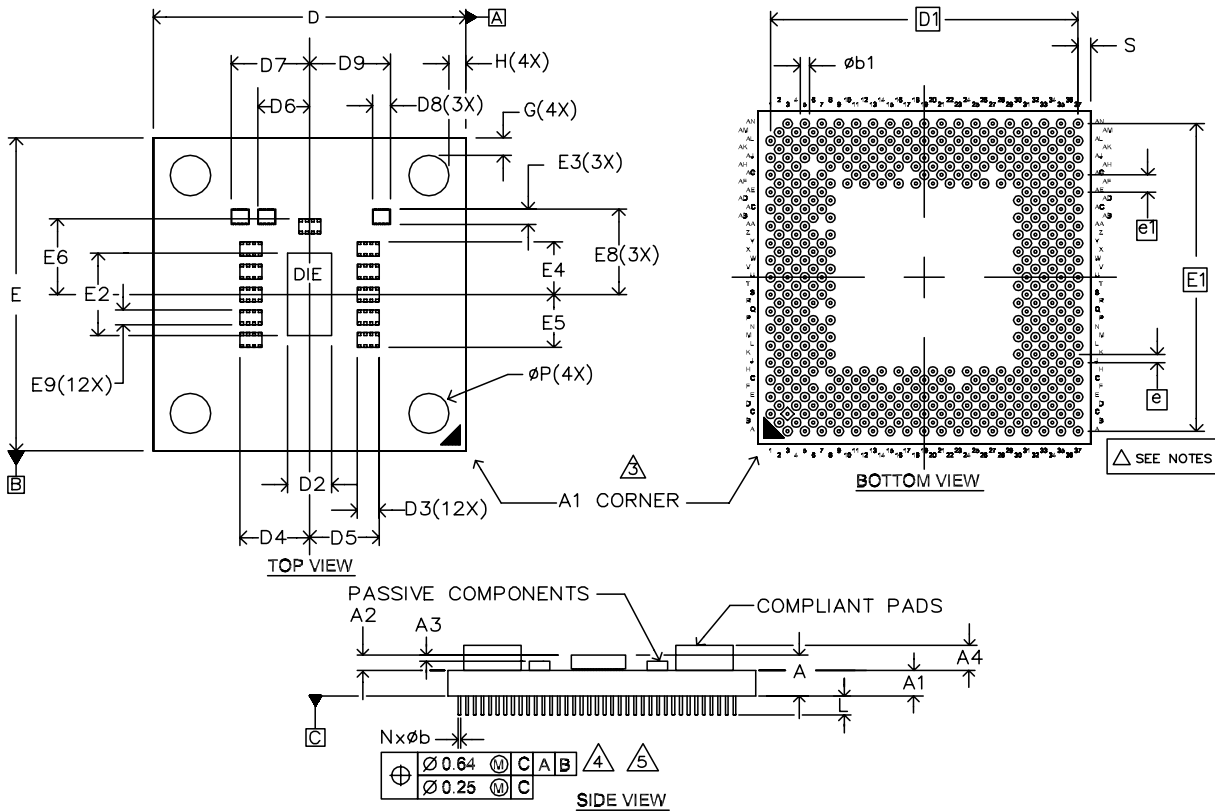
Figure 12. AMD Athlon™ MP Processor Model 10 Part Number 27488 OPGA Package Diagram

### 9.3 AMD Athlon™ MP Processor Model 10 Part Number 27493 OPGA Package Dimensions

Table 18 shows the part number 27493 OPGA package dimensions in millimeters assigned to the letters and symbols shown in the 27493 package diagram, Figure 13 on page 49.

**Table 18. Dimensions for the AMD Athlon™ MP Processor Model 10 Part Number 27493 OPGA Package**

Letter or Symbol	Minimum Dimension <sup>1</sup>	Maximum Dimension <sup>1</sup>	Letter or Symbol	Minimum Dimension <sup>1</sup>	Maximum Dimension <sup>1</sup>
D/E	49.27	49.78	G/H	–	4.50
D1/E1	45.72 BSC		A	1.917 REF	
D2	7.42 REF		A1	0.977	1.177
D3	3.30	3.60	A2	0.80	0.88
D4	10.78	11.33	A3	0.116	–
D5	10.78	11.33	A4	–	1.90
D6	8.13	8.68	φP	–	6.60
D7	12.33	12.88	φb	0.43	0.50
D8	3.05	3.35	φb1	1.40 REF	
D9	12.71	13.26	S	1.435	2.375
E2	13.61 REF		L	3.05	3.31
E3	2.35	2.65	M	37	
E4	7.87	8.42	N	453	
E5	7.87	8.42	e	1.27 BSC	
E6	11.41	11.96	e1	2.54 BSC	
E8	13.28	13.83	Mass <sup>2</sup>	11.0 g REF	
E9	1.66	1.96			
<b>Note:</b>					
1. Dimensions are given in millimeters.					
2. The mass consists of the completed package, including processor, surface mounted parts and pins.					



GENERAL NOTES

1. All dimensions are specified in millimeters (mm).
2. Dimensioning and tolerancing per ASME-Y14.5M-1994.
3.  $\triangle$  This corner is marked with a triangle on both sides of the package identifies pin A1 corner and can be used for handling and orientation purposes.
4.  $\triangle$  Symbol "M" determines pin matrix size and "N" is number of pins.
5.  $\triangle$  Dimension "b" is measured at maximum solder pin diameter on a plane parallel to datum C.
6.  $\triangle$  "x" in front of package variation denotes non-qualified package per AMD 01-002.3.
7. The following features are not shown on drawings:
  - a) Marking on die, label on package
  - b) Laser elements, ink swatch
  - c) Die and passive fudicials
8. The die is centered on the package.

Figure 13. AMD Athlon™ MP Processor Model 10 Part Number 27493 OPGA Package Diagram



## 10 Pin Descriptions

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This chapter includes pin diagrams of the organic pin grid array (OPGA) for the AMD Athlon™ MP processor model 10, a listing of pin name abbreviations, a cross-referenced listing of pin locations to signal names, and detailed pin descriptions.

### 10.1 Pin Diagram and Pin Name Abbreviations

Figure 14 on page 52 shows the staggered Pin Grid Array (PGA) for the AMD Athlon MP processor model 10. Because some of the pin names are too long to fit in the grid, they are abbreviated. Figure 15 on page 53 shows the bottomside view of the array. Table 19 on page 54 lists all the pins in alphabetical order by pin name, along with the abbreviation where necessary.





	A	B	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T	U	V	W	X	Y	Z	AA	AB	AC	AD	AE	AF	AG	AH	AJ	AK	AL	AM	AN	
1			SAOP7		SAOP11		SAOP10		SAOP0		VID[0]		PICCLK		TCK		SCLOCK		TDI		FID[0]		FDI[2]							FERR		IGNH#		INH#				1
2			VSS		VCC		VSS		VSS		VSS		VCC		VSS		VCC		TRST#		VCC		VSS							VCC		VSS		FLUSH#		VCC		2
3	SAOP12	SAOP9	SAOP9		SAOP#		SAOP14		SAOP1		VID[1]		PICOP0		TMS		SCINH		TRST#		FID[1]		FDI[3]						RESET#		INT#						3	
4			VCC		VCC		VSS		VCC		VSS		VCC		VSS		VSS				VCC		VSS						VCC		VSS		VSS		VSS		4	
5	SAOP5	SAOP8	SAOP8		SAOP4		SAOP3		IC		VID[2]		PICOP1		SCINH		SCLOCK2		TDI		VCC		NC						IC		VCC		VCC		VCC		5	
6			VSS		VSS		VSS		VSS		VSS		VCC		VCC		VSS				VCC		VCC						KEY		AMD		CPH#		VCC		6	
7	SAOP3	SAOP2	SAOP2		SAOP6		KEY		VIDE4]		VID[3]		KEY		KEY		THDA		THOC		IC		KEY						KEY		NC		IC		IC		7	
8			VCC		VCC		IC		IC		IC		VCC		VSS		VSS				VCC		VSS						IC		IC		IC		IC		8	
9	SOH55		SOH54		SOH52		KEY																						KEY		NC		IC		IC		9	
10			VSS		VSS		VSS		IC																				IC		VCC		VCC		VCC		10	
11	SOH61		SOH63		SOH50		IC																						IC		IC		IC		IC		11	
12			VCC		VCC		VCC																						VCC		VSS		VSS		VSS		12	
13	SOH53		SOH66		SOH49		IC																						IC		PLM#2		PLM#1		VCC		13	
14			VSS		VSS		VSS																						VCC		VCC		VCC		VCC		14	
15	SOH63		SOH51		SOH63		KEY																						VSS		VSS		VSS		VSS		15	
16			VCC		VCC		VCC																						VSS		VSS		VSS		VSS		16	
17	SOH62		SOH60		SOH48		KEY																						VCC		VCC		VCC		VCC		17	
18			VSS		VSS		VSS																						VSS		VSS		VSS		VSS		18	
19	SOH67		SOH59		SOH58		IC																						VCC		VCC		VCC		VCC		19	
20			VCC		VCC		VCC																						VSS		VSS		VSS		VSS		20	
21	SOH57		SOH56		SOH66		IC																						VCC		VCC		VCC		VCC		21	
22			VSS		VSS		VSS																						VCC		VCC		VCC		VCC		22	
23	SOH59		SOH87		SOH46		KEY																						VCC		VCC		VCC		VCC		23	
24			VCC		VCC		VCC																						VSS		VSS		VSS		VSS		24	
25	SOH35		SOH47		SOH44		KEY																						VCC		VCC		VCC		VCC		25	
26			VSS		VSS		VSS																						VCC		VCC		VCC		VCC		26	
27	SOH34		SOH88		SOH62		IC																						VCC		VCC		VCC		VCC		27	
28			VCC		VCC		VCC																						VSS		VSS		VSS		VSS		28	
29	SOH44		SOH45		SOH63		IC																						VCC		VCC		VCC		VCC		29	
30			VSS		VSS		IC		IC		IC		VSS		VCC		VCC				VSS		VSS					IC		IC		VCC		VCC		30		
31	SOH45		SOH43		SOH62		IC		IC		IC		IC		IC		IC				IC		IC						IC		IC		IC		IC		31	
32			VCC		VCC		VCC																						VSS		VSS		VSS		VSS		32	
33	SOH62		SOH42		SOH68		SOH70		SOH19		SOH64		SOH25		SOH24		SOH7		SOH5		SOH60		SOH61						SOH5		SOH2		SOH2		SOH2		33	
34			VSS		VSS		VCC		IC		IC		VSS		VCC		VCC				VSS		VSS						VCC		VCC		VCC		VCC		34	
35	SOH40		SOH41		SOH61		SOH23		SOH61		SOH62		SOH27		SOH17		SOH15		SOH4		SOH2		SOH3						SOH4		SOH1		SOH4		SOH4		35	
36			VCC		VCC		VCC		SOH29		SOH28		VSS		VCC		VCC				VSS		VSS						VSS		VCC		VCC		VCC		36	
37	SOH60		SOH61		SOH22		SOH21		SOH29		SOH28		SOH18		SOH16		SOH6		SOH0		SOH1		SOH7						SOH9		SOH7		SOH0		SOH0		37	

AMD Athlon™ MP Processor  
Model 10  
Bottomside View

Figure 15. AMD Athlon™ MP Processor Model 10 Pin Diagram – Bottomside View

Table 19. Pin Name Abbreviations

Abbreviation	Full Name	Pin	Abbreviation	Full Name	Pin
	A20M#	AE1		KEY	AG9
	AMD	AH6		KEY	AG15
ANLOG	ANALOG	AJ13		KEY	AG17
CLKFR	CLKFWRST	AJ21		KEY	AG27
	CLKIN	AN17		KEY	AG29
	CLKIN#	AL17		NC	F8
CNNCT	CONNECT	AL23		NC	F30
	COREFB	AG11		NC	G11
	COREFB#	AG13		NC	G13
CPR#	CPU_PRESENCE#	AK6		NC	G19
	DBRDY	AA1		NC	G21
	DBREQ#	AA3		NC	G27
	FERR	AG1		NC	G29
	FID[0]	W1		NC	G31
	FID[1]	W3		NC	H6
	FID[2]	Y1		NC	H8
	FID[3]	Y3		NC	H10
	FLUSH#	AL3		NC	H28
	IGNNE#	AJ1		NC	H30
	INIT#	AJ3		NC	H32
	INTR	AL1		NC	J5
K7CO	K7CLKOUT	AL21		NC	J31
K7CO#	K7CLKOUT#	AN21		NC	K8
	KEY	G7		NC	K30
	KEY	G9		NC	L31
	KEY	G15		NC	N31
	KEY	G17		NC	Q31
	KEY	G23		NC	S31
	KEY	G25		NC	U31
	KEY	N7		NC	W7
	KEY	Q7		NC	W31
	KEY	Y7		NC	Y5
	KEY	AA7		NC	Y31
	KEY	AG7		NC	AA5

Table 19. Pin Name Abbreviations (Continued)

Abbreviation	Full Name	Pin	Abbreviation	Full Name	Pin
	NC	AA31		NC	AM8
	NC	AC7		NC	AN7
	NC	AC31		NC	AN9
	NC	AD8		NC	AN11
	NC	AD30		NC	AN25
	NC	AE7		NC	AN27
	NC	AE31		NMI	AN3
	NC	AF6		PICCLK	N1
	NC	AF8	PICD#0	PICD[0]#	N3
	NC	AF10	PICD#1	PICD[1]#	N5
	NC	AF28	PLBYP#	PLLBYPASS#	AJ25
	NC	AF30	PLBYC	PLLBYPASSCLK	AN15
	NC	AF32	PLBYC#	PLLBYPASSCLK#	AL15
	NC	AG5	PLMN1	PLLMON1	AN13
	NC	AG19	PLMN2	PLLMON2	AL13
	NC	AG21	PLTST#	PLLTST#	AC3
	NC	AG23	PRCRDY	PROCREADY	AN23
	NC	AG25		PWROK	AE3
	NC	AG31		RESET#	AG3
	NC	AH8	RCLK	RSTCLK	AN19
	NC	AH30	RCLK#	RSTCLK#	AL19
	NC	AJ7	SAI#0	SADDIN[0]#	AJ29
	NC	AJ9	SAI#1	SADDIN[1]#	AL29
	NC	AJ11	SAI#2	SADDIN[2]#	AG33
	NC	AJ15	SAI#3	SADDIN[3]#	AJ37
	NC	AJ17	SAI#4	SADDIN[4]#	AL35
	NC	AJ19	SAI#5	SADDIN[5]#	AE33
	NC	AJ27	SAI#6	SADDIN[6]#	AJ35
	NC	AK8	SAI#7	SADDIN[7]#	AG37
	NC	AL7	SAI#8	SADDIN[8]#	AL33
	NC	AL9	SAI#9	SADDIN[9]#	AN37
	NC	AL11	SAI#10	SADDIN[10]#	AL37
	NC	AL25	SAI#11	SADDIN[11]#	AG35
	NC	AL27	SAI#12	SADDIN[12]#	AN29

Table 19. Pin Name Abbreviations (Continued)

Abbreviation	Full Name	Pin	Abbreviation	Full Name	Pin
SAI#13	SADDIN[13]#	AN35	SD#3	SDATA[3]#	Y35
SAI#14	SADDIN[14]#	AN31	SD#4	SDATA[4]#	U35
SAIC#	SADDINCLK#	AJ33	SD#5	SDATA[5]#	U33
SAO#0	SADDOUT[0]#	J1	SD#6	SDATA[6]#	S37
SAO#1	SADDOUT[1]#	J3	SD#7	SDATA[7]#	S33
SAO#2	SADDOUT[2]#	C7	SD#8	SDATA[8]#	AA33
SAO#3	SADDOUT[3]#	A7	SD#9	SDATA[9]#	AE37
SAO#4	SADDOUT[4]#	E5	SD#10	SDATA[10]#	AC33
SAO#5	SADDOUT[5]#	A5	SD#11	SDATA[11]#	AC37
SAO#6	SADDOUT[6]#	E7	SD#12	SDATA[12]#	Y37
SAO#7	SADDOUT[7]#	C1	SD#13	SDATA[13]#	AA37
SAO#8	SADDOUT[8]#	C5	SD#14	SDATA[14]#	AC35
SAO#9	SADDOUT[9]#	C3	SD#15	SDATA[15]#	S35
SAO#10	SADDOUT[10]#	G1	SD#16	SDATA[16]#	Q37
SAO#11	SADDOUT[11]#	E1	SD#17	SDATA[17]#	Q35
SAO#12	SADDOUT[12]#	A3	SD#18	SDATA[18]#	N37
SAO#13	SADDOUT[13]#	G5	SD#19	SDATA[19]#	J33
SAO#14	SADDOUT[14]#	G3	SD#20	SDATA[20]#	G33
SAOC#	SADDOUTCLK#	E3	SD#21	SDATA[21]#	G37
SCNCK1	SCANCLK1	S1	SD#22	SDATA[22]#	E37
SCNCK2	SCANCLK2	S5	SD#23	SDATA[23]#	G35
SCNINV	SCANINTEVAL	S3	SD#24	SDATA[24]#	Q33
SCNSN	SCANSHIFTEN	Q5	SD#25	SDATA[25]#	N33
SCK#0	SCHECK[0]#	U37	SD#26	SDATA[26]#	L33
SCK#1	SCHECK[1]#	Y33	SD#27	SDATA[27]#	N35
SCK#2	SCHECK[2]#	L35	SD#28	SDATA[28]#	L37
SCK#3	SCHECK[3]#	E33	SD#29	SDATA[29]#	J37
SCK#4	SCHECK[4]#	E25	SD#30	SDATA[30]#	A37
SCK#5	SCHECK[5]#	A31	SD#31	SDATA[31]#	E35
SCK#6	SCHECK[6]#	C13	SD#32	SDATA[32]#	E31
SCK#7	SCHECK[7]#	A19	SD#33	SDATA[33]#	E29
SD#0	SDATA[0]#	AA35	SD#34	SDATA[34]#	A27
SD#1	SDATA[1]#	W37	SD#35	SDATA[35]#	A25
SD#2	SDATA[2]#	W35	SD#36	SDATA[36]#	E21

Table 19. Pin Name Abbreviations (Continued)

Abbreviation	Full Name	Pin	Abbreviation	Full Name	Pin
SD#37	SDATA[37]#	C23	SDOC#2	SDATAOUTCLK[2]#	A33
SD#38	SDATA[38]#	C27	SDOC#3	SDATAOUTCLK[3]#	C11
SD#39	SDATA[39]#	A23	SDOV#	SDATAOUTVALID#	AL31
SD#40	SDATA[40]#	A35	SFILLV#	SFILLVALID#	AJ31
SD#41	SDATA[41]#	C35		SMI#	AN5
SD#42	SDATA[42]#	C33	STPC#	STPCLK#	AC1
SD#43	SDATA[43]#	C31		TCK	Q1
SD#44	SDATA[44]#	A29		TDI	U1
SD#45	SDATA[45]#	C29		TDO	U5
SD#46	SDATA[46]#	E23	THDA	THERMDA	S7
SD#47	SDATA[47]#	C25	THDC	THERMDC	U7
SD#48	SDATA[48]#	E17		TMS	Q3
SD#49	SDATA[49]#	E13		TRST#	U3
SD#50	SDATA[50]#	E11	VCC	V <sub>CC_CORE</sub>	B4
SD#51	SDATA[51]#	C15	VCC	V <sub>CC_CORE</sub>	B8
SD#52	SDATA[52]#	E9	VCC	V <sub>CC_CORE</sub>	B12
SD#53	SDATA[53]#	A13	VCC	V <sub>CC_CORE</sub>	B16
SD#54	SDATA[54]#	C9	VCC	V <sub>CC_CORE</sub>	B20
SD#55	SDATA[55]#	A9	VCC	V <sub>CC_CORE</sub>	B24
SD#56	SDATA[56]#	C21	VCC	V <sub>CC_CORE</sub>	B28
SD#57	SDATA[57]#	A21	VCC	V <sub>CC_CORE</sub>	B32
SD#58	SDATA[58]#	E19	VCC	V <sub>CC_CORE</sub>	B36
SD#59	SDATA[59]#	C19	VCC	V <sub>CC_CORE</sub>	D2
SD#60	SDATA[60]#	C17	VCC	V <sub>CC_CORE</sub>	D4
SD#61	SDATA[61]#	A11	VCC	V <sub>CC_CORE</sub>	D8
SD#62	SDATA[62]#	A17	VCC	V <sub>CC_CORE</sub>	D12
SD#63	SDATA[63]#	A15	VCC	V <sub>CC_CORE</sub>	D16
SDIC#0	SDATAINCLK[0]#	W33	VCC	V <sub>CC_CORE</sub>	D20
SDIC#1	SDATAINCLK[1]#	J35	VCC	V <sub>CC_CORE</sub>	D24
SDIC#2	SDATAINCLK[2]#	E27	VCC	V <sub>CC_CORE</sub>	D28
SDIC#3	SDATAINCLK[3]#	E15	VCC	V <sub>CC_CORE</sub>	D32
SDINV#	SDATAINVALID#	AN33	VCC	V <sub>CC_CORE</sub>	F12
SDOC#0	SDATAOUTCLK[0]#	AE35	VCC	V <sub>CC_CORE</sub>	F16
SDOC#1	SDATAOUTCLK[1]#	C37	VCC	V <sub>CC_CORE</sub>	F20

Table 19. Pin Name Abbreviations (Continued)

Abbreviation	Full Name	Pin	Abbreviation	Full Name	Pin
VCC	V <sub>CC_CORE</sub>	F24	VCC	V <sub>CC_CORE</sub>	X30
VCC	V <sub>CC_CORE</sub>	F28	VCC	V <sub>CC_CORE</sub>	X32
VCC	V <sub>CC_CORE</sub>	F32	VCC	V <sub>CC_CORE</sub>	X34
VCC	V <sub>CC_CORE</sub>	F34	VCC	V <sub>CC_CORE</sub>	X36
VCC	V <sub>CC_CORE</sub>	F36	VCC	V <sub>CC_CORE</sub>	Z2
VCC	V <sub>CC_CORE</sub>	H2	VCC	V <sub>CC_CORE</sub>	Z4
VCC	V <sub>CC_CORE</sub>	H4	VCC	V <sub>CC_CORE</sub>	Z6
VCC	V <sub>CC_CORE</sub>	H12	VCC	V <sub>CC_CORE</sub>	Z8
VCC	V <sub>CC_CORE</sub>	H16	VCC	V <sub>CC_CORE</sub>	AB30
VCC	V <sub>CC_CORE</sub>	H20	VCC	V <sub>CC_CORE</sub>	AB32
VCC	V <sub>CC_CORE</sub>	H24	VCC	V <sub>CC_CORE</sub>	AB34
VCC	V <sub>CC_CORE</sub>	K32	VCC	V <sub>CC_CORE</sub>	AB36
VCC	V <sub>CC_CORE</sub>	K34	VCC	V <sub>CC_CORE</sub>	AD2
VCC	V <sub>CC_CORE</sub>	K36	VCC	V <sub>CC_CORE</sub>	AD4
VCC	V <sub>CC_CORE</sub>	M2	VCC	V <sub>CC_CORE</sub>	AD6
VCC	V <sub>CC_CORE</sub>	M4	VCC	V <sub>CC_CORE</sub>	AF14
VCC	V <sub>CC_CORE</sub>	M6	VCC	V <sub>CC_CORE</sub>	AF18
VCC	V <sub>CC_CORE</sub>	M8	VCC	V <sub>CC_CORE</sub>	AF22
VCC	V <sub>CC_CORE</sub>	P30	VCC	V <sub>CC_CORE</sub>	AF26
VCC	V <sub>CC_CORE</sub>	P32	VCC	V <sub>CC_CORE</sub>	AF34
VCC	V <sub>CC_CORE</sub>	P34	VCC	V <sub>CC_CORE</sub>	AF36
VCC	V <sub>CC_CORE</sub>	P36	VCC	V <sub>CC_CORE</sub>	AH2
VCC	V <sub>CC_CORE</sub>	R2	VCC	V <sub>CC_CORE</sub>	AH4
VCC	V <sub>CC_CORE</sub>	R4	VCC	V <sub>CC_CORE</sub>	AH10
VCC	V <sub>CC_CORE</sub>	R6	VCC	V <sub>CC_CORE</sub>	AH14
VCC	V <sub>CC_CORE</sub>	R8	VCC	V <sub>CC_CORE</sub>	AH18
VCC	V <sub>CC_CORE</sub>	T30	VCC	V <sub>CC_CORE</sub>	AH22
VCC	V <sub>CC_CORE</sub>	T32	VCC	V <sub>CC_CORE</sub>	AH26
VCC	V <sub>CC_CORE</sub>	T34	VCC	V <sub>CC_CORE</sub>	AK10
VCC	V <sub>CC_CORE</sub>	T36	VCC	V <sub>CC_CORE</sub>	AK14
VCC	V <sub>CC_CORE</sub>	V2	VCC	V <sub>CC_CORE</sub>	AK18
VCC	V <sub>CC_CORE</sub>	V4	VCC	V <sub>CC_CORE</sub>	AK22
VCC	V <sub>CC_CORE</sub>	V6	VCC	V <sub>CC_CORE</sub>	AK26
VCC	V <sub>CC_CORE</sub>	V8	VCC	V <sub>CC_CORE</sub>	AK30

**Table 19. Pin Name Abbreviations (Continued)**

Abbreviation	Full Name	Pin	Abbreviation	Full Name	Pin
VCC	V <sub>CC_CORE</sub>	AK34		VSS	D22
VCC	V <sub>CC_CORE</sub>	AK36		VSS	D26
VCC	V <sub>CC_CORE</sub>	AJ5		VSS	D30
VCC	V <sub>CC_CORE</sub>	AL5		VSS	D34
VCC	V <sub>CC_CORE</sub>	AM2		VSS	D36
VCC	V <sub>CC_CORE</sub>	AM10		VSS	F2
VCC	V <sub>CC_CORE</sub>	AM14		VSS	F4
VCC	V <sub>CC_CORE</sub>	AM18		VSS	F6
VCC	V <sub>CC_CORE</sub>	AM22		VSS	F10
VCC	V <sub>CC_CORE</sub>	AM26		VSS	F14
VCC	V <sub>CC_CORE</sub>	AM22		VSS	F18
VCC	V <sub>CC_CORE</sub>	AM26		VSS	F22
VCC	V <sub>CC_CORE</sub>	AM30		VSS	F26
VCC	V <sub>CC_CORE</sub>	AM34		VSS	H14
	VCCA	AJ23		VSS	H18
	VID[0]	L1		VSS	H22
	VID[1]	L3		VSS	H26
	VID[2]	L5		VSS	H34
	VID[3]	L7		VSS	H36
	VID[4]	J7		VSS	K2
VREF_S	VREF_SYS	W5		VSS	K4
	VSS	B2		VSS	K6
	VSS	B6		VSS	M30
	VSS	B10		VSS	M32
	VSS	B14		VSS	M34
	VSS	B18		VSS	M36
	VSS	B22		VSS	P2
	VSS	B26		VSS	P4
	VSS	B30		VSS	P6
	VSS	B34		VSS	P8
	VSS	D6		VSS	R30
	VSS	D10		VSS	R32
	VSS	D14		VSS	R34
	VSS	D18		VSS	R36

**Table 19. Pin Name Abbreviations (Continued)**

Abbreviation	Full Name	Pin	Abbreviation	Full Name	Pin
	VSS	T2		VSS	AH36
	VSS	T4		VSS	AK2
	VSS	T6		VSS	AK4
	VSS	T8		VSS	AK12
	VSS	V30		VSS	AK16
	VSS	V32		VSS	AK20
	VSS	V34		VSS	AK24
	VSS	V36		VSS	AK28
	VSS	X2		VSS	AK32
	VSS	X4		VSS	AM4
	VSS	X6		VSS	AM6
	VSS	X8		VSS	AM12
	VSS	Z30		VSS	AM16
	VSS	Z32		VSS	AM20
	VSS	Z34		VSS	AM24
	VSS	Z36		VSS	AM28
	VSS	AB2		VSS	AM32
	VSS	AB8		VSS	AM36
	VSS	AB4		ZN	AC5
	VSS	AB6		ZP	AE5
	VSS	AD32			
	VSS	AD34			
	VSS	AD36			
	VSS	AF2			
	VSS	AF4			
	VSS	AF12			
	VSS	AF16			
	VSS	AH12			
	VSS	AH16			
	VSS	AH20			
	VSS	AH24			
	VSS	AH28			
	VSS	AH32			
	VSS	AH34			



## 10.2 Pin List

Table 20 on page 62 cross-references Socket A pin location to signal name.

The “L” (Level) column shows the electrical specification for this pin. “P” indicates a push-pull mode driven by a single source. “O” indicates open-drain mode that allows devices to share the pin.

**Note:** *The AMD Athlon MP processor supports push-pull drivers. For more information, see “Push-Pull (PP) Drivers” on page 6.*

The “P” (Port) column indicates if this signal is an input (I), output (O), or bidirectional (B) signal. The “R” (Reference) column indicates if this signal should be referenced to VSS (G) or V<sub>CC\_CORE</sub> (P) planes for the purpose of signal routing with respect to the current return paths.

Table 20. Cross-Reference by Pin Location

Pin	Name	Description	L	P	R	Pin	Name	Description	L	P	R
A1	No Pin	page 74	-	-	-	B24	V <sub>CC_CORE</sub>		-	-	-
A3	SADDOUT[12]#		P	O	G	B26	VSS		-	-	-
A5	SADDOUT[5]#		P	O	G	B28	V <sub>CC_CORE</sub>		-	-	-
A7	SADDOUT[3]#		P	O	G	B30	VSS		-	-	-
A9	SDATA[55]#		P	B	P	B32	V <sub>CC_CORE</sub>		-	-	-
A11	SDATA[61]#		P	B	P	B34	VSS		-	-	-
A13	SDATA[53]#		P	B	G	B36	V <sub>CC_CORE</sub>		-	-	-
A15	SDATA[63]#		P	B	G	C1	SADDOUT[7]#		P	O	G
A17	SDATA[62]#		P	B	G	C3	SADDOUT[9]#		P	O	G
A19	SCHECK[7]#	page 74	P	B	G	C5	SADDOUT[8]#		P	O	G
A21	SDATA[57]#		P	B	G	C7	SADDOUT[2]#		P	O	G
A23	SDATA[39]#		P	B	G	C9	SDATA[54]#		P	B	P
A25	SDATA[35]#		P	B	P	C11	SDATAOUTCLK[3]#		P	O	G
A27	SDATA[34]#		P	B	P	C13	SCHECK[6]#	page 74	P	B	G
A29	SDATA[44]#		P	B	G	C15	SDATA[51]#		P	B	P
A31	SCHECK[5]#	page 74	P	B	G	C17	SDATA[60]#		P	B	G
A33	SDATAOUTCLK[2]#		P	O	P	C19	SDATA[59]#		P	B	G
A35	SDATA[40]#		P	B	G	C21	SDATA[56]#		P	B	G
A37	SDATA[30]#		P	B	P	C23	SDATA[37]#		P	B	P
B2	VSS		-	-	-	C25	SDATA[47]#		P	B	G
B4	V <sub>CC_CORE</sub>		-	-	-	C27	SDATA[38]#		P	B	G
B6	VSS		-	-	-	C29	SDATA[45]#		P	B	G
B8	V <sub>CC_CORE</sub>		-	-	-	C31	SDATA[43]#		P	B	G
B10	VSS		-	-	-	C33	SDATA[42]#		P	B	G
B12	V <sub>CC_CORE</sub>		-	-	-	C35	SDATA[41]#		P	B	G
B14	VSS		-	-	-	C37	SDATAOUTCLK[1]#		P	O	G
B16	V <sub>CC_CORE</sub>		-	-	-	D2	V <sub>CC_CORE</sub>		-	-	-
B18	VSS		-	-	-	D4	V <sub>CC_CORE</sub>		-	-	-
B20	V <sub>CC_CORE</sub>		-	-	-	D6	VSS		-	-	-
B22	VSS		-	-	-	D8	V <sub>CC_CORE</sub>		-	-	-

**Table 20. Cross-Reference by Pin Location (continued)**

Pin	Name	Description	L	P	R	Pin	Name	Description	L	P	R
D10	VSS		-	-	-	E33	SCHECK[3]#	page 74	P	B	P
D12	V <sub>CC_CORE</sub>		-	-	-	E35	SDATA[31]#		P	B	P
D14	VSS		-	-	-	E37	SDATA[22]#		P	B	G
D16	V <sub>CC_CORE</sub>		-	-	-	F2	VSS		-	-	-
D18	VSS		-	-	-	F4	VSS		-	-	-
D20	V <sub>CC_CORE</sub>		-	-	-	F6	VSS		-	-	-
D22	VSS		-	-	-	F8	NC Pin	page 74	-	-	-
D24	V <sub>CC_CORE</sub>		-	-	-	F10	VSS		-	-	-
D26	VSS		-	-	-	F12	V <sub>CC_CORE</sub>		-	-	-
D28	V <sub>CC_CORE</sub>		-	-	-	F14	VSS		-	-	-
D30	VSS		-	-	-	F16	V <sub>CC_CORE</sub>		-	-	-
D32	V <sub>CC_CORE</sub>		-	-	-	F18	VSS		-	-	-
D34	VSS		-	-	-	F20	V <sub>CC_CORE</sub>		-	-	-
D36	VSS		-	-	-	F22	VSS		-	-	-
E1	SADDOUT[11]#		P	O	P	F24	V <sub>CC_CORE</sub>		-	-	-
E3	SADDOUTCLK#		P	O	G	F26	VSS		-	-	-
E5	SADDOUT[4]#		P	O	P	F28	V <sub>CC_CORE</sub>		-	-	-
E7	SADDOUT[6]#		P	O	G	F30	NC Pin	page 74	-	-	-
E9	SDATA[52]#		P	B	P	F32	V <sub>CC_CORE</sub>		-	-	-
E11	SDATA[50]#		P	B	P	F34	V <sub>CC_CORE</sub>		-	-	-
E13	SDATA[49]#		P	B	G	F36	V <sub>CC_CORE</sub>		-	-	-
E15	SDATAINCLK[3]#		P	I	G	G1	SADDOUT[10]#		P	O	P
E17	SDATA[48]#		P	B	P	G3	SADDOUT[14]#		P	O	G
E19	SDATA[58]#		P	B	G	G5	SADDOUT[13]#		P	O	G
E21	SDATA[36]#		P	B	P	G7	Key Pin	page 73	-	-	-
E23	SDATA[46]#		P	B	P	G9	Key Pin	page 73	-	-	-
E25	SCHECK[4]#	page 74	P	B	P	G11	NC Pin	page 74	-	-	-
E27	SDATAINCLK[2]#		P	I	G	G13	NC Pin	page 74	-	-	-
E29	SDATA[33]#		P	B	P	G15	Key Pin	page 73	-	-	-
E31	SDATA[32]#		P	B	P	G17	Key Pin	page 73	-	-	-

Table 20. Cross-Reference by Pin Location (continued)

Pin	Name	Description	L	P	R	Pin	Name	Description	L	P	R
G19	NC Pin	page 74	-	-	-	J5	NC Pin	page 74	-	-	-
G21	NC Pin	page 74	-	-	-	J7	VID[4]	page 75	O	O	-
G23	Key Pin	page 73	-	-	-	J31	NC Pin	page 74	-	-	-
G25	Key Pin	page 73	-	-	-	J33	SDATA[19]#		P	B	G
G27	NC Pin	page 74	-	-	-	J35	SDATAINCLK[1]#		P	I	P
G29	NC Pin	page 74	-	-	-	J37	SDATA[29]#		P	B	P
G31	NC Pin	page 74	-	-	-	K2	VSS		-	-	-
G33	SDATA[20]#		P	B	G	K4	VSS		-	-	-
G35	SDATA[23]#		P	B	G	K6	VSS		-	-	-
G37	SDATA[21]#		P	B	G	K8	NC Pin	page 74	-	-	-
H2	V <sub>CC_CORE</sub>		-	-	-	K30	NC Pin	page 74	-	-	-
H4	V <sub>CC_CORE</sub>		-	-	-	K32	V <sub>CC_CORE</sub>		-	-	-
H6	NC Pin	page 74	-	-	-	K34	V <sub>CC_CORE</sub>		-	-	-
H8	NC Pin	page 74	-	-	-	K36	V <sub>CC_CORE</sub>		-	-	-
H10	NC Pin	page 74	-	-	-	L1	VID[0]	page 75	O	O	-
H12	V <sub>CC_CORE</sub>		-	-	-	L3	VID[1]	page 75	O	O	-
H14	VSS		-	-	-	L5	VID[2]	page 75	O	O	-
H16	V <sub>CC_CORE</sub>		-	-	-	L7	VID[3]	page 75	O	O	-
H18	VSS		-	-	-	L31	NC Pin	page 74	-	-	-
H20	V <sub>CC_CORE</sub>		-	-	-	L33	SDATA[26]#		P	B	P
H22	VSS		-	-	-	L35	SCHECK[2]#	page 74	P	B	G
H24	V <sub>CC_CORE</sub>		-	-	-	L37	SDATA[28]#		P	B	P
H26	VSS		-	-	-	M2	V <sub>CC_CORE</sub>		-	-	-
H28	NC Pin	page 74	-	-	-	M4	V <sub>CC_CORE</sub>		-	-	-
H30	NC Pin	page 74	-	-	-	M6	V <sub>CC_CORE</sub>		-	-	-
H32	NC Pin	page 74	-	-	-	M8	V <sub>CC_CORE</sub>		-	-	-
H34	VSS		-	-	-	M30	VSS		-	-	-
H36	VSS		-	-	-	M32	VSS		-	-	-
J1	SADDOUT[0]#	page 74	P	O	-	M34	VSS		-	-	-
J3	SADDOUT[1]#	page 74	P	O	-	M36	VSS		-	-	-

**Table 20. Cross-Reference by Pin Location (continued)**

Pin	Name	Description	L	P	R	Pin	Name	Description	L	P	R
N1	PICCLK	page 70	O	I	-	R34	VSS		-	-	-
N3	PICD#[0]	page 70	O	B	-	R36	VSS		-	-	-
N5	PICD#[1]	page 70	O	B	-	S1	SCANCLK1	page 74	P	I	-
N7	Key Pin	page 73	-	-	-	S3	SCANINTEVAL	page 74	P	I	-
N31	NC Pin	page 74	-	-	-	S5	SCANCLK2	page 74	P	I	-
N33	SDATA[25]#		P	B	P	S7	THERMDA	page 75	-	-	-
N35	SDATA[27]#		P	B	P	S31	NC Pin	page 74	-	-	-
N37	SDATA[18]#		P	B	G	S33	SDATA[7]#		P	B	G
P2	VSS		-	-	-	S35	SDATA[15]#		P	B	P
P4	VSS		-	-	-	S37	SDATA[6]#		P	B	G
P6	VSS		-	-	-	T2	VSS		-	-	-
P8	VSS		-	-	-	T4	VSS		-	-	-
P30	V <sub>CC_CORE</sub>		-	-	-	T6	VSS		-	-	-
P32	V <sub>CC_CORE</sub>		-	-	-	T8	VSS		-	-	-
P34	V <sub>CC_CORE</sub>		-	-	-	T30	V <sub>CC_CORE</sub>		-	-	-
P36	V <sub>CC_CORE</sub>		-	-	-	T32	V <sub>CC_CORE</sub>		-	-	-
Q1	TCK	page 73	P	I	-	T34	V <sub>CC_CORE</sub>		-	-	-
Q3	TMS	page 73	P	I	-	T36	V <sub>CC_CORE</sub>		-	-	-
Q5	SCANSHIFTEN	page 74	P	I	-	U1	TDI	page 73	P	I	-
Q7	Key Pin	page 73	-	-	-	U3	TRST#	page 73	P	I	-
Q31	NC Pin	page 74	-	-	-	U5	TDO	page 73	P	O	-
Q33	SDATA[24]#		P	B	P	U7	THERMDC	page 75	-	-	-
Q35	SDATA[17]#		P	B	G	U31	NC Pin	page 74	-	-	-
Q37	SDATA[16]#		P	B	G	U33	SDATA[5]#		P	B	G
R2	V <sub>CC_CORE</sub>		-	-	-	U35	SDATA[4]#		P	B	G
R4	V <sub>CC_CORE</sub>		-	-	-	U37	SCHECK[0]#	page 74	P	B	G
R6	V <sub>CC_CORE</sub>		-	-	-	V2	V <sub>CC_CORE</sub>		-	-	-
R8	V <sub>CC_CORE</sub>		-	-	-	V4	V <sub>CC_CORE</sub>		-	-	-
R30	VSS		-	-	-	V6	V <sub>CC_CORE</sub>		-	-	-
R32	VSS		-	-	-	V8	V <sub>CC_CORE</sub>		-	-	-

Table 20. Cross-Reference by Pin Location (continued)

Pin	Name	Description	L	P	R	Pin	Name	Description	L	P	R
V30	VSS		-	-	-	Z6	V <sub>CC_CORE</sub>		-	-	-
V32	VSS		-	-	-	Z8	V <sub>CC_CORE</sub>		-	-	-
V34	VSS		-	-	-	Z30	VSS		-	-	-
V36	VSS		-	-	-	Z32	VSS		-	-	-
W1	FID[0]	page 72	O	O	-	Z34	VSS		-	-	-
W3	FID[1]	page 72	O	O	-	Z36	VSS		-	-	-
W5	VREFSYS	page 76	P	-	-	AA1	DBRDY	page 71	P	O	-
W7	NC Pin	page 74	-	-	-	AA3	DBREQ#	page 71	P	I	-
W31	NC Pin	page 74	-	-	-	AA5	NC		-	-	-
W33	SDATAINCLK[0]#		P	I	G	AA7	Key Pin	page 73	-	-	-
W35	SDATA[2]#		P	B	G	AA31	NC Pin	page 74	-	-	-
W37	SDATA[1]#		P	B	P	AA33	SDATA[8]#		P	B	P
X2	VSS		-	-	-	AA35	SDATA[0]#		P	B	G
X4	VSS		-	-	-	AA37	SDATA[13]#		P	B	G
X6	VSS		-	-	-	AB2	VSS		-	-	-
X8	VSS		-	-	-	AB4	VSS		-	-	-
X30	V <sub>CC_CORE</sub>		-	-	-	AB6	VSS		-	-	-
X32	V <sub>CC_CORE</sub>		-	-	-	AB8	VSS		-	-	-
X34	V <sub>CC_CORE</sub>		-	-	-	AB30	V <sub>CC_CORE</sub>		-	-	-
X36	V <sub>CC_CORE</sub>		-	-	-	AB32	V <sub>CC_CORE</sub>		-	-	-
Y1	FID[2]	page 72	O	O	-	AB34	V <sub>CC_CORE</sub>		-	-	-
Y3	FID[3]	page 72	O	O	-	AB36	V <sub>CC_CORE</sub>		-	-	-
Y5	NC Pin	page 74	-	-	-	AC1	STPCLK#	page 75	P	I	-
Y7	Key Pin	page 73	-	-	-	AC3	PLLTEST#	page 74	P	I	-
Y31	NC Pin	page 74	-	-	-	AC5	ZN	page 76	P	-	-
Y33	SCHECK[1]#	page 74	P	B	P	AC7	NC		-	-	-
Y35	SDATA[3]#		P	B	G	AC31	NC Pin	page 74	-	-	-
Y37	SDATA[12]#		P	B	P	AC33	SDATA[10]#		P	B	P
Z2	V <sub>CC_CORE</sub>		-	-	-	AC35	SDATA[14]#		P	B	G
Z4	V <sub>CC_CORE</sub>		-	-	-	AC37	SDATA[11]#		P	B	G

**Table 20. Cross-Reference by Pin Location (continued)**

Pin	Name	Description	L	P	R	Pin	Name	Description	L	P	R
AD2	V <sub>CC_CORE</sub>		-	-	-	AF30	NC Pin	page 74	-	-	-
AD4	V <sub>CC_CORE</sub>		-	-	-	AF32	NC Pin	page 74	-	-	-
AD6	V <sub>CC_CORE</sub>		-	-	-	AF34	V <sub>CC_CORE</sub>		-	-	-
AD8	NC Pin	page 74	-	-	-	AF36	V <sub>CC_CORE</sub>		-	-	-
AD30	NC Pin	page 74	-	-	-	AG1	FERR	page 71	P	O	-
AD32	VSS		-	-	-	AG3	RESET#		-	I	-
AD34	VSS		-	-	-	AG5	NC Pin	page 74	-	-	-
AD36	VSS		-	-	-	AG7	Key Pin	page 73	-	-	-
AE1	A20M#		P	I	-	AG9	Key Pin	page 73	-	-	-
AE3	PWROK		P	I	-	AG11	COREFB	page 71	-	-	-
AE5	ZP	page 76	P	-	-	AG13	COREFB#	page 71	-	-	-
AE7	NC		-	-	-	AG15	Key Pin	page 73	-	-	-
AE31	NC Pin	page 74	-	-	-	AG17	Key Pin	page 73	-	-	-
AE33	SADDIN[5]#		P	I	G	AG19	NC Pin	page 74	-	-	-
AE35	SDATAOUTCLK[0]#		P	O	P	AG21	NC Pin	page 74	-	-	-
AE37	SDATA[9]#		P	B	G	AG23	NC Pin	page 74	-	-	-
AF2	VSS		-	-	-	AG25	NC Pin	page 74	-	-	-
AF4	VSS		-	-	-	AG27	Key Pin	page 73	-	-	-
AF6	NC Pin	page 74	-	-	-	AG29	Key Pin	page 73	-	-	-
AF8	NC Pin	page 74	-	-	-	AG31	NC Pin	page 74	-	-	-
AF10	NC Pin	page 74	-	-	-	AG33	SADDIN[2]#		P	I	G
AF12	VSS		-	-	-	AG35	SADDIN[11]#		P	I	G
AF14	V <sub>CC_CORE</sub>		-	-	-	AG37	SADDIN[7]#		P	I	P
AF16	VSS		-	-	-	AH2	V <sub>CC_CORE</sub>		-	-	-
AF18	V <sub>CC_CORE</sub>		-	-	-	AH4	V <sub>CC_CORE</sub>		-	-	-
AF20	VSS		-	-	-	AH6	AMD Pin	page 70	-	-	-
AF22	V <sub>CC_CORE</sub>		-	-	-	AH8	NC Pin	page 74	-	-	-
AF24	VSS		-	-	-	AH10	V <sub>CC_CORE</sub>		-	-	-
AF26	V <sub>CC_CORE</sub>		-	-	-	AH12	VSS		-	-	-
AF28	NC Pin	page 74	-	-	-	AH14	V <sub>CC_CORE</sub>		-	-	-

Table 20. Cross-Reference by Pin Location (continued)

Pin	Name	Description	L	P	R	Pin	Name	Description	L	P	R
AH16	VSS		-	-	-	AK2	VSS		-	-	-
AH18	V <sub>CC_CORE</sub>		-	-	-	AK4	VSS		-	-	-
AH20	VSS		-	-	-	AK6	CPU_PRESENCE#	page 71	-	-	-
AH22	V <sub>CC_CORE</sub>		-	-	-	AK8	NC Pin	page 74	-	-	-
AH24	VSS		-	-	-	AK10	V <sub>CC_CORE</sub>		-	-	-
AH26	V <sub>CC_CORE</sub>		-	-	-	AK12	VSS		-	-	-
AH28	VSS		-	-	-	AK14	V <sub>CC_CORE</sub>		-	-	-
AH30	NC Pin	page 74	-	-	-	AK16	VSS		-	-	-
AH32	VSS		-	-	-	AK18	V <sub>CC_CORE</sub>		-	-	-
AH34	VSS		-	-	-	AK20	VSS		-	-	-
AH36	VSS		-	-	-	AK22	V <sub>CC_CORE</sub>		-	-	-
AJ1	IGNNE#	page 73	P	I	-	AK24	VSS		-	-	-
AJ3	INIT#	page 73	P	I	-	AK26	V <sub>CC_CORE</sub>		-	-	-
AJ5	V <sub>CC_CORE</sub>		-	-	-	AK28	VSS		-	-	-
AJ7	NC Pin	page 74	-	-	-	AK30	V <sub>CC_CORE</sub>		-	-	-
AJ9	NC Pin	page 74	-	-	-	AK32	VSS		-	-	-
AJ11	NC Pin	page 74	-	-	-	AK34	V <sub>CC_CORE</sub>		-	-	-
AJ13	Analog	page 70	-	-	-	AK36	V <sub>CC_CORE</sub>		-	-	-
AJ15	NC Pin	page 74	-	-	-	AL1	INTR	page 73	P	I	-
AJ17	NC Pin	page 74	-	-	-	AL3	FLUSH#	page 73	P	I	-
AJ19	NC Pin	page 74	-	-	-	AL5	V <sub>CC_CORE</sub>		-	-	-
AJ21	CLKFWRST	page 70	P	I	P	AL7	NC Pin	page 74	-	-	-
AJ23	VCCA	page 75	-	-	-	AL9	NC Pin	page 74	-	-	-
AJ25	PLLBYPASS#	page 74	P	I	-	AL11	NC Pin	page 74	-	-	-
AJ27	NC Pin	page 74	-	-	-	AL13	PLLMON2	page 74	O	O	-
AJ29	SADDIN[0]#	page 74	P	I	-	AL15	PLLBYPASSCLK#	page 74	P	I	-
AJ31	SFILLVALID#		P	I	G	AL17	CLKIN#	page 71	P	I	P
AJ33	SADDINCLK#		P	I	G	AL19	RSTCLK#	page 71	P	I	P
AJ35	SADDIN[6]#		P	I	P	AL21	K7CLKOUT	page 73	P	O	-
AJ37	SADDIN[3]#		P	I	G	AL23	CONNECT	page 71	P	I	P



**Table 20. Cross-Reference by Pin Location (continued)**

Pin	Name	Description	L	P	R	Pin	Name	Description	L	P	R
AL25	NC Pin	page 74	-	-	-	AN11	NC Pin	page 74	-	-	-
AL27	NC Pin	page 74	-	-	-	AN13	PLLMON1	page 74	O	B	-
AL29	SADDIN[1]#	page 74	P	I	-	AN15	PLLBYPASSCLK	page 74	P	I	-
AL31	SDATAOUTVALID#		P	O	P	AN17	CLKIN	page 71	P	I	P
AL33	SADDIN[8]#		P	I	P	AN19	RSTCLK	page 71	P	I	P
AL35	SADDIN[4]#		P	I	G	AN21	K7CLKOUT#	page 73	P	O	-
AL37	SADDIN[10]#		P	I	G	AN23	PROCRDY		P	O	P
AM2	V <sub>CC_CORE</sub>		-	-	-	AN25	NC Pin	page 74	-	-	-
AM4	VSS		-	-	-	AN27	NC Pin	page 74	-	-	-
AM6	VSS		-	-	-	AN29	SADDIN[12]#		P	I	G
AM8	NC Pin	page 74	-	-	-	AN31	SADDIN[14]#		P	I	G
AM10	V <sub>CC_CORE</sub>		-	-	-	AN33	SDATAINVALID#		P	I	P
AM12	VSS		-	-	-	AN35	SADDIN[13]#		P	I	G
AM14	V <sub>CC_CORE</sub>		-	-	-	AN37	SADDIN[9]#		P	I	G
AM16	VSS		-	-	-						
AM18	V <sub>CC_CORE</sub>		-	-	-						
AM20	VSS		-	-	-						
AM22	V <sub>CC_CORE</sub>		-	-	-						
AM24	VSS		-	-	-						
AM26	V <sub>CC_CORE</sub>		-	-	-						
AM28	VSS		-	-	-						
AM30	V <sub>CC_CORE</sub>		-	-	-						
AM32	VSS		-	-	-						
AM34	V <sub>CC_CORE</sub>		-	-	-						
AM36	VSS		-	-	-						
AN1	No Pin	page 74	-	-	-						
AN3	NMI		P	I	-						
AN5	SMI#		P	I	-						
AN7	NC Pin	page 74	-	-	-						
AN9	NC Pin	page 74	-	-	-						

## 10.3 Detailed Pin Descriptions

The information in this section pertains to Table 20 on page 62.

### A20M# Pin

A20M# is an input from the system used to simulate address wrap-around in the 20-bit 8086.

### AMD Pin

AMD Socket A processors do not implement a pin at location AH6. All Socket A designs must have a top plate or cover that blocks this pin location. When the cover plate blocks this location, a non-AMD part (e.g., PGA370) does not fit into the socket. However, socket manufacturers are allowed to have a contact loaded in the AH6 position. Therefore, motherboard socket design should account for the possibility that a contact could be loaded in this position.

### AMD Athlon™ System Bus Pins

See the *AMD Athlon™ and AMD Duron™ System Bus Specification*, order# 21902 for information about the system bus pins—PROCRDY, PWROK, RESET#, SADDIN[14:2]#, SADDINCLK#, SADDOUT[14:2]#, SADDOUTCLK#, SCHECK[7:0]#, SDATA[63:0]#, SDATAINCLK[3:0]#, SDATAINVALID#, SDATAOUTCLK[3:0]#, SDATAOUTVALID#, SFILLVALID#.

### Analog Pin

Treat this pin as a NC.

### APIC Pins, PICCLK, PICD[1:0]#

The Advanced Programmable Interrupt Controller (APIC) is a feature that provides a flexible and expandable means of delivering interrupts in a system using an AMD processor. The pins, PICD[1:0], are the bidirectional message-passing signals used for the APIC and are driven to the Southbridge, a dedicated I/O APIC, or another multiprocessing-enabled AMD Athlon MP processor model 10. The pin, PICCLK, must be driven with a valid clock input.

Refer to “VCC\_2.5V Generation Circuit” found in the section, “Motherboard Required Circuits,” of the *AMD Athlon™ Processor Motherboard Design Guide*, order# 24363 for the required supporting circuitry.

For more information, see Table 15, “APIC Pin AC and DC Characteristics,” on page 40.

### CLKFWRST Pin

CLKFWRST resets clock-forward circuitry for both the system and processor.

<b>CLKIN, RSTCLK (SYSCLK) Pins</b>	<p>Connect CLKIN with RSTCLK and name it SYSCLK. Connect CLKIN# with RSTCLK# and name it SYSCLK#. Length match the clocks from the clock generator to the Northbridge and processor.</p> <p>See “SYSCLK and SYSCLK#” on page 75 for more information.</p>
<b>CONNECT Pin</b>	<p>CONNECT is an input from the system used for power management and clock-forward initialization at reset.</p>
<b>COREFB and COREFB# Pins</b>	<p>COREFB and COREFB# are outputs to the system that provide processor core voltage feedback to the system.</p>
<b>CPU_PRESENCE# Pin</b>	<p>CPU_PRESENCE# is connected to VSS on the processor package. If pulled-up on the motherboard, CPU_PRESENCE# may be used to detect the presence or absence of a processor in the Socket A-style socket.</p>
<b>DBRDY and DBREQ# Pins</b>	<p>DBRDY and DBREQ# are routed to the debug connector. DBREQ# is tied to V<sub>CC_CORE</sub> with a pullup resistor.</p>
<b>FERR Pin</b>	<p>FERR is an output to the system that is asserted for any unmasked numerical exception independent of the NE bit in CR0. FERR is a push-pull active High signal that must be inverted and level shifted to an active Low signal. For more information about FERR and FERR#, see the “Required Circuits” chapter of the <i>AMD Athlon™ Processor-Based Motherboard Design Guide</i>, order# 24363.</p>
<b>FID[3:0] Pins</b>	<p>FID[3] (Y3), FID[2] (Y1), FID[1] (W3), and FID[0] (W1) are the 4-bit processor clock-to-SYSCLK ratio.</p> <p>Table 21 on page 72 describes the encodings of the clock multipliers on FID[3:0].</p>

**Table 21. FID[3:0] Clock Multiplier Encodings**

FID[3:0] <sup>2</sup>	Processor Clock to SYSCLK Frequency Ratio
0000	11
0001	11.5
0010	12
0011	≥ 12.5 <sup>1</sup>
0100	5
0101	5.5
0110	6
0111	6.5
1000	7
1001	7.5
1010	8
1011	8.5
1100	9
1101	9.5
1110	10
1111	10.5

**Notes:**

1. All ratios greater than or equal to 12.5x have the same FID[3:0] code of 0011b, which causes the SIP configuration for all ratios of 12.5x or greater to be the same.
2. BIOS initializes the CLK\_Ctl MSR during the POST routine. This CLK\_Ctl setting is used with all FID combinations and selects a Halt disconnect divisor and a Stop Grant disconnect divisor. For more information, refer to the AMD Athlon™ and AMD Duron™ Processors BIOS, Software, and Debug Developers Guide, order# 21656.

The FID[3:0] signals are open-drain processor outputs that are pulled High on the motherboard and sampled by the chipset to determine the SIP (serial initialization packet) that is sent to the processor. The FID[3:0] signals are valid after PWROK is asserted. The FID[3:0] signals must not be sampled until they become valid. See the *AMD Athlon™ and AMD Duron™ System Bus Specification*, order# 21902 for more information about Serialization Initialization Packets and SIP protocol.

The processor FID[3:0] outputs are open-drain and 2.5-V tolerant. To prevent damage to the processor, do not pull these signals High above 2.5 V. Do not expose these pins to a differential voltage greater than 1.60 V, relative to the processor core voltage.

Refer to “VCC\_2.5V Generation Circuit” found in the section, “Motherboard Required Circuits,” of the *AMD Athlon™ Processor Motherboard Design Guide*, order# 24363 for the required supporting circuitry.

See “Frequency Identification (FID[3:0])” on page 27 for the DC characteristics for FID[3:0].

<b>FLUSH# Pin</b>	FLUSH# must be tied to $V_{CC\_CORE}$ with a pullup resistor. If a debug connector is implemented, FLUSH# is routed to the debug connector.
<b>IGNNE# Pin</b>	IGNNE# is an input from the system that tells the processor to ignore numeric errors.
<b>INIT# Pin</b>	INIT# is an input from the system that resets the integer registers without affecting the floating-point registers or the internal caches. Execution starts at 0_FFFF_FFF0h.
<b>INTR Pin</b>	INTR is an input from the system that causes the processor to start an interrupt acknowledge transaction that fetches the 8-bit interrupt vector and starts execution at that location.
<b>JTAG Pins</b>	TCK, TMS, TDI, TRST#, and TDO are the JTAG interface. Connect these pins directly to the motherboard debug connector. Pull TDI, TCK, TMS, and TRST# up to $V_{CC\_CORE}$ with pullup resistors.
<b>K7CLKOUT and K7CLKOUT# Pins</b>	K7CLKOUT and K7CLKOUT# are each run for two to three inches and then terminated with a resistor pair: 100 ohms to $V_{CC\_CORE}$ and 100 ohms to VSS. The effective termination resistance and voltage are 50 ohms and $V_{CC\_CORE}/2$ .
<b>Key Pins</b>	These 16 locations are for processor type keying for forwards and backwards compatibility (G7, G9, G15, G17, G23, G25, N7, Q7, Y7, AA7, AG7, AG9, AG15, AG17, AG27, and AG29). Motherboard designers should treat key pins like NC (No Connect) pins. A socket designer has the option of creating a top mold piece that allows PGA key pins only where designated. However, sockets that populate all 16 key pins must be allowed, so the motherboard must always provide for pins at all key pin locations.

See “NC Pins“ for more information.

<b>NC Pins</b>	The motherboard should provide a plated hole for an NC pin. The pin hole should not be electrically connected to anything.
<b>NMI Pin</b>	The motherboard should provide a plated hole for an NC pin. The pin hole should not be electrically connected to anything.
<b>PGA Orientation Pins</b>	<p>No pin is present at pin locations A1 and AN1. Motherboard designers should not allow for a PGA socket pin at these locations.</p> <p>For more information, see the <i>AMD Athlon™ Processor-Based Motherboard Design Guide</i>, order# 24363.</p>
<b>PLL Bypass and Test Pins</b>	PLLTEST#, PLLBYPASS#, PLLMON1, PLLMON2, PLLBYPASSCLK, and PLLBYPASSCLK# are the PLL bypass and test interface. This interface is tied disabled on the motherboard. All six pin signals are routed to the debug connector. All four processor inputs (PLLTEST#, PLLBYPASS#, PLLMON1, and PLLMON2) are tied to V <sub>CC_CORE</sub> with pullup resistors.
<b>PWROK Pin</b>	<p>The PWROK input to the processor must not be asserted until all voltage planes in the system are within specification and all system clocks are running within specification.</p> <p>For more information, Chapter 8, “Signal and Power-Up Requirements” on page 41.</p>
<b>SADDIN[1:0]# and SADDOUT[1:0]# Pins</b>	The AMD Athlon MP processor model 10 does not support SADDIN[1:0]# or SADDOUT[1:0]#. SADDIN[1]# is tied to VCC with pullup resistors, if this bit is not supported by the Northbridge (future models can support SADDIN[1]#). SADDOUT[1:0]# are tied to VCC with pullup resistors if these pins are supported by the Northbridge. For more information, see the <i>AMD Athlon™ and AMD Duron™ System Bus Specification</i> , order# 21902.
<b>Scan Pins</b>	SCANSHIFTEEN, SCANCLK1, SCANINTEVAL, and SCANCLK2 are the scan interface. This interface is AMD internal and is tied disabled with pulldown resistors to ground on the motherboard.
<b>SCHECK[7:0]# Pins</b>	For systems that do not support ECC, SCHECK[7:0]# should be treated as NC pins.

<b>SMI# Pin</b>	SMI# is an input that causes the processor to enter the system management mode.
<b>STPCLK# Pin</b>	STPCLK# is an input that causes the processor to enter a lower power mode and issue a Stop Grant special cycle.
<b>SYSCLK and SYSCLK#</b>	<p>SYSCLK and SYSCLK# are differential input clock signals provided to the PLL of the processor from a system-clock generator.</p> <p>See “CLKIN, RSTCLK (SYSCLK) Pins” on page 71 for more information.</p>
<b>THERMDA and THERMDC Pins</b>	<p>Thermal Diode anode and cathode pins are used to monitor the actual temperature of the processor die, providing more accurate temperature control to the system.</p> <p>See Table 13, “Thermal Diode Electrical Characteristics,” on page 38 for more information.</p>
<b>VCCA Pin</b>	<p>VCCA is the processor PLL supply. For information about the VCCA pin, see Table 5, “VCCA AC and DC Characteristics,” on page 35 and the <i>AMD Athlon™ Processor-Based Motherboard Design Guide</i>, order# 24363.</p> <p>To prevent damage to the processor, do not pull this signal High above 2.5 V. Do not expose this pin to a differential voltage greater than 1.60 V, relative to the processor core voltage.</p>
<b>VID[4:0] Pins</b>	<p>The VID[4:0] (Voltage Identification) outputs are used to dictate the <math>V_{CC\_CORE}</math> voltage level. The VID[4:0] pins are strapped to ground or left unconnected on the processor package. The VID[4:0] pins are pulled up on the motherboard and used by the <math>V_{CC\_CORE}</math> DC/DC converter.</p> <p>The VID codes and corresponding voltage levels are shown in Table 22, “VID[4:0] Code to Voltage Definition,” on page 76.</p>

**Table 22. VID[4:0] Code to Voltage Definition**

VID[4:0]	V <sub>CC_CORE</sub> (V)	VID[4:0]	V <sub>CC_CORE</sub> (V)
00000	1.850	10000	1.450
00001	1.825	10001	1.425
00010	1.800	10010	1.400
00011	1.775	10011	1.375
00100	1.750	10100	1.350
00101	1.725	10101	1.325
00111	1.675	10111	1.275
01000	1.650	11000	1.250
01001	1.625	11001	1.225
01010	1.600	11010	1.200
01011	1.575	11011	1.175
01100	1.550	11100	1.150
01101	1.525	11101	1.125
01110	1.500	11110	1.100
01111	1.475	11111	No CPU

For more information, see the “Required Circuits” chapter of the *AMD Athlon™ Processor-Based Motherboard Design Guide*, order# 24363.

**VREFSYS Pin**

VREFSYS (W5) drives the threshold voltage for the system bus input receivers. The value of VREFSYS is system specific. In addition, to minimize V<sub>CC\_CORE</sub> noise rejection from VREFSYS, include decoupling capacitors. For more information, see the *AMD Athlon™ Processor-Based Motherboard Design Guide*, order# 24363.

**ZN and ZP Pins**

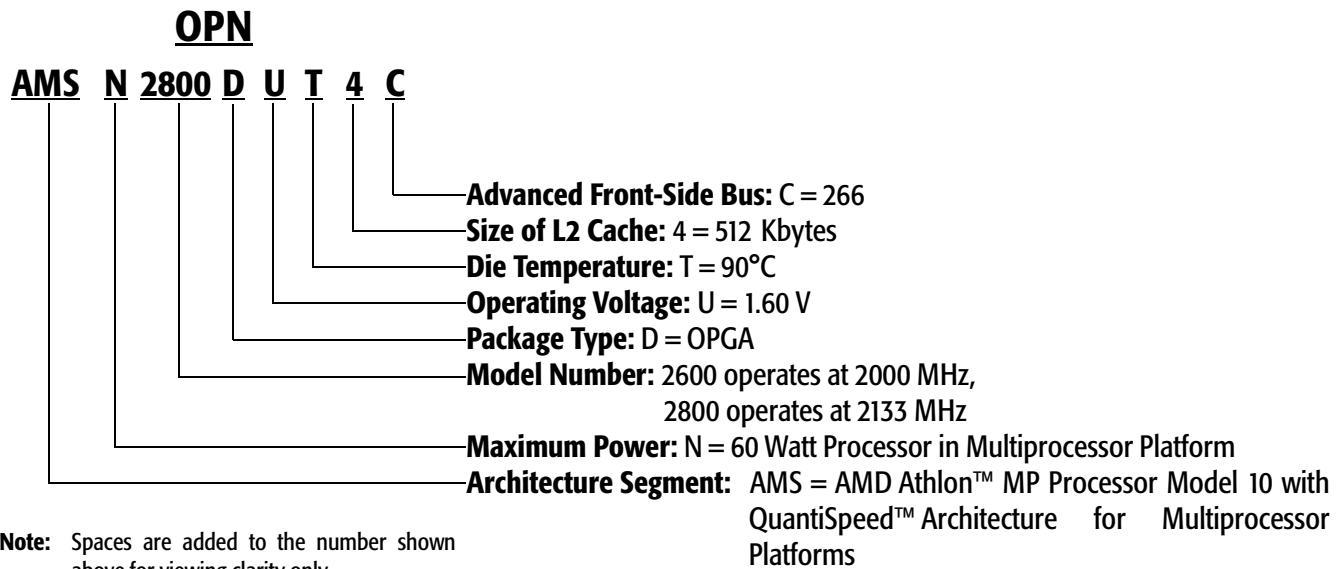
ZN (AC5) and ZP (AE5) are the push-pull compensation circuit pins. In Push-Pull mode (selected by the SIP parameter SysPushPull asserted), ZN is tied to V<sub>CC\_CORE</sub> with a resistor that has a resistance matching the impedance Z<sub>0</sub> of the transmission line. ZP is tied to VSS with a resistor that has a resistance matching the impedance Z<sub>0</sub> of the transmission line.



## 11 Ordering Information

### Standard AMD Athlon™ MP Processor Model 10 Products

AMD standard products are available in several operating ranges. The Ordering Part Numbers (OPN) are formed by a combination of the elements, as shown in Figure 16.



**Figure 16. OPN Example for the AMD Athlon™ MP Processor Model 10**



# Appendix A

## Thermal Diode Calculations

This section contains information about the calculations for the on-die thermal diode of the AMD Athlon™ MP processor model 10. For electrical information about this thermal diode, see Table 13, “Thermal Diode Electrical Characteristics,” on page 38.

### Ideal Diode Equation

The ideal diode equation uses the variables and constants defined in Table 23.

**Table 23. Constants and Variables for the Ideal Diode Equation**

Equation Symbol	Variable, Constant Description
$\eta_f$ , lumped	Lumped ideality factor
$k$	Boltzmann constant
$q$	Electron charge constant
$T$	Diode temperature (Kelvin)
$V_{BE}$	Voltage from base to emitter
$I_C$	Collector current
$I_S$	Saturation current

Equation (1) shows the ideal diode calculation.

$$V_{BE} = n_{f, lumped} \cdot \frac{k}{q} \cdot T \cdot \ln\left(\frac{I_C}{I_S}\right) \quad (1)$$

Sourcing two currents and using Equation (1) derives the difference in the base-to-emitter voltage that leads to finding the diode temperature as shown in Equation (2). The use of dual sourcing currents allows the measurement of the thermal diode temperature to be more accurate and less susceptible to die and process revisions. Temperature sensors that utilize series resistance cancellation can use more than two sourcing currents and are suitable to be used with the AMD thermal diode. Equation (2) is the formula for calculating the temperature of a thermal diode.

$$T = \frac{V_{BE, high} - V_{BE, low}}{n_{f, lumped} \cdot \frac{k}{q} \cdot \ln\left(\frac{I_{high}}{I_{low}}\right)} \quad (2)$$

## Temperature Offset Correction

A temperature offset may be required to correct the value measured by a temperature sensor. An offset is necessary if a difference exists between the lumped ideality factor of the processor and the ideality factor assumed by the temperature sensor. The lumped ideality factor can be calculated using the equations in this section to find the temperature offset that should be used with the temperature sensor.

Table 24 shows the constants and variables used to calculate the temperature offset correction.

**Table 24. Constants and Variables Used in Temperature Offset Equations**

Equation Symbol	Variable, Constant Description
$n_{f, actual}$	Actual ideality factor
$n_{f, lumped}$	Lumped ideality factor
$n_{f, TS}$	Ideality factor assumed by temperature sensor
$I_{high}$	High sourcing current
$I_{low}$	Low sourcing current

**Table 24. Constants and Variables Used in Temperature Offset Equations**

Equation Symbol	Variable, Constant Description
$T_{die, spec}$	Die temperature specification
$T_{offset}$	Temperature offset

The formulas in Equation (3) and Equation (4) can be used to calculate the temperature offset for temperature sensors that do not employ series resistance cancellation. The result is added to the value measured by the temperature sensor. Contact the vendor of the temperature sensor being used for the value of  $n_{f,TS}$ . Refer to the document, *On-Die Thermal Diode Characterization*, order# 25443, for further details.

Equation (3) shows the equation for calculating the lumped ideality factor ( $n_{f, lumped}$ ) in sensors that do not employ series resistance cancellation.

$$n_{f, lumped} = n_{f, actual} + \frac{R_T \cdot (I_{high} - I_{low})}{\frac{k}{q}(T_{die, spec} + 273.15) \cdot \ln\left(\frac{I_{high}}{I_{low}}\right)} \quad (3)$$

Equation (4) shows the equation for calculating temperature offset ( $T_{offset}$ ) in sensors that do not employ series resistance cancellation.

$$T_{offset} = (T_{die, spec} + 273.15) \cdot \left(1 - \frac{n_{f, lumped}}{n_{f, TS}}\right) \quad (4)$$

Equation (5) is the temperature offset for temperature sensors that utilize series resistance cancellation. Add the result to the value measured by the temperature sensor. Note that the value of  $n_{f,TS}$  in Equation (5) may not equal the value used in Equation (4).

$$T_{offset} = (T_{die, spec} + 273.15) \cdot \left(1 - \frac{n_{f, actual}}{n_{f, TS}}\right) \quad (5)$$



# Appendix B

## Conventions and Abbreviations

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This section contains information about the conventions and abbreviations used in this document.

### Signals and Bits

- **Active-Low Signals**—Signal names containing a pound sign, such as SFILL#, indicate active-Low signals. They are asserted in their Low-voltage state and negated in their High-voltage state. When used in this context, High and Low are written with an initial upper case letter.
- **Signal Ranges**—In a range of signals, the highest and lowest signal numbers are contained in brackets and separated by a colon (for example, D[63:0]).
- **Reserved Bits and Signals**—Signals or bus bits marked *reserved* must be driven inactive or left unconnected, as indicated in the signal descriptions. These bits and signals are reserved by AMD for future implementations. When software reads registers with reserved bits, the reserved bits must be masked. When software writes such registers, it must first read the register and change only the non-reserved bits before writing back to the register.
- **Three-State**—In timing diagrams, signal ranges that are high impedance are shown as a straight horizontal line half-way between the high and low levels.
- **Invalid and Don't-Care**—In timing diagrams, signal ranges that are invalid or don't-care are filled with a screen pattern.

## Data Terminology

The following list defines data terminology:

- Quantities
  - A *word* is two bytes (16 bits)
  - A *doubleword* is four bytes (32 bits)
  - A *quadword* is eight bytes (64 bits)
- Addressing—Memory is addressed as a series of bytes on eight-byte (64-bit) boundaries in which each byte can be separately enabled.
- Abbreviations—The following notation is used for bits and bytes:
  - Kilo (K, as in 4-Kbyte page)
  - Mega (M, as in 4 Mbits/sec)
  - Giga (G, as in 4 Gbytes of memory space)

See Table 25 on page 85 for more abbreviations.

- Little-endian Convention—The byte with the address *xx...xx00* is in the least-significant byte position (little end). In byte diagrams, bit positions are numbered from right to left—the little end is on the right and the big end is on the left. Data structure diagrams in memory show low addresses at the bottom and high addresses at the top. When data items are aligned, bit notation on a 64-bit data bus maps directly to bit notation in 64-bit-wide memory. Because byte addresses increase from right to left, strings appear in reverse order when illustrated.
- Bit Ranges—In text, bit ranges are shown with a dash (for example, bits 9–1). When accompanied by a signal or bus name, the highest and lowest bit numbers are contained in brackets and separated by a colon (for example, AD[31:0]).
- Bit Values—Bits can either be set to 1 or cleared to 0.
- Hexadecimal and Binary Numbers—Unless the context makes interpretation clear, hexadecimal numbers are followed by an h and binary numbers are followed by a b.



## Abbreviations and Acronyms

Table 25 contains the definitions of abbreviations used in this document.

**Table 25. Abbreviations**

Abbreviation	Meaning
A	ampere
F	farad
G	giga-
Gbit	gigabit
Gbyte	gigabyte
GHz	gigahertz
H	henry
h	hexadecimal
K	kilo-
Kbyte	kilobyte
lbf	foot-pound
M	mega-
Mbit	megabit
Mbyte	megabyte
MHz	megahertz
m	milli-
ms	millisecond
mW	milliwatt
μ	micro-
μA	microampere
μF	microfarad
μH	microhenry
μs	microsecond
μV	microvolt
n	nano-
nA	nanoampere
nF	nanofarad
nH	nanohenry
ns	nanosecond
Ω	ohm

**Table 25. Abbreviations (Continued)**

Abbreviation	Meaning
p	pico-
pA	picoampere
pF	picofarad
pH	picohenry
ps	picosecond
s	second
V	volt
W	watt

Table 26 contains the definitions of commonly-used acronyms .

**Table 26. Acronyms**

Abbreviation	Meaning
ACPI	Advanced Configuration and Power Interface
AGP	Accelerated Graphics Port
APCI	AGP Peripheral Component Interconnect
API	Application Programming Interface
APIC	Advanced Programmable Interrupt Controller
BAR	basic address register
BGA	ball grid array
BIOS	basic input/output system
BIST	built-in self-test
BIU	bus interface unit
CAD	computer-aided design
CCGA	ceramic column grid array
CLGA	ceramic line grid array
CMOS	complementary metal-oxide semiconductor
CPGA	ceramic pin grid array
CPU	central processing unit—replace with “the processor”
DDR	double-data rate
DIMM	dual inline memory module
DMA	direct memory access
DRAM	direct random access memory

**Table 26. Acronyms (Continued)**

<b>Abbreviation</b>	<b>Meaning</b>
DSP	digital signal processing
DTR	desktop replacement
DUT	device under test
ECC	error correction code
EEPROM	electronically erasable programmable read-only memory
EIDE	Enhanced Integrated Device Electronics
EISA	Extended Industry Standard Architecture
EOI	end of interrupt
EPROM	enhanced programmable read-only memory
FID	frequency identifier
FIFO	first in, first out
FON	full on
FPU	floating-point unit
FSB	front-side bus
GART	graphics address remapping table
HSTL	high-speed transistor logic
IC	integrated circuit
IDE	Integrated Drive (Device) Electronics
IPC	instructions per cycle
IRQ	interrupt request
ISA	Industry Standard Architecture
ISDN	Integrated Services Digital Network
ISO	International Organization for Standardization
ISR	interrupt service routine and in-service register
JEDEC	Joint Electron Device Engineering Council
JTAG	Joint Test Action Group
LAN	local area network
LPT	local printer terminal
LRU	least-recently used
LSB	least-significant bit
MOESI	A cache-state characteristic: exclusive modified, owner, exclusive, shared, invalid
MOSFET	metal-oxide semiconductor field-effect transistor
MSB	most significant bit

**Table 26. Acronyms (Continued)**

<b>Abbreviation</b>	<b>Meaning</b>
MSR	model-specific register
MTRR	memory type and range registers
MUX	multiplexer
NMI	non-maskable interrupt
NOP	no operation
OBGA	organic ball grid array
OCW	operation command word
OD	open-drain
OPGA	organic pin grid array
PA	physical address
PBGA	plastic ball grid array
PCB	printed circuit board
PCI	peripheral component interconnect
PDE	page directory entry
PDT	page directory table
PGA	pin grid array
PIB	processor internal buffer
PIC	programmable interrupt command
PLL	phase locked loop
PM	power management
PMSM	Power Management State Machine
PNP (or PnP)	Plug 'n Play or Plug and Play
POS	power-on suspend
POST	power-on self-test
PPA	physical page address
PQ	probe queue
PRA	probe response alert
PSQ	probe system data and control queue
RAM	random access memory
RAS	remote access storage
RDMSR	read MSR
RID	read if dirty
RIH	read if hit
ROM	read only memory

**Table 26. Acronyms (Continued)**

<b>Abbreviation</b>	<b>Meaning</b>
RSD	reference system design
RTC	real-time clock
RXA	read acknowledge queue
SBA	sideband address
SCI	system controller interrupt
SCSI	small computer system interface
SDI	system DRAM interface
SDRAM	synchronous direct random access memory
SIMD	single instruction multiple data
SIP	serial initialization packet
SMBus	system management bus
SMC	SDRAM memory controller
SMI	system management interrupt
SMM	system management mode
SOFF	soft off
SPD	serial presence detect
SPSC	system power state controller
SRAM	static random access memory
SROM	serial read only memory
STP	shielded twisted pair
TCP/IP	Transmission Control Protocol/Internet Protocol
TDP	thermal dissipating power
TLB	translation lookaside buffer
TOM	top of memory
TTL	Transistor Transistor Logic
USB	universal serial bus
VAS	virtual address space
VGA	Video Graphics Adapter
VPA	virtual page address
VRM	voltage regulator module
USB	universal serial bus
WB	writeback
WBT	write buffer tag
WC	write combining

**Table 26. Acronyms (Continued)**

Abbreviation	Meaning
WDB	write data buffer
WP	write protect
WRMSR	write MSR
WT	writethrough
XOR	exclusive OR
ZDB	Zero Delay Buffer

## Related Publications

These documents provide helpful information about the AMD Athlon™ MP processor model 10, and can be found with other related documents at the AMD Web site, <http://www.amd.com>.

- *AMD Athlon™ Processor x86 Code Optimization Guide*, order# 22007
- *AMD Processor Recognition Application Note*, order# 20734
- *Methodologies for Measuring Temperature on AMD Athlon™ and AMD Duron™ Processors*, order# 24228
- *AMD Thermal, Mechanical, and Chassis Cooling Design Guide*, order# 23794
- *Builders Guide for 2P Capable Servers and Workstations*, order# 25823
- *System Considerations for Dual AMD Athlon™ XP Processors in Tower and 1U Form*, order# 25325

Other Web sites of interest include the following:

- JEDEC home page—[www.jedec.org](http://www.jedec.org)
- IEEE home page—[www.computer.org](http://www.computer.org)
- AGP Forum—[www.agpforum.or](http://www.agpforum.or)