Semiconductor, Inc.

Ei68C153
Bus Interrupter Module (VME)

FEATURES

- Programmable interrupt controller for VMEbus and VERSAbus ™ systems
- Receives and prioritizes 4 independent local interrupt sources
- 7 programmable interrupt request levels for each local interrupt source
- Separate control and vector registers for each local interrupt source
- Interrupt enable and interrupt clear bits
- Two response modes: Internal (vectored mode) or external (interrupting device-sup plies-the-vector mode)
- Interrupt acknowledge daisy chain
- Flag bits with auto-clear capability
- Pin & function compatible with Motorola MC68153
- Single 5.0 volt power supply
- Advanced CMOS low-power technology

DESCRIPTION

The Bus Interrupter Module (BIM) provides an interface between interrupting devices and a system bus such as the VMEbus or VERSAbus™. It generates a maximum of 7 bus interrupts on the IRQ1-IRQ7 outputs and responds to interrupt acknowledge cycles for up to 4 independent slaves. The BIM can also supply an interrupt vector during an interrupt acknowledge cycle. Moreover, it sits in the interrupt acknowledge daisy-chain which allows for multiple interrupts on the level acknowledged.

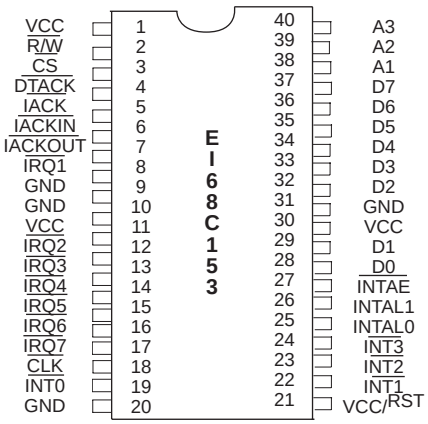
The BIM accepts device interrupt requests on inputs INT0, INT1, INT2 and INT3. Each input is regulated by Bit 4 (IRE) of the associated control register (CRO controls INT0, CR! controls INT1,etc.). If IRE (Interrupt Enable) is set and a device input is asserted, an Interrupt Request open-collector output (IRQ1 - IRQ7) is asserted. The asserted IRQX output is selected by the value programmed in Bits 0, 1, and 2 of the control register (L0, L1, and L3).

This 3-bit field determines the interrupt request level as set by software.

Two or more interrupt sources can be programmed to the same request level. The corresponding IRQX output will remain asserted until multiple interrupt acknowledge cycles respond to all requests.

If the interrupt request level is set to zero, the interrupt is disabled because there is no corresponding IRQ output.

PIN CONFIGURATION



40-PIN DIP

Interrupt Acknowledge

The response of an interrupt Handler to a bus interrupt request is an interrupt acknowledge cycle. The IACK cycle is initiated in BIM by receiving IACK low R/W, A1, A2, A3 are latched, and the interrupt level on line A1-A3 is compared with any interrupt requests pending in the chip. Further activity can be one of four cases.

1. No further action required — This occurs if IACKIN is not asserted. Asserting IACKN only starts the BIM activity. If the daisy chain signal never reaches the BIM (IACKIN is not asserted), another inter rupter has responded to the IACK cycle. The cycle will end, the IACK is negated, and no additional action is required.

2. Pass on the interrupt daisy chain — For this case, IACKIN input is asserted by the preceding daisy chain interrupter, and IACKOUT output is in turn asserted. The daisy chain signal is passed on when no interrupts are pending on a matching level or when any possible interrupts are dis abled. The Interrupt Enable (IRE) bit of a control register can disable any interrupt requests, and in turn, any possible matches

3. Respond internally — For this case, IACKIN is asser-ted and a match is found. The BIM completes the IACK cycle by sup plying an interrupt vector from the proper vector register followed by a DTACK signal asserted because the interrupt acknowl edge cycle is completed by this device. For the BIM to respond in this mode of operation, the EXTERNAL/INTERNAl con trol register bit (X/IN) must be zero. For each source of interrupt request, the asso ciated control register determines the BIM response to an IACK cycle, and the X/IN bit sets this response either inter-nally (X/IN =.0) or externally (X/IN = !).

4. Respond externally — For the final case, IACKIN is also asserted, a match is found and the associated control register has X/IN bit set to one. The BIM does not assert IACKOUT and does assert INTAE low.INTAE signals that the requesting device must com-plete the IACK cycle (supplying a vector and DTACK) and that the 2-bit code contained on outputs INTA LO and INTAL1 shows which interrupt source is being acknowledged

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VMEbus /VERSAbus INTERFACE BLOCK DIAGRAM