Preliminary

GENERAL DESCRIPTION

EM73475 is a highly-integrated digital answering machine controller in which control function and signal amplification capability are integrated into a monolithic device. The EMC EM73400 based 4-bit controller contains 4K-byte ROM, 244-nibble RAM, 5 interrupt sources, a melody generator, two 12-bit timer/counters, a time-based interrupt and 14 general purpose I/O pins to provide interfaces with keyboard, LED display, DAA circuit, tape mechanism and DTMF detection circuit etc. Total component counts and production cost can therefore be reduced.
The linear amplifier portion combines all necessary amplifiers with Automatic Level Control function for signal amplification and conditioning, analog switches and digital attenuator, designed to provide the most integrated design for the Single Deck Tape-Based Telephone Answering Device applications.

FEATURES

4-bit controller of EM73475 is based on EMC EM73400 family which provides:

- Operating voltage : 4.5 to 5.5 V. (System clock frequency : 3.58 MHz).
- Clock source : Single clock system available for resonator or crystal and external clock source by mask option.
- Instruction set : 108 powerful instructions with cycle time of less than 2.2μs (fosc=3.58MHz)
- ROM capacity : 4K x 8 bits.
- RAM capacity : 244 x 4 bits.
- Input port : 2 port (3 bits)
  Port 12 : Schmitt trigger. (SCH1, SCH2)
  Port 14/ (Wakeup) : Pull up resistor and sleep/hold releasing function are available by mask option.
- I/O port : 5 ports (19 bits)
  Port 1, 2 : R-option, push-pull or NMOS open drain, high current output for driving LED.
  Port 7 : push-pull or open drain available by mask option.
  Port 8,9 : Initial high/low, push-pull or open drain available by mask option.
- 12-bit Timer/Counters : Two 12-bit Timer/Counters are programmable for timer, event counter, or pulse width measurement mode.
- Built-in Time Base : 8 kinds of frequencies.
- Subroutine nesting : Up to 13 levels.
- Interrupt : External ... 2 Input interrupt sources.
  Internal .... 2 Timer overflow interrupts. 1 Time base interrupt.
- Power saving function : Sleep function, CPU hold internal state and stop oscillating.
  Hold function, CPU hold internal state and oscillator still working.
- Data Pointer (DP) : Data conversion or table look-up.
- Built-in melody : Programmable melody generator.

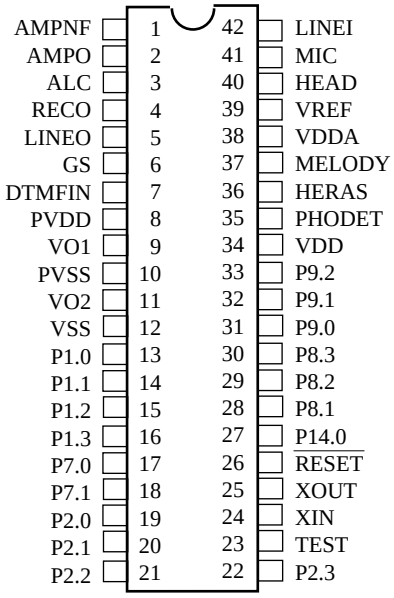
Built-in Amplifiers for Telephone Answering Device Application.

- SCF based with full DTMF detection for remote control.
- Pre-Amplifier for Tape Head, Microphone, Telephone Line signal Amplification
- Automatic Level Control to accommodate wide range of signal amplitude
- Differential output type power amplifier drive speaker directly.
- LineO amplifier, Speaker amplifier buffer and Mute function.
- Sixteen stage digital attenuator for implementing Digital Volume Control with no extra cost.
- Complete set of analog switches configurable for all operation modes required by TAD applications.
- Package : SDIP 42.

Preliminary

PIN ASSIGNMENT

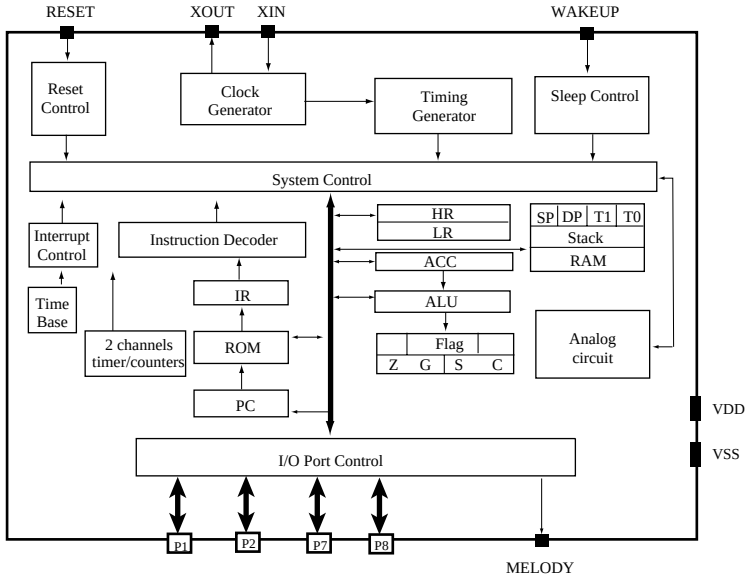
EM73475



S-DIP

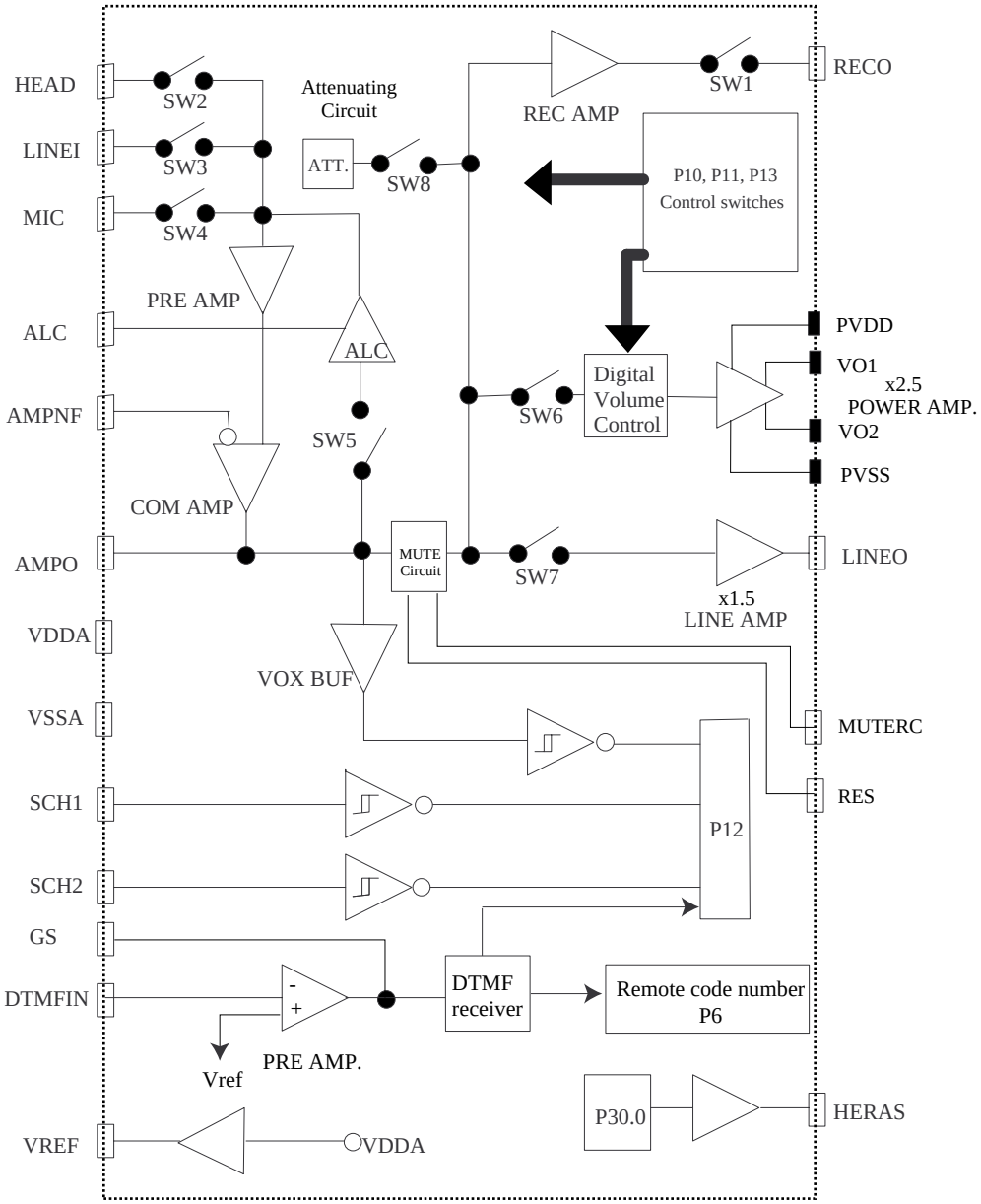
FUNCTIONAL BLOCK DIAGRAM

Digital Circuit



Preliminary

Analog Circuit



PIN DESCRIPTIONS

Preliminary

Symbol	Function
VDDA, VSSA	Power supply (+, -) for analog circuit.
*SCH1,*SCH2	Schmitt trigger 1, 2.
PVDD, PVSS	Power supply (+,-) for power amplifier.
VO1, VO2	Audio signal output to speaker for differential output, direct drive speaker.
LINEO	Audio signal output to telephone line.
ALC	Automatic Level Control adjustment pin. (R=68k, C=22μF is connected to VSSA)
AMPO	The COM-amplifier output.
AMPNF	The negative feedback input of COM-amplifier.
VREF	Analog circuit reference voltage output.
MIC	Microphone input.
LINEI	Telephone line input.
HEAD	Play head signal input.
RECO	Audio signal output for recording in RECORD mode, otherwise it presents a high impedance state.
HERAS	Erase bias current output.
*RES	Set the noise level of mute function for active and deactive threshold. (R=50K~180K is connected to VREF)
*MUTERC	Set the mute active response time adjustment pin. (R=560K~820K, C=1μF is connected to VSSA) Note : The RC time constant of mute function must be designed at the value that large than the RC time constant of ALC function.
MELODY	Melody generator output pin.
DTMFIN	DTMF signal input with the negative feedback input of amplifier.
GS	Gain select and DTMF-amplifier output.
VDD, VSS	Power supply (+, -) for digital circuit.
P1.0 ~ P1.3 P2.0 ~ P2.3	I/O port with high current sink NMOS for directly driving LEDs mask option : R-option enable, push-pull or open drain.
P7.0, P7.1 *P7.2, *P7.3	General purpose I/O ports. mask- option : push-pull or open drain.
P8.0(INT1) P8.1(TRGB) P8.2(INT0) P8.3(TRGA)	I/O port. (initial : high/low active) P8.0 with external interrupt (INT1) input. P8.1 with timer 1 external pin (TRGB). P8.2 with external interrupt (INT0) input. P8.3 with timer 0 external pin (TRGA). mask option : push-pull or open drain, initial high/low active.
P9.0 ~ P9.2	General purpose I/O ports. mask option : push-pull or open drain, initial high/low active.
XIN, XOUT	Oscillator (or resonator) input/output. For external clock input, XIN is used and XOUT is left open.
RESET	System reset input, active low Internal pull up or none by mask option.
TEST	No connection, reserved for testing.
WAKEUP	1-bit input pin shared with WAKEUP pin. mask option : Internal pull up or none.

* : not available for S-DIP 42

Preliminary

FUNCTION DESCRIPTIONS

The controller of EM73475 is based on EMC EM73400 family 4-bit controller. For detailed Function description of the controller, please refer to specifications of EM73400 series single clock 4-bit controller and 4-Bit Controller Programming Guide. The following is a brief description of EM73475 function blocks.

Memory configuration

Program ROM

The 4K bytes of ROM can be used to store user's program, constants, look-up-tables, and conversion tables, etc. It can be divided into 5 sections.

a. Address 000H : Reset start address.
b Addresses 002H - 00CH : 5 interrupt service entry addresses.
c. Addresses 00EH - 086H : SCALL subroutine entry addresses.
d. Addresses 0000H-07FFH : LCALL subroutine entry address.
e. Address 0000H - 0FFFH : The data pointer (DP) to indicate to ROM address, then to get the ROM code data.
f. Addresses 000H - 0FFFH : Any section other than the above can be used for user's program code and constants.

FLAGS

There are 3 kinds of flag, CF (Carry flag), ZF (Zero flag) and SF (Status flag), these 3 1-bit flags are affected by arithmatic, logic and comparative ... operation.

All flags will be put into stack when an interrupt subrountine is served, and the flags will be restored after RTI instruction executed.

Data RAM

There is total 244-nibble data RAM from 00H to F3H which is divided into 6 parts:

a. Addresses 00H - 0FH : Zero page region.
b. Addresses 0C0H - 0F3H : Stack region.
c. Addresses 0F4H - 0FAH : Timer region.
d. Addresses 0FBH - 0FEH : Data pointer (DP) region.
e. Address 0FFH : Stack pointer region.
f. Addresses 00H - 0F3H : Data area.

Interrupt function

The EM73475 provides 5 interrupt sources:

a. Time base interrupt (TBI).
b. Timer 0 overflow interrupt (TRGA).
c. Timer 1 overflow interrupt (TRGB).
d. External interrupt (INT0).
e. External interrupt (INT1).

I/O port configuration

The data transfer with external circuits and the command/status/ data transfer with the internal circuit are performed by executing I/O instructions. There are 4 types of ports:

a. I/O port: : Data transfer with external circuit.
b. Command port: : Control of internal circuit.
c. Status port: : Status of internal circuit.
d. Data register: : Data transfer with internal circuit.

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Name	Type	Function
External I/O Ports		
P1	I/O	General purpose I/O. LED low nibble output with R-option.
P2	I/O	General purpose I/O. LED high nibble output with R-option.
P7	I/O	General purpose I/O.
P8	I/O	General purpose I/O.
P9	I/O	General purpose I/O.
P14	Input	CPU status.
Internal I/O Ports		
P6	Data input	Remote control code input port.
P10	Control	Analog switch control port.
P11	Control	Analog switch control port.
P12	Status	Status monitor port .
P13	Control	Volume control port.
P15	Control	DTMF validity lenght and INT1 trigger type control port
P16	Control	Sleep control port.
P20.3	Control	R-option control port.
P23	Control	Low nibble control port of melody generator.
P24	Control	High nibble control port of melody generator.
P25	Control	Time Base Interrupt control port.
P28	Control	Timer/Counter 1 control port.
P29	Control	Timer/Counter 2 control port.
P30	Control	Melody, erase head and VOX sensitivity selection control port.

External I/O ports

P1.0 ~ P1.3, P2.0 ~ P2.3

Type : I/O ports.
Mask option : R-option, push-pull or NMOS open drain type.
Applicable instructions : TFP p, b; TTP p, b; SEP p, b; CLP p, b; INA p; INM p; OUTA p; OUTM p; OUT #k, p.
Function : Port 1 and Port 2 are both 4-bit I/O ports with high current sink NMOS to drive LEDs.

P7.0 ~ P7.3

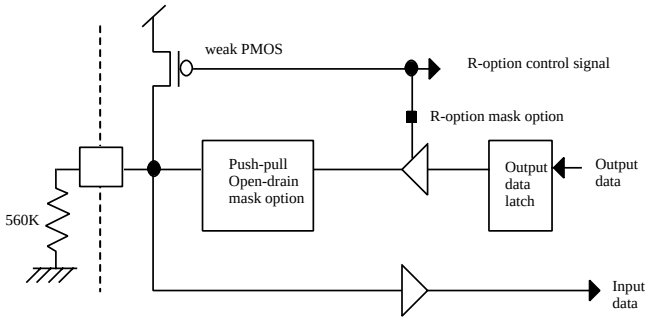
Type : I/O ports.
Mask option : Push-pull or NMOS open drain type.
Applicable instructions : TFP p, b; TTP p, b; SEP p, b; CLP p, b; INA p; INM p; OUTA p; OUTM p; OUT #k, p, CLPL, SEPL, TFPL.
Function : 4-bit general purpose I/O ports. Each pin of P6 and P7 can be set, cleared and tested by instruction of SEPL, CLPL and TFPL which is specified by L register. The relation of L register with P6 and P7 is as below:

LR = C→ P7.0
LR = D → P7.1
LR = E → P7.2
LR = F → P7.3

Preliminary

R-option function

The ports P1, P2 are equipped with R-option which provide extra for I/O pins. For example, it can be used as a normal I/O pin as firmware option. When the R-option is disabled, the I/O pin is a normal I/O pin. When the R-option function is enabled, this I/O pin can be used as an input pin to detect external status of this pin. The structurs of the I/O pin with R-option function is presented below :



R-option provides the Hi-impedance function for output driver and use the weak PMOS to pull up. When the R-option control signal P20.3 is high (R-option disabled), the weak PMOS is turned off and the output data latch is in the normal mode. In this case, there are two options (push-pull, open-drain) for this I/O pin. When the R-option control signal P20.3 is low (R-option enabled), the weak PMOS turns on and the driver of output data latch presents a Hi-impedance state. In this case, the external R-option status can be detected as low when this pin connects through a 560KΩ external resistor to GND, high when this pad is open.

P8.0/INT1; P8.1/TRGB; P8.2/INT0; P8.3/TRGA

Type : I/O Port with hysteresis type inputs.
Mask option : Initial high/low active, Push-pull or NMOS open drain type.
Related instruction : TFP p, b; TTP p, b; SEP p, b; CLP p, b; INA p; INM p; OUTA p; OUTM p; OUT #k, p.
Function : Port 8 is a 4-bit I/O port with special interrupt and timer/counter inputs.
P8.0/INT1 and P8.2/INT0 can be the external interrupt input pins for INT1 and INT0;
P8.1/TRGB, P8.3/TRGA can be the external timer/counter inputs for Timer 1 and Timer 0, respectively.
INT1 accepts falling edge and both edge trigger determined by internal command port P15.3.

P8

bit 3	bit 2	bit 1	bit 0	
1/0	1/0	1/0	1/0	Initial Value
TRGA	INT0	TRGB	INT1	

P15

bit 3	bit 2	bit 1	bit 0	
1	*	*	*	Initial Value
INT1T	*	*	GT	

INT1T (INT1 trigger Type)

0 : Both Edge Trigger
1 : Falling Edge Trigger

GT (Guard Time Adjustment) ; see page 13

Preliminary

P9.0~P9.2

Type : I/O Port with hysteresis type inputs.
Mask: option : Initial high/low active, Push-pull or NMOS open drain type.
Applicable instruction : TFP p, b; TTP p, b; SEP p, b; CLP p, b; INA p; INM p; OUTA p; OUTM p; OUT #k, p.
Function : Port 9 is a 3-bit I/O port.

P9

bit 3	bit 2	bit 1	bit 0	
*	1/0	1/0	1/0	Initial Value

WAKEUP/P14.0

Type : Input port with hysteresis type input.
Mask option : Pull-up resistor or none.
Function : Input pin for releasing sleep condition (active high).

P14

bit 3	bit 2	bit 1	bit 0	
*	*	*	1	Initial Value
*	*	*	SLEEP	

Internal command I/O ports

Analog switches control ports (P10 and P11)

P10 and P11 control the ON/OFF state of internal analog switches and can be configured to any mode as demanded by applications.

All switches are initialized to "0" during reset. These two ports can be set, cleared and tested for each bit as specified by "SET"or ‘"CLR" instructions.

			State	
Port	**Name**	**Description**	**0**	**1**
P10.3	SW1	Record amplifier output path	OFF	ON
P10.2	SW2	HEAD input path	OFF	ON
P10.1	SW3	LINEI input path	OFF	ON
P10.0	SW4	MIC input path	OFF	ON
P11.3	SW5	ALC comparator path	OFF	ON
P11.2	SW6	Audio path to digital attenuator	OFF	ON
P11.1	SW7	Audio path to Line buffer	OFF	ON
P11.0	SW8	Attenuate audio signal	OFF	ON

Preliminary

Examples:

a) ICM Record mode: This mode is used to record the Incoming Messages through Telephone line.

PORT NAME	P10				P11			
BIT NUMBER	bit 3	bit 2	bit 1	bit 0	bit 3	bit 2	bit 1	bit 0
CONTENT	1	0	1	0	1	1	0	0

b) ICM Playback mode: This mode is used to remotely play back the Incoming Messages.

PORT NAME	P10				P11			
BIT NUMBER	bit 3	bit 2	bit 1	bit 0	bit 3	bit 2	bit 1	bit 0
CONTENT	0	1	0	0	0	1	1	0

c) OGM out mode: This mode is for playing OGM to the calling party via telephone line.

PORT NAME	P10				P11			
BIT NUMBER	bit 3	bit 2	bit 1	bit 0	bit 3	bit 2	bit 1	bit 0
CONTENT	0	1	0	0	0	1	1	0

d) OGM change mode: This mode is intended for changing the OGM with a remote phone.

PORT NAME	P10				P11			
BIT NUMBER	bit 3	bit 2	bit 1	bit 0	bit 3	bit 2	bit 1	bit 0
CONTENT	1	0	1	0	1	1	0	0

Status monitor port (P12)

The internal input port P12 reflects the status of VOX, SCH1 and SCH2 inputs. The bit 2 of P12 is VOX (Voice signal detection bit), bit 1 is SCH1 (Schmitt trigger 1) and bit 0 is SCH2 (Schmitt trigger 2).

P12

bit 3	bit 2	bit 1	bit 0	
1	1	1	1	Initial Value
StD	VOX	SCH1	SCH2	

VOX signal detection bit

0 : The voltage of AMPO pin ≥ V_{REF}+VOXt2.
1 : The voltage of AMPO pin ≤ V_{REF}-VOXt1.

User can select among four sets of VOXt1 and VOXt2 based on the requirements of the applications. For further details, please refer to the descriptions in the paragraph of VOX sensitivity control port (P30.3, P30.2) of this document.

SCH1 bit

0 : SCH1 pin is > 0.7 V_{DD}.
1 : SCH1 pin is < 0.3 V_{DD}.

SCH2 bit

0 : SCH2 pin > 0.7 V_{DD}.
1 : SCH2 pin < 0.3 V_{DD}.

StD pin : Delayed steering input; see page 13

Preliminary

Digital volume control port (P13)

The port P13 controls the level of audio signal output to power anplifier. Programming P13 to be 0000B to get the maximum, and 1111B to get silence.

P13

bit 3	bit 2	bit 1	bit 0	
0	0	0	0	Initial Value
ST8	ST4	ST2	ST1	

The audio signal output level is attenuated as follows:

Stage 0	0000 :	0 dB	Stage 8	1000 :	-18.7 dB
Stage 1	0001 :	- 2.3 dB	Stage 9	1001 :	-21.1 dB
Stage 2	0010 :	- 4.6 dB	Stage 10	1010 :	-23.5 dB
Stage 3	0011 :	- 6.9 dB	Stage 11	1011 :	-26.2 dB
Stage 4	0100 :	- 9.2 dB	Stage 12	1100 :	-28.5 dB
Stage 5	0101 :	-11.5 dB	Stage 13	1101 :	-31.0 dB
Stage 6	0110 :	-13.9 dB	Stage 14	1110 :	-33.5 dB
Stage 7	0111 :	-16.3 dB	Stage 15	1111 :	silence

SLEEP control port (P16)

P16

bit 3	bit 2	bit1	bit0	
1	*	1	1	Initial Value
WURM		WUWT		

WURM (Wake-Up Release Mode)

* 0 : Reserved.
0 1 : wake-up in edge release mode.
1 1 : wake-up in level release mode.

WUWT (Wake-Up Warm-up Time)

0 0 : 2^18 / XIN.
0 1 : 2^14 / XIN.
1 0 : 2^16 / XIN.
1 1 : Zero warm-up time for external clock mode.

INT1 trigger type control port (P15.3)

INT1 accepts falling edge or both edge trigger controlled by internal command port P15.3. It is useful for tape positioning and tape-end detection function.

P15

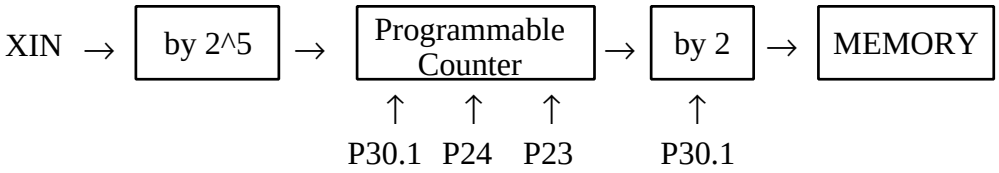
bit 3	bit 2	bit 1	bit 0	
1	*	*	0	Initial Value
INT1T	*	*	GT	

INT1T (INT1 trigger Type)

0: Both Edge Trigger
1: Falling Edge Trigger

Preliminary

Melody generator control port (P23, P24 and P30.1)



The melody generator consists of a XIN/2^5 clock source (if XIN = 3.58 MHz, the clock source is 112 KHz) and a 8-stage programmable binary counter. The internal ports P23 and P24 control low-nibble and high-nibble of the counter respectively. The contents of P23 and P24 will be loaded into programmable counter automatically when OUTA P23 or OUTM P23 instruction is executed. Bit 1 of P30 controls ON/OFF of melody generator.

P23

bit 3	bit 2	bit 1	bit 0	
0	0	0	0	Initial Value

P24

bit 7	bit 6	bit 5	bit 4	
0	0	0	0	Initial Value

P30

bit 3	bit 2	bit 1	bit 0	
*		1	1	Initial Value
*		DIMLD	DIEHD	

DIMLD : Melody generator enable/disable bit

0 = enable
1 = disable

Note :

a) If DIMLD bit is "1" the melody generator is disabled and the MELODY pin is switched to "low" level; if the b7 to b0 are 00000000 and DIMLD is 0, the MELODY pin is switched to "high" level, otherwise the MELODY pin will issue melody tone.

b) The MELODY frequency = XIN / 2^5 /(b7, b6, b5, b4, b3, b2, b1, b0)/2

Preliminary

Time Base Interrupt control port (P25)

The time base can be used to generate a fixed frequency interrupt. 4 frequencies are available which can be selected by setting P25 as follows:

P25

bit 3	bit 2	bit 1	bit 0	Interrupt Frequency
0	0	0	0	Initial Value
0	0	*		Interrupt Disabled
0	1	0	0	XIN/2^10=3496 Hz
0	1	0	1	XIN/2^11=1748 Hz
0	1	1	0	XIN/2^12=874 Hz
0	1	1	1	XIN/2^13=437 Hz
1	*			Reserved

For XIN = 3.58 MHz

Timer/Counter 0, Timer/Counter 1 control ports (P28, P29)

The P28 and P29 control the operating modes of Timer/Counter 0 and Timer/Counter 1 respectively.

P28

bit 3	bit 2	bit 1	bit 0	
0	0	0	0	Initial Value
TMS0		IPS0		

P29

bit 3	bit 2	bit 1	bit 0	
0	0	0	0	Initial Value
TMS1		IPS1		

The Timer/Counters can be configured to operate in one of three modes:

a. Event counter.
b. Timer.
c. Pulse-width measurement.

TMS (Timer/counter Mode Selection)

0	0	Stop.
0	1	Event counter mode.
1	0	Timer mode.
1	1	Pulse width measurement mode.

IPS (Internal Pulse-rate Selection)

0	0	XIN/2^10 Hz
0	1	XIN/2^14 Hz
1	0	XIN/2^18 Hz
1	1	XIN/2^22 Hz

Preliminary

DTMF remote code input port (P6) and Delayed steering input (P12.3)

DTMF input		Key	P12.3	Port 6			
F-low	F-high	number	StD	bit 3	bit 2	bit 1	bit 0
697	1209	1	0	0	0	0	1
697	1336	2	0	0	0	1	0
697	1477	3	0	0	0	1	1
770	1209	4	0	0	1	0	0
770	1336	5	0	0	1	0	1
770	1477	6	0	0	1	1	0
852	1209	7	0	0	1	1	1
852	1336	8	0	1	0	0	0
852	1477	9	0	1	0	0	1
941	1209	*	0	1	0	1	0
941	1336	0	0	1	0	1	1
941	1477	#	0	1	1	0	0
697	1633	A	0	1	1	0	1
770	1633	B	0	1	1	1	0
852	1633	C	0	1	1	1	1
941	1633	D	0	0	0	0	0
X	X	X	1	X	X	X	X

X : Don't care.

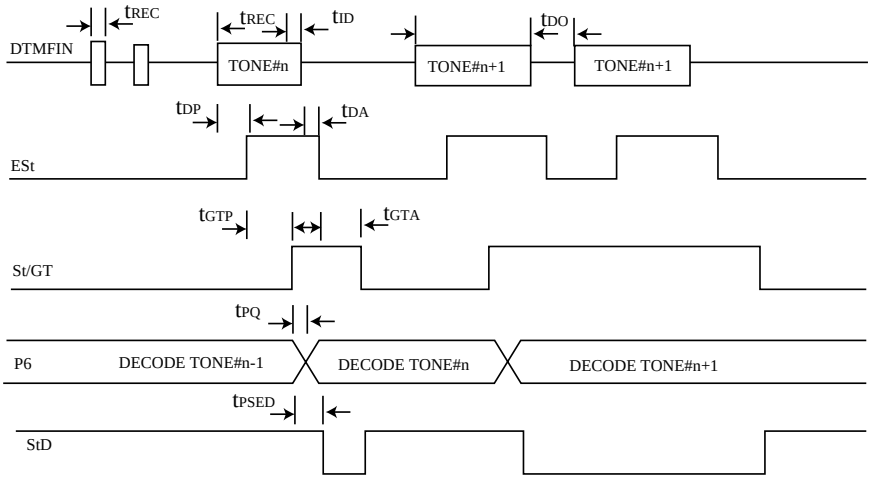
StD (P12.3) : Delayed steering input. (internal port)

P15

bit 3	bit 2	bit 1	bit 0	
1	*	*	0	Initial Value
INT1T	*	*	GT	

GT (GTP : Guard Time Present; GTA : Guard Time Absent)
0 : 20 ms
1 : 30 ms

TIMING DIAGRAM ; see page 17



Preliminary

VOX sensitivity, Melody, Erase-head control port (P30)

The VOXLVL1, VOXLVL0 bits control sensitivity of VOX schmitt trigger. The user can select the required sensitivity among 4 levels available based on the needs of the applications.

P30	bit 3	bit 2	bit1	bot 0
Name	VOXLVL1	VOXLVL0	DIMLD	DIEHD
Initial Value	1	1	1	1

Sensitivity

VOXLVL1	VOXLVL0	VOXt1	VOXt2
1	1	VREF-0.4 VDC	VREF+0.4VDC
1	0	VREF-0.3 VDC	VREF+0.3VDC
0	1	VREF-0.15 VDC	VREF+0.15VDC
0	0	VREF-0.1 VDC	VREF+0.1VDC

Mute function

Mask option : Enable or Disable mute function.

Function : When the MUTE function is enabled, the EM73475 supports the noise-reduced function. This function is designed to suppress (MUTE) the white noise at the duration of silence in message play mode. The suppressing level and suppressing active response time can be tuned by RES pin and MUTERC pin.
When the MUTE function is disabled, the RES and MUTERC pins must be open.

Preliminary

ABSOLUTE MAXIMUM RATINGS

Items	Sym.	Rating	Condition
Supply Voltage	V_{DD}	-0.3 to 6 V	
Input Voltage	V_{IN}	-0.3 to V_{DD}+0.3 V	
Output Voltage	V_O	-0.3 to V_{DD}+0.3 V	
Output Current	I_O	30 mA 3.2 mA	Port P1 and P2 Port P6, P7, P8, P9, Melody
Power Dissipation	P_D	300 mW	T_{OPR}=50 °C
Operating Temperature	T_{OPR}	0 to 50 °C	
Storage Temperature	T_{STR}	-50 to 125 °C	

ELECTRICAL CHARACTERISTICS (V_{SS} = 0V, V_{DD} = 5.0 V, fosc=3.58 MHz unless otherwise noted)

Parameter	Sym.	Min.	Typ.	Max.	Unit	Condition
Supply Voltag	V_{DD}	4.5	5	5.5	V	
Input Voltage	V_{IH} V_{IL}	0.8 0	- -	1 0.2	 V_{DD}	 V_{DD} =4.5V ~ 5.5V
Supply Current	I_{DD} $I_{DD\,S}$	-	10 -	15 5	mA µA	Normal Mode, fosc=3.58MHz Sleep Mode V_{DD} = 5.5V, No load
Input Current	I_{IH}	-	-	2	µA	TEST, RESET & WAKEUP pins without pull up/down resistor
Input Current	I_{IL}	-	-	2	mA	Push-pull output pin,V_{DD} =5.5V, V_{IN} = 0.4V
Input Resistance	R_{IN}	100 30	220 70	450 150	Kohm	RESET, V_{DD} = 5.5V WAKEUP, V_{DD}= 5.5V
Open drain Output pin leakage current	I_{LK}	-	0.01	2	µA	V_{DD} = 5.5V, V_{OUT} = 5.5V
Melody Output Current	I_{MOH} I_{MOL}	0.5 0.5	- -	- -	mA	V_{DD} = 4.5V, V_{MO} = 4.0V V_{DD} = 4.5V, V_{MO} = 0.5V
P1, P2, P7, P8, P9 Output Voltage	V_{OH}	2.4	-	-	V	V_{DD} = 4.5V, I_{OH} = 200 uA
P7, P8, P9 Output Voltage	V_{OL}	-	-	0.4		V_{DD} = 4.5V, I_{OL} = 1.6 mA
P1, P2 Output Voltage	V_{OL}	-	-	1.2	V	V_{DD} = 4.5V, I_{OL} = 20 mA

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ELECTRICAL CHARACTERISTICS (V_{SS} = 0V, V_{DD} = 5.0 V, fosc=3.58 MHz unless otherwise noted)

Parameter	Sym.	Min.	Typ.	Max.	Unit	Condition
OP-AMP General Specification						
Power Supply Rejection Ratio	PSRR	-	60	-	dB	
DC open loop voltage gain	AVOL	-	65	-	dB	
Open Loop Unit Gain Bandwidth	FC	-	1.5	-	MHz	
Output Voltage Swing	VO	-	1.6	-	VPP	ALC ON
	VO	-	-	3.0	VPP	ALC OFF
Pre-Amplifier Specification						
Voltage Gain for LINE1 Input	GainL	9	9.5	10	dB	
Voltage Gain for MIC input	GainM	19.5	20	20.5	dB	
Voltage Gain for HEAD	GainH	31	32	33	dB	
COM-Amplifier Specification						
Voltage Gain	GainC	49	50	51	dB	Note 1
COM-Amp Output Voltage with ALC turned on	Vpre	470	550	620	mVrms	Note 1
ALC Circuit Specification						
ALC turn on voltage point	Valcon	-53	-	-	dBm	Notes 1, 2, 3, 4
ALC operating range	ALCR	36	40	44	dB	Notes 1, 4
ALC saturation Voltage	VALC	4.8	-	-	V	Notes 1, 5, 6
Line Amplifier Specification						
Voltage Gain	GainL	-	3.5	-	dB	
Volume Buffer						
Voltage Gain	GainV	-	0	-	dB	
Miscellaneous						
Source Current of REC Amplifier	Ireco	200	400	600	μA	f=1 KHz, Rreco=5 Kohms Vrec0=550 mVrms
SCH1, SCH2 Input Voltage	VsH	0.7	-	1	V_{DD}	
	VsL	0	-	0.3	V_{DD}	
Source Current	IoeraH	6	8	12	mA	Vheras=2.5V
Sink Current of HERAS pin	IoeraL	0.2	0.5	2	mA	Vheras=0.5V
VREF Output Voltage	VREF	2.4	2.5	2.6	V	

Notes:

1. Refer to Test Circuit
2. dBm: Decibels referenced to one milliwatt into a 600 ohms load.
3. External sine wave signal connected to HEAD, LINEI, or MIC input pin.
4. COM-amplifier output voltage = 470 ~ 620 mVrms
5. Load resistance of ALC pin is 68 Kohms.
6. -27 dBm sine wave signal connected to LINEI, MIC, HEAD input pins.

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Parameter	Sym.	Min.	Typ.	Max.	Unit	Condition
Power Amplifier (PVDD= 5V, RL = 8ohm)						
Power Supply Voltage	PVDD	4.5	5	5.5	V	
Voltage Gain	Av	-	60	-	dB	1KHz
Bandwidth	BW	-	-	1	MHz	
Power Supply Rejection Ratio	PSRR	-	60	-	dB	1KHz
Total harmonic distortion	THD	-	0.5	1	%	I_{LP-P}= ±150mA,1KHz
Output voltage swing	VO	3.2	-	4	Vpp	|VO1-VO2|
VO1, VO2 offset voltage	VO_{1-2}	-	20	-	mV	
Quiescent Current	I_Q	-	3	-	mA	V_{IN}=0V
Output Current	P_{OUT}	-	-	250	mW	THD=10%
Short Circuit Current	I_S(max)	-	400	-	mA	
DTMF receiver gain setting amplifier						
Power Supply Rejection Ratio	PSRR	-	60	-	dB	1 KHz
DC open loop voltage gain	Avol	-	65	-	dB	
Open Loop Unit Gain Banwidth	fc	-	1.5	-	MHz	1 KHz
Output Voltage Swing	Vo	-	4.5	-	Vpp	RL≥100Kohm to V_{SS}
Valid Input Signal level (each tone signal)	V_I	-40	-	-	dBm	
		7.75	-	-	mVrms	
		-	-	+1	dBm	
		-	-	883	mVrms	
Dual Tone Rwist Accept	TW	-	±10	-	dB	
Acceptable Frequency Deviation	Δf	-	-	±1.5% ±2Hz	-	
Frequency Deviation Reject	Δf_R	±3.5%	-	-	-	
Third Tone Tolerance	T3rd	-	-16	-	dB	
Noise Tolerance	T_N	-	-12	-	dB	
Dial Tone Tolerance	DT	-	18	-	dB	
Crystal clock frequency	fck	3.5759	3.5795	3.5831	MHz	
DTMF receiver timing						
Tone Present Detection Time	t_{DP}	5	14	16	ms	
Tone Absent Detection Time	t_{DA}	0.5	4	8.5	ms	
Tone Duration Accept	t_{REC}	-	-	40	ms	
Tone Duration Reject	t_{REC}	20	-	-	ms	
Interdigit pause Accept	t_{ID}	-	-	40	ms	
Interdigit pause Reject	t_{ID}	20	-	-	ms	
Propagation Delay (St to Q)	t_{PQ}	-	8	11	μs	
Propagation Delay (St to StD)	t_{PSED}	-	12	-	μs	

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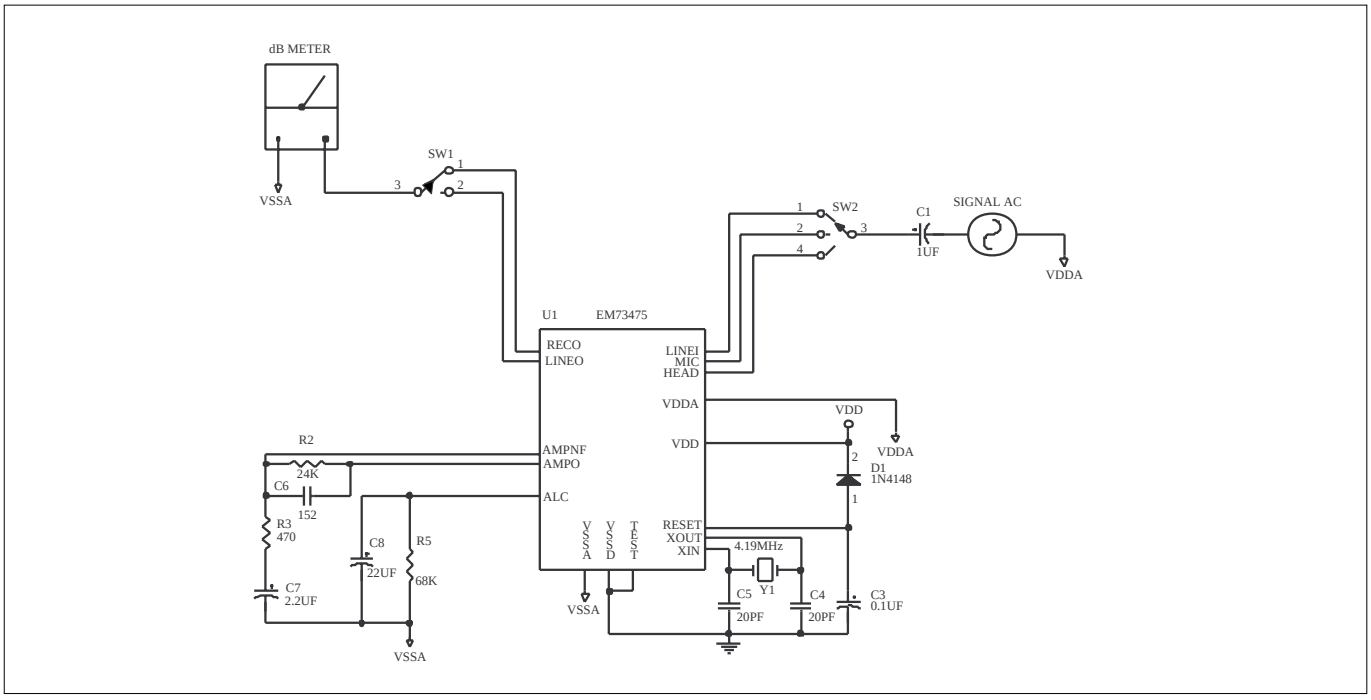
Note : 1. DBm = decibels above or below a reference power of 1mW into a 600 Ohm load.
2. Digit sequences consists of all 16 DTMF tones.
3. Tone duration = 10ms; Tone pause = 40ms.
4. Nominal DTMF frequencies are used.
5. Both tones in the composite signal have an equal amplitude.
6. Tone pair is deviated by ±1.5%±2Hz.
7. Bandwidth limited (3KHz) Gaussian Noise.
8. The precise dial tone frequencies are (350Hz and 440Hz)±2%.
9. For an error rate of less than 1 in 10,000.
10. Referenced to the lowest level frequency component in DTMF signal.
11. Added A 0.1μF capacitor between V_{DD} and V_{SS}.

TEST CIRCUIT



Frequency response (1KHz, 0dB, ALC OFF)

Testing path : signal (1KHz)→ Mic input → Amp output → Rec. output → Tape (Deck type : MEC. ML-756) → Head input → Amp output

S/N	-	34	-	dB
300 Hz	-	-7.5	-	dB
3 KHz	-	-7	-	dB

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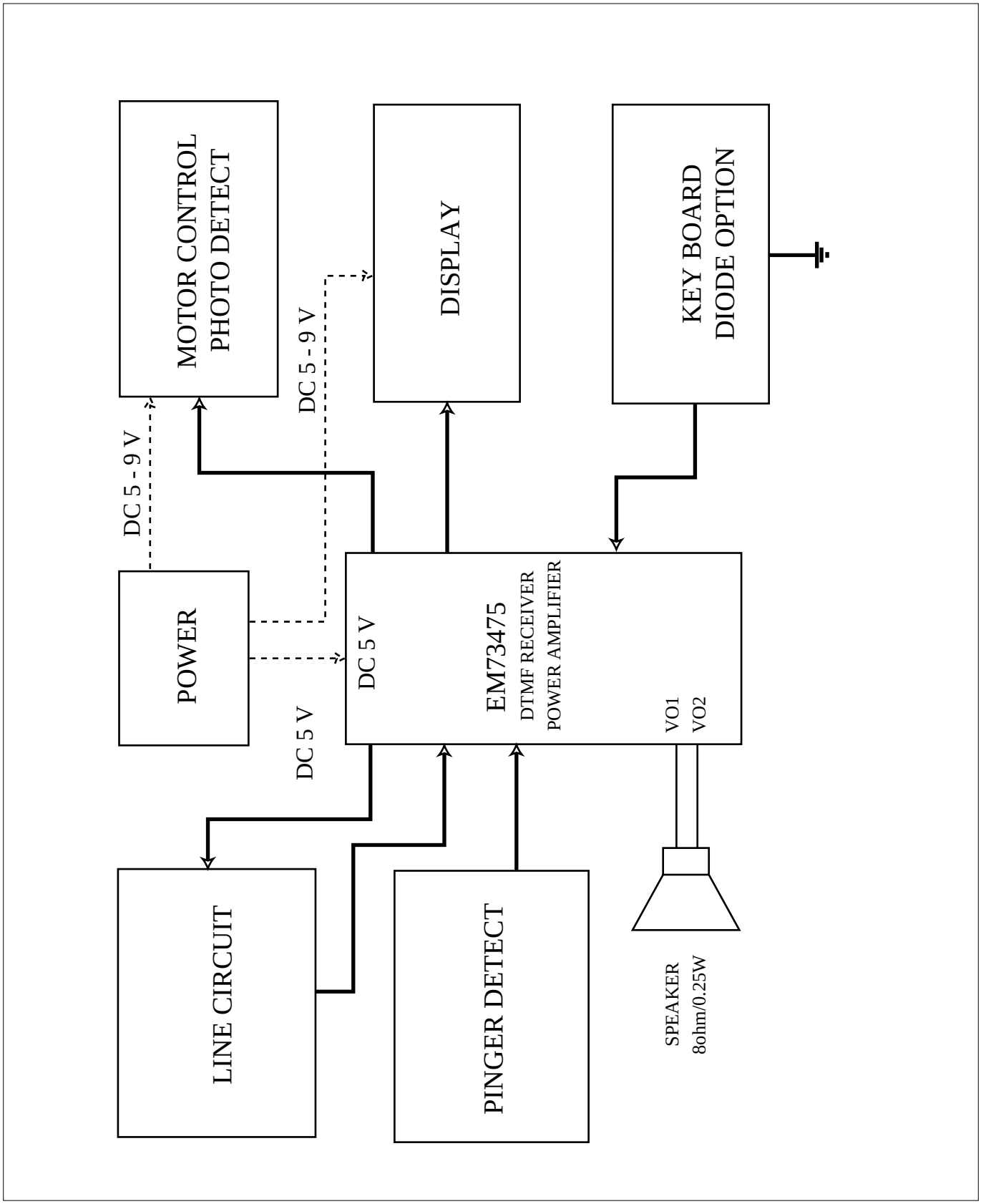
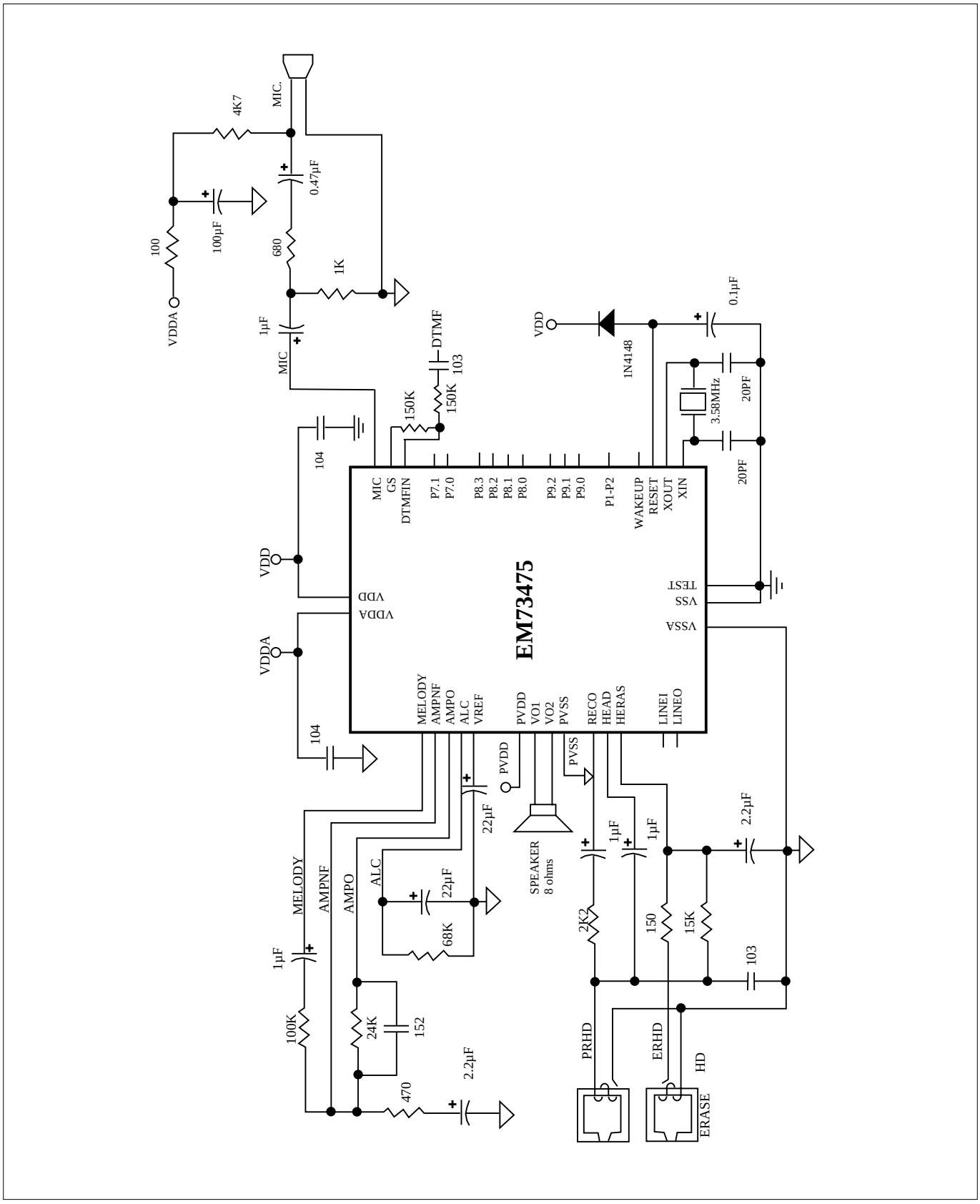
APPLICATION CIRCUIT(1)



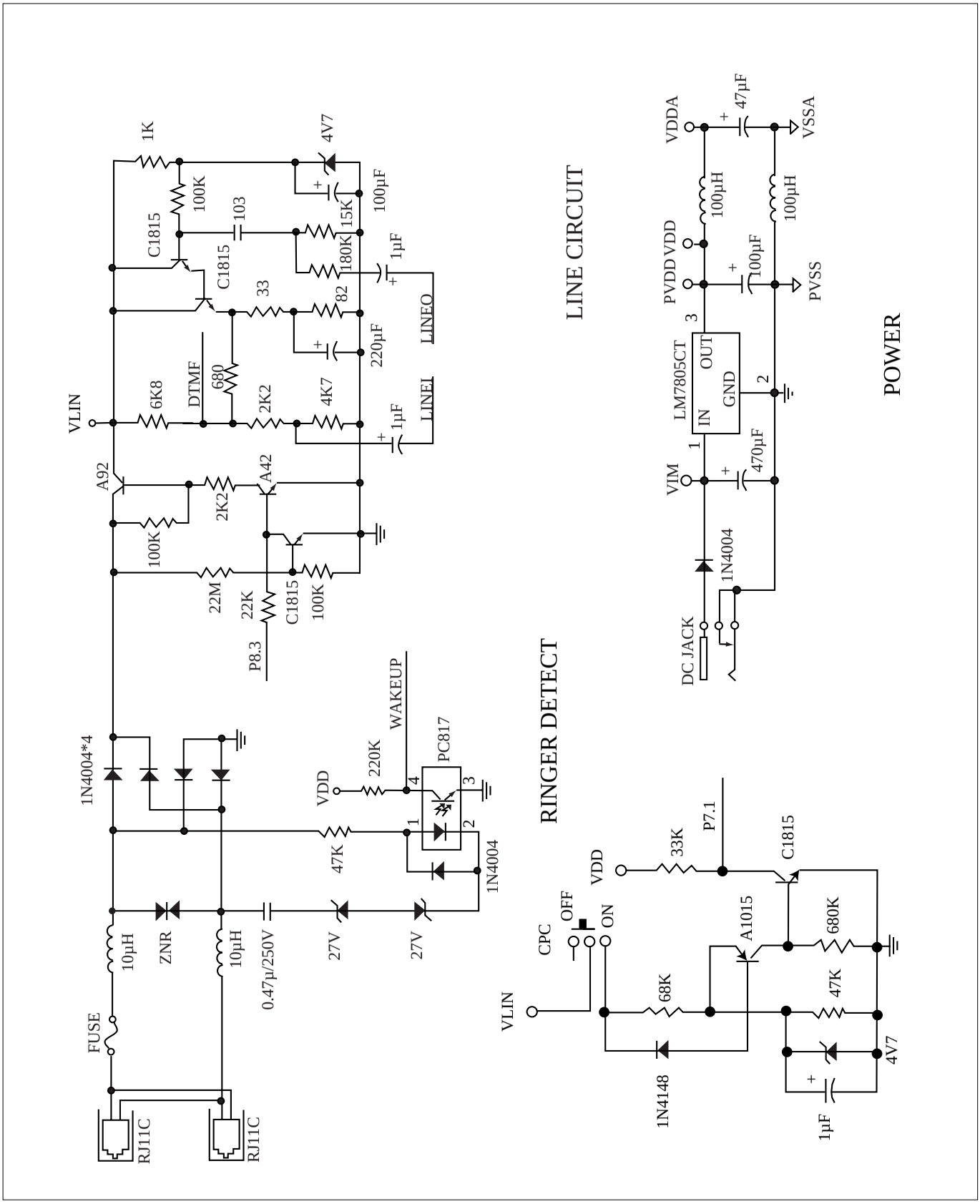
Preliminary

APPLICATION CIRCUIT(2)



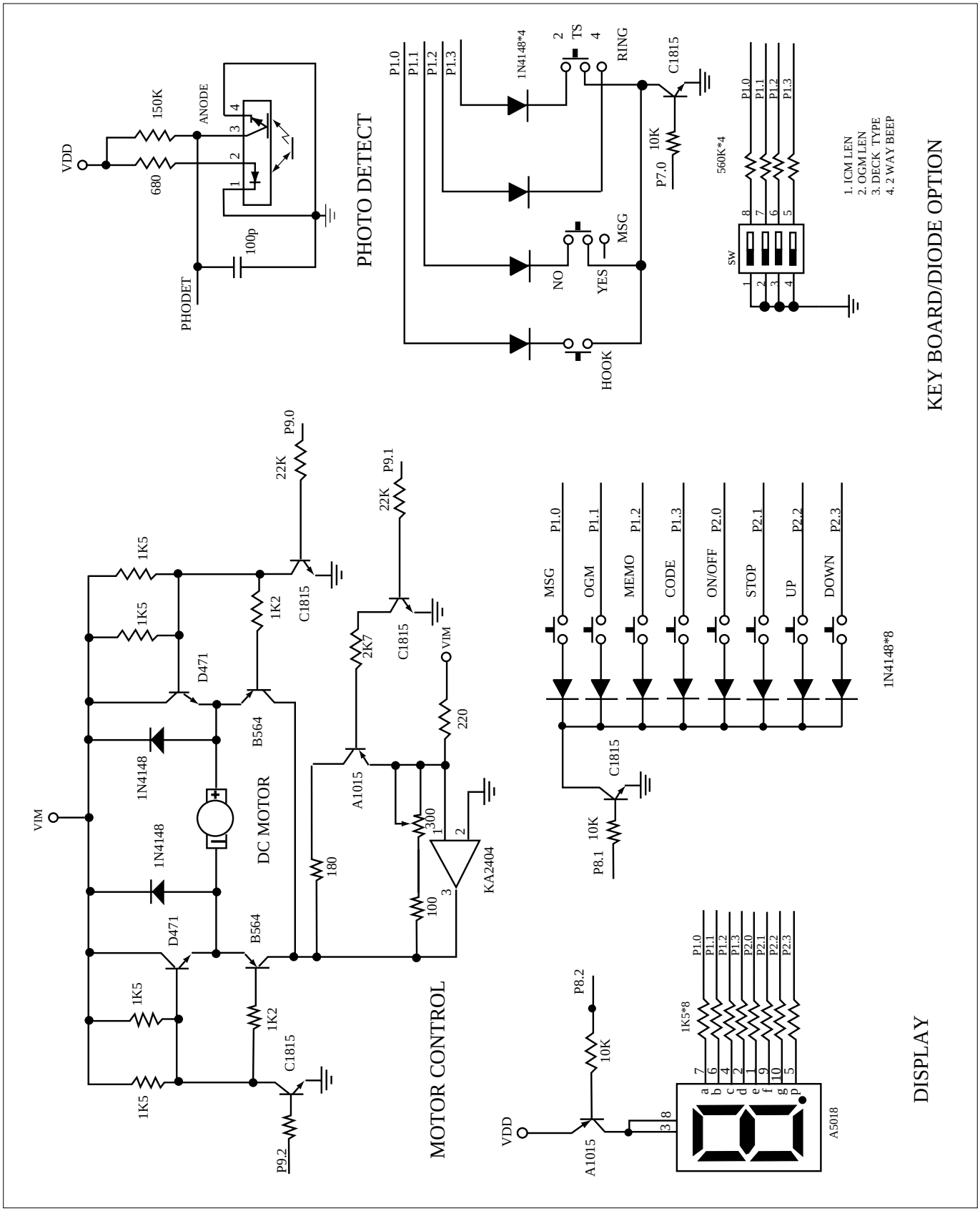
Preliminary

APPLICATION CIRCUIT(3)



Preliminary

APPLICATION CIRCUIT(4)



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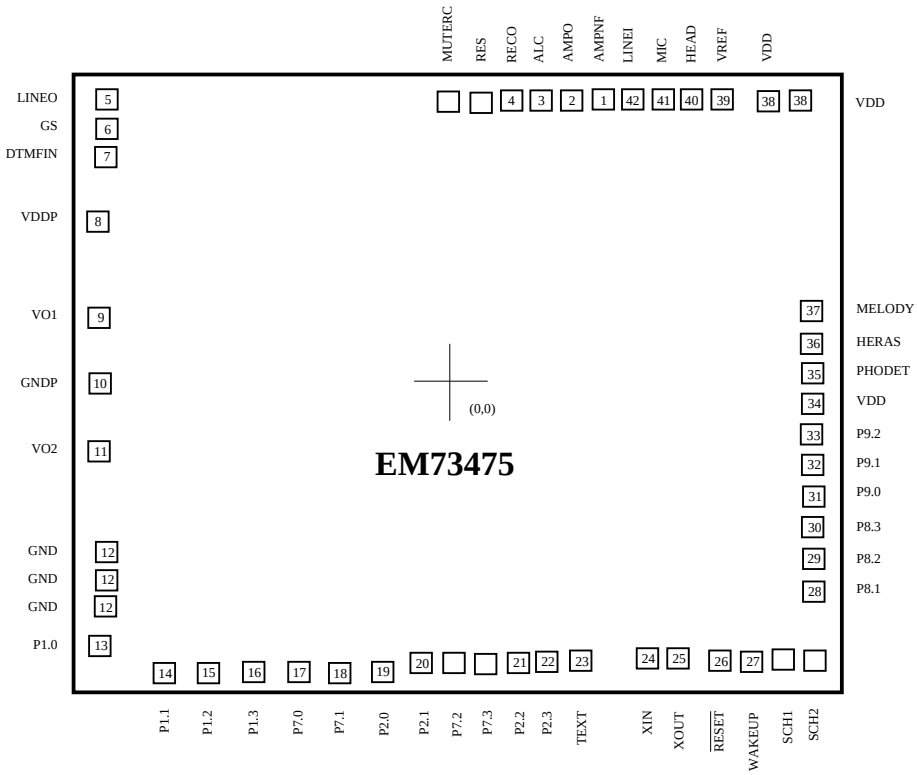
PAD DIAGRAM



Chip Size : 3880 μm x 3170 μm

PadNo.	Symbol	X	Y
1	AMPNF	711.1	1381.7
2	AMPO	560.5	1381.7
3	ALC	411.2	1381.7
4	RECO	255.2	1381.7
	RES	110.7	1381.7
	MUTERC	-45.2	1381.7
5	LINEO	-1727.7	1403.6
6	GS	-1727.7	1256.6
7	DTMFIN	-1731.6	1108.5
8	VDDP	-1768.7	800.1
9	VO1	-1768.7	326.5
10	GNDP	-1768.7	-1.5
11	VO2	-1768.7	-329.5
12	GND	-1742.0	-829.7
12	GND	-1742.0	-963.0
12	GND	-1742.0	-1100.9
13	P1.0	-1776.7	-1289.6
14	P1.1	-1462.8	-1428.2
15	P1.2	-1252.9	-1428.2
16	P1.3	-1031.7	-1428.2

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PadNo.	Symbol	X	Y
17	P7.0	-810.9	-1429.0
18	P7.1	-601.9	-1429.0
19	P2.0	-385.5	-1428.4
20	P2.1	-194.8	-1383.4
	P7.2	-37.9	-1393.0
	P7.3	113.6	-1393.0
21	P2.2	280.8	-1383.4
22	P2.3	421.8	-1383.4
23	TEST	583.3	-1373.2
24	XIN	914.1	-1373.2
25	XOUT	1061.1	-1371.5
26	$\overline{\text{RESET}}$	1271.9	-1386.3
27	WAKEUP	1429.4	-1386.3
	SCH1	1584.0	-1382.8
	SCH2	1735.2	-1382.8
28	P8.1	1729.8	-1042.8
29	P8.2	1729.8	-879.6
30	P8.3	1729.8	-719.8
31	P9.0	1729.8	-575.4
32	P9.1	1729.8	-413.4
33	P9.2	1729.8	-268.9
34	VDD	1731.5	-117.2
35	PHODET	1729.8	33.1
36	HERAS	1731.2	179.2
37	MELODY	1729.8	341.9
38	VDD	1685.0	1373.7
39	VREF	1301.4	1381.7
40	HEAD	1150.7	1381.7
41	MIC	1006.3	1381.7
42	LINEI	855.6	1381.7

Unit : μm

Note : For PCB layout, IC substrate must be floated, or connect to V_{SS} .

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INSTRUCTION TABLE

(1) Data Transfer

Mnemonic	Object code (binary)	Operation description	Byte	Cycle	Flag		
					C	Z	S
LDA x	0110 1010 xxxx xxxx	Acc←RAM[x]	2	2	-	Z	1
LDAM	0101 1010	Acc ←RAM[HL]	1	1	-	Z	1
LDAX	0110 0101	Acc←ROM[DP]$_L$	1	2	-	Z	1
LDAXI	0110 0111	Acc←ROM[DP]$_H$,DP+1	1	2	-	Z	1
LDH #k	1001 kkkk	HR←k	1	1	-	-	1
LDHL x	0100 1110 xxxx xx00	LR←RAM[x],HR←RAM[x+1]	2	2	-	-	1
LDIA #k	1101 kkkk	Acc←k	1	1	-	Z	1
LDL #k	1000 kkkk	LR←k	1	1	-	-	1
STA x	0110 1001 xxxx xxxx	RAM[x]←Acc	2	2	-	-	1
STAM	0101 1001	RAM[HL]←Acc	1	1	-	-	1
STAMD	0111 1101	RAM[HL]←Acc, LR-1	1	1	-	Z	C
STAMI	0111 1111	RAM[HL]←Acc, LR+1	1	1	-	Z	C'
STD #k,y	0100 1000 kkkk yyyy	RAM[y]←k	2	2	-	-	1
STDMI #k	1010 kkkk	RAM[HL]←k, LR+1	1	1	-	Z	C'
THA	0111 0110	Acc←HR	1	1	-	Z	1
TLA	0111 0100	Acc←LR	1	1	-	Z	1

(2) Rotate

Mnemonic	Object code (binary)	Operation description	Byte	Cycle	Flag		
					C	Z	S
RLCA	0101 0000	←CF←Acc←	1	1	C	Z	C'
RRCA	0101 0001	→CF→Acc→	1	1	C	Z	C'

(3) Arithmetic operation

Mnemonic	Object code (binary)	Operation description	Byte	Cycle	Flag		
					C	Z	S
ADCAM	0111 0000	Acc←Acc + RAM[HL] + CF	1	1	C	Z	C'
ADD #k,y	0100 1001 kkkk yyyy	RAM[y]←RAM[y] +k	2	2	-	Z	C'
ADDA #k	0110 1110 0101 kkkk	Acc←Acc+k	2	2	-	Z	C'
ADDAM	0111 0001	Acc←Acc + RAM[HL]	1	1	-	Z	C'
ADDH #k	0110 1110 1001 kkkk	HR←HR+k	2	2	-	Z	C'
ADDL #k	0110 1110 0001 kkkk	LR←LR+k	2	2	-	Z	C'
ADDM #k	0110 1110 1101 kkkk	RAM[HL]←RAM[HL] +k	2	2	-	Z	C'
DECA	0101 1100	Acc←Acc-1	1	1	-	Z	C
DECL	0111 1100	LR←LR-1	1	1	-	Z	C
DECM	0101 1101	RAM[HL]←RAM[HL] -1	1	1	-	Z	C
INCA	0101 1110	Acc←Acc + 1	1	1	-	Z	C'

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INCL	0111 1110	LR←LR + 1	1	1	-	Z	C'
INCM	0101 1111	RAM[HL]←RAM[HL]+1	1	1	-	Z	C'
SUBA #k	0110 1110 0111 kkkk	Acc←k-Acc	2	2	-	Z	C
SBCAM	0111 0010	Acc←RAM[HL] - Acc - CF'	1	1	C	Z	C
SUBM #k	0110 1110 1111 kkkk	RAM[HL]←k - RAM[HL]	2	2	-	Z	C

(4) Logical operation

Mnemonic	Object code (binary)	Operation description	Byte	Cycle	Flag		
					C	Z	S
ANDA #k	0110 1110 0110 kkkk	Acc←Acc&k	2	2	-	Z	Z'
ANDAM	0111 1011	Acc←Acc & RAM[HL]	1	1	-	Z	Z'
ANDM #k	0110 1110 1110 kkkk	RAM[HL]←RAM[HL]&k	2	2	-	Z	Z'
ORA #k	0110 1110 0100 kkkk	Acc←Acc ¦k	2	2	-	Z	Z'
ORAM	0111 1000	Acc ←Acc ¦ RAM[HL]	1	1	-	Z	Z'
ORM #k	0110 1110 1100 kkkk	RAM[HL]←RAM[HL]¦k	2	2	-	Z	Z'
XORAM	0111 1001	Acc←Acc^RAM[HL]	1	1	-	Z	Z'

(5) Exchange

Mnemonic	Object code (binary)	Operation description	Byte	Cycle	Flag		
					C	Z	S
EXA x	0110 1000 xxxx xxxx	Acc↔RAM[x]	2	2	-	Z	1
EXAH	0110 0110	Acc↔HR	1	2	-	Z	1
EXAL	0110 0100	Acc↔LR	1	2	-	Z	1
EXAM	0101 1000	Acc↔RAM[HL]	1	1	-	Z	1
EXHL x	0100 1100 xxxx xx00	LR↔RAM[x], HR↔RAM[x+1]	2	2	-	-	1

(6) Branch

Mnemonic	Object code (binary)	Operation description	Byte	Cycle	Flag		
					C	Z	S
SBR a	00aa aaaa	If SF=1 then PC←$PC_{12-6}.a_{5-0}$ else null	1	1	-	-	1
LBR a	1100 aaaa aaaa aaaa	If SF= 1 then PC←a else null	2	2	-	-	1
SLBR a	0101 0101 1100 aaaa aaaa aaaa (a:1000~1FFFh)	If SF=1 then PC←a else null	3	3	-	-	1
	0101 0111 1100 aaaa aaaa aaaa (a:0000~0FFFh)						

(7) Compare

Mnemonic	Object code (binary)	Operation description	Byte	Cycle	Flag		
					C	Z	S
CMP #k,y	0100 1011 kkkk yyyy	k-RAM[y]	2	2	C	Z	Z'
CMPA x	0110 1011 xxxx xxxx	RAM[x]-Acc	2	2	C	Z	Z'

Mnemonic	Object code (binary)	Operation description	Byte	Cycle	Flag		
					C	Z	S
CMPAM	0111 0011	RAM[HL] - Acc	1	1	C	Z	Z'
CMPH #k	0110 1110 1011 kkkk	k - HR	2	2	-	Z	C
CMPIA #k	1011 kkkk	k - Acc	1	1	C	Z	Z'
CMPL #k	0110 1110 0011 kkkk	k-LR	2	2	-	Z	C

(8) Bit manipulation

Mnemonic	Object code (binary)	Operation description	Byte	Cycle	Flag		
					C	Z	S
CLM b	1111 00bb	$RAM[HL]_b \leftarrow 0$	1	1	-	-	1
CLP p,b	0110 1101 11bb pppp	$PORT[p]_b \leftarrow 0$	2	2	-	-	1
CLPL	0110 0000	$PORT[LR_{3-2}+4]LR_{1-0} \leftarrow 0$	1	2	-	-	1
CLR y,b	0110 1100 11bb yyyy	$RAM[y]_b \leftarrow 0$	2	2	-	-	1
SEM b	1111 01bb	$RAM[HL]_b \leftarrow 1$	1	1	-	-	1
SEP p,b	0110 1101 01bb pppp	$PORT[p]_b \leftarrow 1$	2	2	-	-	1
SEPL	0110 0010	$PORT[LR_{3-2}+4]LR_{1-0} \leftarrow 1$	1	2	-	-	1
SET y,b	0110 1100 01bb yyyy	$RAM[y]_b \leftarrow 1$	2	2	-	-	1
TF y,b	0110 1100 00bb yyyy	$SF \leftarrow RAM[y]_b'$	2	2	-	-	*
TFA b	1111 10bb	$SF \leftarrow Acc_b'$	1	1	-	-	*
TFM b	1111 11bb	$SF \leftarrow RAM[HL]_b'$	1	1	-	-	*
TFP p,b	0110 1101 00bb pppp	$SF \leftarrow PORT[p]_b'$	2	2	-	-	*
TFPL	0110 0001	$SF \leftarrow PORT[LR_{3-2}+4]LR_{1-0}'$	1	2	-	-	*
TT y,b	0110 1100 10bb yyyy	$SF \leftarrow RAM[y]_b$	2	2	-	-	*
TTP p,b	0110 1101 10bb pppp	$SF \leftarrow PORT[p]_b$	2	2	-	-	*

(9) Subroutine

Mnemonic	Object code (binary)	Operation description	Byte	Cycle	Flag		
					C	Z	S
LCALL a	0100 0aaa aaaa aaaa	STACK[SP]←PC, SP←SP -1, PC←a	2	2	-	-	-
SCALL a	1110 nnnn	STACK[SP]←PC, SP←SP - 1, PC←a, a = 8n + 6 (n =1~15),0086h (n = 0)	1	2	-	-	-
RET	0100 1111	SP←SP + 1, PC←STACK[SP]	1	2	-	-	-

(10) Input/output

Mnemonic	Object code (binary)	Operation description	Byte	Cycle	Flag		
					C	Z	S
INA p	0110 1111 0100 pppp	Acc←PORT[p]	2	2	-	Z	Z'
INM p	0110 1111 1100 pppp	RAM[HL]←PORT[p]	2	2	-	-	Z'
OUT #k,p	0100 1010 kkkk pppp	PORT[p]←k	2	2	-	-	1
OUTA p	0110 1111 000p pppp	PORT[p]←Acc	2	2	-	-	1
OUTM p	0110 1111 100p pppp	PORT[p]←RAM[HL]	2	2	-	-	1
OUT12	0111 0111	PORT[2].PORT[1]← ROM[FE0h+CF.RAM[HL]]	1	2	-	-	1

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(11) Flag manipulation

Mnemonic	Object code (binary)	Operation description	Byte	Cycle	Flag		
					C	Z	S
TFCFC	0101 0011	SF←CF', CF←0	1	1	0	-	*
TTCFS	0101 0010	SF←CF, CF←1	1	1	1	-	*
TZS	0101 1011	SF←ZF	1	1	-	-	*

(12) Interrupt control

Mnemonic	Object code (binary)	Operation description	Byte	Cycle	Flag		
					C	Z	S
CIL r	0110 0011 11rr rrrr	IL←IL & r	2	2	-	-	1
DICIL r	0110 0011 10rr rrrr	EIF←0,IL←IL&r	2	2	-	-	1
EICIL r	0110 0011 01rr rrrr	EIF←1,IL←IL&r	2	2	-	-	1
EXAE	0111 0101	MASK↔Acc	1	1	-	-	1
RTI	0100 1101	SP←SP+1,FLAG.PC ←STACK[SP],EIF ←1	1	2	*	*	*

(13) CPU control

Mnemonic	Object code (binary)	Operation description	Byte	Cycle	Flag		
					C	Z	S
NOP	0101 0110	no operation	1	1	-	-	-

(14) Timer/Counter & Data pointer & Stack pointer control

Mnemonic	Object code (binary)	Operation description	Byte	Cycle	Flag		
					C	Z	S
LDADPL	0110 1010 1111 1100	Acc←$[DP]_L$	2	2	-	Z	1
LDADPM	0110 1010 1111 1101	Acc←$[DP]_M$	2	2	-	Z	1
LDADPH	0110 1010 1111 1110	Acc←$[DP]_H$	2	2	-	Z	1
LDASP	0110 1010 1111 1111	Acc←SP	2	2	-	Z	1
LDATAL	0110 1010 1111 0100	Acc←$[TA]_L$	2	2	-	Z	1
LDATAM	0110 1010 1111 0101	Acc←$[TA]_M$	2	2	-	Z	1
LDATAH	0110 1010 1111 0110	Acc←$[TA]_H$	2	2	-	Z	1
LDATBL	0110 1010 1111 1000	Acc←$[TB]_L$	2	2	-	Z	1
LDATBM	0110 1010 1111 1001	Acc←$[TB]_M$	2	2	-	Z	1
LDATBH	0110 1010 1111 1010	Acc←$[TB]_H$	2	2	-	Z	1
STADPL	0110 1001 1111 1100	$[DP]_L$←Acc	2	2	-	-	1
STADPM	0110 1001 1111 1101	$[DP]_M$←Acc	2	2	-	-	1
STADPH	0110 1001 1111 1110	$[DP]_H$←Acc	2	2	-	-	1
STASP	0110 1001 1111 1111	SP←Acc	2	2	-	-	1
STATAL	0110 1001 1111 0100	$[TA]_L$←Acc	2	2	-	-	1
STATAM	0110 1001 1111 0101	$[TA]_M$←Acc	2	2	-	-	1
STATAH	0110 1001 1111 0110	$[TA]_H$←Acc	2	2	-	-	1
STATBL	0110 1001 1111 1000	$[TB]_L$←Acc	2	2	-	-	1
STATBM	0110 1001 1111 1001	$[TB]_M$←Acc	2	2	-	-	1
STATBH	0110 1001 1111 1010	$[TB]_H$←Acc	2	2	-	-	1

Preliminary

**** SYMBOL DESCRIPTION

Symbol	Description	Symbol	Description
HR	H register	LR	L register
PC	Program counter	DP	Data pointer
SP	Stack pointer	STACK[SP]	Stack specified by SP
A_{CC}	Accumulator	FLAG	All flags
CF	Carry flag	ZF	Zero flag
SF	Status flag	GF	General flag
EI	Enable interrupt register	IL	Interrupt latch
MASK	Interrupt mask	PORT[p]	Port (address : p)
TA	Timer/counter A	TB	Timer/counter B
RAM[HL]	Data memory (address : HL)	RAM[x]	Data memory (address : x)
$ROM[DP]_L$	Low 4-bit of program memory	$ROM[DP]_H$	High 4-bit of program memory
$[DP]_L$	Low 4-bit of data pointer register	$[DP]_M$	Middle 4-bit of data pointer register
$[DP]_H$	High 4-bit of data pointer register	$[TA]_L([TB]_L)$	Low 4-bit of timer/counter A (timer/counter B) register
$[TA]_M([TB]_M)$	Middle 4-bit of timer/counter A (timer/counter B) register	$[TA]_H([TB]_H)$	High 4-bit of timer/counter A (timer/counter B) register
←	Transfer	↔	Exchange
+	Addition	-	Substraction
&	Logic AND		Logic OR
^	Logic XOR	¦	Inverse operation
.	Concatenation	#k	4-bit immediate data
x	8-bit RAM address	y	4-bit zero-page address
p	4-bit or 5-bit port address	b	Bit address
r	6-bit interrupt latch	PC_{12-6}	Bit 12 to 6 of program counter
LR_{1-0}	Contents of bit assigned by bit 1 to 0 of LR	a_{5-0}	Bit 5 to 0 of destination address for branch instruction
LR_{3-2}	Bit 3 to 2 of LR		