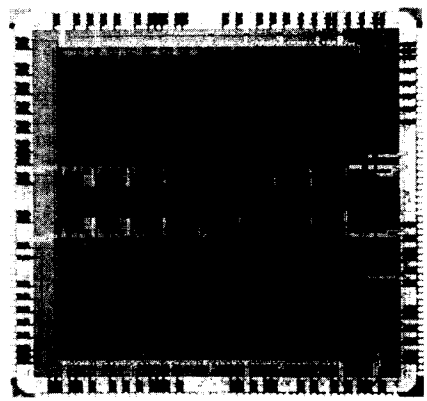
L64230
Binary Filter and Template Matcher (BFIR)

LSI LOGIC

Description

The L64230 is a 1024-tap high-speed binary transversal filter processor and template matcher. The processor can be configured as a 1-D (one-dimensional) filter for radar or other signal processing applications, or as a 2-D (two-dimensional) filter for image processing applications. The processor accepts 2-D data directly from a L64210/L64211 Variable-Length Video Shift Register or other video source. The coefficients can be changed in time to perform adaptive filtering and correlation. The window and/or precision of a 1-D or 2-D filter is expandable using more L64230 processors with minimal external logic.

The processor is ideally suited for real-time image processing applications, like video pattern matching, noise removal and the morphological operations, erosion and dilation. The maximum window size is 32 x 32 for a single chip. Video output formatting circuitry is also available on chip to clip the ouput to a single bit. Data throughput of 20 MHz (WCCOM) makes the processor suitable for radar processing. Implemented in 1.5-micron drawn gate length (0.9-micron effective channel length) low power HCMOS technology, the L64230 is available in a 155-lead Ceramic Pin Grid Array package.



L64230 Chip

Features

- Performs FIR filtering, template matching, erosion and dilation
- Compatible with the L64200 family of products
- 1024-tap sections, each operating on 1-bit data and 1 1/2-bit coefficients
- Reconfigurable for 1-D and 2-D correlation/convolution/morphology
- Multiple processors can be used to extend data and/or coefficient precision
- Multiple processors can achieve window sizes of over 64K taps
- 16-bit output precision
- Double buffering of coefficients
- High speed operation

Commercial	Military
20 MHz	16 MHz
15 MHz	12 MHz

- Available in 155-lead CPGA (Ceramic Pin Grid Array) package

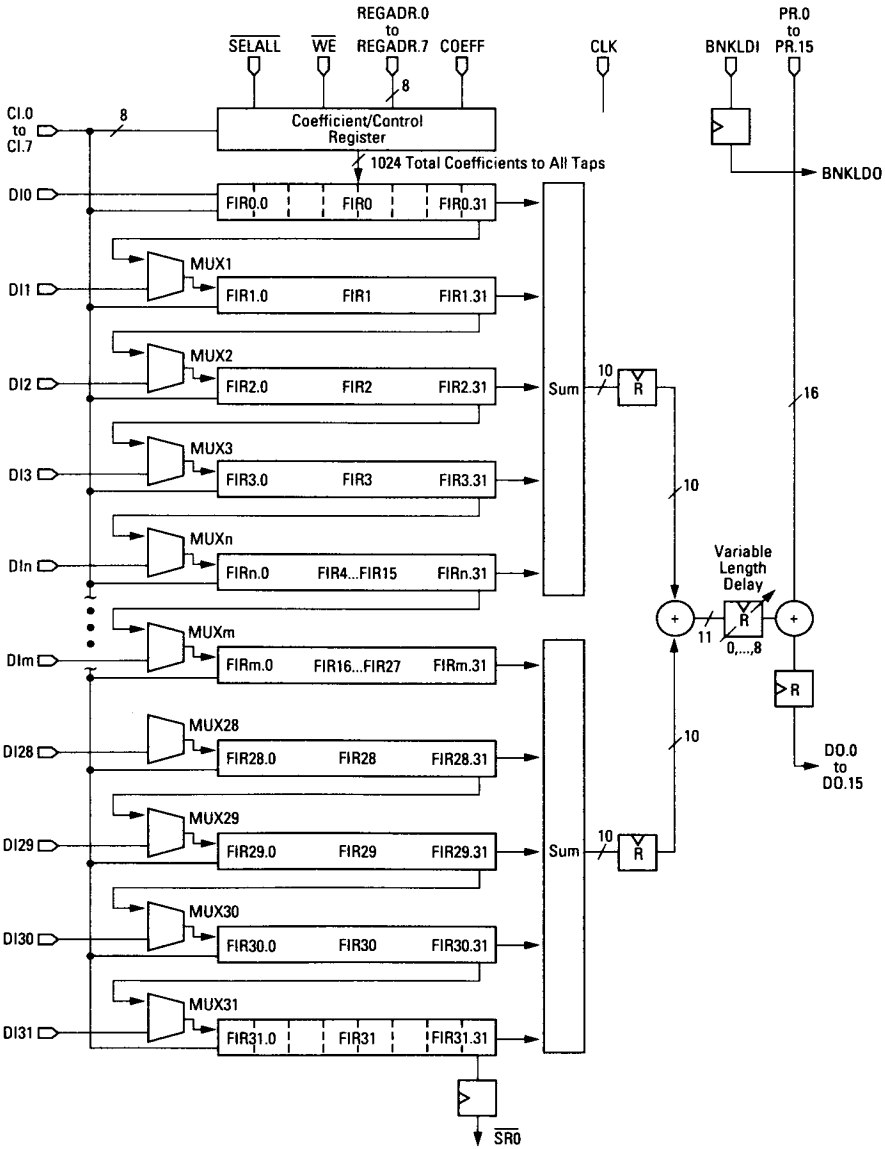
Architecture

The core of the processor is organized as 32 32-tap filter sections. The outputs of all 32-tap sections are summed and delayed by the variable-length shift register. This delayed output is added to an incoming partial result to form the processor output. The partial result input is used to sum partial results in a multi-processor system and to set the threshold value to clip the output to a single bit. The variable-length shift register is used only in multiprocessor systems to compensate for additional latency acquired in the partial result path.

Each filter tap performs the basic XNOR and AND operations. The Ai, j and Bi, j are stored in double buffered registers. Bi, j controls the XNOR gate and Ai, j controls the AND gate. The XNOR gate performs inversion (erosion) or magnitude differencing (template matching). The AND gate performs masking (template matching) or 1-bit multiplication (FIR filtering, dilation erosion). The outputs of all taps are summed to produce the final result. It should be noted that no significant bits of any signal are lost.

The processor has 32 single-bit inputs (DI0-DI31). For 1-D filtering, the only active input is DI0. When performing 2-D operations over N x M window, N of the inputs are active. Normally, when performing 2-D operations, an L64210/11 Video Shift Register, with a raster-scanned signal as its input, would provide the N active data inputs. In this case, the output of the processor, DO(n) represents the raster-scanned output.

Block Diagram



Note: All 32 FIR filter banks contain 32 binary FIR filters.

Pin Listing and Description

DI0 to DI31
32 single-bit data input pins. When the L64230 is used as a 1-D processor, only pin DI0 is used. The remaining data input pins are left unconnected. When used as a 2-D filter processor with a 32 x 32 window, the L64230 operates with all 32 data input pins active.

$\overline{SRO}$
Shift register output. In a 1-D configuration, $\overline{SRO}$ is the DI0 input delayed by 1025 cycles and inverted. Typically, this signal is connected to DI0 of the next L64230 in a 1-D multiprocessor system. $\overline{SRO}$ is not used in 2-D processing.

CI.0 to CI.7
Coefficient/control input pins. A set of eight control bits or four sets of coefficients (both Ai, j and Bi, j) can be loaded into the master section of the coefficient/control registers.

$\overline{SELALL}$
Input signal. When LOW, $\overline{SELALL}$ enables the loading of the values at CI.0 to CI.7 into the master latches of all 256 4-tap groups in the processor simultaneously. This quickly initializes the processor. When HIGH, permits loading of those values into master latches at destinations determined by COEFF and REGADR.0 to REGADR.7.

BNKLDI
Bank load input. Set HIGH to bank load coefficient/control inputs from master to slave registers. When asynchronously loading coefficients/controls with respect to CLK, BNKLDI is held LOW until bank loading occurs. When coefficient/control loading is synchronous to CLK, BNKLDI is always held HIGH.

BNKLDO
Bank load output. BNKLDI signal delayed by one CLK cycle. This may be used as BNKLDI for the next L64230 in a 1-D multiprocessor system.

$\overline{WE}$
Active LOW write enable unit. Used to enable the loading of coefficients/control signals into the register location indicated by COEFF and REGADR.0 to REGADR.7.

COEFF
Coefficient input indicator. When HIGH, specifies that data on the CI bus are coefficients. When LOW, data on the CI bus are control inputs.

REGADR.0 to REGADR.7
Coefficient/control register address inputs. Indicate the register location for coefficients or control signals. Loading occurs when $\overline{WE}$ is LOW. REGADR.7 is the MSB.

CLK
System clock, positive edge triggered.

DO.0 to DO.15
16-bit data output. The value of the output is derived from delayed sum of all the 1024 taps and the partial result (PR.0 to PR.15). DO.15 is the MSB and DO.0 is the LSB.

PR.0 to PR.15
16-bit partial result input. The partial result is summed with the processor results to provide the final data output value. During multiprocessor operation, the DO.0 to DO.15 outputs of the preceding processor are connected to the corresponding partial result input. When any PR pins are left unconnected, the processor assumes a LOW value. The partial results can also be used to vary the threshold when clipping the output to a single bit. PR.15 is the MSB and PR.0 is the LSB.

Pin Description Summary

Signal	No. of Pins	I/O	Description
DI0-DI31	32	I	Data inputs 0 to 31
CI.0	8	I	Coefficient/control input bus
PR.0-PR.15	16	I	Partial result input
DO.0-DO.15	16	O	Filter output
CLK	1	I	System clock
BNKLDI	1	I	Bank loads
BNKLDO	1	O	BNKLDI delayed one CLK cycle
$\overline{WE}$	1	I	Write enable for coefficient/control registers
REGADR.0-REGADR.7	8	I	Address of coefficient/control registers
COEFF	1	I	Indicates if CI are coefficient or control inputs
$\overline{SELALL}$	1	I	Selects all coefficient registers

Functional Overview

The L64230 performs binary FIR filtering, template matching and morphological operations over very large windows. The basic functions performed are:

$$1D: y(n) = PR(n-1) + \sum_{i=0}^{1023} [(Bi \text{ XNOR } DIO(n - i - D1 - 3)) \text{AND } \overline{Ai}]$$

$$2D: y(n) = PR(n-1) + \sum_{i=0}^{31}\sum_{j=0}^{31} [(Bi, j \text{ XNOR } DIi(n - j - D1 - 3)) \text{AND } \overline{Ai, j}]$$

By appropriately setting the Ai, j and Bi, j all of the above functions can be implemented. For template matching, Bi, j is the template and Ai, j is the "don't care" mask. For FIR filtering, Bi, j=1 and Ai, j is the inverted impulse response. Dilation is virtually the same as FIR filtering except that the multi-bit output is clipped to a single bit. Hence, Bi, j=1 and Ai, j is the inverted structuring element. For erosion, Bi, j=0 and Ai, j is the inverted structuring element. These conditions are summarized in the table below.

In the preceding equations, all Dli, Ai, j and Bi, j are a single bit wide while the output is 16 bits wide. The multibit output can be clipped to a user preset threshold if a single bit output is desired.

The 1024 taps can be reconfigured to the following window sizes: 2 x 512, 4 x 256, 8 x 128, 16 x 64 or 32 x 32. In addition, for all functions it is possible to reduce the effective window size by masking some elements within the window (by setting Ai, j=1) D1 is the value of the variable length output delay.

Functional Summary

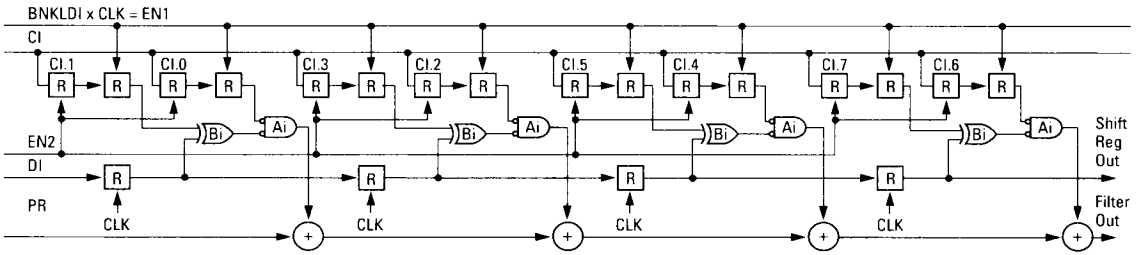
Function	Ai,j	Bi,j	PR	Output
FIR Filter	Inverted Impulse Response	1	0	DO is the Filter Output
Template Matching	"Don't Care" Mask	Template	0	DO Represents Correlation to Template
Erosion	Inverted Structuring Element	0	-1	DO.15 is Output
Dilation	Inverted Structuring Element	1	-1	DO.15 is Inverted Output

Data I/O

The first 32-tap FIR filter section (FIR0) receives data directly from the input pin (DIO). The last 31 32-tap FIR filter sections (FIR1-FIR31) receive input data from either an external input or from the shift register output of the previous section. The multiplexer at the input to these sections determines the window shape of the filter. For example, if all multiplexers are set such that all sections receive input from the previous shift register output, then the filter behaves as a 1024-tap filter with only the DIO input active. When all multiplexers are set such that each of the 32 sections receives its input from the 32 inputs, then the filter behaves as a 32 x 32 2-D filter. By selectively setting the multiplexers to pass data from the input buses to the filter sections, it is possible to set the window shape to 1 x 1024, 2 x 512, 4 x 256, 8 x 128, 16 x 64 or 32 x 32.

Data I/O
(Continued)

4-Cell Filter Section



Coefficient/Control Signal Loading

The diagram above shows four of the 32 filter taps that make up FIR0, FIR1, etc. Coefficients and control signals are double-buffered with two level triggered latches (master and slave) placed before each cell. To load a new coefficient or control signal, the value is first placed on the CI bus. The data on the CI bus is latched into the internal master register designated by REGADR.0 to REGADR.7 and COEFF when $\overline{WE}$ is LOW. Alternatively, the data on the CI bus are interpreted as coefficients when $\overline{SELALL}$ is LOW and latched simultaneously into all 256 groups of 4 filter taps. The next step involves transferring the data in the master latch to the slave or active latch. There are three methods of performing these operations:

- The first method is to load the coefficient or control signal to the master latch asynchronously to the system CLK and transfer it to the slave latch synchronously to the CLK. The data is loaded into the master latch at the filter location selected by REGADR.0– REGADR.7 and COEFF when $\overline{WE}$ is LOW. This is then repeated for each new coefficient for other filter cells in the processor. When the master latches of all the filter cells have been updated, the coefficients can be simultaneously made active by enabling the slave latches with EN1 (when BNKLDI and CLK are HIGH). The transfer of coefficients from the master to the slave latches is synchronous to the CLK. This method provides flexibility in the loading of new coefficients into the processor without modifying the active set of coefficients.

- The second method is to load and transfer coefficients synchronously to the system clock. This can be done with BNKLDI tied HIGH. $\overline{WE}$ is pulsed LOW when CLK is LOW. During this time, a new coefficient on bus CI is loaded into the master latch of the filter cell whose location has been determined by REGADR.0–REGADR.7 and COEFF. On the next rising edge of CLK, the coefficient is transferred to the slave latch, thus becoming the active coefficient or control signal. In this way, a new coefficient can replace the current one within one clock cycle. This can be done only with slower clock speed, with cycle time 80ns (COM) or more.

- The third method is to asynchronously load and transfer new coefficients over several cycles. This technique is used if it is not convenient to supply BNKLDI or $\overline{WE}$ signals sychronous to CLK. BNKLDI can be tied HIGH and $\overline{WE}$ operated asynchronously. In this case every time a new coefficient is loaded, the processor output could be invalid for up to 20 cycles after the rising edge of $\overline{WE}$. If control signals (COEFF = 0) are loaded, the processor could be invalid for up to 1050 cycles after the rising edge of $\overline{WE}$.

  To make is possible to quickly initialize all of the processor coefficients, all FIR tap coefficients can be loaded with the data on CI by setting $\overline{SELALL}$ LOW. Normally $\overline{SELALL}$ is left HIGH.

Operation

The processor is operated in a very simple manner. After internal registers indicating the operating mode of the device have been loaded, the user need only supply a system/data clock and the input data. If desired, some or all of the coefficients (the set of Ai, j and Bi, j) can be changed while the processor is running.

Control Signals

To initialize the processor, all coefficients, the delay value of the variable delay element and the configuration must be specified. The Processor Control/Coefficient Memory Map table shows the memory map for the processor.

If $\overline{\text{SELALL}}$ is HIGH, only one set of eight control/coefficient bits will be latched each time $\overline{\text{WE}}$ goes LOW. When $\overline{\text{SELALL}}$ goes LOW, all 1024 Ai, Bi will be loaded as shown in the Processor Control/Coefficient Memory Map table ($\overline{\text{WE}}$ can be HIGH or LOW). The $\overline{\text{MUXCON}}$ and OUTDEL values will, however, change only when $\overline{\text{WE}}$ is LOW.

OUTDEL.0 to OUTDEL.4 set the number of delays performed by the variable delay element. Values greater than eight are not legal delay values. The Window Configurations table shows the window shape and active data inputs for some values of the $\overline{\text{MUXCON}}$ signal. Other configurations can be obtained.

Processor Control/Coefficient Memory Map

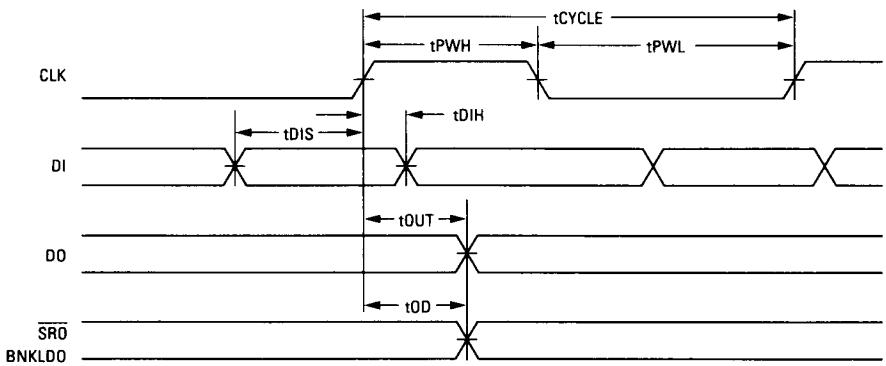
COEFF	REGADR.0 REGADR.7	CI.7	CI.6	CI.5	CI.4	CI.3	CI.2	CI.1	CI.0
0	0	X	X	X	$\overline{\text{MUXCON.4}}$	$\overline{\text{MUXCON.3}}$	$\overline{\text{MUXCON.2}}$	$\overline{\text{MUXCON.1}}$	$\overline{\text{MUXCON.0}}$
0	1	X	X	X	X	OUTDEL.3	OUTDEL.2	OUTDEL.1	OUTDEL.0
1	0	B0,3	A0,3	B0,2	A0,2	B0,1	A0,1	B0,0	A0,0
1	1	B0,7	A0,7	B0,6	A0,6	B0,5	A0,5	B0,4	A0,4
1	2	B0,11	A0,11	B0,10	A0,10	B0,9	A0,9	B0,8	A0,8
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
1	7	B0,31	A0,31	B0,30	A0,30	B0,29	A0,29	B0,28	A0,28
1	8	B1,3	A1,3	B1,2	A1,2	B1,1	A1,1	B1,0	A1,0
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
1	15	B1,31	A1,31	B1,30	A1,30	B1,29	A1,29	B1,28	A1,28
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
1	247	B30,31	A30,31	B30,30	A30,30	B30,30	A30,29	B30,28	A30,28
1	248	B31,3	A31,3	B31,2	A31,2	B31,1	A31,1	B31,0	A31,0
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
1	255	B31,31	A31,31	B31,30	A31,30	B31,29	A31,29	B31,28	A31,28

Window Configurations

$\overline{\text{MUXCON.4}}$-$\overline{\text{MUXCON.0}}$	Configuration	Active Inputs
11111	1 x 1024	DI0
11110	2 x 512	DI0, DI16
11100	4 x 256	DI0, DI8, DI16, DI24
11000	8 x 128	DI0, DI4, DI8, DI12, DI16, DI20, DI24, DI28
10000	16 x 16	DI0, DI2, DI4, DI6, DI8, DI10, DI12, DI14 DI16, DI18, DI20, DI22, DI24, DI26, DI28, DI30
00000	32 x 32	All

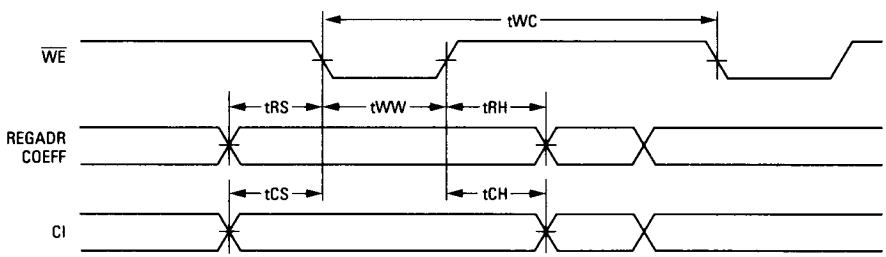
AC Timing Waveforms

Normal Filter Operation

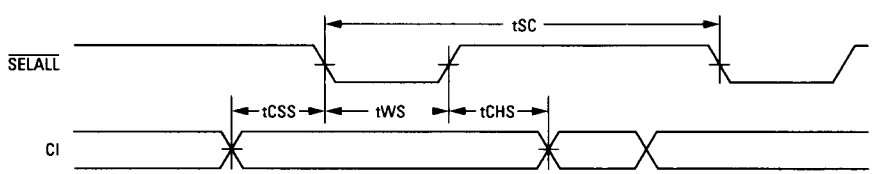


Loading Controls into Master Section (Methods I, II, III)

Using $\overline{WE}$ ($\overline{SELALL}$ HIGH):

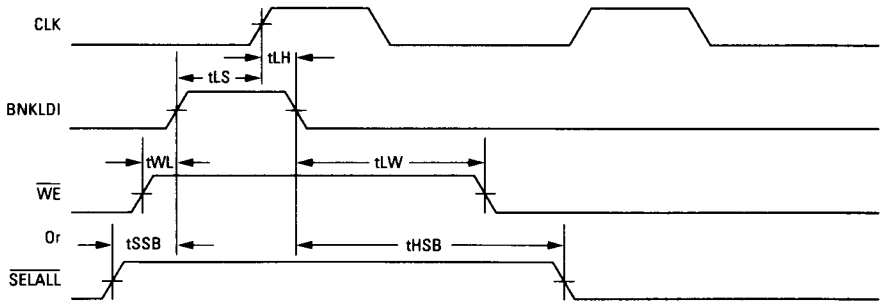


Using $\overline{SELALL}$ ($\overline{WE}$ HIGH):

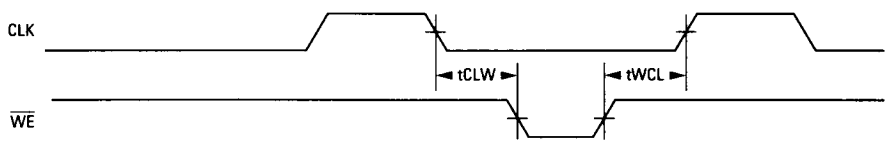


AC Timing Waveforms
(Continued)

Bank Loading of Controls–Synchronous Transfer From Master to Slave Registers (Method I)

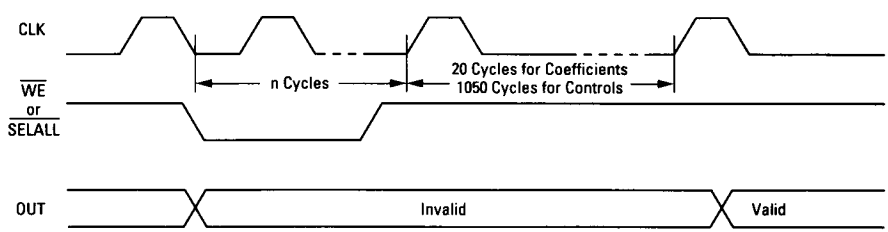


Synchronous Loading of Master and Synchronous Transfer to Slave Section with SELALL HIGH (Method II)



Minimum CLK cycle time, tCYCLE = 80 ns.

Asynchronous Loading of Master Section and Asynchronous Transfer to Slave Section with Bank Load HIGH (Method III)



AC Switching Chararcteristics: Commercial (TA = 0°C to 70°C, VDD = 4.75 V to 5.25 V)

Symbol	Parameter	L64230-20		L64230-15	
		Min	Max	Min	Max
tCYCLE	Minimum clock (CLK) cycle time	50		65	
tPWH	Minimum clock (CLK) pulse width HIGH	20		25	
tPWL	Minimum clock (CLK) pulse width LOW	20		25	
tDIS	Input data (DI) set-up time	15		20	
tDIH	Input data (DI) hold time	5		7	
tPRS	Input partial result (PR) set-up time	30		40	
tPRH	Input partial result (PR) hold time	5		7	
tOUT	Output delay (DO) from CLK↑		15		20
tOD	Output delay (SRO, BNKLDO) from CLK↑		15		20
tLS	BNKLDI set-up time with respect to CLK↑	15		20	
tLH	BNKLDI hold time with respect to CLK↑	5		7	
tWL	$\overline{WE}$ set-up time with respect to BNKLDI↑	5		7	
tLW	$\overline{WE}$ hold time with respect to BNKLDI↓	tPWH + 15		tPWH + 20	
tSSB	$\overline{SELALL}$ set-up time with respect to BNKLDI↑	100		150	
tHSB	$\overline{SELALL}$ hold time with respect to BNKLDI↓	100		150	
tRS	REGADR set-up time with respect to $\overline{WE}$↓	10		15	
tRH	REGADR hold time with respect to $\overline{WE}$↑	10		15	
tCS	CI set-up time with respect to $\overline{WE}$↓	10		15	
tCH	CI hold time with respect to $\overline{WE}$↑	10		15	
tCSS	CI set-up time with $\overline{SELALL}$↓	100		150	
tCHS	CI hold time with $\overline{SELALL}$↑	100		150	
tSC	$\overline{SELALL}$ cycle time	250		350	
tWS	$\overline{SELALL}$ pulse width LOW	100		150	
tWW	Minimum $\overline{WE}$ pulse width LOW	20		25	
tWC	Minimum $\overline{WE}$ cycle time	50		65	
tCLW	CLK↓ before $\overline{WE}$↓	20		25	
tWCL	CLK↑ after $\overline{WE}$↑	20		25	

Note: All units in ns, output loading = 50 pF.

AC Switching Characteristics: Military (TA = -55°C to 125°C, VDD = 4.5 V to 5.5 V)

Symbol	Parameter	L64230-16		L64230-12	
		Min	Max	Min	Max
tCYCLE	Minimum clock (CLK) cycle time	60		75	
tPWH	Minimum clock (CLK) pulse width HIGH	25		30	
tPWL	Minimum clock (CLK) pulse width LOW	25		30	
tDIS	Input data (DI) set-up time	20		25	
tDIH	Input data (DI) hold time	7		15	
tPRS	Input partial result (PR) set-up time	40		50	
tPRH	Input partial result (PR) hold time	7		15	
tOUT	Output delay (DO) from CLK↑		20		25
tOD	Output delay ($\overline{SRO}$, BNKLDO) from CLK↑		20		25
tLS	BNKLDI set-up time with respect to CLK↑	20		25	
tLH	BNKLDI hold-time with respect to CLK↑	7		15	
tWL	$\overline{WE}$ set-up time with respect to BNKLDI↑	7		15	
tLW	$\overline{WE}$ hold time with respect to BNKLDI↓	tPWH + 20		tPWH + 25	
tSSB	$\overline{SELALL}$ set-Up time with respect to BNKLDI↑	150		200	
tHSB	$\overline{SELALL}$ hold time with respect to BNKLDI↓	150		200	
tRS	REGADR set-up time with respect to $\overline{WE}$↓	15		20	
tRH	REGADR hold time with respect to $\overline{WE}$↑	15		20	
tCS	CI set-up time with despect to $\overline{WE}$↓	15		20	
tCH	CI hold time with respect to $\overline{WE}$↑	15		20	
tCSS	CI set-up time with $\overline{SELALL}$↓	150		200	
tCHS	CI hold time with $\overline{SELALL}$↑	150		200	
tSC	$\overline{SELALL}$ cycle time	300		400	
tWS	$\overline{SELALL}$ pulse width LOW	150		200	
tWW	Minimum $\overline{WE}$ pulse width LOW	25		30	
tWC	Minimum $\overline{WE}$ cycle time	60		75	
tCLW	CLK↓ before $\overline{WE}$↓	25		30	
tWCL	CLK↑ after $\overline{WE}$↑	25		30	

Note: All units in ns, output loading = 50 pF.

Operating Characteristics

Absolute Maximum Ratings (Reference to GND)

Parameter	Symbol	Limits	Unit
DC supply voltage	VDD	-0.3 to +7	V
Input voltage	VIN	-0.3 to VDD +0.3	V
DC input current	IIN	±10	mA
Storage temperature range	TSTG	-65 to +150	°C

Recommended Operating Conditions

Parameter	Symbol	Limits	Unit
DC supply voltage	VDD	+3 to +6	V
Operating ambient temperature range			
Military	TA	-55 to +125	°C
Commercial	TA	0 to +70	°C

DC Characteristics: Specified at VDD = 5 V over the specified temperature and voltage ranges[1]

Symbol	Parameter	Condition			Min	Typ	Max	Units	
VIL	Low level input voltage							0.8	V
VIH	High level input voltage Commercial temperature range Military temperature range					 2.0 2.25			 V V
IIN	Input current	VIN = VDD				-150		200	µA
VOH	High level output voltage		Comm		Mil				
	IOH =	-4 mA	-3.2 mA		2.4	4.5		V	
VOL	Low level output voltage		Comm		Mil				
	IOL =	4 mA	3.2 mA			0.2	0.4	V	
IOS	Output short circuit current [2]	VDD = Max, VO = VDD				15		130	mA
		VDD = Max, VO = OV				-5		-100	mA
IDDQ	Quiescent supply current	VIN = VDD or VSS						10	mA
IDD	Operating supply current	tCYCLE = 50 ns					300		mA
CIN	Input capacitance	Any input					5		pF
COUT	Output capacitance	Any output					10		pF

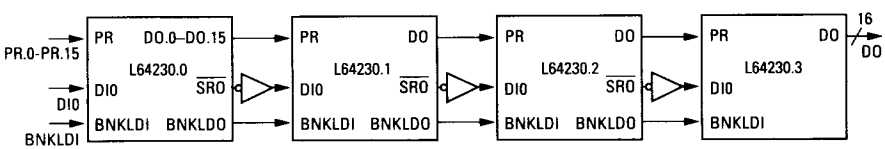
Notes:
1. Military temperature range is -55°C to +125°C, ±10% power supply; commercial temperature range is 0°C to 70°C, ±5% power supply.
2. Not more than one output should be shorted at a time. Duration of short circuit test must not exceed one second.

Application Examples

Example No. 1: 1-D System Example
The system window size can be increased beyond 1024 taps using multiple L64230s. This can be done for both 1-D and 2-D systems by cascading multiple processors, as shown in the following examples.

In this case, each processor computes 1024 of the 4096 taps.

1 x 4096 Window, 1-Bit Data, 1-Bit Coefficient



BNKLDO of any processor is shown as the input to the succeeding processor. This is done to prevent skews between the coefficients bank loaded into the filter taps and the partial results or input data, both of which encounter an extra cycle of latency in output registers.

Initialization of System

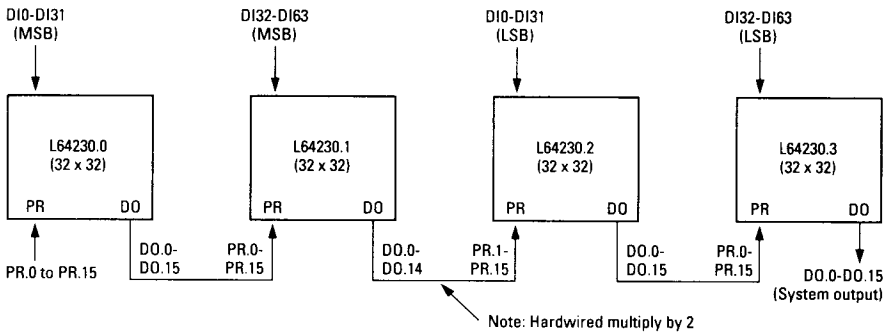
Device	Pins/Internal Control Signals	Value	Comments
L64230.0	PR.0–PR.15	Constant	Can be set to zero by leaving pins unconnected. Non-zero value useful for setting thresholds.
All	OUTDEL.3–OUTDEL.0	0001	One extra pipeline stage.
All	MUXCON.4–MUXCON.0	11111	All processors configured for 1-D processing.

Application Examples
(Continued)

Example No. 2: 2-D FIR Filter Example

In this case, each processor computes the filter output over a 32 x 32 region with either an MSB or LSB data input. The first two processors together compute the filter output over a 64 x 32 window (64 inputs, 32 taps per input) with the MSB of the 2-bit data. Similarly, the last two processors perform the computations on the LSB of the data. Between the two sets of processors is a hard-wired shift by two to appropriately weight the MSB results with respect to the LSB results.

64 x 32 Window, 2-Bit Unsigned Data, 1-Bit Unsigned Coefficient



Initialization of System

Device	Pins/Internal Control Signals	Value	Comments
L64230.0	PR.0–PR.15	Constant	Can be set to zero by leaving pins unconnected. Non-zero value may be input to set threshold.
L64230.0	OUTDEL.3–OUTDEL.0	0001	One cycle delay introduced in variable length delay.
L64230.1	OUTDEL.3–OUTDEL.0	0010	Two cycle delay.
L64230.2	OUTDEL.3–OUTDEL.0	0011	Three cycle delay.
L64230.3	OUTDEL.3–OUTDEL.0	0100	Four cycle delay.
All	MUXCON.4–MUXCON.0	00000	Configures each processor as a 2-D (32 x 32) filter.
All	BNKLDI		Tied together.
All	BNKLDO		Unconnected.
L64230.0	A0.0, B0.0–A31.31, B31.31	C0,0–C31,31	First 32 x 32 block of coefficients, template, structuring elements or mask bits.
L64230.1	A0.0, B0.0–A31.31, B31.31	C32,0–C63,31	Second 32 x 32 block of coefficients, template, structuring elements or mask bits.
L64230.2	A0.0, B0.0–A31.31, B31.31	C0,0–C31,31	First 32 x 32 block of coefficients, template, structuring elements or mask bits.
L64230.3	A0.0, B0.0–A31.31, B31.31	C32,0–C63,31	Second 32 x 32 block of coefficients, template, structuring elements or mask bits.

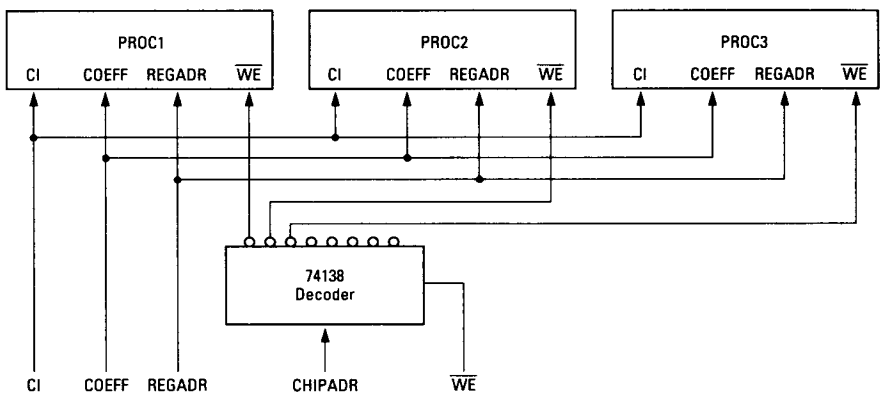
Application Examples (Continued)

As shown on the preceding page, the data outputs of one processor can be the partial result inputs of the next processor in a 2-D system. The presence of the output data registers causes an extra delay of one cycle. Therefore, in a given processor, the latency of the partial result input is greater than that of the filter output sum by one cycle. To compensate for this, it is necessary to provide an extra cycle of latency to the filter output sum. Since the variable length delay provides a maximum of eight extra cycles of delay, a maximum of eight processors can be cascaded in a variety of 2-D configurations without external components.

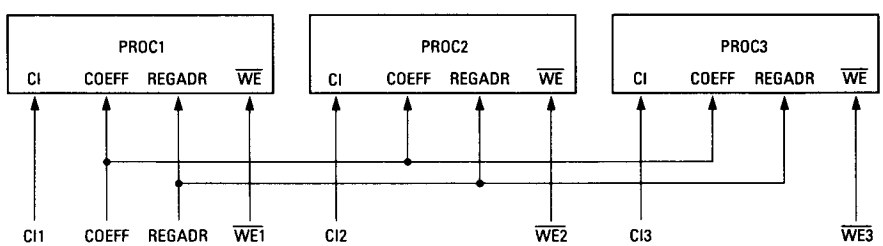
The user has some added flexibility in the amount of time it will take to change the operating parameters of the system. For example, the CI, REGADR, COEFF, and $\overline{WE}$ inputs for all processors could be connected as shown in Low I/O Bandwidth Initialization. In the first case, each chip is initialized in succession and the total time to initialize the system increases with the number of processors. This type of solution is suitable for applications requiring operating parameters to change infrequently.

Another solution would be to connect the signals as shown in High I/O Bandwidth Initialization. In this case, one parameter of each processor can be changed each cycle, keeping the total initialization time to a minimum. Adaptive filters that have a high coefficient update rate could benefit from this configuration.

Low I/O Bandwidth Initialization



High I/O Bandwidth Initialization



Pinout Diagram

155-Pin Ceramic Pin Grid Array (CPGA)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A		VSS	CI.6		CI.2			VSS	VDD				DI2	DI5	VDD	VSS
B	VDD			CI.4				CI.0	CLK		BNK-LDO	DI0	DI3	DI6	DI7	VDD
C	PR.0		CI.7	CI.5	CI.3		CI.1			BNK-LDI		DI1	DI4	DI8	DI9	DI10
D	PR.3	PR.2	PR.1											DI11	DI12	DI13
E	PR.6	PR.5	PR.4											DI14	DI15	DI16
F		PR.7													DI17	
G	PR.9		PR.8											DI18		DI19
H	VSS	PR.10														VSS
J	VDD	PR.11													DI20	VDD
K	PR.12		PR.13											DI22		DI21
L		PR.14													DI23	
M	PR.15	DO.15	DO.14											DI26	DI25	DI24
N	DO.13	DO.12	DO.10											DI29	DI28	DI27
P	DO.11	DO.9	DO.8	DO.5	DO.1				$\overline{SRO}$		REG-ADR.1	COEFF	REG-ADR.3	REG-ADR.7	DI31	DI30
R	VSS	DO.7	DO.6	DO.3	DO.0							REG-ADR.0	$\overline{SELALL}$	REG-ADR.5		VSS
T	VDD	VSS	DO.4	DO.2			VSS	VDD	VSS		REG-ADR.2		$\overline{WE}$	REG-ADR.4	REG-ADR.6	VDD

Top View
Cavity Down

Packaging

155-Pin Grid Array Ceramic Cavity Down Package: See FR Package in Package Selector Guide.

Ordering Information

L64230 G M -XX

- **-XX** — Speed in MHz
- **M** — Temperature Range/Flow Option
  - C = Commercial (0°C to 70°C)
  - M = Military (-55°C to +125°C), Processed to MIL-STD-883C Level B
- **G** — Package Code
  - G = 155-Pin Ceramic Pin Grid Array
- **L64230** — Device Type
  - Binary Filter and Template Matcher