LH1554/M

80-Output LCD Segment Driver LSI Built in RAM

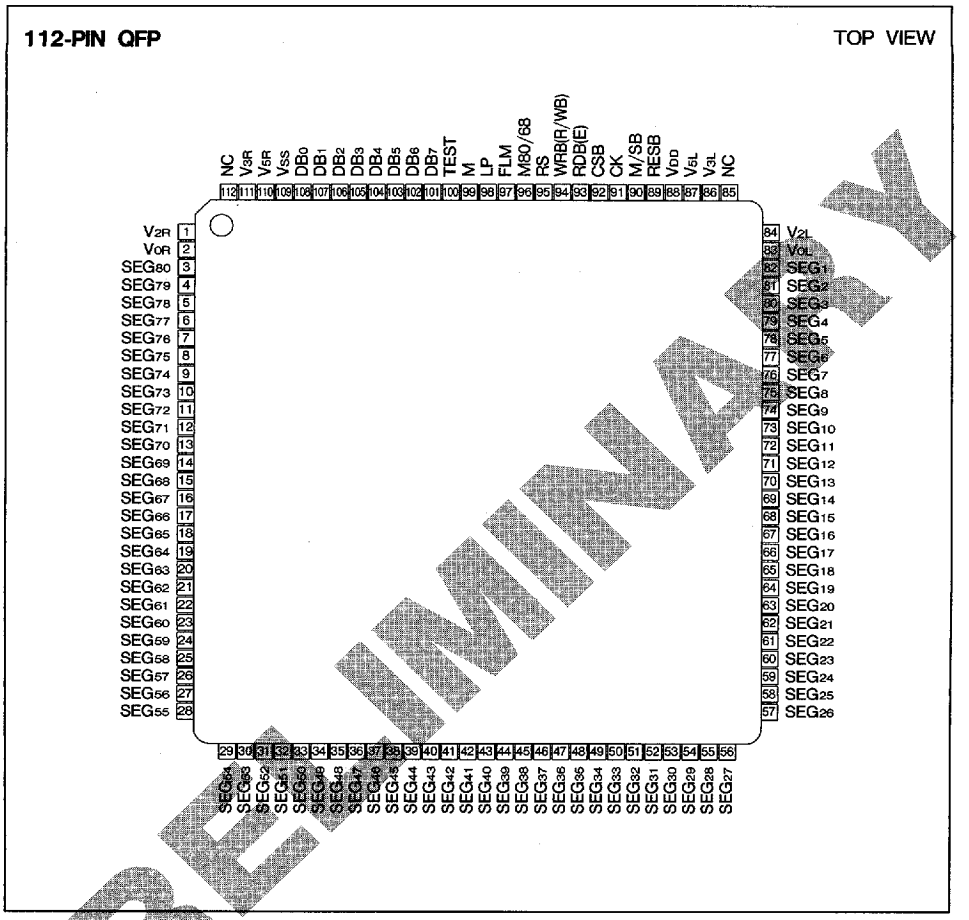
DESCRIPTION

The LH1554/M is a dot matrix LCD pannel system segment driver containing 80-output and display RAM. The driver stores the 8-bit parallel display data from the microcomputer into the internal display RAM and then outputs this RAM data as the LCD drive signals. Since each of the display RAM data bits represents 1 dot on the LCD pannel, various display patterns data can be easily generated with minimum limits. Low power consumption and wide operating voltage enable the chip to be used as interface to LCD pannel system on battery-powered portable information equipment. A dot matrix LCD display system can be easily configured by using this chip together with the common driver LH1531 (64-output common driver).

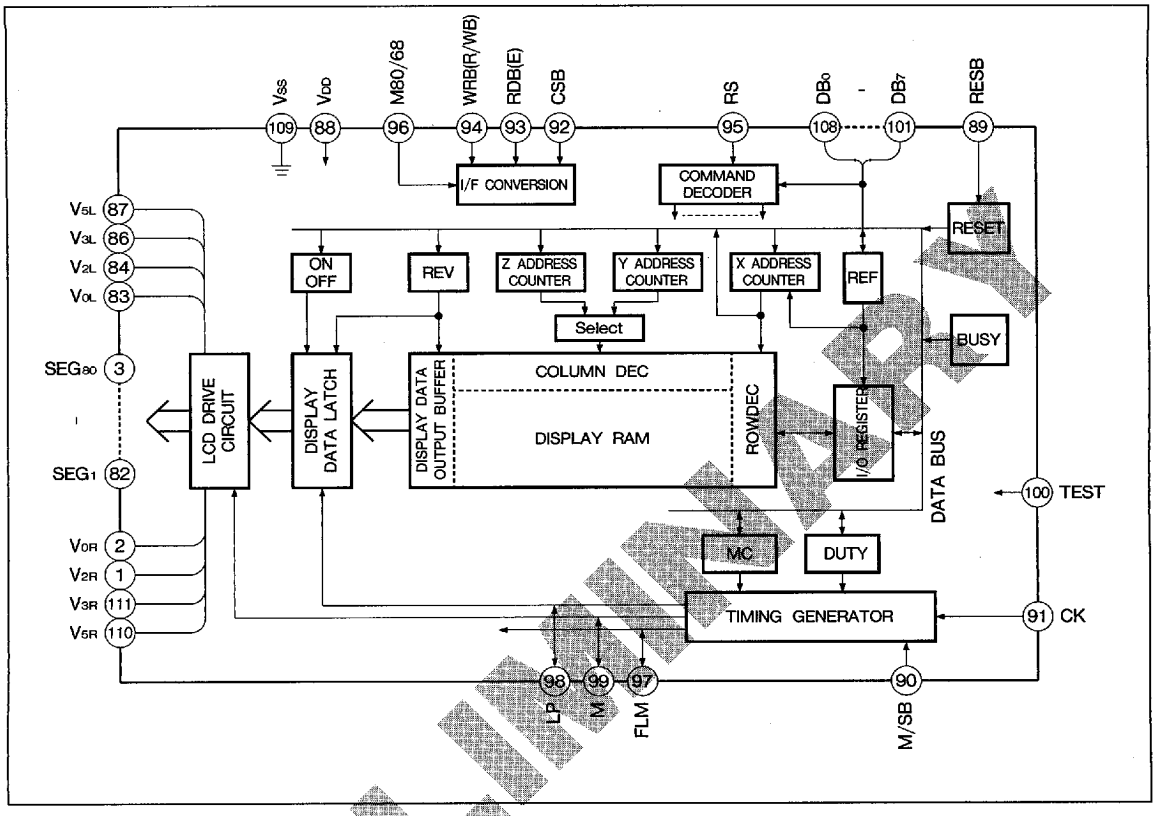
FEATURES

- Supply voltage for LCD drive
  : +10.0 to +30.0 V
- Number of LCD drive outputs : 80-output
- Supply voltage for logic system
  : +2.5 to +5.5 V
- Shift clock fequency
  : 0.5 MHz (Max) (V_{DD} = +2.5 to +4.5 V)
  1 MHz (Max) (V_{DD} = +5 V ± 10%)
- 8-bit parallel interface for direct connection to the bus of a 8-bit general purpose microcomputer (80 or 68 family).
- Display modes : 2
  Non-inverting mode
  : RAM data "0" → dot off
  RAM data "1" → dot on
  Inverting mode
  : RAM data "1" → dot off
  RAM data "0" → dot on
- Display RAM capacity : 1024 bits (80×128)
- Internal display RAM address counter
  Automatic preset of the display start address and automatic address increment
- Various command capabilities
  - Display duty ratio settings
    : selectable 3 types 1/32, 1/64, 1/128
  - LCD AC converting signal frequency settings
    : selectable 3 types
    Frame frequency, 61 line frequency, 13 line frequency
  - Display start line setting : in unit of line
  - Display on/off control
  - Inverting display/non-inverting display control
  - Display RAM read/write
  - Display RAM address increment control
  - Forward/reverse output control of display drive signal
  - Status read
- Automatic 80-bit display data transfer from display RAM to display data latch
- CMOS silicon gate process
- Pakages :
  LH1554 : chip(110-PAD)
  LH1554M : 112-pin QFP(QFP112-P-2020)

PIN CONECTIONS



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	APPLICABLE PINS	RATINGS	UNIT	NOTE
Supply voltage (1)	V_{DD}	V_{DD}	−0.3 to +7.0	V	1, 2
Supply voltage (2)	V_O	V_{OL}, V_{OR}	−0.3 to +32.0	V	
	V_2	V_{2L}, V_{2R}	−0.3 to V_O+0.3	V	
	V_3	V_{3L}, V_{3R}	−0.3 to V_O+0.3	V	
	V_5	V_{5L}, V_{5R}	−0.3 to V_O+0.3	V	
Input voltage	V_I	DB_7-DB_0, RS, CSB RDB, WRB, RESB M80/68, CK, LP, FLM, M M/SB, TEST	−0.3 to V_{DD}+0.3	V	
Storage temperature	Tstg		−45 to +125	°C	

NOTES :

1. Ta = 25°C
2. The maximum applicable voltage on any pin with respect to V_{SS} (0 V).

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage	V_{DD}	V_{DD}	+2.5		+5.5	V	1
Recommended operating voltage	V_O	V_{OL}, V_{OR}	+10.0		+30.0	V	2
Operating temperature	Topr		−20		+85	°C	

NOTES :

1. The applicable voltage on any pin with respect to V_{SS}.
2. Levels of voltages must be : $V_{SS} \leq V_5 < V_3 < V_2 < V_O$.

DC CHARACTERISTICS ($V_{SS}=V_5=0$ V, $V_{DD}=+2.5$ to $+5.5$ V, $V_O=+10.0$ to $+30.0$ V, $Ta=-20$ to $+85$°C)

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNIT	REMARKS
Input high voltage (1)	V_{IH1}			0.8V_{DD}		V_{DD}	V	1
Input low voltage (1)	V_{IL1}			0		0.2V_{DD}	V	
Input high voltage (2)	V_{IH2}			0.8V_{DD}		V_{DD}	V	2
Input low voltage (2)	V_{IL2}			0		0.2V_{DD}	V	
Input high voltage (1)	V_{OH1}	$I_{OH}=-0.4$ mA		$V_{DD}-0.4$			V	3
Input low voltage (1)	V_{OL1}	$I_{OL}=0.4$ mA				0.4	V	
Input high voltage (2)	V_{OH2}	$I_{OH}=-0.4$ mA		$V_{DD}-0.4$			V	4
Input low voltage (2)	V_{OL2}	$I_{OL}=0.4$ mA				0.4	V	
Input leakage current	I_{LI}	$V_I=V_{SS}$ to V_{DD}		−10.0		10.0	μA	5
Output leakage current	I_{LO}	$V_I=V_{SS}$ to V_{DD}		−10.0		10.0	μA	6
LC driver outout on resistance	R_{ON}	$\lvert\Delta V_{ON}\rvert=0.5$ V	$V_O=30$ V		0.7	1.0	kΩ	7
			$V_O=20$ V		1.0	1.5		
Stand-by current	I_{STB}	CK=0 V, CSB=V_{DD}	$V_{DD}=3$ V			5.0	μA	8
			$V_{DD}=5$ V			10.0		
Supply current (1)	I_{DDM1}	Master mode During display(1)	$V_{DD}=3$ V				μA	9
			$V_{DD}=5$ V					
Supply current (2)	I_{DDM2}	Master mode During access(2)	$V_{DD}=3$ V				μA	
			$V_{DD}=5$ V					
Supply current (3)	I_{DDS1}	Slave mode During display(3)	$V_{DD}=3$ V				μA	9
			$V_{DD}=5$ V					
Supply current (4)	I_{DDS2}	Slave mode During access(4)	$V_{DD}=3$ V				μA	
			$V_{DD}=5$ V					
Supply current (5)	I_0	Master mode During access(5)	$V_{DD}=3$ V				μA	10
			$V_{DD}=5$ V					

NOTE :

Forward current direction is defined as one from outside into LSI.

REMARKS (APPLICABLE PINES) :

1. RESB, M80/68, M/SB, FLM, M, LP, CK
2. DB_7 to DB_0, RS, CSB, RDB(E), WRB(R/WB)
3. LP, FLM, M
4. DB_7 to DB_0
5. RESB, M80/68, M/SB, FLM, M, LP, CK, RS, CSB, RDB(E), WRB (R/WB)
6. DB_7 to DB_0 in high impedance state
7. SEG_1 to SEG_{80}
8. V_{SS}
9. V_{DD}
10. V_{OL}, V_{OR}

CONDITIONS :

1. Quiescent current
   Current to V_{DD} pin in master mode, with no CK input, no chip select (CSB=V_{DD})
2. Suppply current (1)
   Current to V_{DD} pin in master mode, with CK input (1 MHz, 50% duty), no chip select (CSB=V_{DD})
3. Supply current (2)
   Current to V_{DD} pin in master mode, with CK input (1 MHz, 50% duty), writing alterating data (reverse/non-reverse) into the display RAM at 1 μs cycle time.
4. Supply current (3)
   Current to V_{DD} pin in slave mode, with no chip select (CSB=V_{DD}) and under the following conditions :
   - CK input (1 MHz, 50% duty)
   - LP input (7.8 kHz, 50% duty)
   - FLM input (61 Hz)
   - M input (30.5 Hz)

   } Input timing as specified in AC characteristics
5. Supply current (4)
   Current to V_{DD} pin in slave mode, when writing alterating data (reverse/non-reverse) into the display RAM at 1 μs cycle time under the following conditions :
   - CK input (1 MHz, 50% duty)
   - LP input (7.8 kHz, 50% duty)
   - FLM input (61 Hz)
   - M input (30.5 Hz)

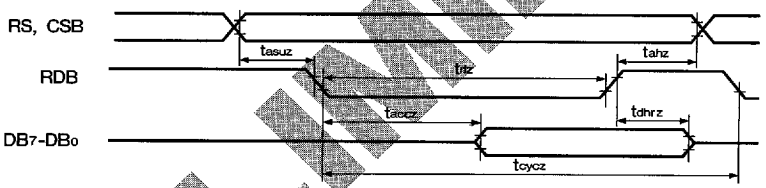
   } Input timing as specified in AC characteristics
6. Supply current (5)
   Current at V_{OR}, V_{OL} pin under condition 3.

AC CHARACTERISTICS

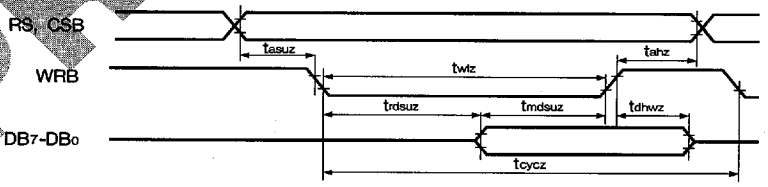
System bus read/write timing (80 family) (V_{SS}=V_5=0 V, V_O=+10 to +30 V, Ta=−20 to +85°C)

PARAMETER	SYMBOL	APPLICABLE PINS	V_{DD}=2.5 to 4.5 V		V_{DD}=4.5 to 5.5 V		UNIT
			MIN.	MAX.	MIN.	MAX.	
Address hold time	t_{ahz}	RS, CSB	20		10		ns
Address set-up time	t_{asuz}		40		20		ns
System cycle time	t_{cycz}	WRB, RDB	2000		1000		ns
Read/write pulse width	t_{rlz}, t_{wlz}		400		200		ns
Data set-up time (memory access)	t_{mdsuz}	DB_0 - DB_7	160		80		ns
Write data hold time	t_{dhwz}		20		10		ns
Read data access time	t_{accz}			180		90	ns
Read data hold time	t_{dhrz}						ns
Input signal rising, falling time	t_r, t_f	All pins		30		15	ns
Data set-up time (register access)	t_{rdsuz}						ns

< Read cycle >



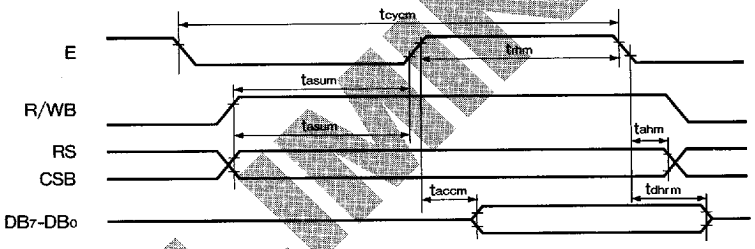
< Write cycle >



System bus read/write timing (68 family) ($V_{SS}=V_5=0$ V, $V_0=+10$ to $+30$ V, Ta $=-20$ to $+85$°C)

PARAMETER		SYMBOL	APPLICABLE PINS	V_{DD}=2.5 to 4.5 V		V_{DD}=4.5 to 5.5 V		UNIT
				MIN.	MAX.	MIN.	MAX.	
System cycle time		t_{cycm}	E	2000		1000		ns
Address set-up time		t_{asum}	RS, CBS, R/WB	40		20		ns
Address hold time		t_{ahm}		20		10		ns
Data set-up time (memory access)		t_{mdsum}		160		80		ns
Write data hold time		t_{dhwm}	DB0 to DB7	20		10		ns
Read data access time		t_{accm}			180		90	ns
Read data hold time		t_{dhrm}						ns
Enable pulse width	Read pulse	t_{rhm}	E	200		100		ns
	Write pulse	t_{whm}		160		80		ns
Input signal rising, falling time		t_r, t_f	All pins		30		15	ns
Data set-up time (register access)		t_{rdsum}						ns

< **Read cycle** >



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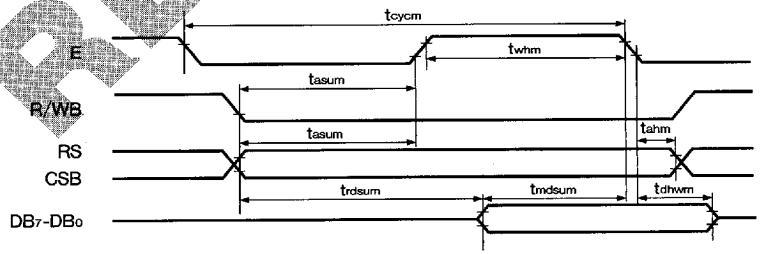
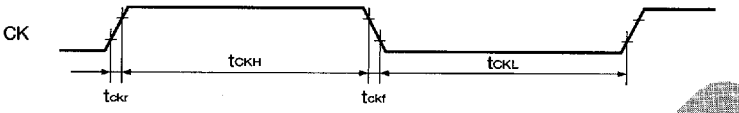


Mster clock input timing (Vss=V5=0 V, Vo=+10 to +30 V, Ta=−20 to +85°C)

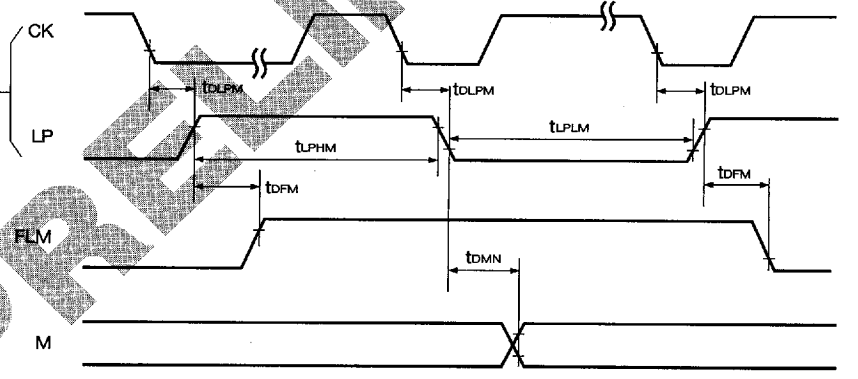
PARAMETER	SYMBOL	APPLICABLE PIN	VDD=2.5 to 4.5 V		VDD=4.5 to 5.5 V		UNIT
			MIN.	MAX.	MIN.	MAX.	
CK low level width	tCKL	CK	1000		500		ns
CK high level width	tCKH		1000		500		ns
CK rising and falling time	tckr, tckf			40		20	ns



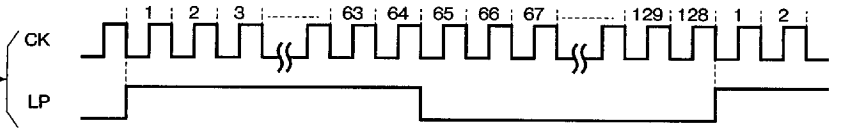
Display control timing

(a) Output timing in Master mode (Vss=V5=0 V, Vo=+10 to +30 V, Ta=−20 to +85°C)

PARAMETER	SYMBOL	APPLICABLE PINS	VDD=2.5 to 4.5 V		VDD=4.5 to 5.5 V		UNIT
			MIN.	MAX.	MIN.	MAX.	
CK fall to LP delay time	tDLPM	LP	10	1000	10	500	ns
LP low level width	tLPLM		64		32		μs
LP high level width	tLPHM		64		32		μs
LP rise to FLM delay time	tDFM	FLM	10	1000	10	500	ns
LP rise to M delay	tDMM	M	10	1000	10	500	ns

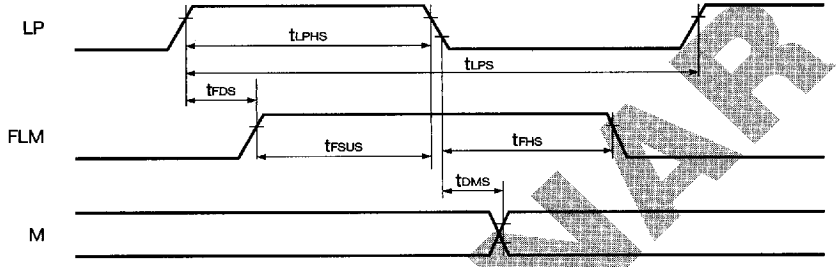


< Timings of CK and LP in master mode are as shown below >



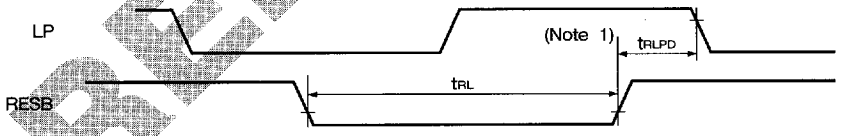
(a) Input timing in the Slave mode ($V_{SS}=V_5=0$ V, $V_O=+10$ to $+30$ V, $Ta=-20$ to $+85$°C)

PARAMETER	SYMBOL	APPLICABLE PINS	V_{DD}=2.5 to 4.5 V		V_{DD}=4.5 to 5.5 V		UNIT
			MIN.	MAX.	MIN.	MAX.	
LP period	t_{LPS}	LP	128		64		μs
LP high level width	t_{LPHS}		64		32		μs
FLM set-up time	t_{FSUS}	FLM	50		50		μs
FLM hold time	t_{FHS}		50		50		μs
LP rise to FLM delay time	t_{FDS}		100		100		μs
LP fall to M delay time	t_{DMS}	M	10	1000	10	500	ns



Reset input timing ($V_{SS}=V_5=0$ V, $V_O=+10$ to $+30$ V, $Ta=-20$ to $+85$°C)

PARAMETER	SYMBOL	APPLICABLE PIN	V_{DD}=2.5 to 4.5 V		V_{DD}=4.5 to 5.5 V		UNIT	NOTE
			MIN.	MAX.	MIN.	MAX.		
RESB low level pulse width	t_{RL}	RESB	1.2				μs	1
RESB off time	t_{RLPD}		100				ns	



NOTE :

1. When the same reset signal is applied to both RESB pin of the LH1554 and DISPOFF pin of the common driver LH1531. If a separate signal is applied to DISPOFF pin of the LH1531 or if the pin is pulled up to high level, this requirement is not applied.

CAUTIONS

Power on and power off

Applying the high LCD drive voltage while the logic supply voltage is in floating status will cause high current to flow into the LSI, which will permanently damage the LSI. The supply voltage to the logic circuits must be turned on prior to turning of the LCD drive voltage. The LCD drive voltage must be turned off prior to turning off of the logic circuit supply.

PIN FUNCTION

● Power supply pins

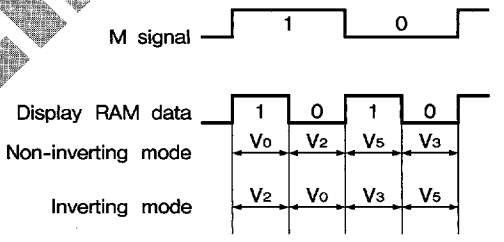
SYMBOL	FUNCTION
V_{DD}	Logic power supply : +2.5 to +5.5 V
V_{SS}	GND potential (0 V)
V_{0L}, V_{0R} V_{2L}, V_{2R} V_{3L}, V_{3R} V_{5L}, V_{5R}	Bias pins of LCD drive voltage ● Bias voltage pins are usually connected to voltage divider network. ● Relationship between voltages should be : $V_{SS} \leq V_5 < V_3 < V_2 < V_0$ ● To minimize difference in waveform among LCD drive outputs on pins SEG_1 through SEG_{80}, connect V_{iL} and V_{iR} (i=0, 2, 3, 5) externally.

● System bus pins

SYMBOL	I/O	FUNCTION
DB_7 - DB_0	I/O	8-bit bidirectional data bus and connects to the data bus of a microcomputer.
RS	I	Toggles between command data and display RAM data that will placed on the DB_7 to DB_0. L : display RAM data ; H : command data Connects to the address bus of the microcomputer.
CSB	I	Active low chip select signal. Usually a decoded address bus signal.
RDB (E)	I	● With 80 family microcomputer Connects to $\overline{RD}$ pin of the microcomputer. When low, this pin is active and the data placed on the LH1554/M internal bus are output to the DB_7 to DB_0. ● With 68 family microcomputer Connects to E (enable clock input) pin of the microcomputer and active high.
WRB (R/WB)	I	● With 80 family microcomputer Connects to $\overline{WR}$ pin of the microcomputer. When low, this pin is active and the data placed on the DB_7 to DB_0 are read in at low to high transition. ● With 68 family microcomputer Connects to input R/$\overline{W}$ select signal. H=read ; L=write
RESB	I	Pulling this pin low starts initializing ● The input signal is level-shifted internally from logic voltage level to LCD drive voltage level, and controls LCD drive circuit. ● When set to V_{SS} level "L", the LCD drive output pins (SEG_1-SEG_{80}) are set to level V_5. Usually connects to the system reset signal.
M80/68	I	Selects between two microcomputer interface types. L=68 family, H=80 family Usually permanently pulled up or low by external circuit.

● LCD drive signal

SYMBOL	I/O	FUNCTION
CK	I	Master clock input which is used to produce the timing clock for internal operation and timing pulse (LP, FLM and M) for LCD display.

SYMBOL	I/O	FUNCTION
LP	I/O	Display data latch signal which, when goes low, increments the display address counter (Z counter). Also used as the shift clock when connected to CK pin of the common driver LH1531. Setting of master/slave set pin M/SB. M/SB=L (input, slave) M/SB=H (output, master)
FLM	I/O	The signal to synchronize display with common side. High level on this pin sets the display start line address data (content of AZ register) into the address counter (Z counter). Input to the common driver is either on pin DI_{O1} or DI_{O2} depending on shift direction. Setting of master/slave set pin M/SB. M/SB=L (input, slave) M/SB=H (output, master)
M	I/O	AC conversion signal of LCD drive output ● This signal is level-shifted internally from logic voltage level to LCD drive voltage level, and controls LCD drive circuit. Connects to FR pin of the common driver LH1531. Setting of master/slave set pin M/SB. M/SB=L (input, slave) M/SB=H (output, master)
SEG_1 - SEG_{80}	O	Segment drive outputs to LCD. Polarity of display RAM data : Non-inverting Mode : OFF when "0", ON when "1" Inverting Mode : OFF when "1", ON when "0" One of levels, V_0, V_2, V_3, and V_5, is selected according to M signal and display data.  **NOTE :** There are two kinds of power supply (logic level voltage and LCD drive voltage) for LCD driver. Please supply regular voltage which assigned by specification for each power pin.
M/SB	I	This pin selects between master and slave operation and should be permanently pulled up (high) or pulled down (low). M/SB=L (slave) M/SB=H (master)

● **Remaining pins**

SYMBOL	I/O	FUNCTION
TEST	I	Testable input pin. Usually should be pulled down (L).

INPUT/OUTPUT CIRCUIT

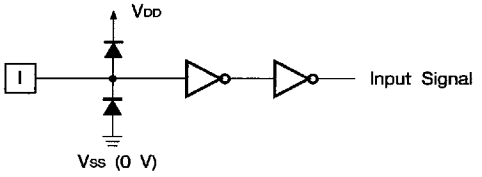


Fig. 1 Input Circuit (1)

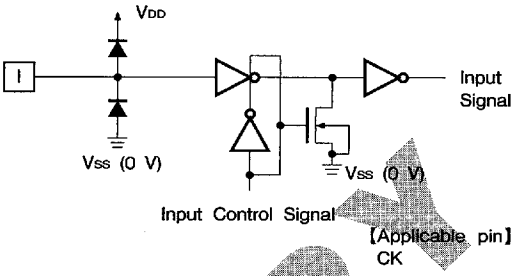


Fig. 2 Input Circuit (2)

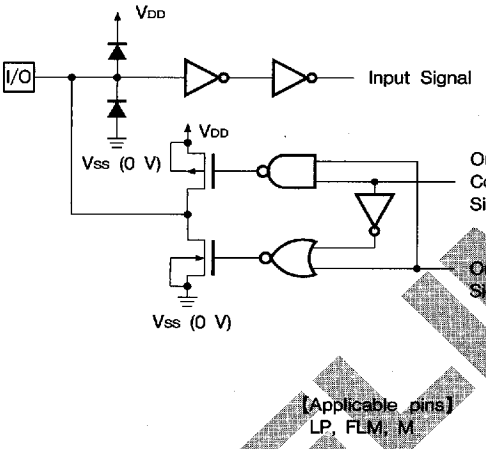


Fig. 3 Input/Output Circuit (1)

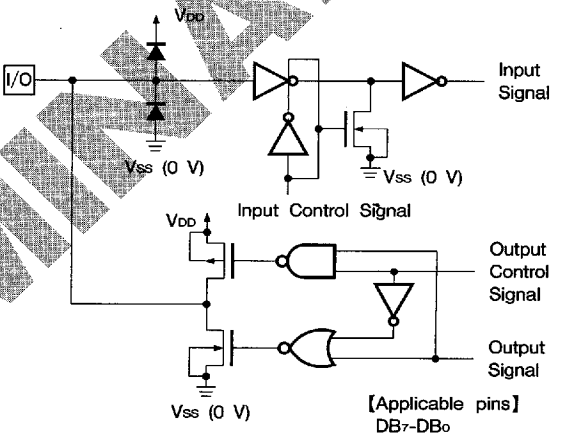


Fig. 4 Input/Output Circuit (2)

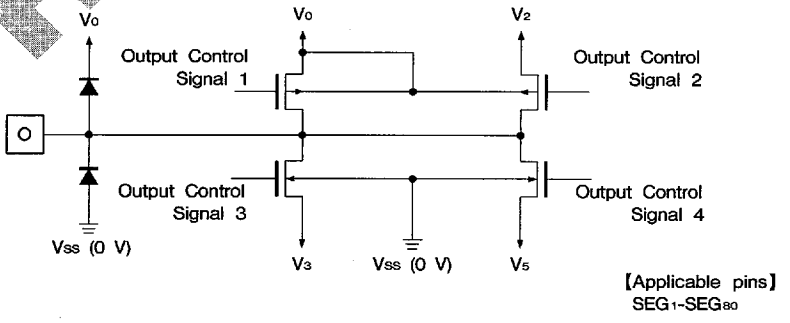


Fig. 5 LCD Drive Output Circuit

LCD DRIVE OUTPUT TIMING

Display timing in the Non-inverting mode

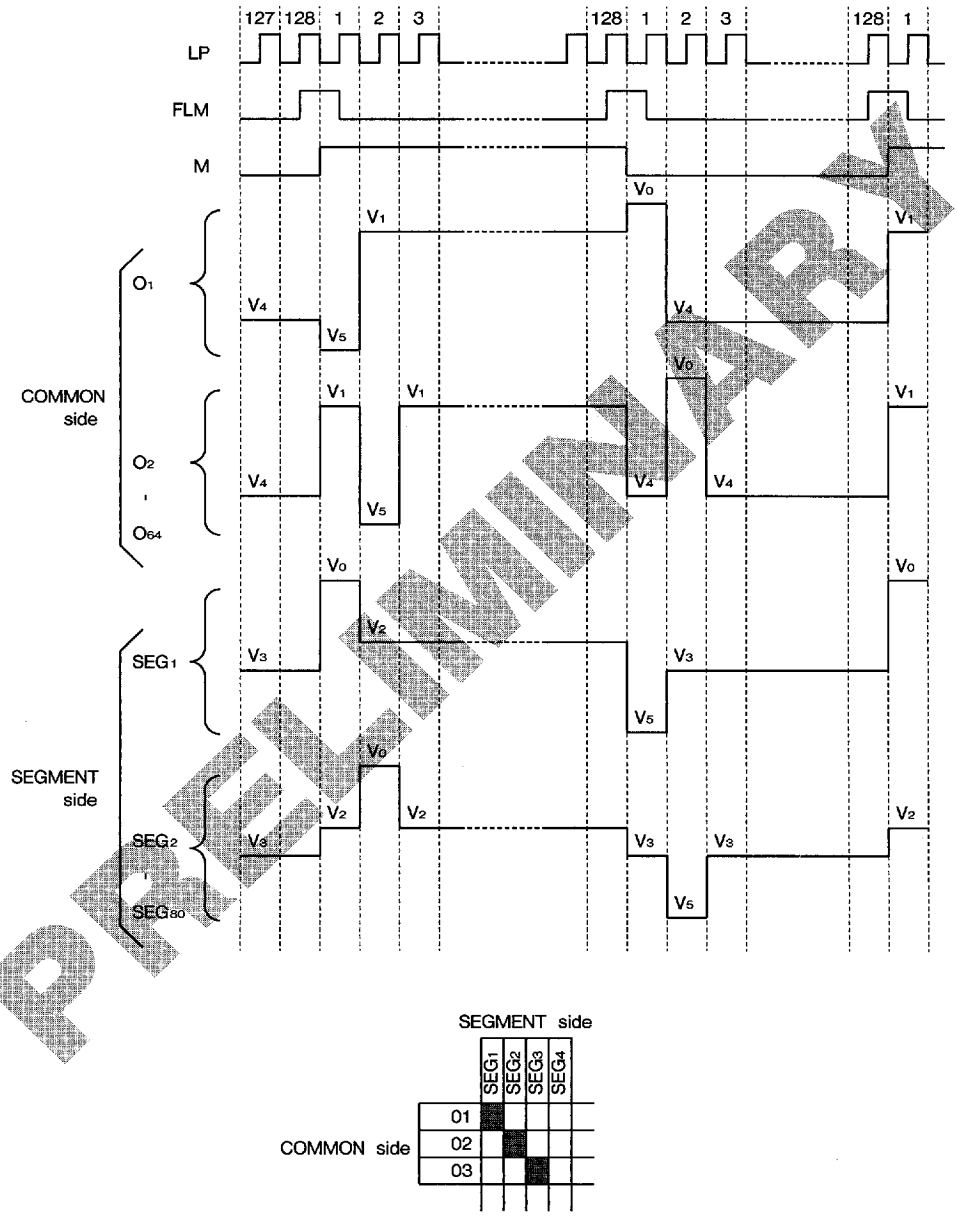
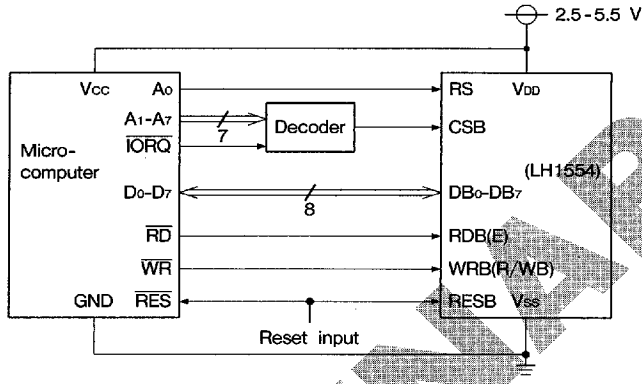


Fig. 6 Example of Display Waveform

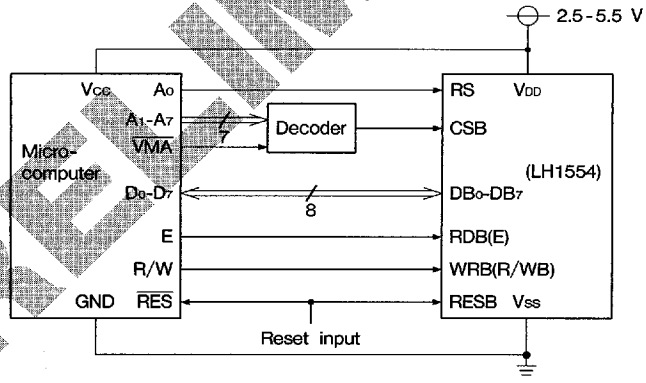
TYPICAL APPLICATIONS (REFERENCE ONLY)

Connection to microcomputer

(a) 80 family microcomputer



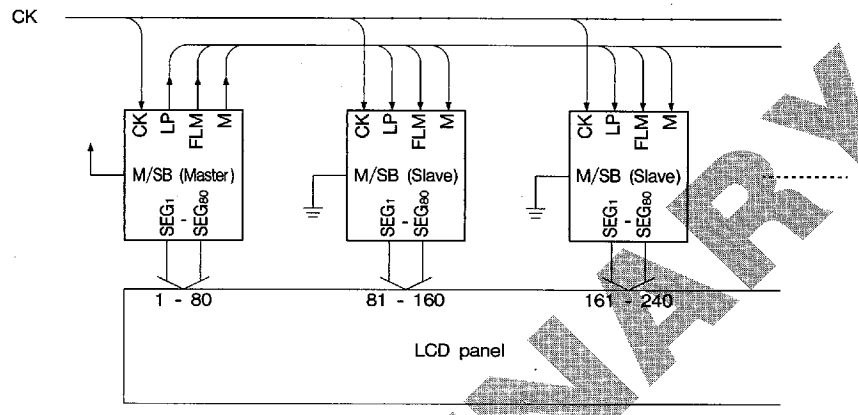
(b) 68 family microcomputer



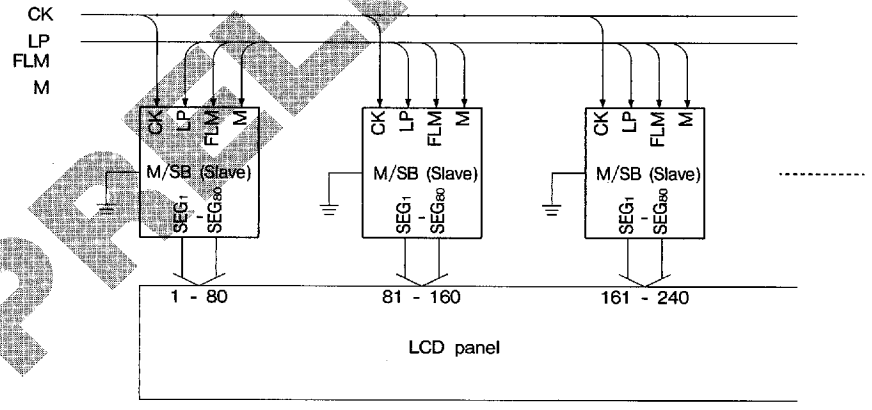
When connecting the microcomputer to two or more LH1554's, adjust the decoding conditions of the address signal to be applied to each CSB pin.

Connection of display signals when two or more LH1554's are used

(a) Master → slave → slave ···



(b) Slave → slave → slave ···



FUNCTIONAL DESCRIPTION

MICROCOMPUTER INTERFACE

Selecting type of interface

The LH1554's 8-bit data bus can directly connect in parallel, to a general purpose 8-bit microcomputer. Either 80 or 68 family 8-bit microcomputer interface can be selected by the setting of M80/68 pin.

M80/68 = L : 68 computer interface
M80/68 = H : 80 computer interface

Accessing command register

Data bus I/O pins (DB_7 (MSB) to DB_0 (LSB)), chip enable pin CSB, display RAM/register select pin RS, read/write control pin RDB and WRB pin are used when accessing the command register. If CSB is at high level, the interface is not selected, inhibiting accessing to the command register. To access the register, be sure to pull CSB low. Selection between the access to the display RAM data I/O register and access to the command register is through the input to RS.

RS = L : display RAM data I/O register
RS = H : command register

Display RAM data I/O register

The display RAM data I/O register is a combination of input register and output register. The input register temporarily holds the data from the microcomputer, until the data is automatically written into the display RAM. When writing operating is attempted with RS = L and CSB = L, the data placed on DB_7-DB_0 is written into the input register on the rising edge of the WRB (with 80 family) or the falling edge of E (68 family). The output register temporarily holds the data read from the display RAM. The data is then read by the microcomputer. When reading operating is attempted with RS = L and CSB = L, the data stored in the output register is placed on DB_7-DB_0 while the RDB = L (80 family) or while the E = H (68 family). Upon completion output register data reading, the register is automatically filled with the data read from the display RAM. At the same time, the address is also advanced according to the setting in the Automatic Increment mode. Because the data in the display RAM is read through the output register, the first reading operation after an address setting cannot reach the display data stored in the display RAM, at the addressed location; the second reading operation will reach that momory location. The first display RAM reading should be designed as a dummy reading. The read timing diagram is shown in Fig. 7.

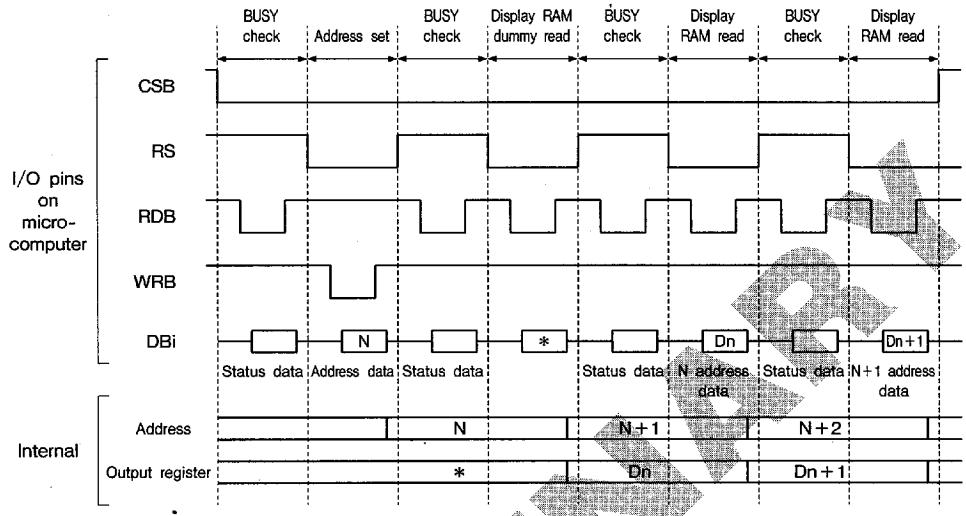


Fig. 7 Display RAM Read Timing Diagram

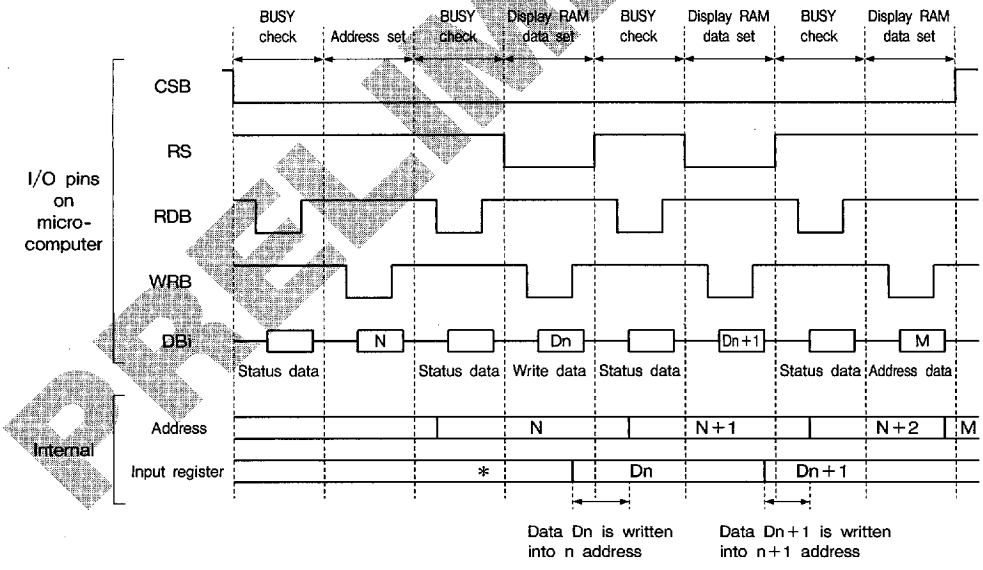


Fig. 8 Display RAM Write Timing Diagram

NOTES :

- BUSY check may be repeated until BUSY=0 is verified.
- The address shown is being incremented.

BUSY CHECK

The BUSY flag, when at "1" level, shows that current operation is internal and that all commands but the status read are illegal. Any of these commands must be issued while BUSY flag is at "0" level. Exception : When SRCH=1, BUSY check is not neccessary before register reading (other than status) or command writing.

DISPLAY RAM

Addressing display RAM

The display RAM contains 80×128 bit of memory locations which can be accessed in unit of 8 bit denoted by X and Y addresses from the microcomputer. Means can be provided to automatically increment the X and Y addresses through the address control register. The addresses are incremented each time the microcomputer reads or writes the display RAM. Further information is found in command description. Fig. 9 shows the display RAM configuration. A row is selected by the AX address and a column by the Y address. The X addresses of AH-FH are reserved : do not use these X addresses. The column address is an 80-bit Z address data read into the display data latch circuit at line frequency on the rising edge of the LP; and then output from the display data latch circuit on the falling edge of the LP. The Z address is the value of the AZ register preset into the Z address counter while the FLM signal output at the frame frequency is at high state. The address is incremented in synchronous with the input LP signal. The incrementing loop depends on the duty ratio. For further information, see the command description. The Z address counter operates in synchronous with other LCD related timing signals, and independently of the X and Y address counters. For the AZ address register, specify the column line of the display RAM to be displayed on the top line. This is mainly used to change screen scrolling and page.

Display RAM data vs LCD

One bit of display RAM data represents one dot on the LCD. The status of each dot depends on the non-inverting display/inverting display setting of the REV register.

- With non-inverting display (REV=0)
  : dot is off when RAM data= "0"
  dot is on when RAM data= "1"
- With inverting display (REV=1)
  : dot is on when RAM data= "0"
  dot is off when RAM data= "1"

Display output Segment forward/reverse setting

Reversing the display RAM accessing from the microcomputer through the REF register, reverse the output order of the display outputs SEG1-SEG80. For further information, see "COMMAND FUNCTION".

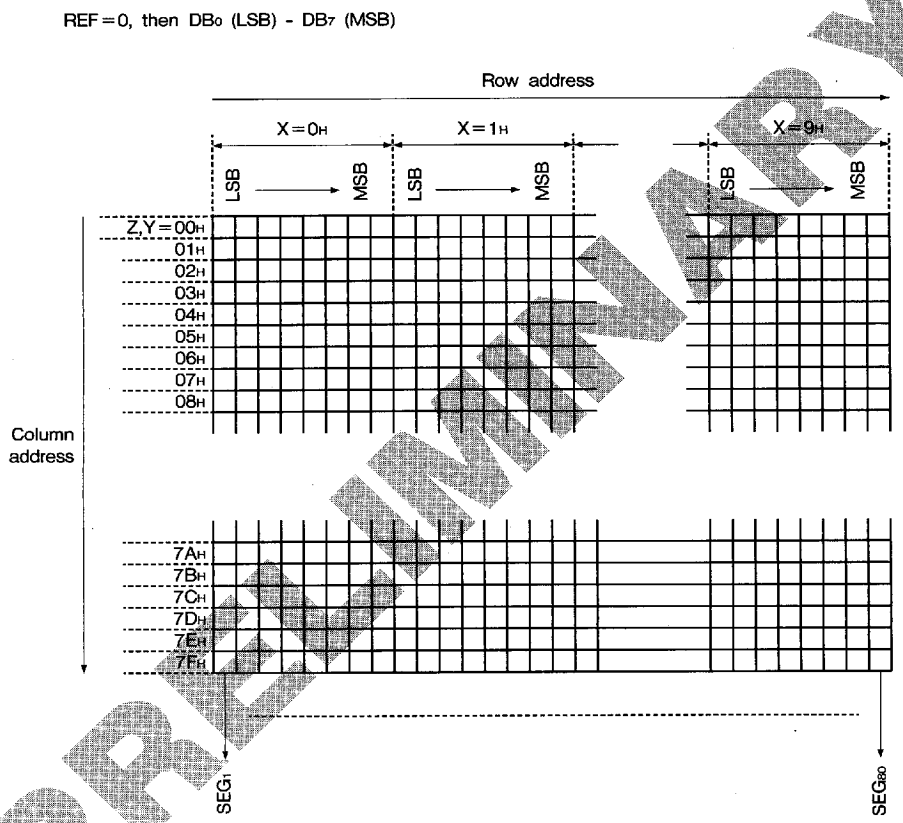


Fig. 9 Display RAM Configuration vs Segment Outputs

TIMING GENERATOR

The timing generator derives the timing clock for internal operation and the timing pulse (LP, FLM, M) from the master clock CK. The state of the timing pulse pins and timing generator are shown in Fig. 10.

H/SB PIN	MODE	LP PIN	M PIN	FLM PIN	STATE OF TIMING GENERATOR
L	Slave	In	In	In	LP, M, FLM generation circuits stop
H	Master	Out	Out	Out	Operating

Fig. 10 State of The Timing Pulse Pins and Timing Generator

For signals LP, M and FLM, see "LCD drive signal" in "PIN FUNCTION".

INITIAL SETTINGS

Placing low level on the RESB pin starts initialization. During initialization sequence, RESET flag in the status register is "1", requiring inhibition of operations other than the status register reading.

When changing default settings after the initialization, first set the value of the REF register, DUTY register and MC register.

BLOCK		DEFAULT SETTING	
Display RAM		Unknown	
Pins DB_0 to DB_7		Input mode	
Registers	Y address register	AY_6 - AY_0 = 00H	Column address 00H
	X address register	AX_3 - AX_0 = 0H	Row address 0H
	Status read selector	SRCH = 0	Status read mode
	Z address registers	AZ_6 - AZ_0 = 00H	Display starting line : 1st line
	X, Y address increment	AIM, AYI, AXI = 0	No increment
	M signal period	$MC_{1,0}$ = 0H	Duty raio x LP (frame period)/2
	Duty ratio	$DUTY_{1,0}$ = 0H	1/128
	Display control	REF = 0, REV = 0, ON/OFF = 1	SEG_1 to SEG_{80} in normal order, non-inverting, display off
	LCD output SEG_1 to SEG_{80} pins	Output is at V_5 level during RESB = L	

Fig. 11 Default Settings

COMMAND FUNCTIONS

Table 1 Commands

COMMAND	CSB	RS	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0	SETTING BY RDB (E), WRB (R/WB) Read mode	SETTING BY RDB (E), WRB (R/WB) Write mode	FUNCTION
Display RAM I/O	0	0	VRAM7-0 (Don't care)								Read on SRCH=0	Write on SRCH=0	DBi←→VRAMi raed/write (i=0-7)
Y address	0	1	1	AY6-0 (00H)							Set SRCH to "1"		Set display RAM column address/read
X address	0	1	0	0	0	0	AX3-0 (0H)				Write command code	Write on SRCH=0	Set display RAM row address/read
Status read select	0	1	0	0	0	1				SRCH (0)			Set read register selection
Z address (LSB)	0	1	0	0	1	0	AZ3-0 (0H)						Set column address of display RAM to be displayed on top of LCD/read
Z address (MSB)	0	1	0	0	1	1		AZ6-4 (0H)			Read data code		
X, Y address increment control	0	1	0	1	0	0		AIM (0)	AYI (0)	AXI (0)	Return SRCH to "0"		Controls increment operation of X and Y address counters
Set M signal period, duty ratio	0	1	0	1	0	1	MC 1, 0 (0H)		DUTY 1, 0 (0H)		* SRCH register cannot be read		Set M period/read (3 types) / Set duty ratio/read (3 types)
Display control	0	1	0	1	1	0		REF (0)	REV (0)	ON OFF (1)			● ON/OFF : Display on/off ● REV : Invert black and white ● REF : Set SEG out order (F/R)
Read status	0	1	BUSY	RESET	ON OFF	REV	AX3-0				Read on SRCH=0	—	● BUSY : Internal, operation state ● RESET : Default settings ● Other bits : Register value

NOTE :
Figures in parentheses are default settings.

SYSTEM CONFIGURATION EXAMPLE