PALCE20RA10 Family

Lattice/Vantis

24-Pin Asynchronous EE CMOS Programmable Array Logic

DISTINCTIVE CHARACTERISTICS

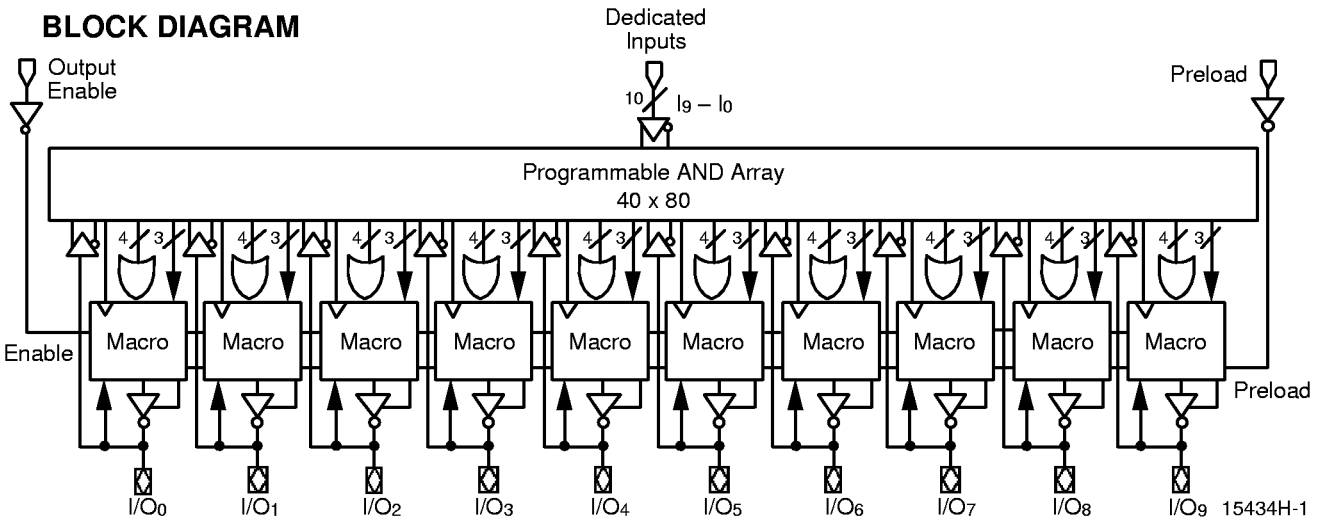
- **Low power at 100 mA I_{CC}**
- **As fast as 7.5 ns maximum propagation delay and 100 MHz f_{MAX} (external)**
- **Individually programmable asynchronous clock, preset, reset, and enable**
- **Registered or combinatorial outputs**
- **Programmable polarity**
- **Programmable replacement for high-speed CMOS or TTL logic**
- **TTL-level register preload for testability**
- **Extensive third-party software and programmer support through FusionPLD partners**
- **24-pin PDIP and 28-pin PLCC packages save space**
- **7.5 ns, 10 ns, and 15 ns versions utilize split leadframes for improved performance**

GENERAL DESCRIPTION

The PALCE20RA10 is an advanced PAL device built with low-power, high-speed, electrically-erasable CMOS technology. The PALCE20RA10 offers asynchronous clocking for each of the ten flip-flops in the device. The ten macrocells feature programmable clock, preset, reset, and enable, and all can operate asynchronously to other macrocells in the same device. The PALCE20RA10 also has flip-flop bypass, allowing any combination of registered and combinatorial outputs.

The PALCE20RA10 utilizes the familiar sum-of-products (AND/OR) architecture that allows users to implement complex logic functions easily and efficiently. Multiple levels of combinatorial logic can always be reduced to sum-of-products form, taking advantage of the very wide input gates available in PAL devices. The equations are programmed into the device through floating-gate cells in the AND logic array that can be erased electrically.

BLOCK DIAGRAM



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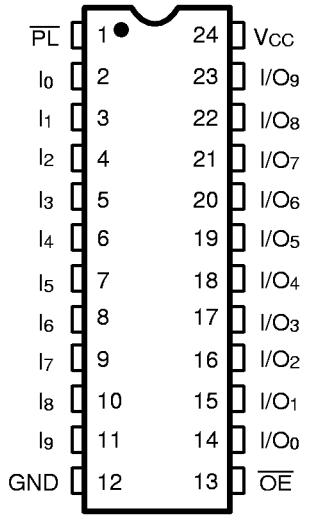
CONNECTION DIAGRAMS

Top View

SKINNYDIP



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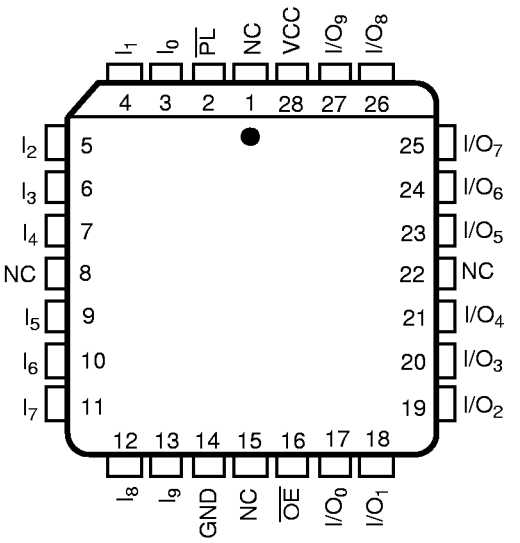
PLCC JEDEC



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Note: *Pin 1 is marked for orientation.*

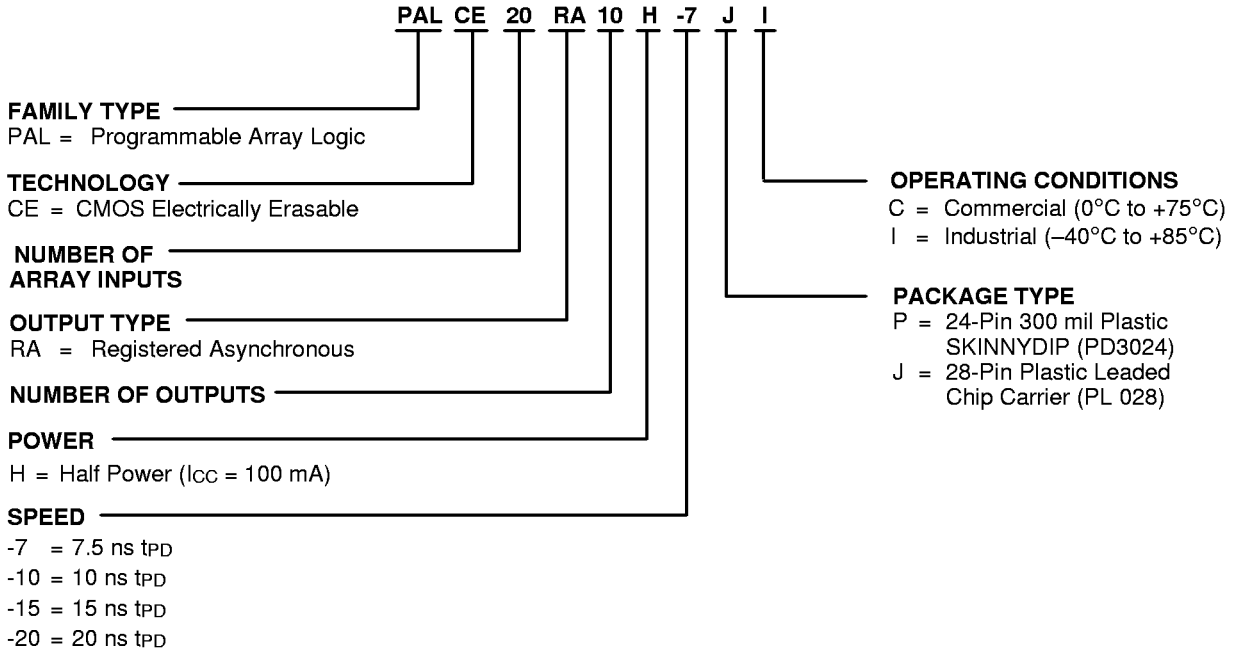
PIN DESIGNATIONS

GND	=	Ground
I	=	Input
I/O	=	Input/Output
NC	=	No Connect
$\overline{OE}$	=	Output Enable
$\overline{PL}$	=	Preload
V_{CC}	=	Supply Voltage

ORDERING INFORMATION

Commercial and Industrial Products

Programmable logic products for commercial and industrial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
PALCE20RA10H-7	JC, JI
PALCE20RA10H-10	PC, JC, PI, JI
PALCE20RA10H-15	
PALCE20RA10H-20	

Valid Combinations

Valid Combinations lists configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

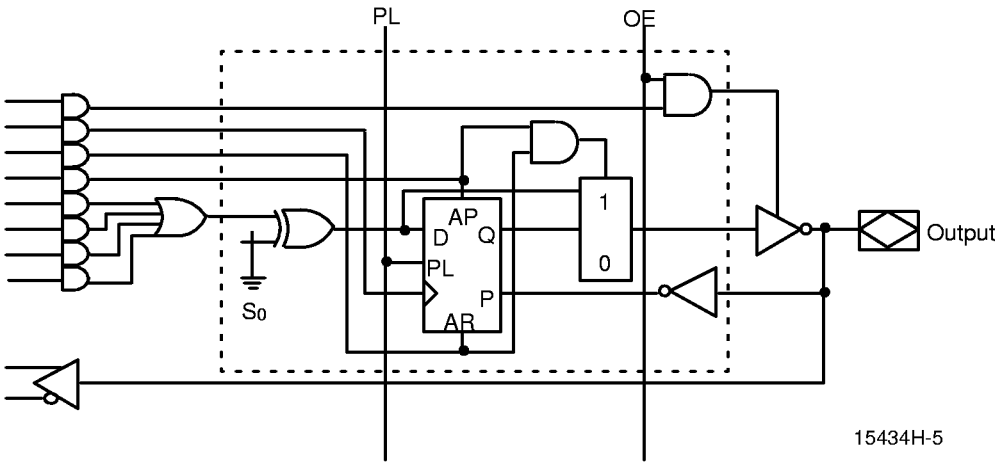


Figure 1. PALCE20RA10 Macrocell

FUNCTIONAL DESCRIPTION

The PALCE20RA10 has ten dedicated input lines and ten programmable I/O macrocells. The Registered Asynchronous (RA) macrocell is shown in Figure 1. $\overline{PL}$ serves as global register preload and $\overline{OE}$ serves as global output enable. Programmable output polarity is available to provide user-programmable output polarity for each individual macrocell.

The programmable functions in the PALCE20RA10 are automatically configured from the user's design specification, which can be in a number of formats. The design specification is processed by development software to verify the design and create a programming file. This file, once downloaded to a programmer, configures the device according to the user's desired function.

Programmable Preset and Reset

In each macrocell, two product lines are dedicated to asynchronous preset and asynchronous reset. If the preset product line is HIGH, the Q output of the register becomes a logic 1 and the output pin will be a logic 0. If the reset product line is HIGH, the Q output of the register becomes a logic 0 and the output pin will be logic 1. The operation of the programmable preset and reset overrides the clock.

Combinatorial/Registered Outputs

If both the preset and reset product lines are HIGH, the flip-flop is bypassed and the output becomes combinatorial. Otherwise, the output is from the register. Each output can be configured to be combinatorial or registered.

Programmable Clock

The clock input to each flip-flop comes from the programmable array, allowing any flip-flop to be clocked independently if desired.

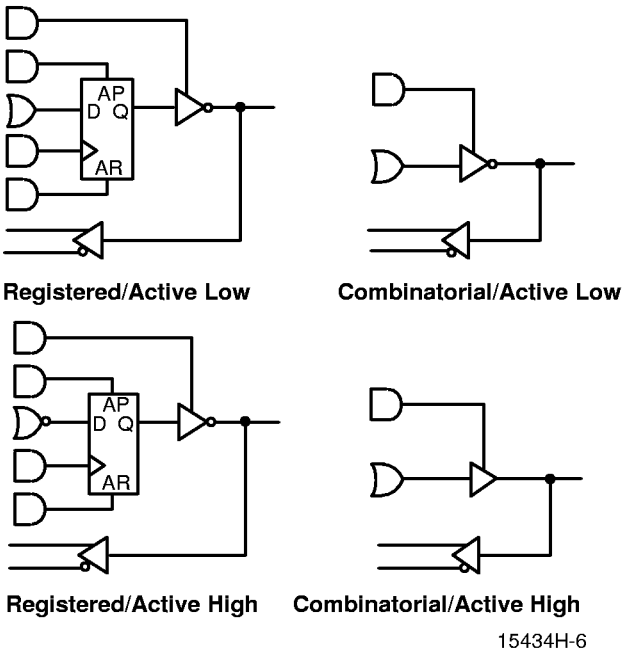


Figure 2. Macrocell Configurations

Three-State Outputs

The devices provide a product term dedicated to local output control. There is also a global output control pin. The output is enabled if both the global output control pin is LOW and the local output control product term is HIGH. If the global output control pin is HIGH, all outputs will be disabled. If the local output control product term is LOW, then that output will be disabled.

Security Bit

A security bit is also provided to prevent unauthorized copying of PAL device patterns. Once the bit is programmed, the circuitry enabling verification is permanently disabled, and the array will read as if every bit is programmed. With verification not operating, it is impossible to simply copy the PAL device pattern on a PAL device programmer. The security bit can only be erased in conjunction with the entire pattern.

Programmable Polarity

The outputs can be programmed either active-LOW or active-HIGH. This is represented by the Exclusive-OR gate shown in the PALCE20RA10 logic diagram. When the output polarity bit is programmed, the lower input to the Exclusive-OR gate is HIGH, so the output is active-HIGH. Similarly when the output polarity bit is unprogrammed, the output is active-LOW. The programmable output polarity feature allows the user a higher degree of flexibility when writing equations.

Programming and Erasing

The PALCE20RA10 can be programmed on standard logic programmers. Approved programmers are listed at the end of this databook. It also may be erased to reset a previously configured device back to its virgin state. Erasure is automatically performed by the programming hardware. No special erase operation is required.

Output Register Preload

The output registers on the PALCE20RA10 can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery. Register preload is controlled by a TTL-level signal, making it a convenient board-level initialization function. Details on output register preload can be found on page 16.

Power-Up Reset

All flip-flops power up to a logic LOW for predictable system initialization. Registered outputs of the PALCE20RA10 will be HIGH due to the output inverter. The state of combinatorial outputs will be a function of the logic. Details on power-up reset can be found on page 16.

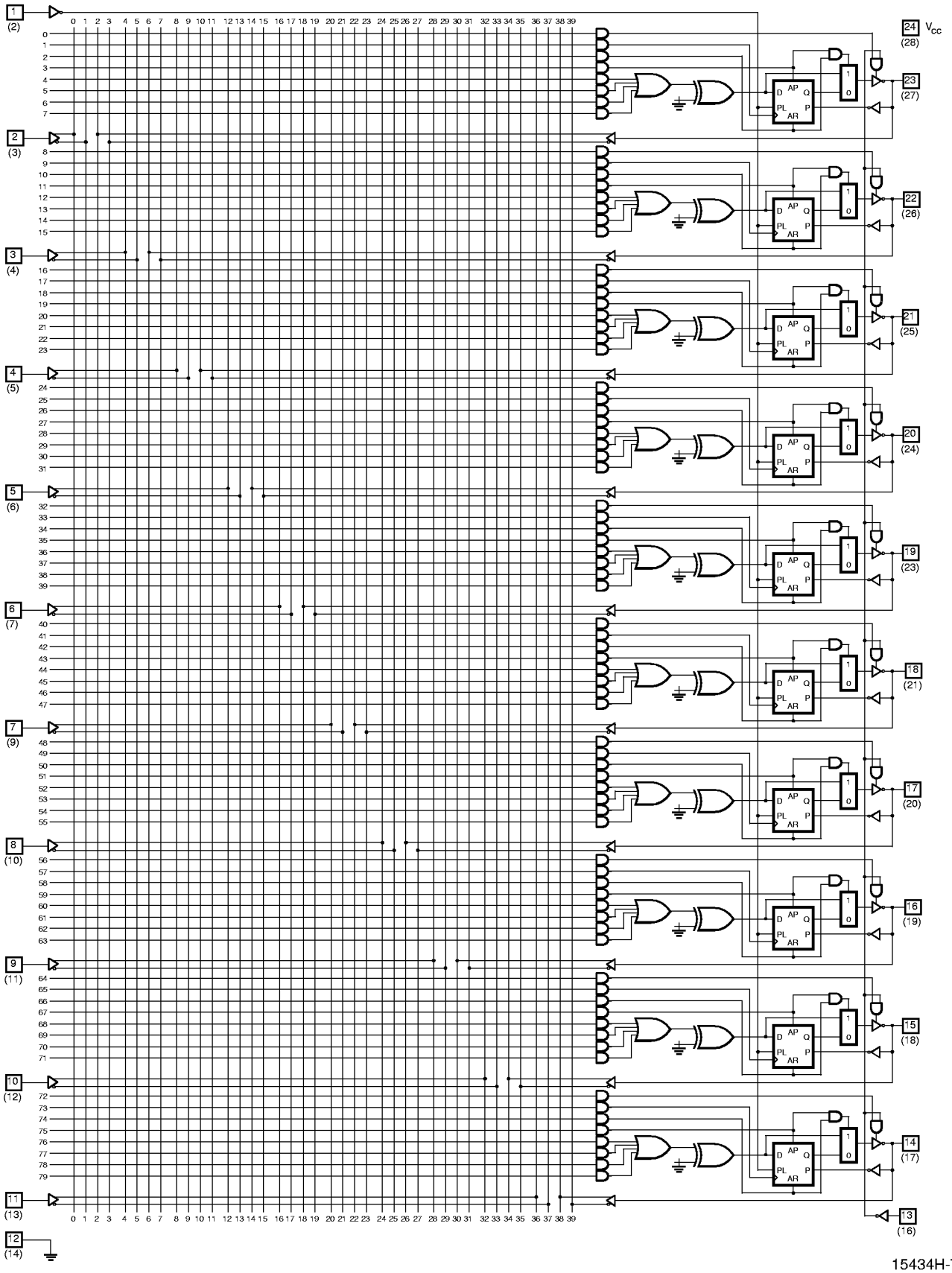
Quality and Testability

The PALCE20RA10 offers a very high level of built-in quality. The erasability of the device provides a means of verifying performance of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming yields and post-programming functional yields in the industry.

Technology

The high-speed PALCE20RA10 is fabricated with Our advanced electrically erasable (EE) CMOS process. The array connections are formed with proven EE cells. Inputs and outputs are designed to be compatible with TTL devices. This technology provides strong input clamp diodes, output slew-rate control, and a grounded substrate for clean switching.

LOGIC DIAGRAM
SKINNYDIP (PLCC JEDEC) Pinouts



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ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature with Power Applied . . . . . –55°C to +125°C

Supply Voltage with Respect to Ground . . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current (T_A = –40°C to +85°C) . . . . . 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air . . . . . 0°C to +75°C

Supply Voltage (V_{CC}) with Respect to Ground . . . . . +4.75 V to +5.25 V

Industrial (I) Devices

Ambient Temperature (T_A) Operating in Free Air . . . . . –40°C to +85°C

Supply Voltage (V_{CC}) with Respect to Ground . . . . . +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL and INDUSTRIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min			0.4	V
V_{IH}	Input HIGH Voltage Voltage for all Inputs	Guaranteed Input Logical HIGH (Note 1)		2.0		V
V_{IL}	Input LOW Voltage Voltage for all Inputs	Guaranteed Input Logical LOW (Note 1)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.5 V, V_{CC} = Max			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max			–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.5 V, V_{CC} = Max V_{IN} = V_{IL} or V_{IH} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IL} or V_{IH} (Note 2)			–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)		–30	–130	mA
I_{CC} (Static)	Commercial Supply Current	V_{IN} = 0 V, Outputs Open	-7/10/15		100	mA
		I_{OUT} = 0 mA, V_{CC} = Max, (Note 4)	-20		90	mA
I_{CC} (Static)	Industrial Supply Current	V_{IN} = 0 V, Outputs Open	-7/10/15		115	mA
		I_{OUT} = 0 mA, V_{CC} = Max, (Note 4)	-20		100	mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
4. *This parameter is guaranteed under worst case test conditions.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description		Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	Inputs	V_{IN} = 2.0 V	V_{CC} = 5.0 V	5	pF
		$\overline{OE}$		T_A = +25°C	9	
C_{OUT}	Output Capacitance		V_{OUT} = 2.0 V	f = 1 MHz	8	

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

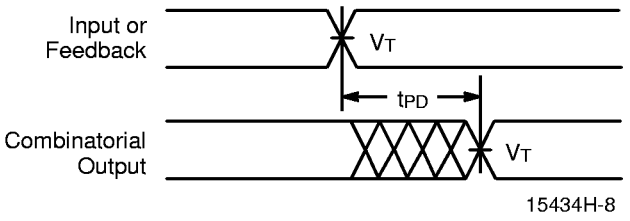
SWITCHING CHARACTERISTICS over COMMERCIAL and INDUSTRIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			-7		-10		-15		-20		Unit
				Min (3)	Max	Min (3)	Max	Min (3)	Max	Min (3)	Max	
t_{PD}	Input or Feedback to Combinatorial Output				7.5		10		15		20	ns
t_S	Setup Time from Input, Feedback or SP to Clock			2.5		3		4		4		ns
t_H	Hold Time			2.5		3		4		4		ns
t_{CO}	Clock to Output or Feedback				7.5		10		15		20	ns
t_{AP}	Asynchronous Preset to Registered Output				7.5		10		15		20	ns
t_{APW}	Asynchronous Preset Width (Note 3)			5		8		10		12		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 3)				5		7		10		12	ns
t_{AR}	Asynchronous Reset to Registered Output				7.5		10		15		20	ns
t_{ARW}	Asynchronous Reset Width (Note 3)			5		8		10		12		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 3)				5		7		10		12	ns
t_{WL}	Clock Width	LOW		4		5		8		12		ns
t_{WH}		HIGH		4		5		8		12		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S + t_{CO})$	100		76.9		52.6		37		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	125		100		62.5		41.6		MHz
t_{PZX}	$\overline{OE}$ to Output Enable				5		8		10		15	ns
t_{PXZ}	$\overline{OE}$ to Output Disable				5		8		10		15	ns
t_{EA}	Input to Output Enable Using Product Term Control				7.5		10		15		20	ns
t_{ER}	Input to Output Disable Using Product Term Control				7.5		10		15		20	ns
t_{WP}	Preload Pulse Duration			5		7		10		15		ns
t_{SP}	Preload Setup Time			5		7		10		15		ns
t_{HP}	Preload Hold Time			5		7		10		15		ns

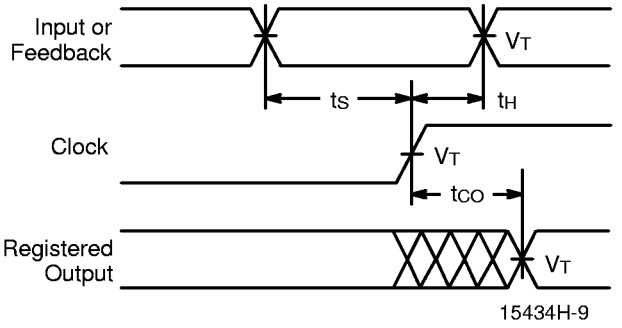
Notes:

2. *See Switching Test Circuit for test conditions.*
3. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.*
4. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where the frequency may be affected.*

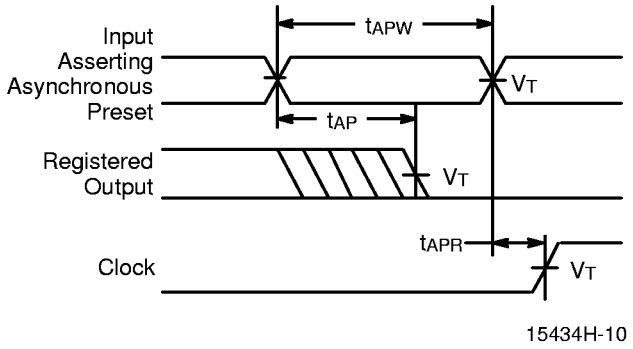
SWITCHING WAVEFORMS



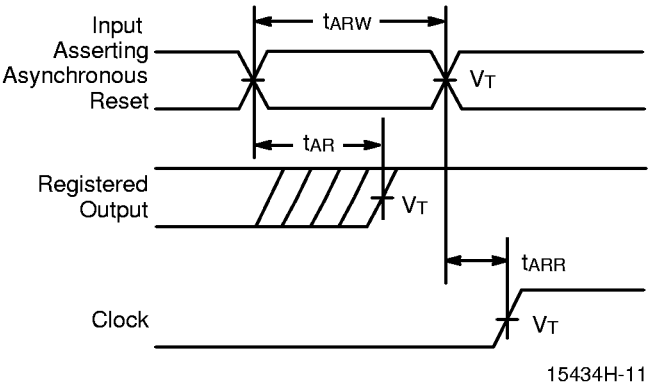
Combinatorial Output



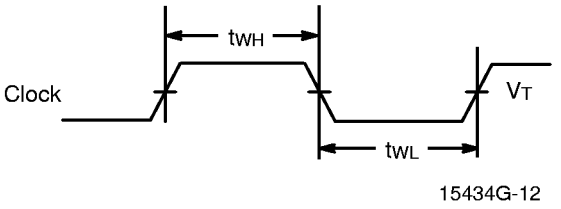
Registered Output



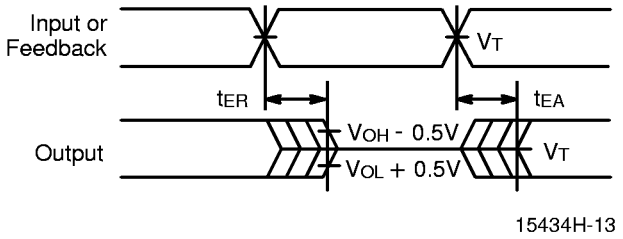
Asynchronous Preset



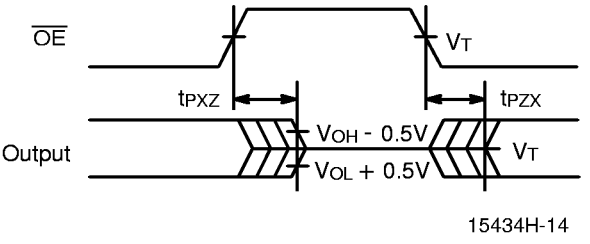
Asynchronous Reset



Clock Width



Input to Output Disable/Enable

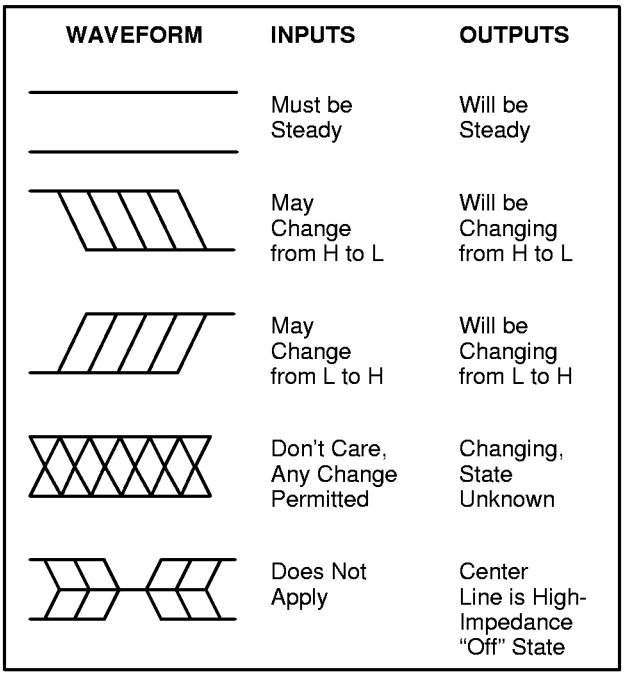


$\overline{OE}$ to Output Disable/Enable

Notes:

1. *V_T = 1.5 V*
2. *Input pulse amplitude 0 V to 3.0 V*
3. *Input rise and fall times 2 ns – 5 ns typical.*

KEY TO SWITCHING WAVEFORMS



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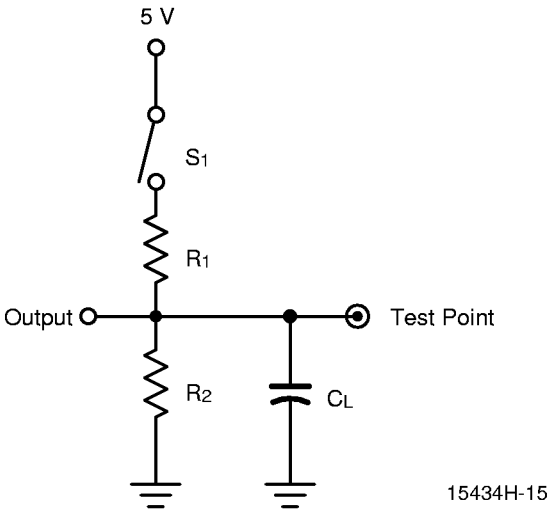
SWITCHING TEST CIRCUIT



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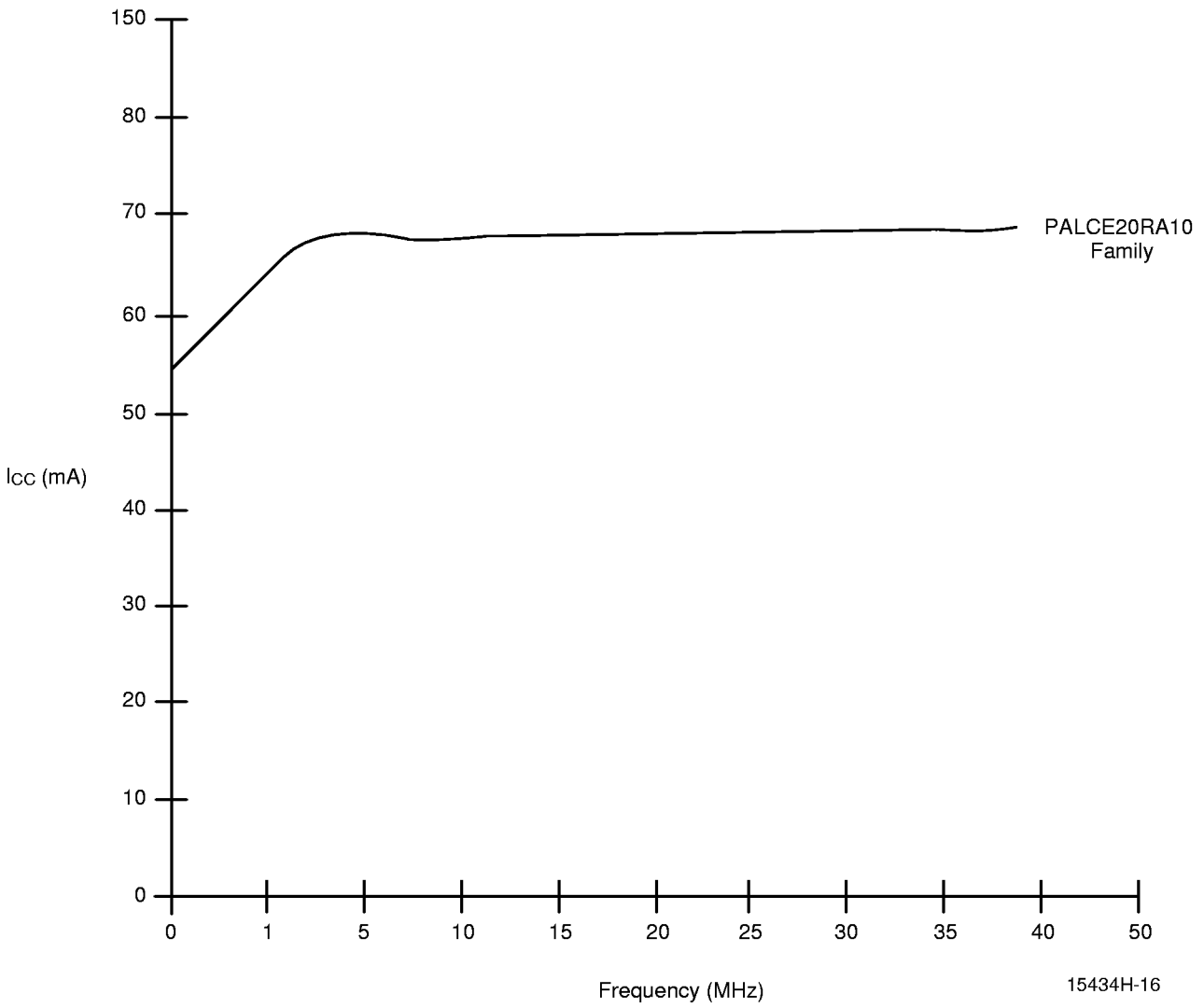
Specification	S_1	C_L	Commercial and Industrial R_1	Commercial and Industrial R_2	Measured Output Value
t_{PD}, t_{CO}	Closed	50 pF	All except H-20: 300 Ω	All except H-20: 300 Ω	1.5 V
t_{PZX}, t_{EA}	Z → H: Open Z → L: Closed				1.5 V
t_{PXZ}, t_{ER}	H → Z: Open L → Z: Closed	5 pF	H-20: 560 Ω	H-20: 1.1 kΩ	H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

TYPICAL I_{CC} CHARACTERISTICS

V_{CC} = 5 V, T_A = 25°C



I_{CC} vs. Frequency

The selected "typical" pattern utilized 50% of the device resources. Half of the macrocells were programmed as registered, and the other half were programmed as combinatorial. Half of the available product terms were used for each macrocell. On any vector, half of the outputs were switching.

By utilizing 50% of the device, a midpoint is defined for I_{CC}. From this midpoint, a designer may scale the I_{CC} graphs up or down to estimate the I_{CC} requirements for a particular design.

ENDURANCE CHARACTERISTICS

The PALCE20RA10 is manufactured using our advanced Electrically Erasable process. This technology uses an EE cell to replace the fuse link used in bipolar parts. As a result, the device can be erased and reprogrammed—a feature which allows 100% testing at the factory.

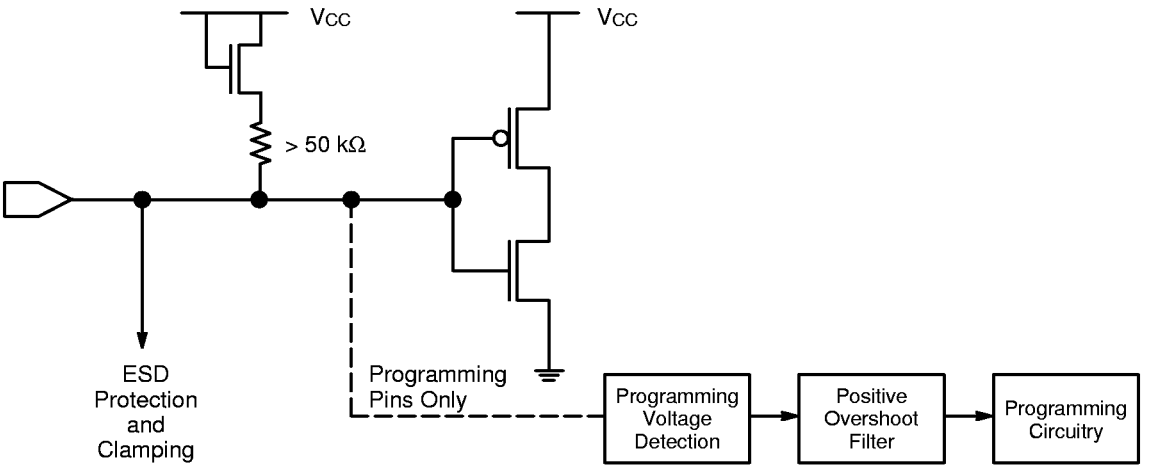
Symbol	Parameter	Test Conditions	Min	Unit
t_{DR}	Min Pattern Data Retention Time	Max Storage Temperature	10	Years
		Max Operating Temperature	20	Years
N	Min Reprogramming Cycles	Normal Programming Conditions	100	Cycles

Robustness

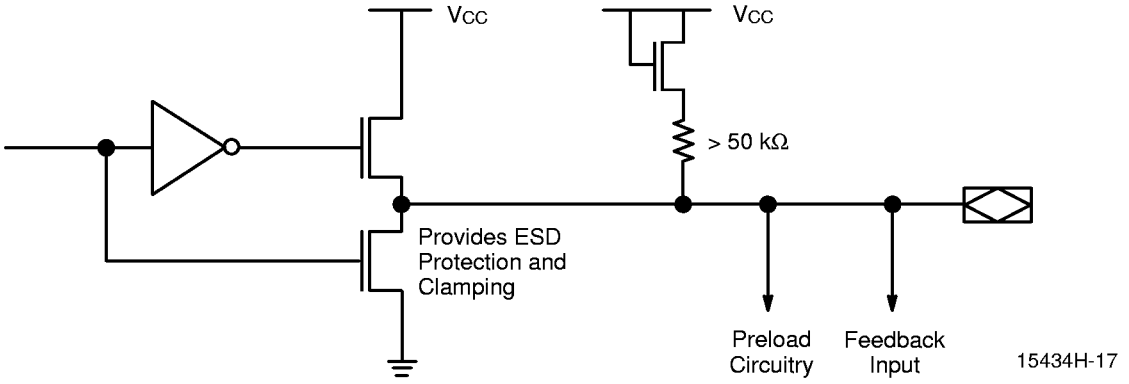
The PALCE20RA10 has been designed with some unique features that make it extremely robust, even when operating in high-speed design environments. Pull-up resistors on the inputs and I/Os cause unconnected pins to default to the HIGH state. Please note that these pull-up resistors are only for this purpose, and do not provide enough current to sufficiently pull a bus line high. We recommend that external pull-up or pull-down resistors be used if the condition of a floating bus line exists.

Input-clamping circuitry limits negative overshoot, eliminating the possibility of false clocking caused by subsequent ringing. A special noise filter makes the programming circuitry completely insensitive to any positive overshoot that has a pulse width of less than about 100 ns.

INPUT/OUTPUT EQUIVALENT SCHEMATICS



Typical Input



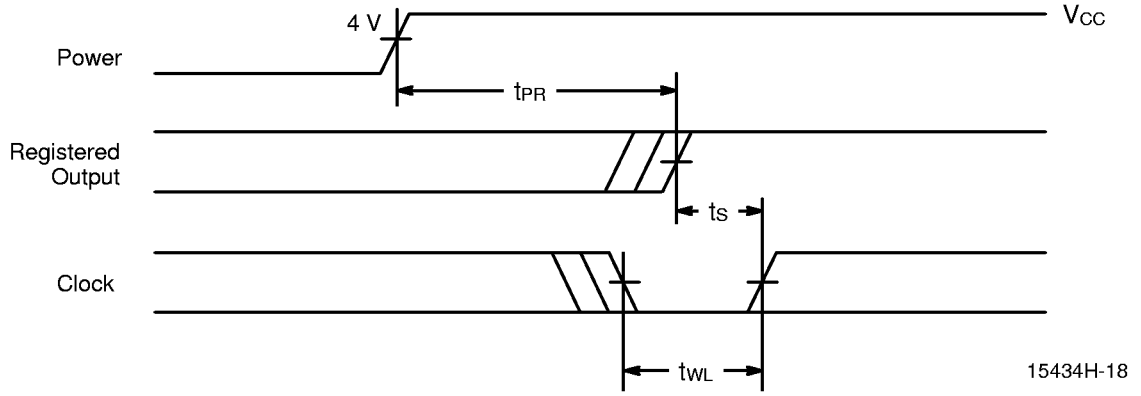
Typical Output

POWER-UP RESET

The PALCE20RA10 has been designed with the capability to reset during system power-up. Following power-up, all flip-flops will be reset to LOW. The output state will be HIGH independent of the logic polarity. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

- The V_{CC} rise must be monotonic.
- Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Descriptions	Max	Unit
t_{PR}	Power-Up Reset Time	1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		

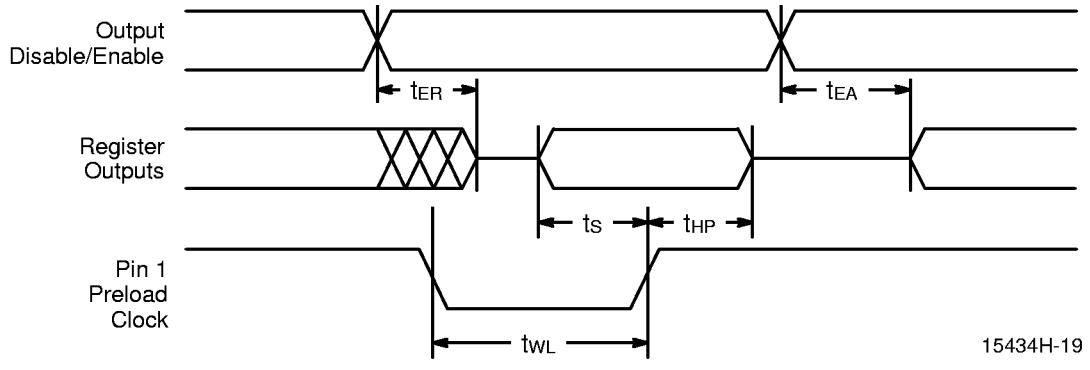


Power-Up Reset Waveform

OUTPUT REGISTER PRELOAD

The preload function allows the register to be loaded from the output pins. This feature aids functional testing of sequential designs by allowing direct setting of output states. The procedure for preloading follows.

1. Disable output registers.
2. Apply either V_{IH} or V_{IL} to all registered outputs. Leave combinatorial outputs floating.
3. Pulse $\overline{PL}$ from V_{IH} to V_{IL} to V_{IH}.
4. Remove V_{IL}/V_{IH} from all registered output pins.
5. Enable the output registers.
6. Verify V_{OL}/V_{OH} at all registered output pins. Note that because of the output inverter, a register that has been preloaded HIGH will provide a LOW at the output. Also note that because there is an inverter on the register preload input, the level presented on the register preload input at the time of preload will be present on the register output pin following the preload sequence e.g., a low on the register pin at the time of preload will result in a low on that pin after preload.



Output Register Preload Waveform