1M x 32 CMOS Static RAM Module

Features

- ☐ High-density 4 megabyte Static RAM module
- ☐ Low profile 72-pin ZIP (Zig-zag In-line vertical Package) or 72-pin SIMM (Single In-line Memory Module)
- ☐ Fast access time: 20 ns (max.)
- ☐ Surface mounted plastic components on an epoxy laminate (FR-4) substrate Single 5V (±10%) power supply
- ☐ Multiple GND pins and decoupling capacitors for maximum noise immunity
- ☐ Inputs/outputs directly TTL compatible

Description

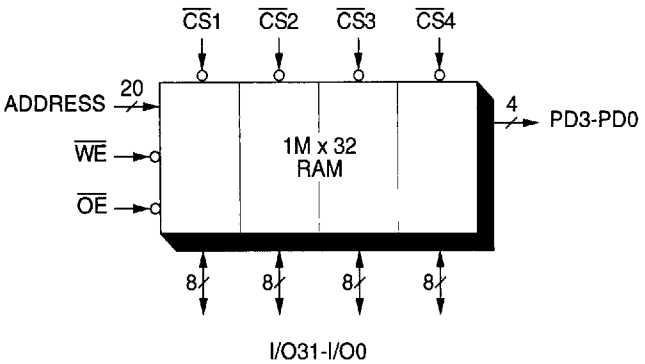
The PDM4M4120 is a 1M x 32 static RAM module constructed on an epoxy laminate (FR-4) substrate using eight 1M x 4 static RAMs in plastic SOJ packages. Availability of four chip select lines (one for each of two RAMs) provides byte access. The PDM4M4120 is available with access times as fast as 20 ns with minimal power consumption.

The PDM4M4120 is packaged in a 72-pin FR-4 ZIP (Zig-zag In-line vertical Package) or a 72-pin SIMM (Single In-line Memory Module). The ZIP configuration allows 72 pins to be placed on a package 3.950" long and 0.365" wide. At only 0.590" high, this low-profile package is ideal for systems with minimum board spacing. The SIMM configuration allows use of edge mounted sockets to secure the module.

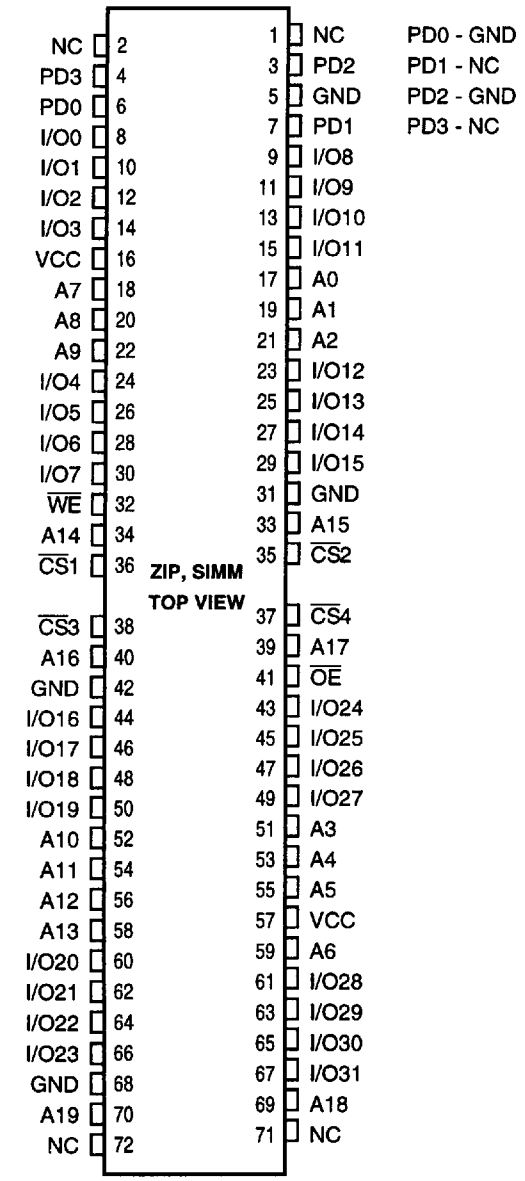
All inputs and outputs of the PDM4M4120 are TTL compatible and operate from a single 5V supply. Full asynchronous circuitry requires no clock or refresh for operation and provides equal access and cycle times for ease of use.

Four identification pins (PD0, PD1, PD2, PD3) are provided for applications in which different density versions of the module are used. In this way, the target system can read the respective levels of PD0, PD1, PD2, PD3 to determine a 1M depth.

Functional Block Diagram



Pin Configuration[1]



NOTE: 1. Pins 3, 4, 6, and 7 (PD0, PD1, PD02, and PD3 respectively) are read by the user to determine the density of the module. If PD0 reads GND, PD1 reads NC, PD2 reads GND, PD3 reads NC then the module has a 1M depth.

Pin Assignment

Pin	Signal
I/O31-I/O0	Data Inputs/Outputs
A19-A0	Addresses
$\overline{CS4}$-$\overline{CS1}$	Chip Selects
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
PD3-PD0	Depth Identification
Vcc	Power
GND	Ground

Truth Table

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	High-Z	Standby
Read	L	L	H	$DATA_{OUT}$	Active
Write	L	X	L	$DATA_{IN}$	Active
Read	L	H	H	High-Z	Active

Absolute Maximum Ratings(1)

Symbol	Rating	Com'l.	Ind.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_{BIAS}	Temperature Under Bias	–10 to +85	–10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
T_A	Operating Temperature	0 to +70	0 to +70	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE: 1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
GND	Supply Voltage	0	0	0	V
Commercial	Ambient Temperature	0	25	70	°C

DC Electrical Characteristics (V_{CC} = 5.0V ± 5%, T_A = 0°C to 70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
I_{LI}	Input Leakage Current (Address)	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	80	µA
I_{LI}	Input Leakage Current (Data)	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}, V_{CC} = Max., $\overline{CS}$ = V_{IH}	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = 8 mA, V_{CC} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OL} = –4 mA, V_{CC} = Min.	2.4	—	V
V_{IH}	Input High Voltage		2.2	6.0	V
V_{IL}	Input Low Voltage		–0.5[1]	0.8	V

NOTE 1. V_{IL} = –1.5V for pulse widths less than 10 ns, once per cycle.

Power Supply Characteristics

Symbol	Parameter	Max[1]	Unit
I_{CC}	Operating Current $\overline{CS}$ = V_{IL}, V_{CC} = Max., f = f_{MAX}, Outputs Open	1280	mA
I_{SB}	Standby Current $\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., f = f_{MAX}, Outputs Open	480	mA
I_{SB1}	Full Standby Current $\overline{CS}$ ≥ V_{CC} – 0.2V, f = 0, V_{IN} > V_{CC} – 0.2V or < 0.2V, Outputs Open	120	mA

NOTE 1. Preliminary specification only.

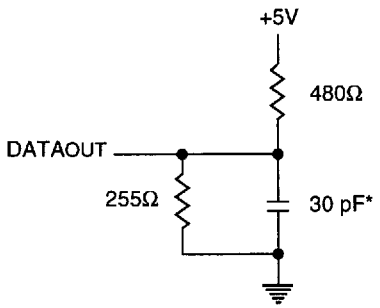
Capacitance[1] (T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter	Max.	Unit
$C_{I/O}$	Data I/O Capacitance, V_{IN} = 0V	15	pF
$C_{IN(1)}$	Input Capacitance, (Address) V_{IN} = 0V	60	pF
$C_{IN(2)}$	Input Capacitance, ($\overline{WE}$, $\overline{OE}$) V_{IN} = 0V	75	pF
$C_{IN(3)}$	Input Capacitance, ($\overline{CS}$), V_{IN} = 0V	20	pF

NOTE 1. This parameter is determined by device characteristics but is not production tested.

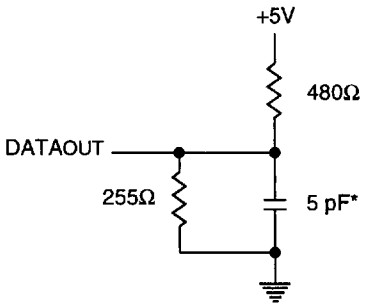
AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5 ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2



* Including scope and jig capacitances

Figure 1. Output Load



* Including scope and jig capacitances

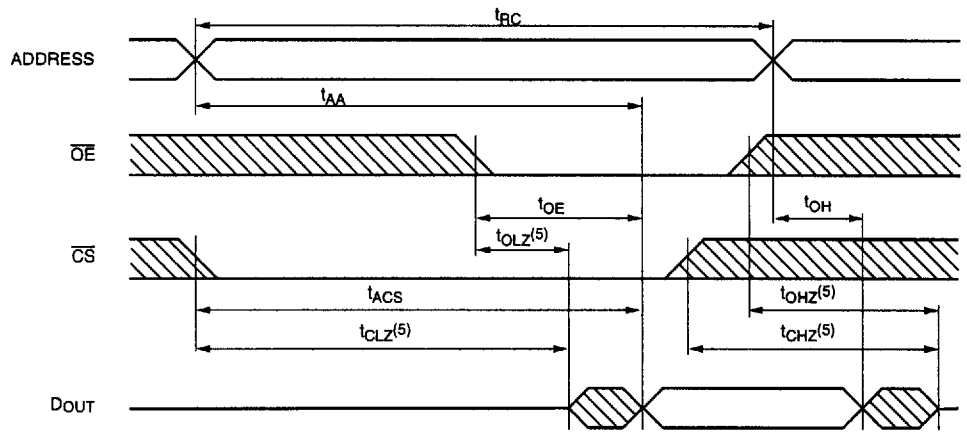
Figure 2. Output Load
(for tOHZ, tCHZ, tOLZ, and tCLZ)

AC Electrical Characteristics (Vcc = 5V ± 5%, T_A = 0°C to +70°C)

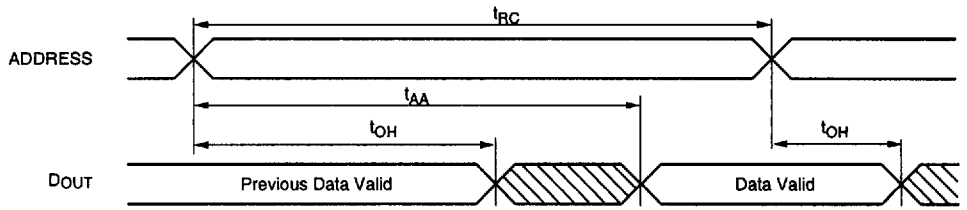
Symbol	Parameter	PDM4M4120SXXZ, PDM4M4120SXXM						Unit
		-20 ns		-25 ns		-35 ns		
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	20	—	25	—	35	—	ns
t_{AA}	Address Access Time	—	20	—	25	—	35	ns
t_{ACS}	Chip Select Access Time	—	20	—	25	—	35	ns
t_{CLZ}(1)	Chip Select to Output inLow-Z	3	—	3	—	3	—	ns
t_{OE}	Output Enable to Output Valid	—	10	—	15	—	18	ns
t_{OLZ}(1)	Output Enable to Output in Low-Z	0	—	0	—	0	—	ns
t_{CHZ}(1)	Chip Deselect to Output in High-Z	—	10	—	12	—	18	ns
t_{OHZ}(1)	Output Disable to Output in High-Z	—	10	—	12	—	18	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	ns
t_{PU}(1)	Chip Select to Power-Up Time	0	—	0	—	0	—	ns
t_{PD}(1)	Chip Deselect to Power-Down Time	—	20	—	25	—	35	ns
Write Cycle								
t_{WC}	Write Cycle Time	20	—	25	—	35	—	ns
t_{CW}	Chip Select to End of Write	17	—	20	—	30	—	ns
t_{AW}	Address Valid to End of Write	17	—	20	—	30	—	ns
t_{AS}	Address Setup Time	0	–	0	—	0	—	ns
t_{WP}	Write Pulse Width	15	—	20	—	30	—	ns
t_{WR}	Write Recovery Time	3	—	3	—	3	—	ns
t_{WHZ}(1)	Write Enable to Output in High-Z	—	10	—	15	—	20	ns
t_{DW}	Data to Write Time Overlap	12	—	15	—	20	—	ns
t_{DH}	Data Hold from Write Time	0	—	0	—	0	—	ns
t_{OW}(1)	Output Active from End of Write	0	—	0	—	0	—	ns

NOTE 1. This parameter is determined by device characteristics but is not production tested.

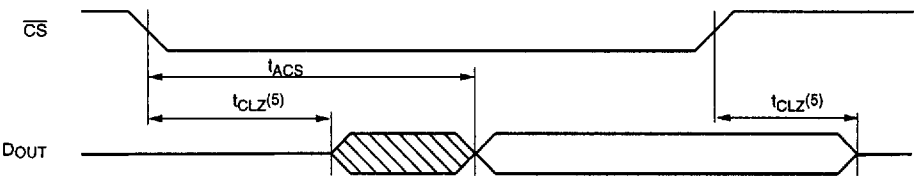
Timing Waveforms of Read Cycle No.1(1)



Timing Waveforms of Read Cycle No.2(1,2,4)

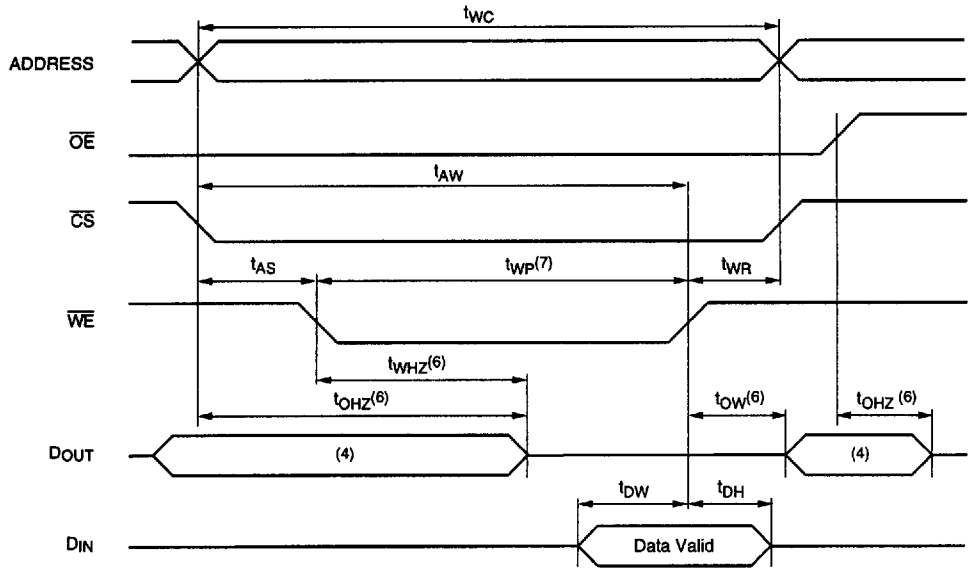


Timing Waveforms of Read Cycle No.3(1,3,4)

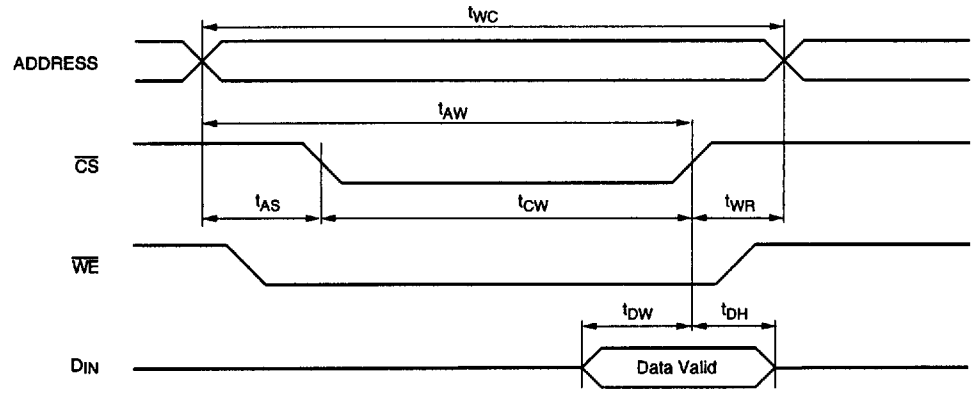


NOTES 1. $\overline{WE}$ is HIGH for Read Cycle.
2. Device is continuously selected. $\overline{CS} = V_{IL}$.
3. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
4. $\overline{OE} = V_{IL}$.
5. Transition is measured ±200 mV for steady state. This parameter is determined by device characteristics but is not production tested.

Timing Waveforms of Write Cycle No.1 ($\overline{WE}$ Controlled)(1,2,3,7)



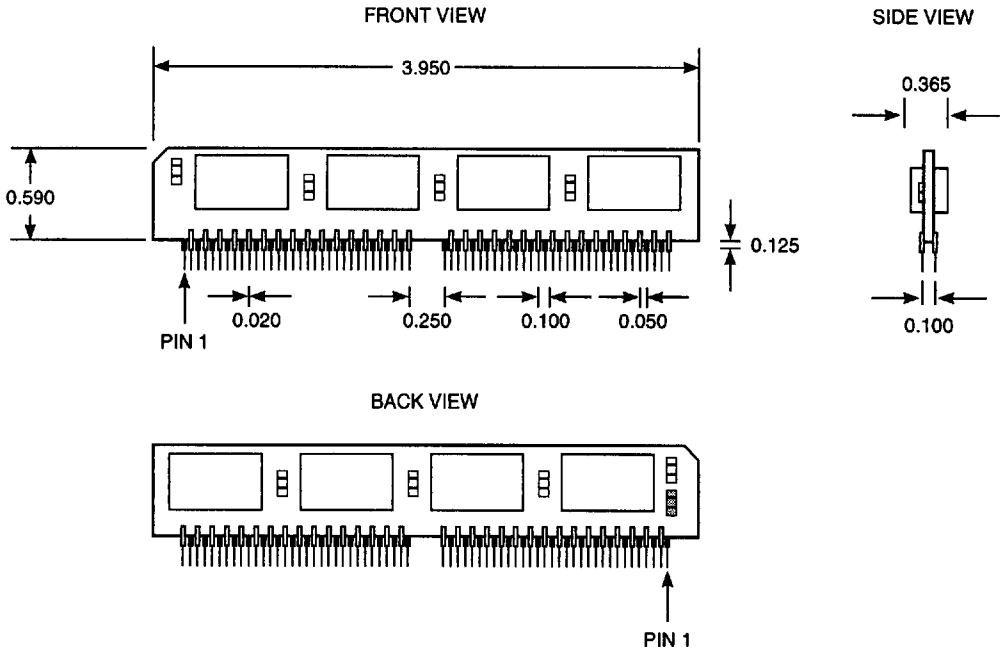
Timing Waveforms of Write Cycle No.2 ($\overline{CS}$ Controlled)(1,2,3,5)



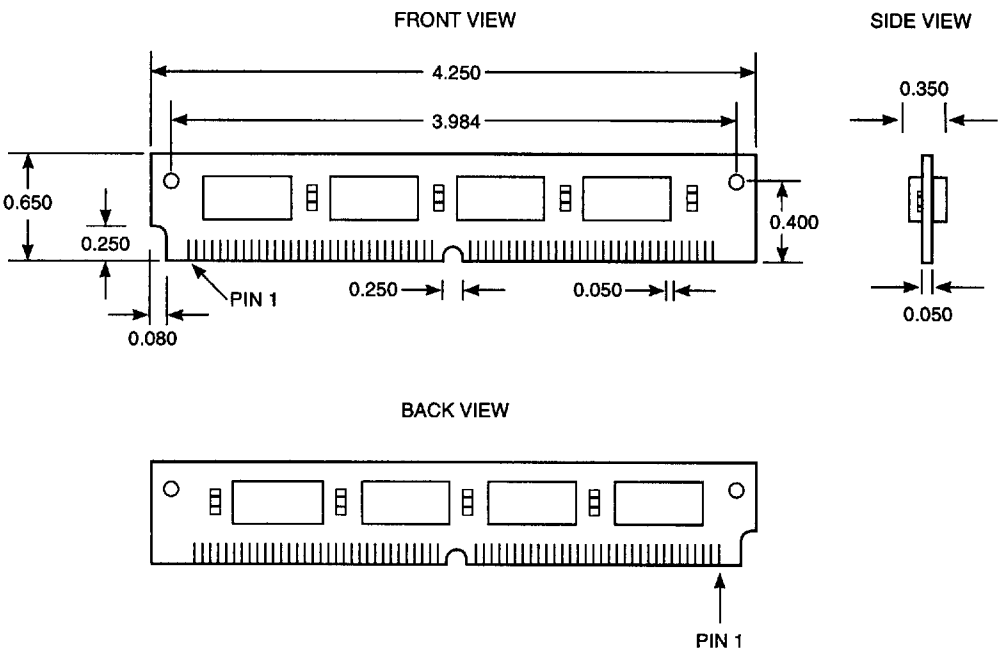
NOTES 1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to end the write cycle.
4. During this period, I/O pins are in the output state, and input signals must be applied.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
6. Transition is measured ±200 mV for steady state with a 5 pF load (including scope and jig). This parameter is determined by device characteristics but is not production tested.
7. If $\overline{OE}$ is LOW during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or ($t_{WHZ} + t_{DW}$) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse width can be as short as the specified t_{WP}.

Package Dimensions

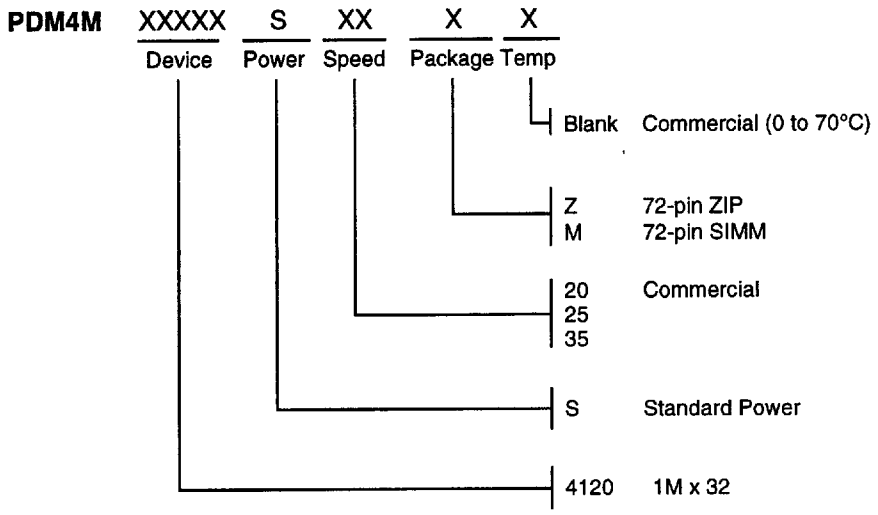
ZIP Version



SIMM Version



Ordering Information



Advanced Packaging

Advances in packaging techniques permit a wide variety of solutions to board space problems.

Modules are comprised of individual semiconductor devises with other support devises, such as decoders and capacitors as required, mounted on a multilayer substrate. The substrate is custom designed to provide appropriate circuitry for the components in a package configuration that meets thermal and mechanical design objectives in a minimal amount of board real estate. The final module may have a through-hole pin configuration or may be surface mountable device.

Commercial modules are generally developed using components encapsulated in plastic, surface mounted on FR4 epoxy laminate substrates. The surface mountable component packages may be SOJ, SOIC, VSOP, TSOP, or QFP styles.

Ceramic packaging may be used for devices that need to be hermetic or require extended temperature range performance, such as military applications. Ceramic modules may use LCC or CSOJ component packaging on ceramic substrates with sidebrazed lead attach, or may use multiple die bonded in an MCM-C package.

Module Package Styles

Many module package styles are available from Paradigm. Features and relative board space are described here.

SIP

Vertically mounted, the SIP (Single In-line Package) contains a single row of pins along on edge for through-hole assembly. Pins are on a 100-mil pitch. Components may be mounted on both sides of the substrate. The device is most commonly constructed using plastic encapsulated components on an FR4 substrate, but it may be constructed of ceramic, as well. The vertical orientation and the ability to mount components on both sides of the substrate adds up to exceptional density.

ZIP

ZIP (Zig-zag In-line Package) is similar in space savings to the SIP, since both feature vertical substrate configurations. They also feature the additional advantages of larger pin counts with the structural stability of two rows of pins. Pins are placed on a 100-mil pitch, with 100-mil spacing between the rows.

SIMM

The SIMM (Single In-line Memory Module) package is similar to the SIP. The major difference is, rather than a single row of pins, the bottom edge has a row of connector contacts that are designed to plug into a socket mounted on the motherboard. Spacing between contacts is either 50- or 100-mil pitch. Since socket mounted SIMMs may be changed easily, they offer greater system flexibility by allowing multiple densities and speed grades.

CELP/DIMM

Like the SIMM, the DIMM (Dual readout In-line Memory Module) is socket mounted, but its dual readout contains larger pinouts for extremely high density in a compact component.

DIP

DIP (Dual In-line Package) modules offer a low profile with excellent mechanical ruggedness. Historically, DIP modules have provided the same form, fit, and function as future generation memory devices. Ceramic DIP modules have also been the preferred package for military applications.

PGA

The PGA (Pin Grid Array) has an array of pins arranged in a matrix on a 100-mil grid. This ceramic package style provides a large pin count in a smaller area than possible in package styles with pins only on the package edge or perimeter. With its large number of through-hole contract points, it offers exceptional structural integrity. This package style is also commonly used for multichip arrays bonded within a single cavity.