NEC

MOS INTEGRATED CIRCUIT

μPD23C8000L

8M-BIT MASK-PROGRAMMABLE ROM
1M-WORD BY 8-BIT (BYTE MODE) / 512K-WORD BY 16-BIT (WORD MODE)

Description

The μPD23C8000L is a 8,388,608 bits mask-programmable ROM. The word organization is selectable (BYTE mode : 1,048,576 words by 8 bits, WORD mode : 524,288 words by 16 bits).

The active levels of OE (Output Enable Input) can be selected with mask-option.

The μPD23C8000L are packed in 42-pin plastic DIP, 44-pin plastic SOP, 48-pin plastic TSOP (I) and 44-pin plastic TSOP (II).

Features

- Word organization
  - 1,048,576 words by 8 bits (BYTE mode)
  - 524,288 words by 16 bits (WORD mode)
- Operating supply voltage : V_{CC} = 2.7 to 3.6 V

Operating supply voltage V_{CC}	Access time ns (MAX.)	Power supply current (Active mode) mA (MAX.)	Standby current (CMOS level input) μA (MAX.)
3.0 V ± 0.3 V	140	30	30
3.3 V ± 0.3 V	120	35	30

Ordering Information

Part number	Package
μPD23C8000LCZ-xxx	42-pin plastic DIP (600 mil)
μPD23C8000LGX-xxx	44-pin plastic SOP (600 mil)
μPD23C8000LGY-xxx-MJH	48-pin plastic TSOP (I) (12 × 18 mm) (Normal bent)
μPD23C8000LGY-xxx-MKH	48-pin plastic TSOP (I) (12 × 18 mm) (Reverse bent)
μPD23C8000LG5-xxx-7JF	44-pin plastic TSOP (II) (400 mil) (Normal bent)

(xxx : ROM code suffix No.)

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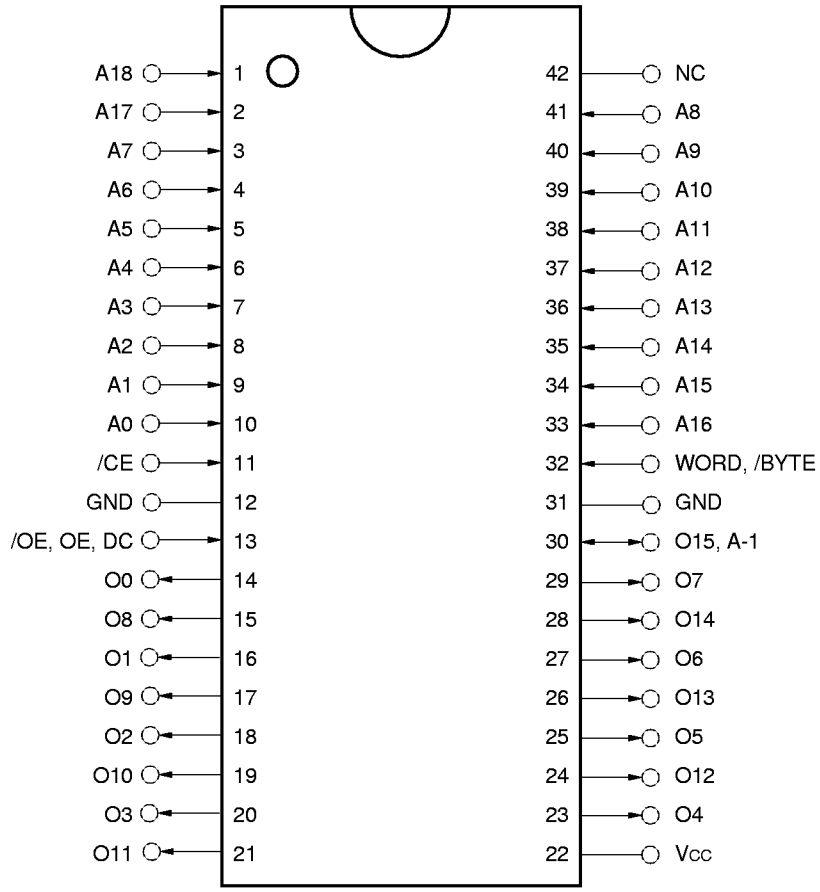
The mark ★ shows major revised points.

Pin Configuration (Marking Side)

/xxx indicates active low signal.

42-pin Plastic DIP (600 mil)

[μPD23C8000LCZ-xxx]

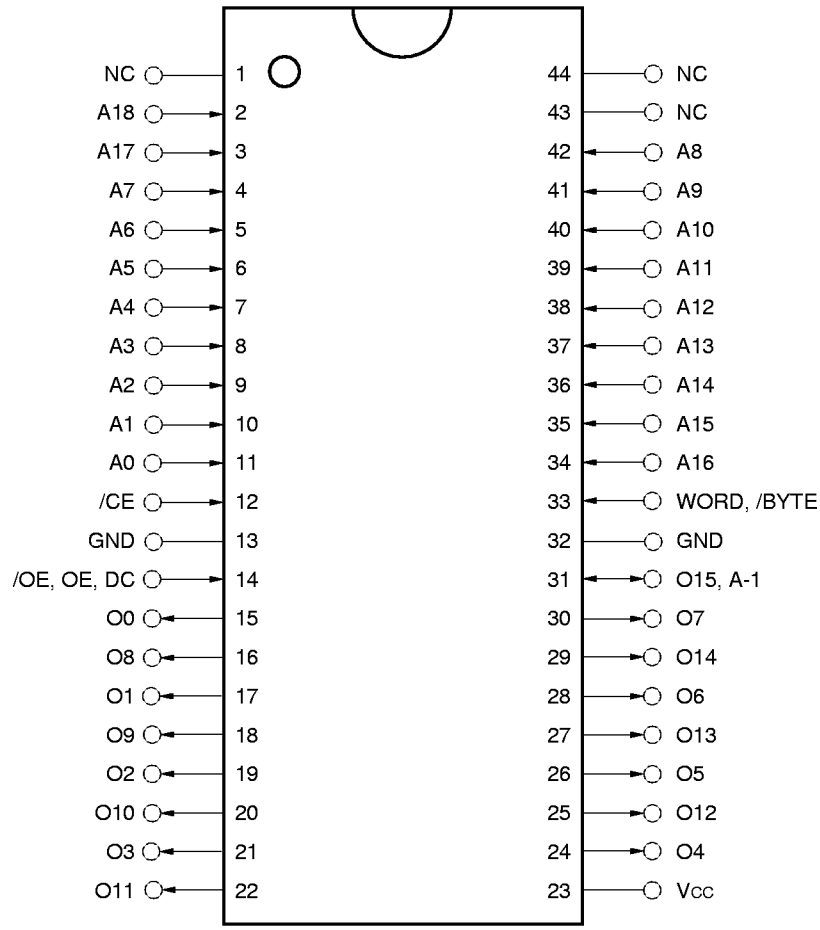


A0 - A18	: Address inputs
O0 - O7, O8 - O14	: Data Outputs
O15, A–1	: Data 15 Output (WORD mode), LSB Address input (BYTE mode)
WORD, /BYTE	: Mode select
/CE	: Chip Enable
/OE, OE	: Output Enable
Vcc	: Supply Voltage
GND	: Ground
NC Note	: No Connection
DC	: Don't Care

Note Some signals can be applied because this pin is not connected to the inside of the chip.

44-pin Plastic SOP (600 mil)

[μPD23C8000LGX-xxx]

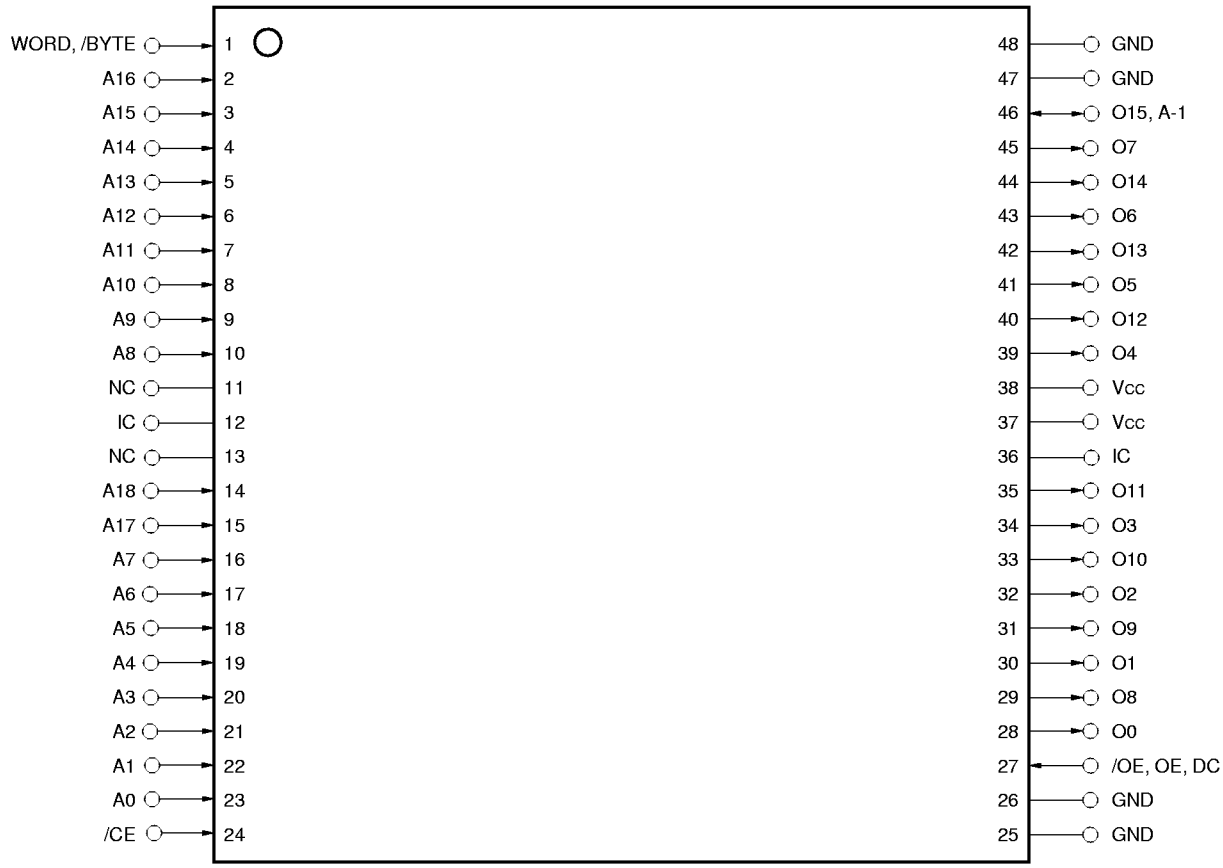


A0 - A18	: Address inputs
O0 - O7, O8 - O14	: Data Outputs
O15, A–1	: Data 15 Output (WORD mode), LSB Address input (BYTE mode)
WORD, /BYTE	: Mode select
/CE	: Chip Enable
/OE, OE	: Output Enable
Vcc	: Supply Voltage
GND	: Ground
NC Note	: No Connection
DC	: Don't Care

Note Some signals can be applied because this pin is not connected to the inside of the chip.

48-pin Plastic TSOP (I) (12 × 18 mm) (Normal Bent)

[μPD23C8000LGY-xxx-MJH]



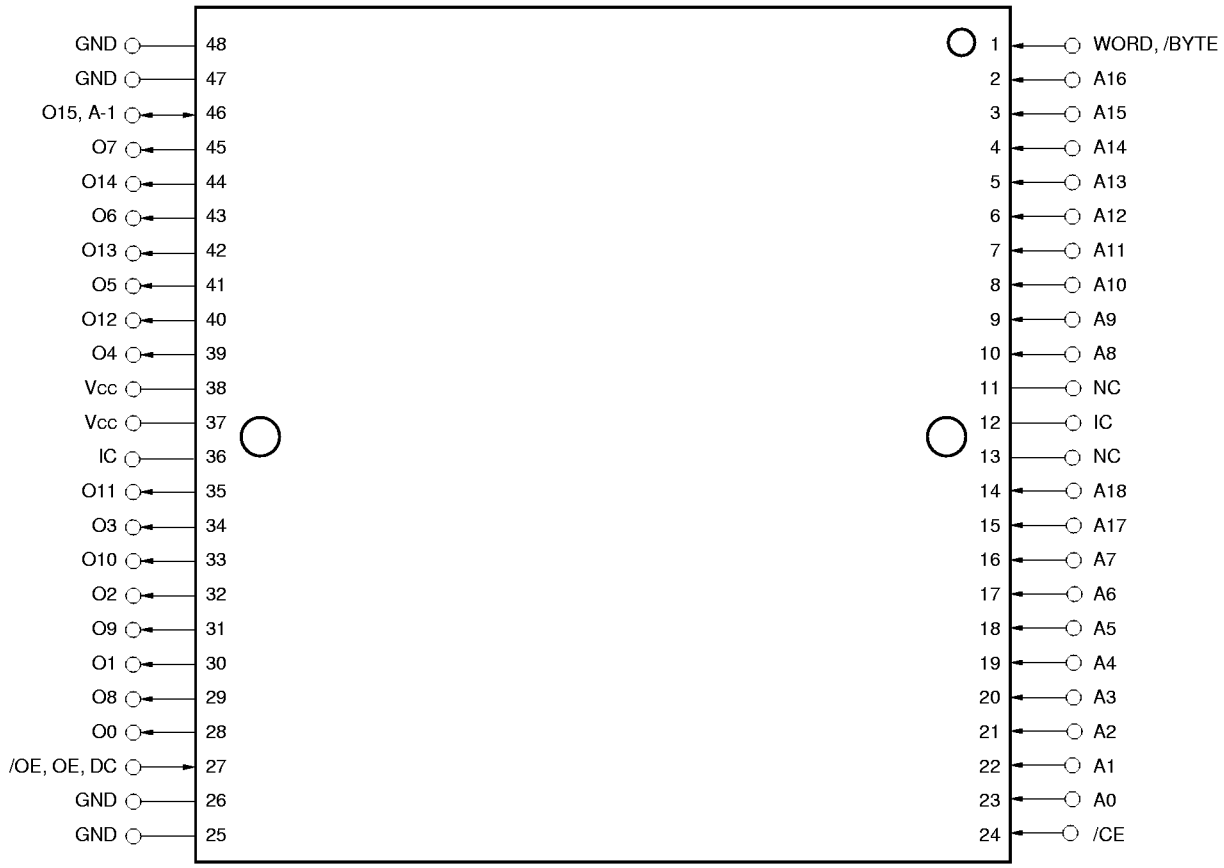
A0 - A18	: Address inputs
O0 - O7, O8 - O14	: Data Outputs
O15, A–1	: Data 15 Output (WORD mode), LSB Address input (BYTE mode)
WORD, /BYTE	: Mode select
/CE	: Chip Enable
/OE, OE	: Output Enable
Vcc	: Supply Voltage
GND	: Ground
NC Note1	: No Connection
IC Note2	: Internal Connection
DC	: Don't Care

Notes 1. Some signals can be applied because this pin is not connected to the inside of the chip.

2. Leave this pin unconnected or connect to GND.

48-pin Plastic TSOP (I) (12 × 18 mm) (Reverse Bent)

[μPD23C8000LGY-xxx-MKH]



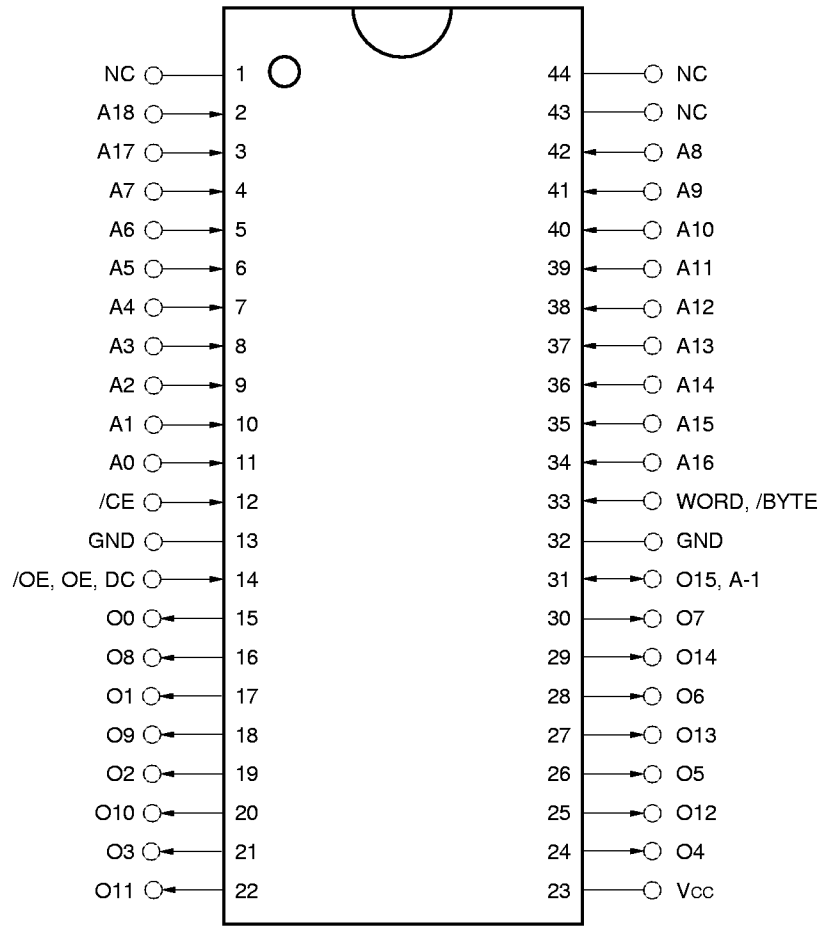
A0 - A18	: Address inputs
O0 - O7, O8 - O14	: Data Outputs
O15, A–1	: Data 15 Output (WORD mode), LSB Address input (BYTE mode)
WORD, /BYTE	: Mode select
/CE	: Chip Enable
/OE, OE	: Output Enable
Vcc	: Supply Voltage
GND	: Ground
NC Note1	: No Connection
IC Note2	: Internal Connection
DC	: Don't Care

Notes 1. Some signals can be applied because this pin is not connected to the inside of the chip.

2. Leave this pin unconnected or connect to GND.

44-pin Plastic TSOP (II) (400 mil) (Normal Bent)

[μPD23C8000LG5-xxx-7JF]



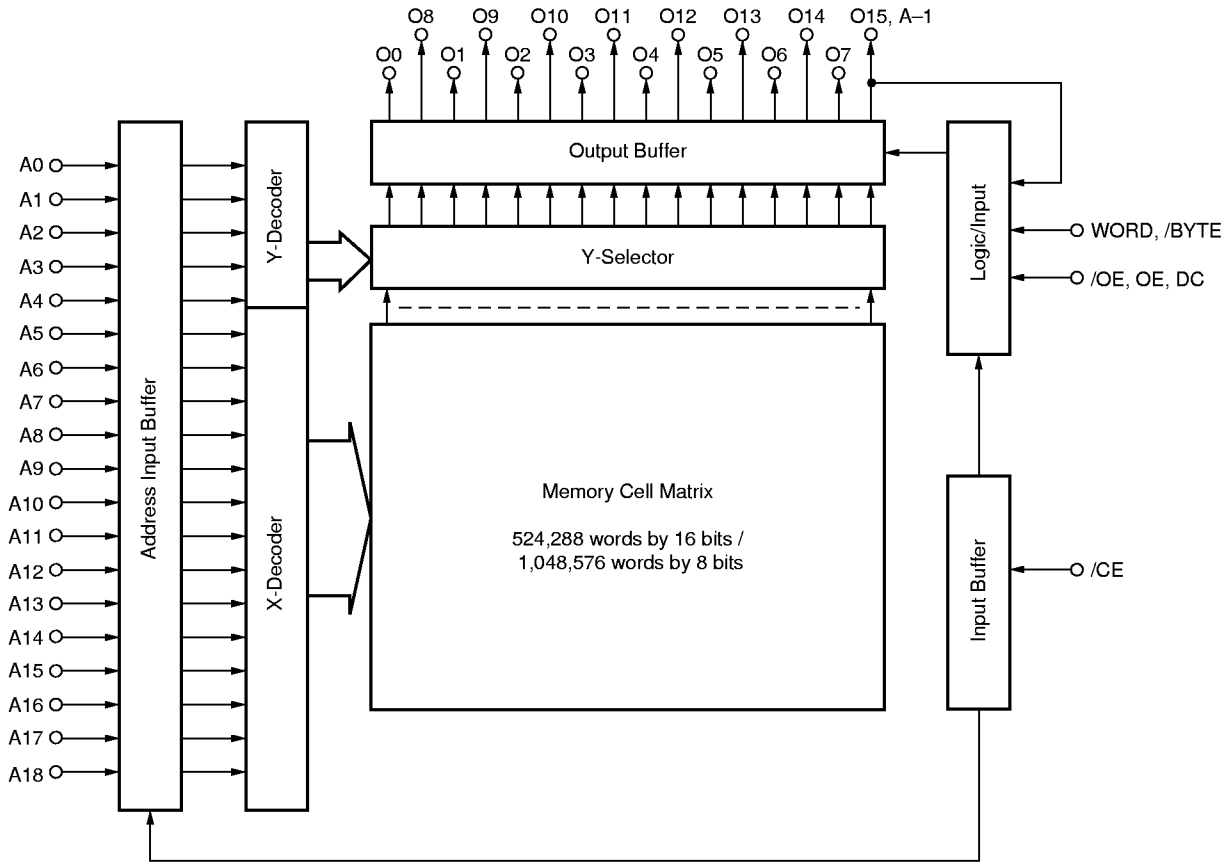
A0 - A18	: Address inputs
O0 - O7, O8 - O14	: Data Outputs
O15, A–1	: Data 15 Output (WORD mode), LSB Address input (BYTE mode)
WORD, /BYTE	: Mode select
/CE	: Chip Enable
/OE, OE	: Output Enable
Vcc	: Supply Voltage
GND	: Ground
NC Note	: No Connection
DC	: Don't Care

Note Some signals can be applied because this pin is not connected to the inside of the chip.

Input / Output Pin Functions

Pin name	Input / Output	Function
WORD, /BYTE	Input	The pin for switching WORD mode and BYTE mode. **High level** : WORD mode (512K-word by 16-bit) **Low level** : BYTE mode (1M-word by 8-bit)
A0 to A18 (Address input)	Input	Address bus. A0 to A18 are used differently in the WORD mode and the BYTE mode. **WORD mode (512K-word by 16-bit)** A0 to A18 are used as 19 bits address signals. **BYTE mode (1M-word by 8-bit)** A0 to A18 are used as the upper 19 bits of total 20 bits of address signal. (The least significant bit (A–1) is combined to O15.)
O0 to O7, O8 to O14 (Data output)	Output	Output data bus. O0 to O7, O8 to O14 are used differently in the WORD mode and the BYTE mode. **WORD mode (512K-word by 16-bit)** The lower 15 bits of 16 bits data outputs to O0 to O14. (The most significant bit (O15) combined to A–1.) **BYTE mode (1M-word by 8-bit)** 8 bits data outputs to O0 to O7 and also O8 to O14 are high impedance.
O15, A–1 (Data output 15, LSB address input)	Output, Input	O15, A–1 are used differently in the WORD mode and the BYTE mode. **WORD mode (512K-word by 16-bit)** The most significant output data bus (O15). **BYTE mode (1M-word by 8-bit)** The least significant address bus (A–1).
/CE (Chip Enable)	Input	Chip activating signal. When the OE is active, output states are following. **High level**: High impedance **Low level** : Data out
/OE, OE, DC (Output Enable, Don't Care)	Input	Output enable signal. The active level of OE is mask option. The active level of OE can be selected from high active, low active and Don't care at order.
V_{CC}	–	Supply voltage
GND	–	Ground
NC	–	Not internally connected (The signal can be connected).
IC	–	Internally connected (Leave this pin unconnected or connect to GND).

Block Diagram



Mask Option

The active levels of output enable pin (/OE, OE, DC) are mask programmable and optional, and can be selected from among "0" "1" "×" shown in the table below.

Option	/OE, OE, DC	OE active level
0	/OE	L
1	OE	H
×	DC	Don't care

Operation modes for each option are shown in the tables below.

Operation mode (Option : 0)

/CE	/OE	Mode	Output state
L	L	Active	Data out
	H		High impedance
H	H or L	Standby	High impedance

Operation mode (Option : 1)

/CE	OE	Mode	Output state
L	L	Active	High impedance
	H		Data out
H	H or L	Standby	High impedance

Operation mode (Option : ×)

/CE	DC	Mode	Output state
L	H or L	Active	Data out
H	H or L	Standby	High impedance

Remark L : Low level input
H : High level input

Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{CC}		–0.3 to +4.6	V
Input voltage	V_I		–0.3 to V_{CC} + 0.3	V
Output voltage	V_O		–0.3 to V_{CC} + 0.3	V
Operating ambient temperature	T_A		–10 to +70	°C
Storage temperature	T_{stg}		–65 to +150	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Capacitance (T_A = 25 °C)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f = 1 MHz			10	pF
Output capacitance	C_O				12	pF

DC Characteristics (T_A = –10 to +70 °C, V_{CC} = 2.7 to 3.6 V)

Parameter	Symbol	Test condition		MIN.	TYP.	MAX.	Unit
High level input voltage	V_{IH}			2.0		V_{CC} + 0.3	V
Low level input voltage	V_{IL}			–0.3		+0.5	V
High level output voltage	V_{OH}	I_{OH} = –100 μA		2.4			V
Low level output voltage	V_{OL}	I_{OL} = 2.1 mA				0.4	V
Input leakage current	I_{LI}	V_I = 0 V to V_{CC}		–10		+10	μA
Output leakage current	I_{LO}	V_O = 0 V to V_{CC}, Chip deselected		–10		+10	μA
Power supply current	I_{CC1}	/CE = V_{IL} (Active mode),	V_{CC} = 3.0 V ± 0.3 V			30	mA
		I_O = 0 mA	V_{CC} = 3.3 V ± 0.3 V			35	
Standby current	I_{CC3}	/CE = V_{CC} – 0.2 V (Standby mode)				30	μA

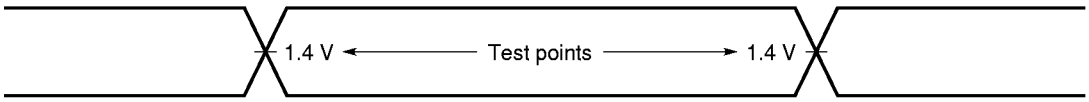
AC Characteristics (T_A = –10 to +70 °C, V_{CC} = 2.7 to 3.6 V)

Parameter	Symbol	Test condition	V_{CC} = 3.0 V ± 0.3 V			V_{CC} = 3.3 V ± 0.3 V			Unit
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Address access time	t_{ACC}				140			120	ns
Chip enable access time	t_{CE}				140			120	ns
Output enable access time	t_{OE}				50			40	ns
Output hold time	t_{OH}		0			0			ns
Output disable time	t_{DF}		0		30	0		25	ns
WORD, /BYTE access time	t_{WB}				140			120	ns

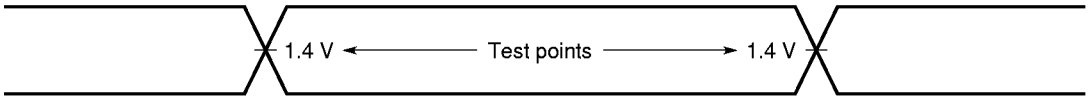
Remark t_{DF} is the time from inactivation of /CE or /OE, OE to high-impedance state output.

AC Test Conditions

Input Waveform (Rise / Fall Time ≤ 5 ns)



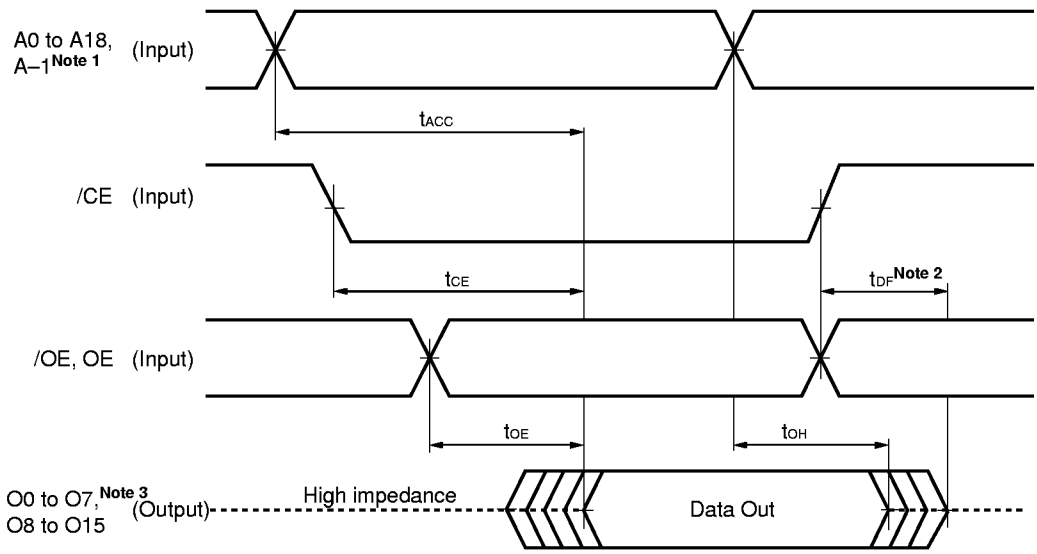
Output Waveform



Output Load

1 TTL + 100 pF

Read Cycle Timing Chart

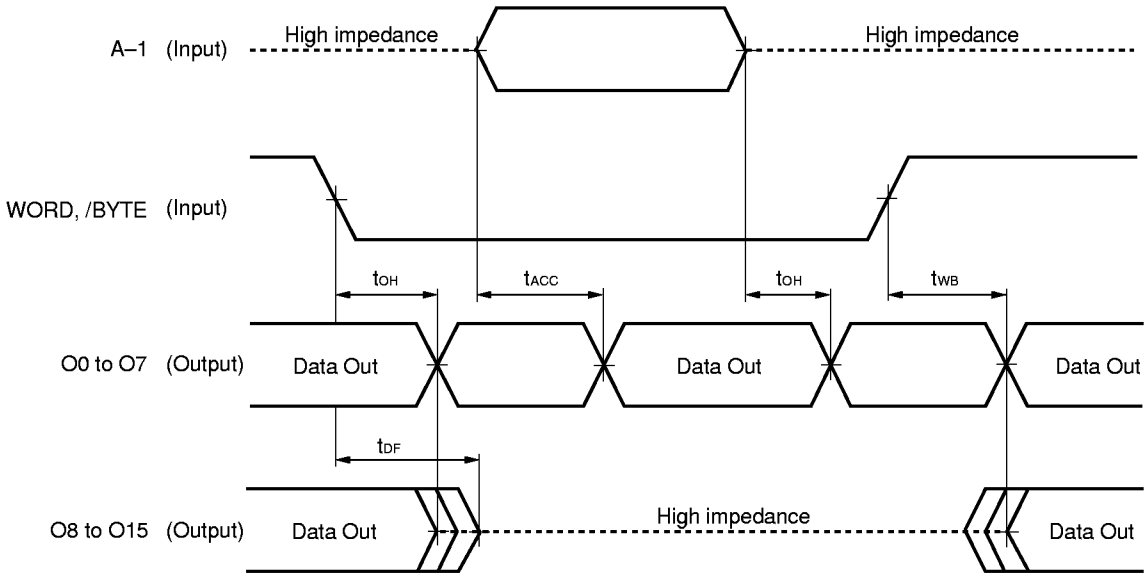


Notes 1. During WORD mode, A–1 is O15.

2. t_{DF} is specified when one of /CE, /OE, OE is inactivated.

3. During BYTE mode, O8 to O14 are high impedance and O15 is A–1.

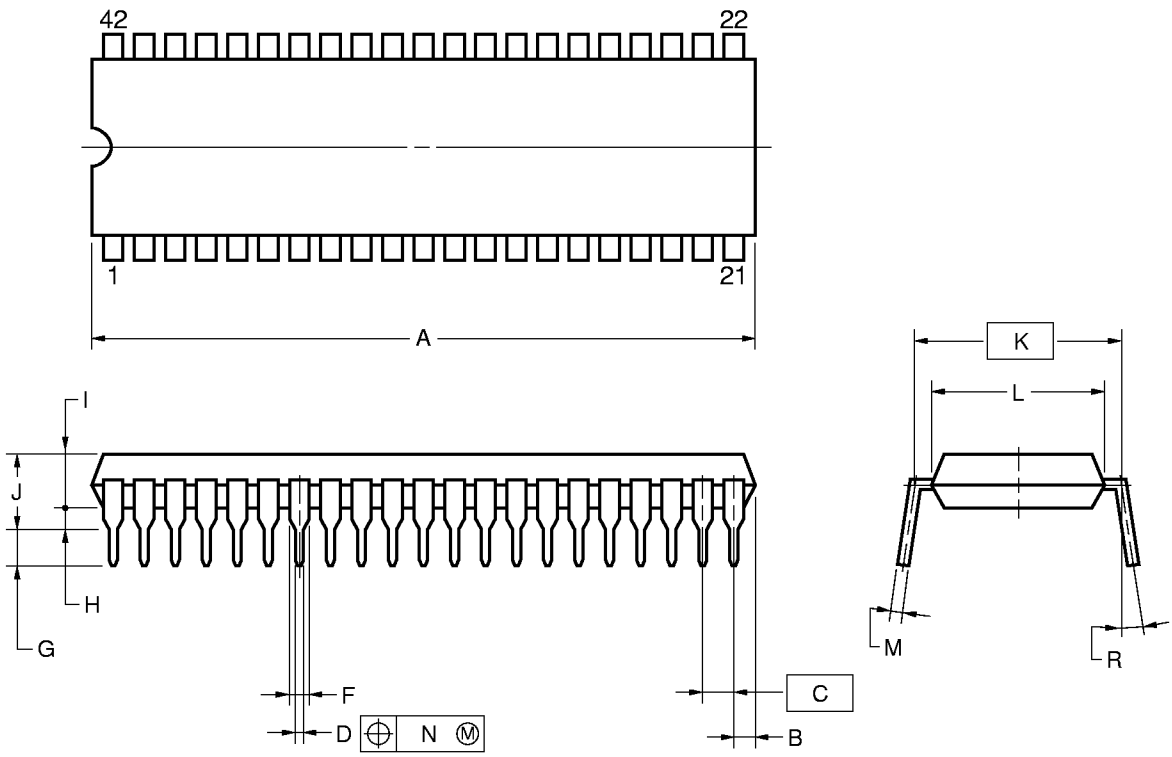
WORD, /BYTE Switch Timing Chart



Remark /OE, OE and /CE : Active.

Package Drawings

42PIN PLASTIC DIP (600 mil)



NOTES

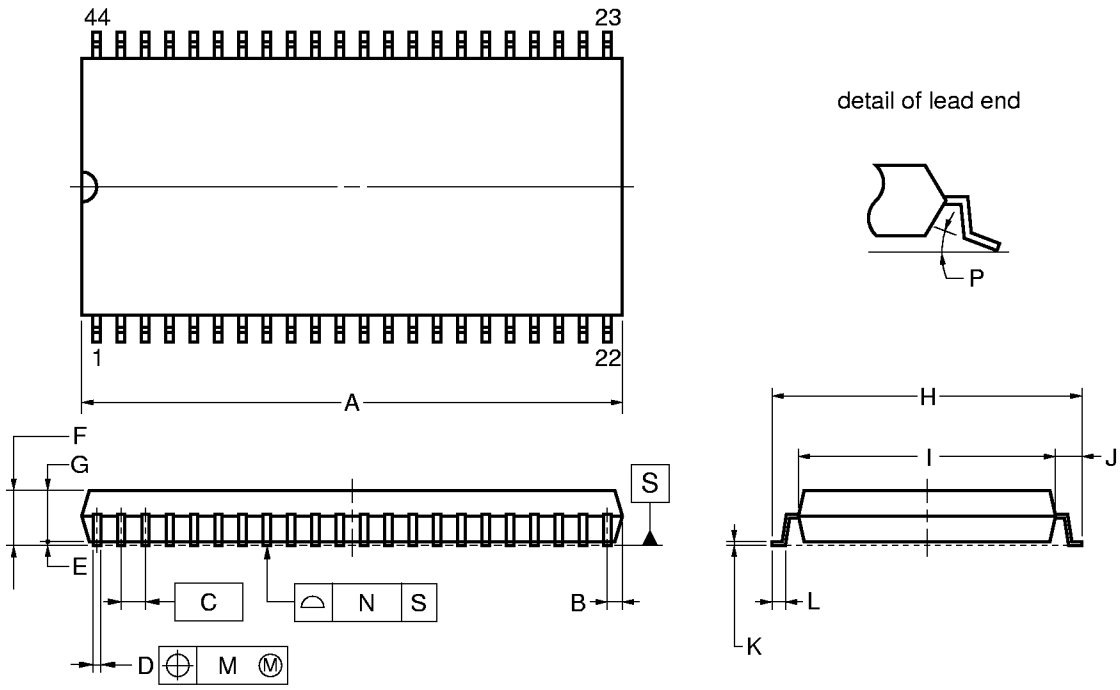
1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	55.88 MAX.	2.200 MAX.
B	2.54 MAX.	0.100 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	0.50 ± 0.10	$0.020^{+0.004}_{-0.005}$
F	1.2 MIN.	0.047 MIN.
G	3.6 ± 0.3	0.142 ± 0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.72 MAX.	0.226 MAX.
K	15.24 (T.P.)	0.600 (T.P.)
L	13.2	0.520
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.25	0.01
R	0~15°	0~15°

P42C-100-600A,B-1

44 PIN PLASTIC SOP (600 mil)



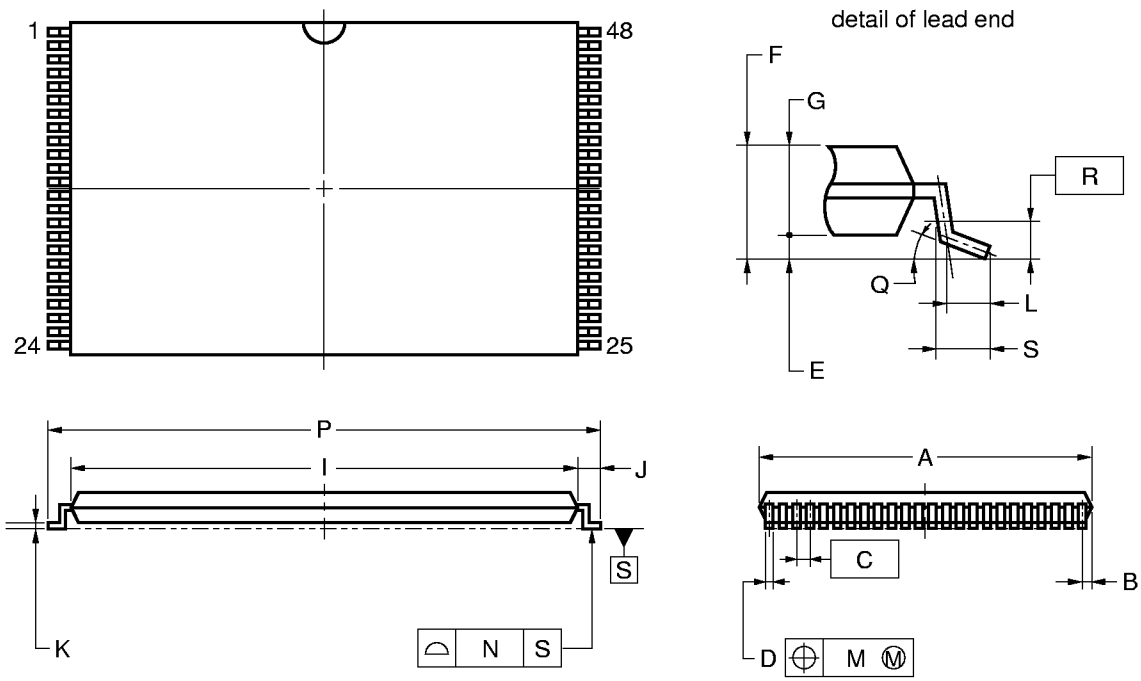
NOTE

1. Controlling dimension —— millimeter.
2. Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	$27.83^{+0.4}_{-0.05}$	$1.096^{+0.016}_{-0.003}$
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.42^{+0.08}_{-0.07}$	$0.017^{+0.003}_{-0.004}$
E	0.15±0.1	0.006±0.004
F	3.0 MAX.	0.119 MAX.
G	2.7±0.05	$0.106^{+0.003}_{-0.002}$
H	16.04±0.3	$0.631^{+0.013}_{-0.012}$
I	13.24±0.1	$0.521^{+0.005}_{-0.004}$
J	1.4±0.2	0.055±0.008
K	$0.22^{+0.08}_{-0.07}$	$0.009^{+0.003}_{-0.004}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	0.12	0.005
N	0.10	0.004
P	$3°^{+7°}_{-3°}$	$3°^{+7°}_{-3°}$

P44GX-50-600A-3

48 PIN PLASTIC TSOP (I) (12×18)



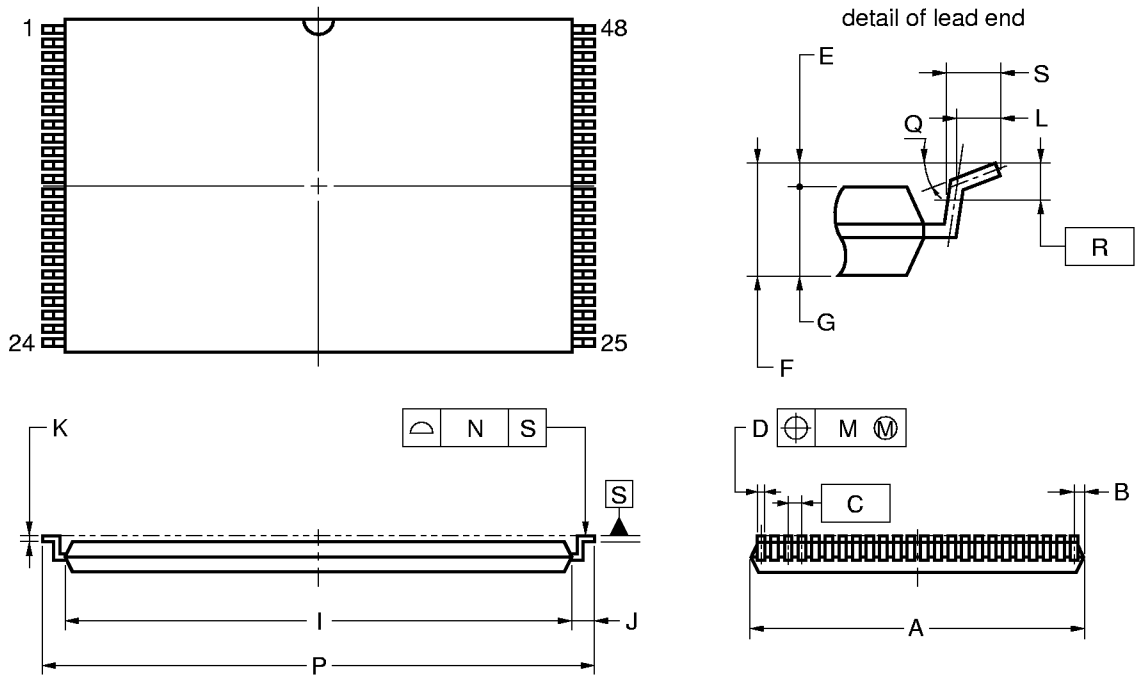
NOTES

1. Controlling dimension — Millimeter.
2. Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.
3. "A" excludes mold flash. (Includes mold flash : 12.4 mm MAX. <0.489 inch MAX.>)

ITEM	MILLIMETERS	INCHES
A	12.0±0.1	$0.472^{+0.005}_{-0.004}$
B	0.45 MAX.	0.018 MAX.
C	0.5 (T.P.)	0.020 (T.P.)
D	0.22±0.05	$0.009^{+0.002}_{-0.003}$
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	1.0±0.05	$0.039^{+0.003}_{-0.002}$
I	16.4±0.1	$0.646^{+0.004}_{-0.005}$
J	0.8±0.2	$0.031^{+0.009}_{-0.008}$
K	0.145±0.05	$0.006^{+0.002}_{-0.003}$
L	0.5	0.020
M	0.10	0.004
N	0.10	0.004
P	18.0±0.2	$0.709^{+0.008}_{-0.009}$
Q	$3°^{+5°}_{-3°}$	$3°^{+5°}_{-3°}$
R	0.25	0.010
S	0.60±0.15	$0.024^{+0.006}_{-0.007}$

S48GY-50-MJH1

48 PIN PLASTIC TSOP (I) (12×18)



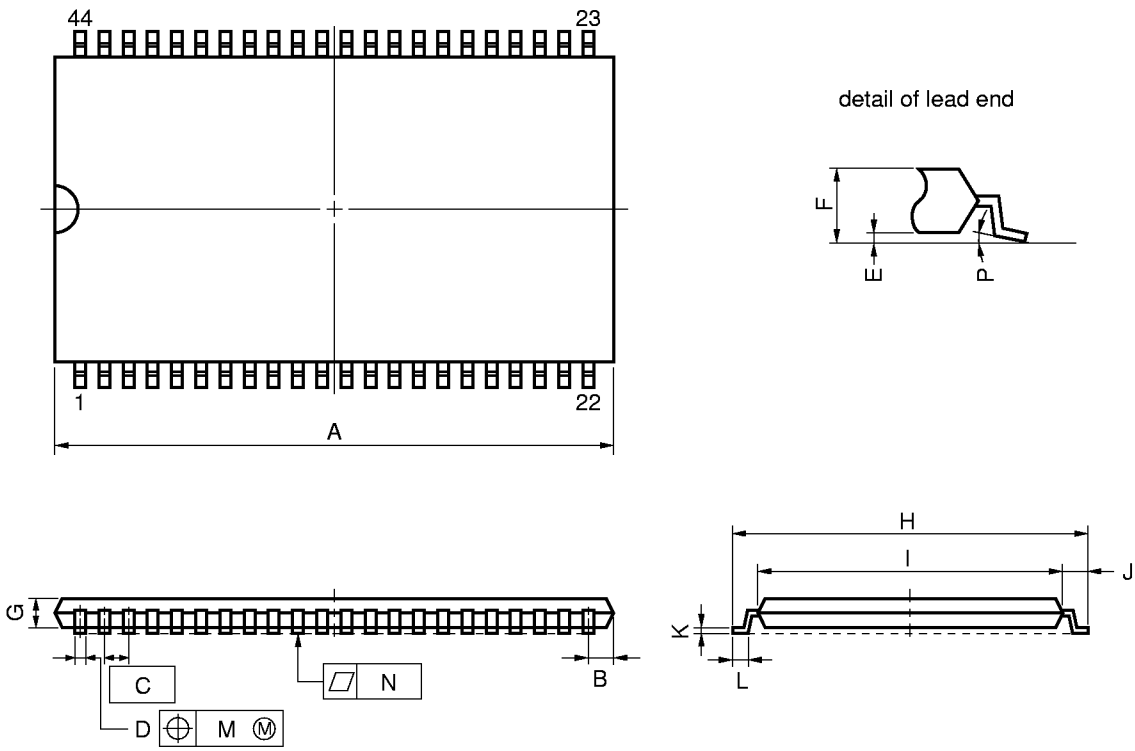
NOTES

1. Controlling dimension —— Millimeter.
2. Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.
3. "A" excludes mold flash. (Includes mold flash : 12.4 mm MAX. <0.489 inch MAX.>)

ITEM	MILLIMETERS	INCHES
A	12.0±0.1	$0.472^{+0.005}_{-0.004}$
B	0.45 MAX.	0.018 MAX.
C	0.5 (T.P.)	0.020 (T.P.)
D	0.22±0.05	$0.009^{+0.002}_{-0.003}$
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	1.0±0.05	$0.039^{+0.003}_{-0.002}$
I	16.4±0.1	$0.646^{+0.004}_{-0.005}$
J	0.8±0.2	$0.031^{+0.009}_{-0.008}$
K	0.145±0.05	$0.006^{+0.002}_{-0.003}$
L	0.5	0.020
M	0.10	0.004
N	0.10	0.004
P	18.0±0.2	$0.709^{+0.008}_{-0.009}$
Q	$3°^{+5°}_{-3°}$	$3°^{+5°}_{-3°}$
R	0.25	0.010
S	0.60±0.15	$0.024^{+0.006}_{-0.007}$

S48GY-50-MKH1

44 PIN PLASTIC TSOP(II) (400 mil)



NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	18.63 MAX.	0.734 MAX.
B	0.93 MAX.	0.037 MAX.
C	0.8 (T.P.)	0.031 (T.P.)
D	$0.32^{+0.08}_{-0.07}$	0.013±0.003
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	$0.031^{+0.009}_{-0.008}$
K	$0.145^{+0.025}_{-0.015}$	0.006±0.001
L	0.5±0.1	$0.020^{+0.004}_{-0.005}$
M	0.13	0.005
N	0.10	0.004
P	$3°^{+7°}_{-3°}$	$3°^{+7°}_{-3°}$

S44G5-80-7JF5

★ Recommended Soldering Conditions

The following conditions (see table below) must be met when soldering the μPD23C8000L.

For more details, refer to our document **"SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (C10535E)**.

Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

Types of Surface Mount Device

μPD23C8000LGX : 44-pin plastic SOP (600 mil)

μPD23C8000LGY-MJH : 48-pin plastic TSOP (I) (12 × 18 mm) (Normal Bent)

μPD23C8000LGY-MKH : 48-pin plastic TSOP (I) (12 × 18 mm) (Reverse Bent)

μPD23C8000LG5-7JF : 44-pin plastic TSOP (II) (400 mil) (Normal Bent)

Please consult with our sales offices.

Type of Through Hole Mount Device

μPD23C8000LCZ : 42-pin plastic DIP (600 mil)

Soldering process	Soldering conditions
Wave soldering (Only to leads)	Solder temperature : 260 °C or below, Flow time : 10 seconds or below
Partial heating method	Terminal temperature : 300 °C or below, Time : 3 seconds or below (per one lead)

Caution Do not jet molten solder on the surface of package.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.