Features

- Meets jitter requirements of Telcordia GR-253-CORE for OC-12, OC-3, and OC-1 rates
- Meets jitter requirements of ITU-T G.813 for STM-4, and STM-1 rates
- Provides one differential LVPECL output clock selectable to 19.44 MHz, 38.88 MHz, 77.76 MHz, 155.52 MHz, or 622.08 MHz
- Provides a single-ended CMOS output clock at 19.44 MHz
- Accepts a single-ended CMOS reference at 19.44 MHz or a differential LVDS, LVPECL, or CML reference at 19.44 MHz or 77.76 MHz
- Provides a LOCK indication
- 3.3 V supply

Applications

- SONET/SDH line cards

September 2006

Ordering Information

ZL30415GGC	64 Ball CABGA	Trays
ZL30415GGF	64 Ball CABGA	Tape & Reel, Bake & Drypack
ZL30415GGG2	64 Ball CABGA**	Trays, Bake & Drypack
ZL30415GGF2	64 Ball CABGA**	Tape & Reel, Bake & Drypack

**Pb Free Tin/Silver/Copper

-40°C to +85°C

Description

The ZL30415 is an analog phase-locked loop (APLL) designed to provide jitter attenuation and rate conversion for SDH (Synchronous Digital Hierarchy) and SONET (Synchronous Optical Network) networking equipment. The ZL30415 generates low jitter output clocks that meet the jitter requirements of Telcordia GR-253-CORE OC-12, OC-3, OC-1 rates and ITU-T G.813 STM-4 and STM-1 rates.

The ZL30415 accepts a CMOS compatible reference at 19.44 MHz or a differential LVDS, LVPECL, or CML reference at 19.44 MHz or 77.76 MHz and generates a differential LVPECL output clock selectable to 19.44 MHz, 38.88 MHz, 77.76 MHz, 155.52 MHz, or 622.08 MHz, and a single-ended CMOS clock at 19.44 MHz. The ZL30415 provides a lock indication.

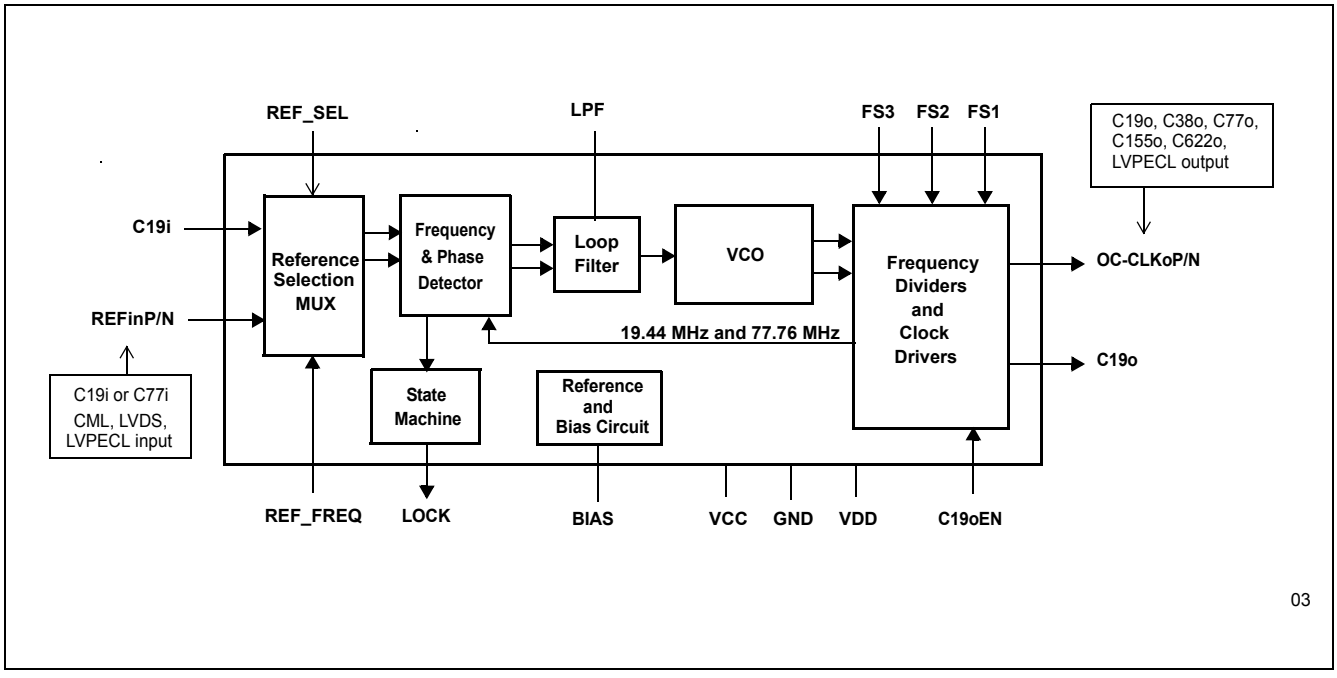


Figure 1 - Functional Block Diagram

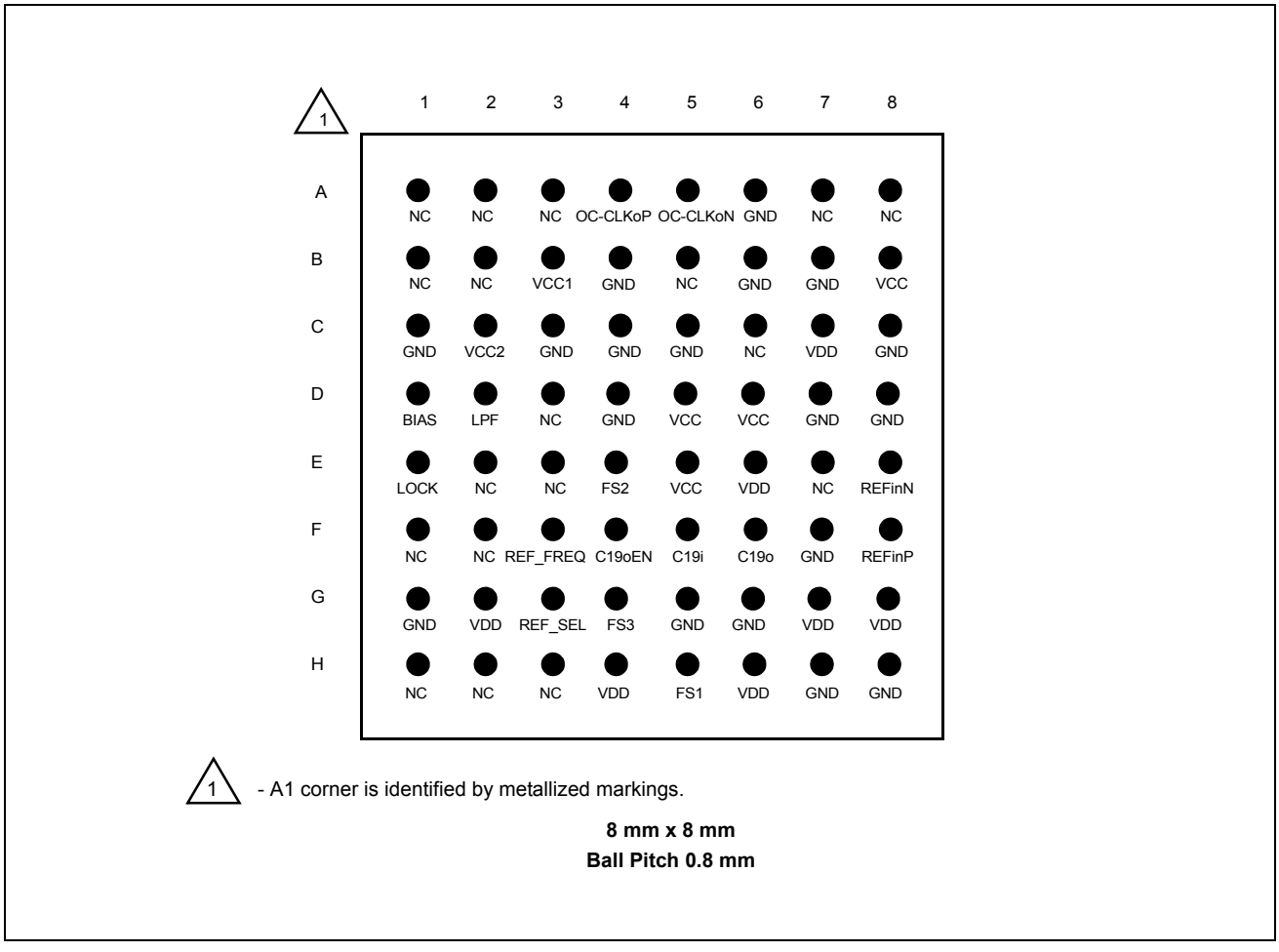


Figure 2 - BGA 64 Ball Package (Top View)

1.0 Ball Description

Ball Description Table

Ball #	Name	Description
A1, A2 A3	NC	**No internal bonding Connection.** Leave unconnected.
A4 A5	OC-CLKoP OC-CLKoN	**SONET/SDH Clock (LVPECL Output)**. These outputs provide a selectable differential LVPECL clock at 19.44 Hz, 38.88 MHz, 77.76 MHz, 155.52 MHz, and 622.08 MHz. The output frequency is selected with FS3, FS2 and FS1 inputs.
A6	GND	**Ground.** 0 volt
A7, A8 B1, B2	NC	**No internal bonding Connection.** Leave unconnected.
B3	VCC1	**Positive Analog Power Supply.** +3.3 V +/-10%
B4	GND	**Ground.** 0 volt
B5	NC	**No internal bonding Connection.** Leave unconnected.

Ball Description Table (continued)

Ball #	Name	Description
B6, B7	GND	**Ground.** 0 volt
B8	VCC	**Positive Analog Power Supply.** +3.3 V ±10%
C1	GND	**Ground.** 0 volt
C2	VCC2	**Positive Analog Power Supply.** +3.3 V ±10%
C3, C4 C5	GND	**Ground.** 0 volt
C6	NC	**No internal bonding Connection.** Leave unconnected.
C7	VDD	**Positive Digital Power Supply.** +3.3 V ±10%
C8	GND	**Ground.** 0 volt
D1	BIAS	**Bias Circuit.**
D2	LPF	**External Low-Pass Filter** (Analog). Connect external RC network for the low-pass filter.
D3	NC	**No internal bonding Connection.** Leave unconnected.
D4	GND	**Ground.** 0 volt
D5, D6	VCC	**Positive Analog Power Supply.** +3.3 V ±10%
D7, D8	GND	**Ground.** 0 volt
E1	LOCK	**Lock Indicator (CMOS Output).** This output goes high when the PLL is frequency locked to the selected input reference.
E2, E3	NC	**No internal bonding Connection.** Leave unconnected.
E4 G4 H5	FS2 FS3 FS1	**Frequency Select 3-1 (CMOS Input)**. These inputs select the clock frequency on the OC-CLKo output. The possible output frequencies are: 19.44 MHz (000), 38.88 MHz (001), 77.76 MHz (010), 155.52 MHz (011), 622.08 (100)
E5	VCC	**Positive Analog Power Supply.** +3.3 V ±10%
E6	VDD	**Positive Digital Power Supply.** +3.3 V ±10%
E7	NC	**No internal bonding Connection.** Leave unconnected.
E8 F8	REFinN REFinP	**Differential Reference Clock Input (CML/LVDS/LVPECL Compatible Input)**. These inputs accept a differential clock at 77.76 MHz or 19.44 MHz as the reference for synchronization. These inputs do not have on-chip AC coupling capacitors.
F1, F2	NC	**No internal bonding Connection.** Leave unconnected.
F3	REF_FREQ	**Reference Frequency (CMOS Input)**. This input selects the rate of the differential input clock (REFinP/N) to be either 77.76 MHz or 19.44 MHz.
F4	C19oEN	**C19o Output Enable (CMOS Input).** If tied high this control input enables the C19o output clock. Pulling this pin low forces the output driver into a high impedance state.

Ball Description Table (continued)

Ball #	Name	Description
F5	C19i	**C19 Reference Input (CMOS Input).** This is a single-ended input reference source used for synchronization. This input accepts 19.44 MHz.
F6	C19o	**Clock 19.44 MHz (CMOS Output)**. This output provides a single-ended CMOS clock at 19.44 MHz.
F7, G1	GND	**Ground.** 0 volt
G2	VDD	**Positive Digital Power Supply.** +3.3 V ±10%
G3	REF_SEL	**Reference Select (CMOS Input).** If tied low then the C19i single-ended reference is used as the input reference source. If tied high then the REFinP/N differential pair is used as the input reference source.
G4	FS3	See E4 ball description.
G5, G6	GND	**Ground.** 0 volt
G7, G8	VDD	**Positive Digital Power Supply.** +3.3 V ±10%
H1, H2 H3	NC	**No internal bonding Connection.** Leave unconnected.
H4	VDD	**Positive Digital Power Supply.** +3.3 V ±10%
H5	FS1	See E4 ball description.
H6	VDD	**Positive Digital Power Supply.** +3.3 V ±10%
H7, H8	GND	**Ground.** 0 volt.

2.0 Functional Description

The ZL30415 is an analog phased-locked loop which provides rate conversion and jitter attenuation for SONET/SDH OC-12/STM-4 and OC-3/STM-1 applications. A functional block diagram of the ZL30415 is shown in Figure 1 and a brief description is presented in the following sections.

2.1 Reference Selection Multiplexer

The ZL30415 accepts two types of input reference clocks:

- differential: operating at 19.44 MHz or 77.76 MHz, compatible with LVDS/LVPECL/CML threshold levels
- single-ended: operating at 19.44 MHz, compatible with CMOS switching levels.

The REF_SEL input determines whether the single-ended CMOS reference input (REFin) or the differential reference inputs (REFinP/N) are used as input reference clocks. The REF_FREQ input selects the rate of the differential input clock to be either 19.44 MHz, or 77.76 MHz. See Table 1 for details.

REF_SEL	REF_FREQ	Selected Input Reference	Reference Frequency
0	x	C19i	19.44 MHz (CMOS)
1	0	REFin	77.76 MHz (Differential)
1	1	REFin	19.44 MHz (Differential)

Table 1 - Input Reference Selection

2.2 Frequency/Phase Detector

The Frequency/Phase Detector compares the frequency/phase of the input reference signal with the feedback signal from the Frequency Divider circuit and provides an error signal equal to the frequency/phase difference between the two. This error signal is passed to the Loop Filter circuit.

2.3 Lock Indicator

The ZL30415 has a built-in LOCK detector that measures frequency difference between input reference clock C19i and the VCO frequency. When the VCO frequency is less than ±300 ppm apart from the input reference frequency then the LOCK output is set high. The LOCK output is pulled low if the frequency difference exceeds ±1000 ppm.

2.4 Loop Filter

The Loop Filter is a low-pass filter. This low-pass filter eliminates high frequency spectral components from a phase error signal produced by the Phase Detector. This ensures low output jitter that meets network jitter requirements. The corner frequency of the Loop Filter is configurable with an external capacitor and resistor connected to the LPF ball and ground as shown in Figure 3.

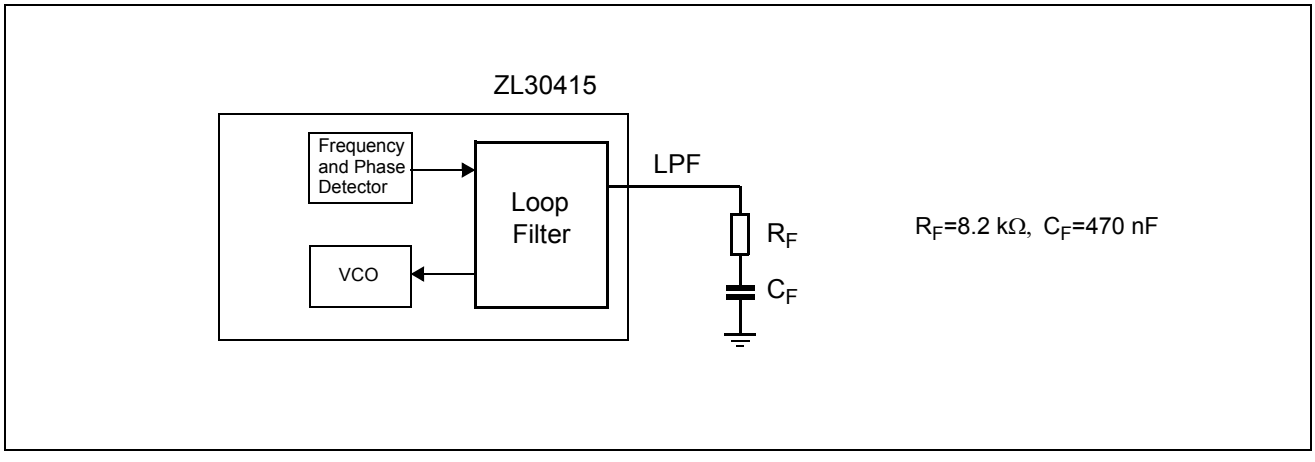


Figure 3 - Loop Filter Elements

2.5 VCO

The voltage-controlled oscillator (VCO) receives the filtered error signal from the Loop Filter, and based on the voltage of the error signal generates a primary frequency. The VCO output is connected to the "Frequency Dividers and Clock Drivers" block that divides VCO frequency and buffer generated clocks.

2.6 Frequency Dividers and Clock Drivers

The output of the VCO feeds the high frequency clock to the "Frequency Dividers and Clock Drivers" circuit to provide one differential LVPECL compatible clock with selectable frequency and one single-ended 19.44 MHz C19o output clock. The C19o clock can be enabled or disabled with the associated C19oEN Output Enable ball. Internally, this block provides a feedback clock that closes the PLL loop.

The frequency of the OC-CLKo differential output clock is selected with FS3, FS2 and FS1 inputs as is shown in the following table.

FS3	FS2	FS1	OC-CLKo Frequency
0	0	0	19.44 MHz
0	0	1	38.88 MHz
0	1	0	77.76 MHz
0	1	1	155.52 MHz
1	0	0	622.08 MHz
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Table 2 - OC-CLKo Clock Frequency Selection

3.0 ZL30415 Performance

The following are some of the ZL30415 performance indicators that complement results listed in the Characteristics section of this data sheet.

3.1 Input Jitter Tolerance

Jitter tolerance is a measure of the PLL's ability to operate properly (i.e., remain in lock and/or regain lock in the presence of large jitter magnitudes at various jitter frequencies) in the presence of jitter applied to its input reference. The input jitter tolerance of the ZL30415 is shown in Figure 4. On this graph, the single line at the top represents the input jitter tolerance and the three overlapping lines below represent the specification for minimum input jitter tolerance for OC-192, OC-48 and OC-12 network interfaces. The jitter tolerance is expressed in picoseconds (pk-pk) to accommodate requirements for interfaces operating at different rates.

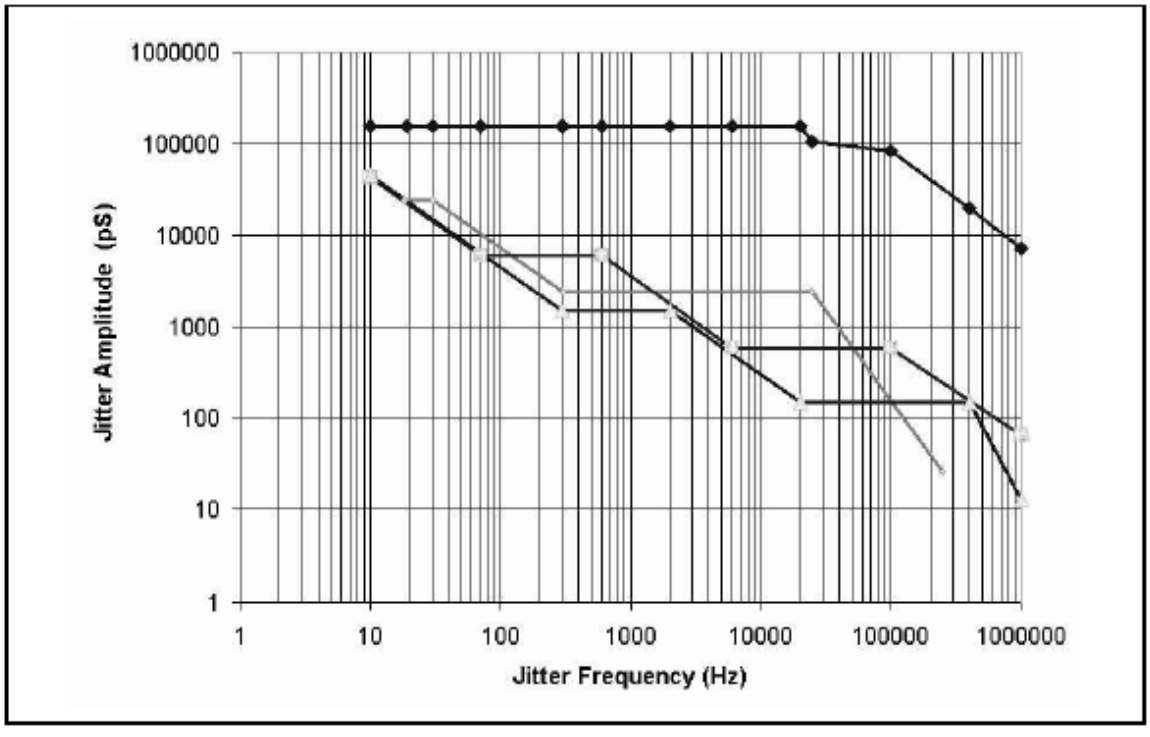


Figure 4 - Input Jitter Tolerance

3.2 Jitter Transfer Characteristic

Jitter Transfer Characteristic represents a ratio of the jitter at the output of a PLL to the jitter applied to the input of a PLL. This ratio is expressed in dB and it characterizes the PLL's ability to attenuate (filter) jitter. The ZL30415 jitter transfer characteristic complies with the maximum 0.1 dB jitter gain specified in Telcordia's GR-253-CORE.

4.0 Applications

4.1 Generation of Low Jitter SONET/SDH Equipment Clocks

The functionality and performance of the ZL30415 complements the entire family of the Zarlink's advanced network synchronization PLL's. Its jitter filtering characteristics exceed requirements of SONET/SDH optical interfaces operating up to OC-12/STM-4 rates (622 Mbit/s). The ZL30415 in combination with the MT90401 or the ZL30407 (SONET/SDH Network Element PLL's) provides the core building blocks for high quality equipment clocks suitable for network synchronization (see Figure 5).

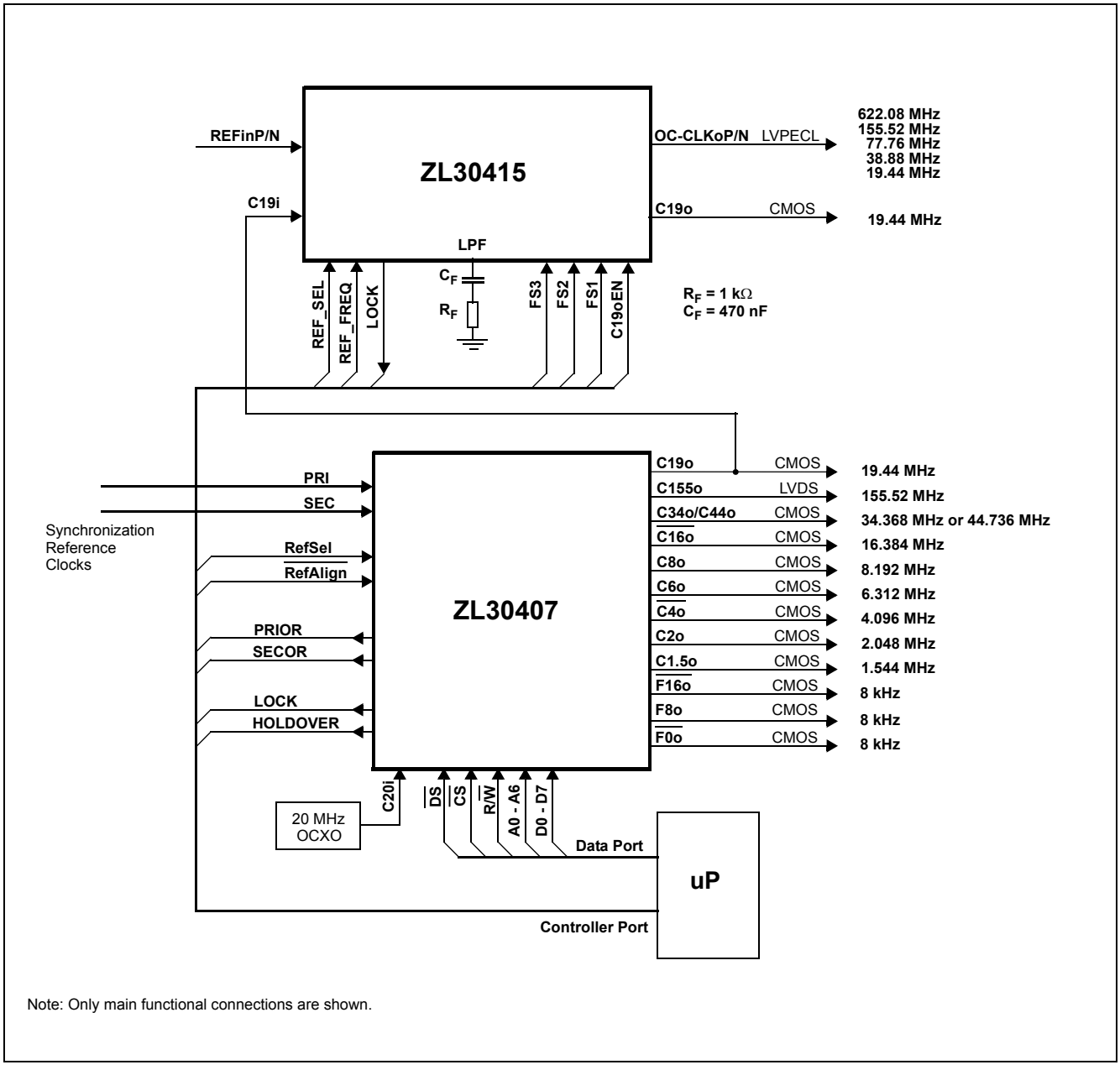


Figure 5 - SONET/SDH Equipment Clock

The ZL30415 in combination with the MT9046 provides an optimum solution for SONET/SDH line cards (see Figure 6).

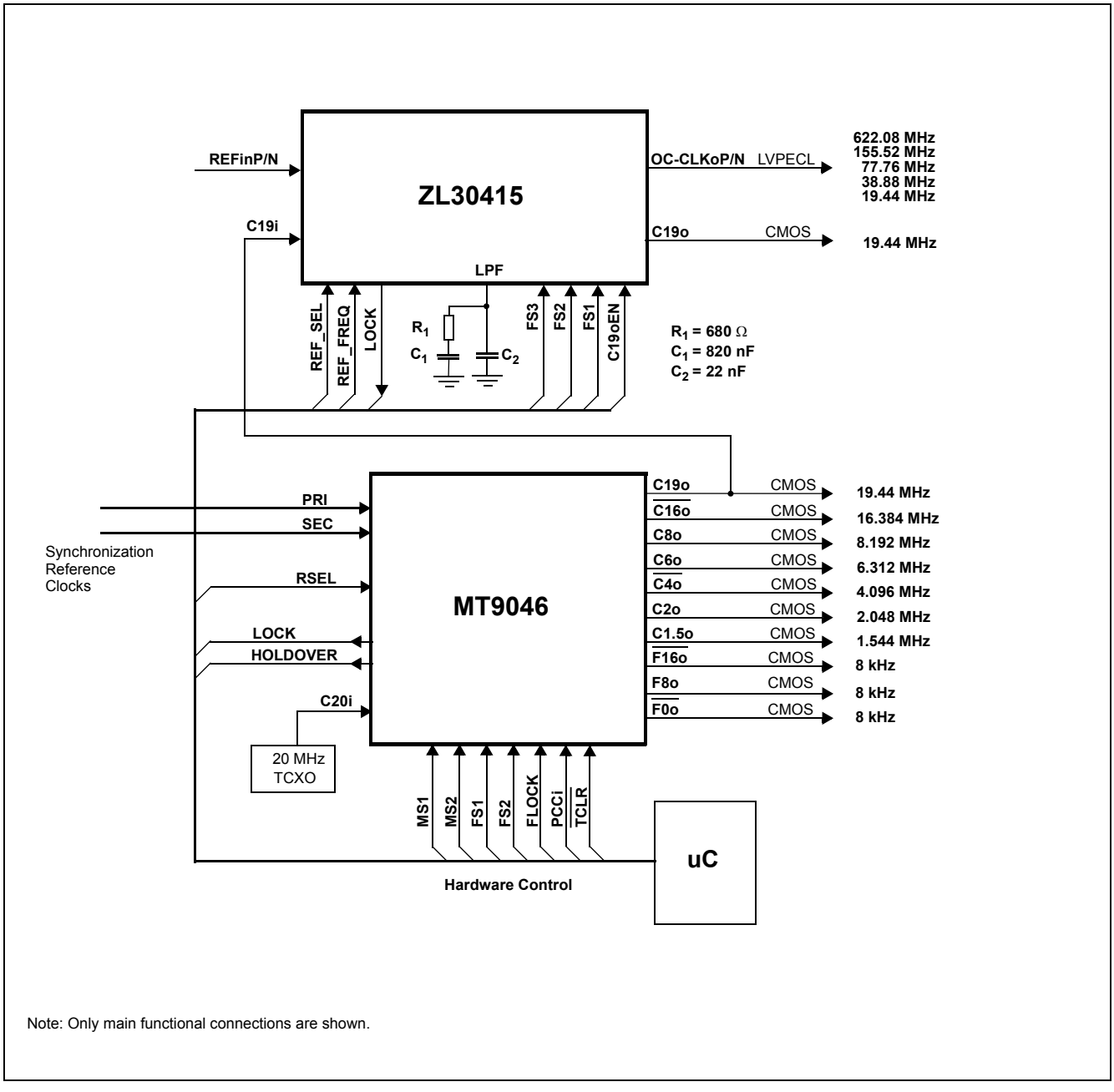


Figure 6 - SONET/SDH Line Card

4.2 Recommended Interface circuit

4.2.1 Interfacing to REFin Receiver

4.2.1.1 Interfacing REFin Receiver to LVPECL Driver

The ZL30415 REFin differential receiver can be connected to LVPECL compatible driver with an interface circuit, as shown in Figure 8. The R1s and R2s terminating resistors should be placed close to the REFin input balls.

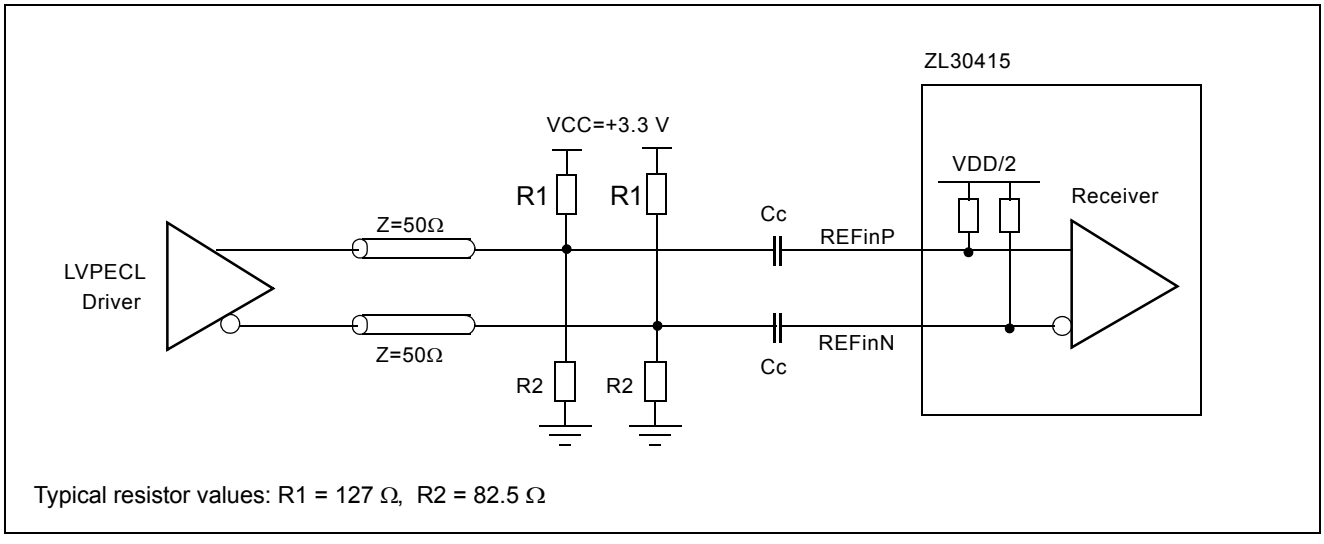


Figure 7 - Interfacing to LVPECL Driver

4.2.1.2 Interfacing REFin Receiver to LVDS or CML Drivers

The ZL30415 REFin differential receiver can be connected to LVDS or CML driver with an interface circuit, as shown in Figure 8. The 100 Ω terminating resistors should be placed close to the REFin input balls.

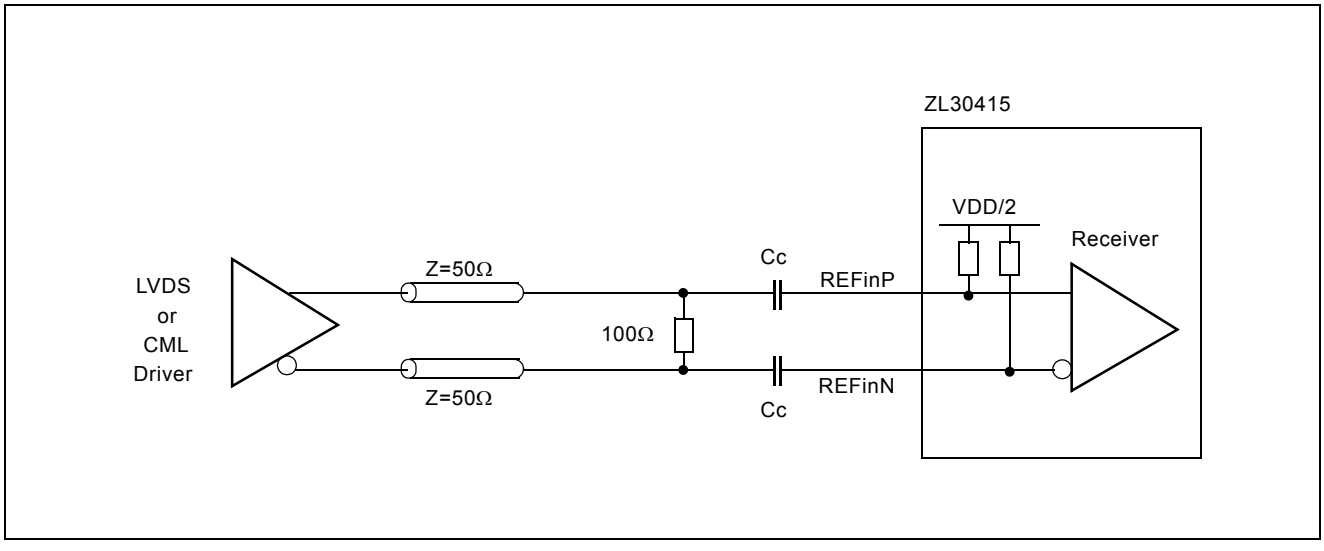


Figure 8 - Interfacing to LVDS or CML Driver

4.2.2 Interfacing to OC-CLKo Output

4.2.2.1 LVPECL to LVPECL Interface

The OC-CLKo outputs provide differential LVPECL clocks at 622.08 MHz, 155.52 MHz, 77.76 MHz, 38.88 MHz and 19.44 MHz selectable with FS3, FS2 and FS1 frequency select inputs. The LVPECL output drivers require a 50 Ω termination connected to the Vcc-2V source for each output terminal at the terminating end as shown below. The terminating resistors should be placed close to the LVPECL receiver.

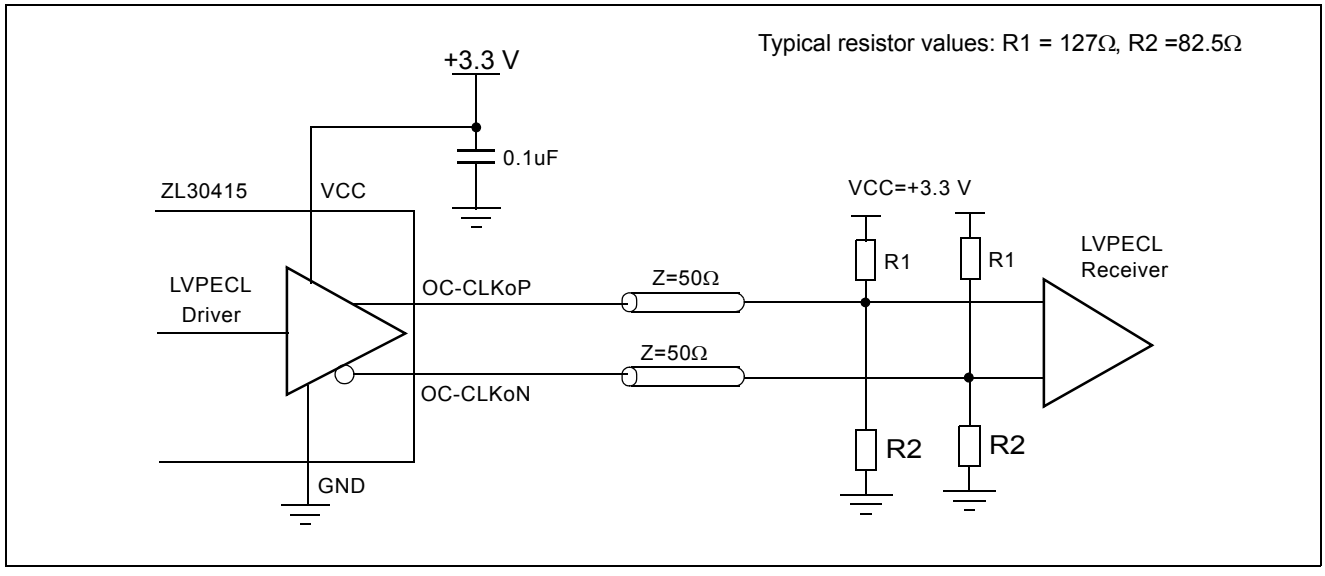
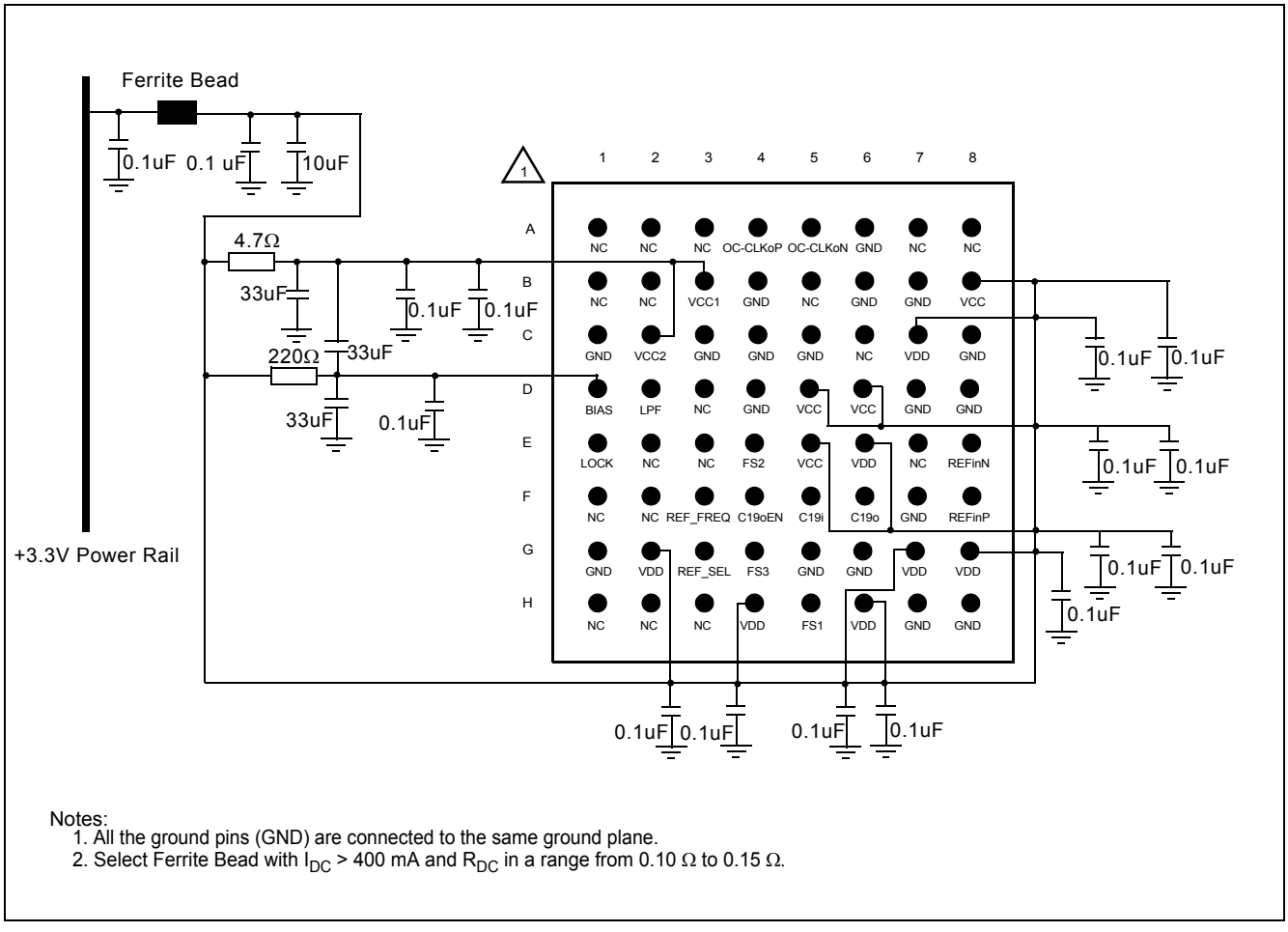


Figure 9 - LVPECL to LVPECL Interface

4.3 Power Supply and BIAS Circuit Filtering Recommendations

Figure 10 presents a complete filtering arrangement that is recommended for applications requiring maximum jitter performance. The level of required filtering is subject to further optimization and simplification. Please check Zarlink's web site for updates.



Notes:
1. All the ground pins (GND) are connected to the same ground plane.
2. Select Ferrite Bead with I_{DC} > 400 mA and R_{DC} in a range from 0.10 Ω to 0.15 Ω.

Figure 10 - Power Supply and BIAS Circuit Filtering

5.0 Characteristics

Absolute Maximum Ratings†

	Characteristics	Sym.	Min.‡	Max.‡	Units
1	Supply voltage	V_{DDR}, V_{CCR}	TBD	TBD	V
2	Voltage on any ball	V_{BALL}	-0.5	V_{CC} + 0.5 V_{DD} + 0.5	V
3	Current on any ball	I_{BALL}	-0.5	30	mA
4	ESD rating	V_{ESD}		1250	V
5	Storage temperature	T_{ST}	-55	125	°C
6	Package power dissipation	P_{PD}		1.0	W

† Voltages are with respect to ground unless otherwise stated.

‡ Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions†

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	Operating temperature	T_{OP}	-40	25	+85	°C	
2	Positive supply	V_{DD}, V_{CC}	3.0	3.3	3.6	V	

† Voltages are with respect to ground unless otherwise stated.

‡ Typical figures are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics†

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	Supply current	I_{DD}+I_{CC}		185		mA	Note 1 Note 2
2	CMOS: High-level input voltage	V_{IH}	0.7V_{DD}		V_{DD}	V	
3	CMOS: Low-level input voltage	V_{IL}	0		0.3V_{DD}	V	
4	CMOS: Input leakage current	I_{IL}		1	5	uA	$V_I = V_{DD}$ or 0V
5	CMOS: Input bias current for pulled-down inputs: FS1, FS2 and FS3	I_{B-PU}		300		uA	$V_I = V_{DD}$
6	CMOS: Input bias current for pulled-up inputs: C19oEN	I_{B-PD}		90		uA	V_I = 0 V
7	CMOS: High-level output voltage	V_{OH}	2.4			V	I_{OH} = 8 mA

DC Electrical Characteristics† (continued)

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Notes
8	CMOS: Low-level output voltage	V_{OL}			0.4	V	I_{OL} = 4 mA
9	CMOS: C19o output rise time	T_R		1.8	3.3	ns	18 pF load
10	CMOS: C19o output fall time	T_F		1.1	1.4	ns	18 pF load
11	LVPECL: Differential output voltage	$\|V_{OD\_LVPECL}\|$		1.30		V	for 622 MHz Note 2
12	LVPECL: Offset voltage	V_{OS_LVPECL}	Vcc-1.38	Vcc-1.27	Vcc-1.15	V	for 622 MHz Note 2
13	LVPECL: Output rise/fall times	T_{RF}		260		ps	for 622 MHz Note 2

† Voltages are with respect to ground unless otherwise stated.

‡ Typical figures are for design aid only: not guaranteed and not subject to production testing.

Supply voltage and operating temperature are as per Recommended Operating Conditions.

Note 1: The I_{LVPECL} current is determined by the external termination network connected to LVPECL outputs. More than 25% of this current (10 mA) flows outside the chip and it does not contribute to the internal power dissipation. The Supply Current value listed in the table includes this current to reflect total current consumption of the ZL30415 and the attached LVPECL termination network.

Note 2: LVPECL outputs terminated with Z_T = 50 Ω resistors biased to V_{CC}-2V (see Figure 9).

AC Electrical Characteristics† - Output Timing Parameters Measurement Voltage Levels

	Characteristics	Sym.	CMOS	LVPECL	Units
1	Threshold voltage	$V_{T\text{-}CMOS}$ $V_{T\text{-}LVPECL}$	$0.5V_{DD}$	$0.5V_{OD\_LVPECL}$	V
2	Rise and fall threshold voltage high	V_{HM}	$0.7V_{DD}$	$0.8V_{OD\_LVPECL}$	V
3	Rise and fall threshold voltage low	V_{LM}	$0.3V_{DD}$	$0.2V_{OD\_LVPECL}$	V

† Voltages are with respect to ground unless otherwise stated.

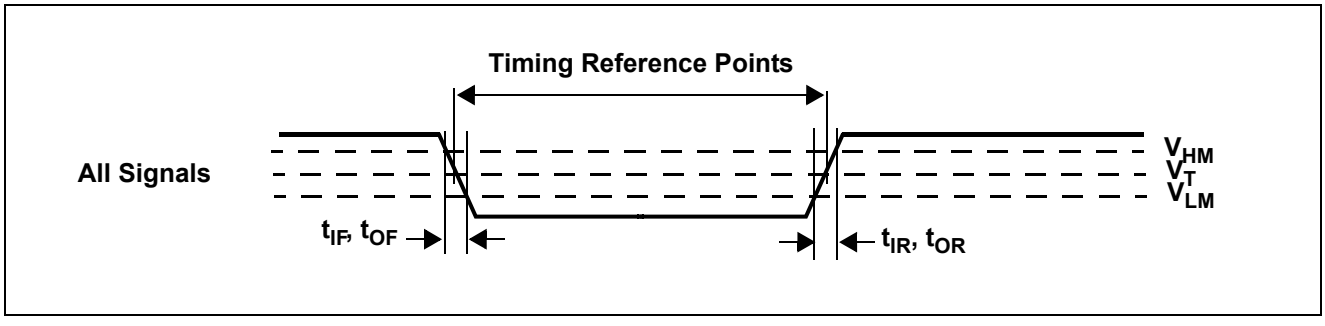


Figure 11 - Output Timing Parameter Measurement Voltage Levels

AC Electrical Characteristics† - C19i Input to C19o Output Timing

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	C19i to C19o delay	t_{C19D}	4.4	6.7	9.4	ns	

† Supply voltage and operating temperature are as per Recommended Operating Conditions.

‡ Typical figures are for design aid only: not guaranteed and not subject to production testing.

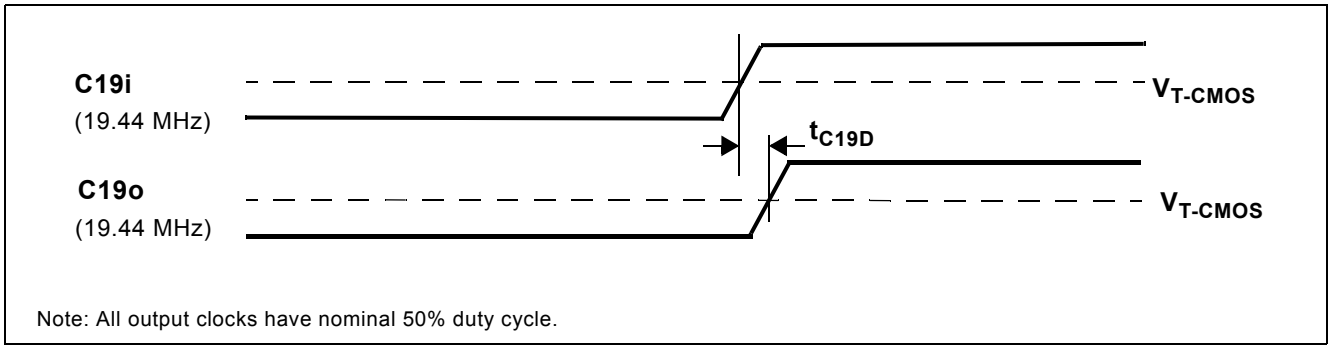


Figure 12 - C19i Input to C19o Output Timing

AC Electrical Characteristics† - REFin to C19o Output Timings

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	REFin (19.44 MHz) to C19o (19.44 MHz) delay	$t_{R19OC19D}$	1.4	7.8	10	ns	
2	REFin (77.76 MHz) to C19o (19.44 MHz) delay	$t_{R77OC77D}$	7.9	9.9	13	ns	

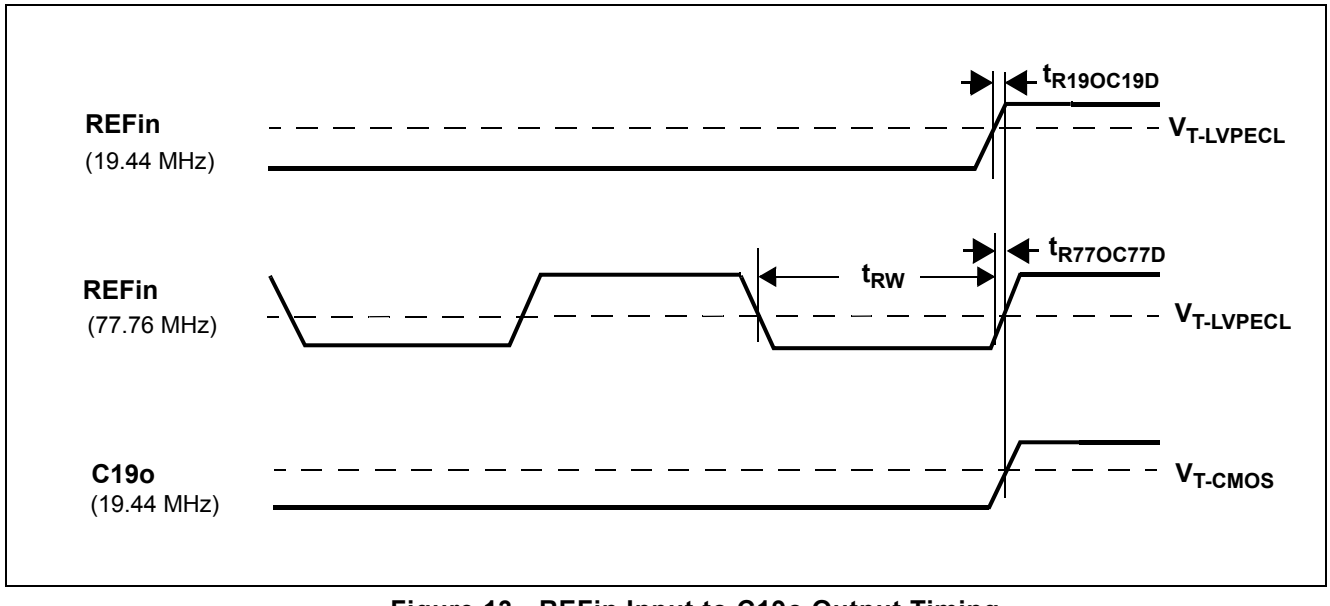


Figure 13 - REFin Input to C19o Output Timing

AC Electrical Characteristics† - C19i Input to OC-CLKo Output Timing

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	C19i(CMOS) to C19o(LVPECL) delay	t_{C19D}	1.4	3.3	5.1	ns	
2	C19i(CMOS) to OC-CLKo(38) delay	t_{C38D}	1.2	3.0	4.8	ns	
3	C19i(CMOS) to OC-CLKo(77) delay	t_{C77D}	0.9	2.6	4.4	ns	
4	C19i(CMOS) to OC-CLKo(155) delay	t_{C155D}	0.6	2.3	4.1	ns	
5	C19i(CMOS) to OC-CLKo(622) delay	t_{C622D}	0	0.8	1.6	ns	
6	All Output Clock duty cycle	d_C	48	50	52	%	

† Supply voltage and operating temperature are as per Recommended Operating Conditions.

‡ Typical figures are for design aid only: not guaranteed and not subject to production testing.

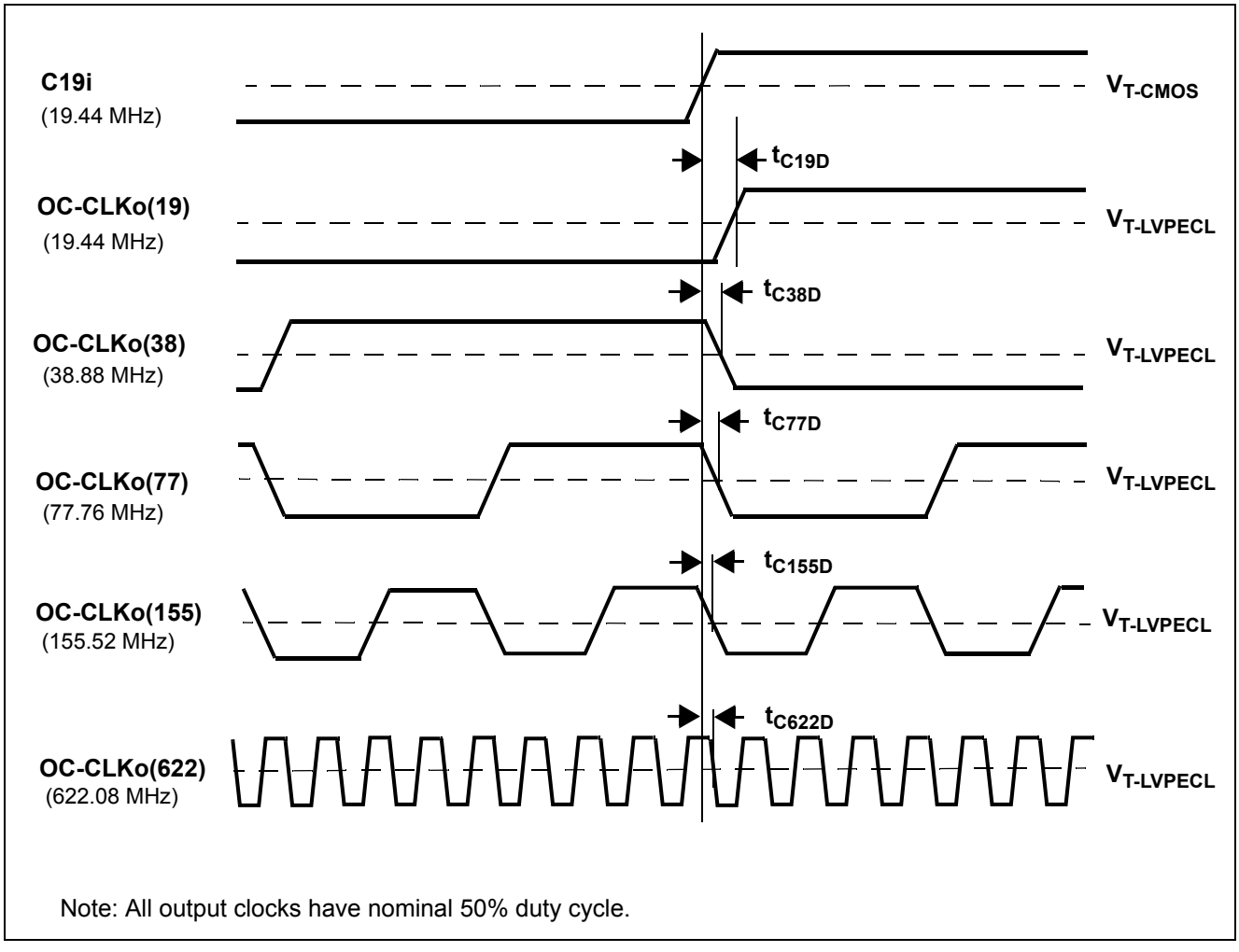


Figure 14 - C19i Input to OC-CLKo Output Timing

AC Electrical Characteristics† - REFin (19.44 MHz) Input to OC-CLKo Output Timing

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	REFin(19.44 MHz) to OC-CLKo(19) delay	$t_{C19-19D}$	2.4	4.3	6.2	ns	
2	REFin(19.44 MHz) to OC-CLKo(38) delay	$t_{C19-38D}$	1.9	4.0	6.0	ns	
3	REFin(19.44 MHz) to OC-CLKo(77) delay	$t_{C19-77D}$	1.7	3.7	5.6	ns	
4	REFin(19.44 MHz) to OC-CLKo(155) delay	$t_{C19-155D}$	1.4	3.4	5.3	ns	
5	REFin(19.44 MHz) to OC-CLKo(622) delay	$t_{C19-622D}$	0	0.8	1.6	ns	

† Supply voltage and operating temperature are as per Recommended Operating Conditions.

‡ Typical figures are for design aid only: not guaranteed and not subject to production testing.

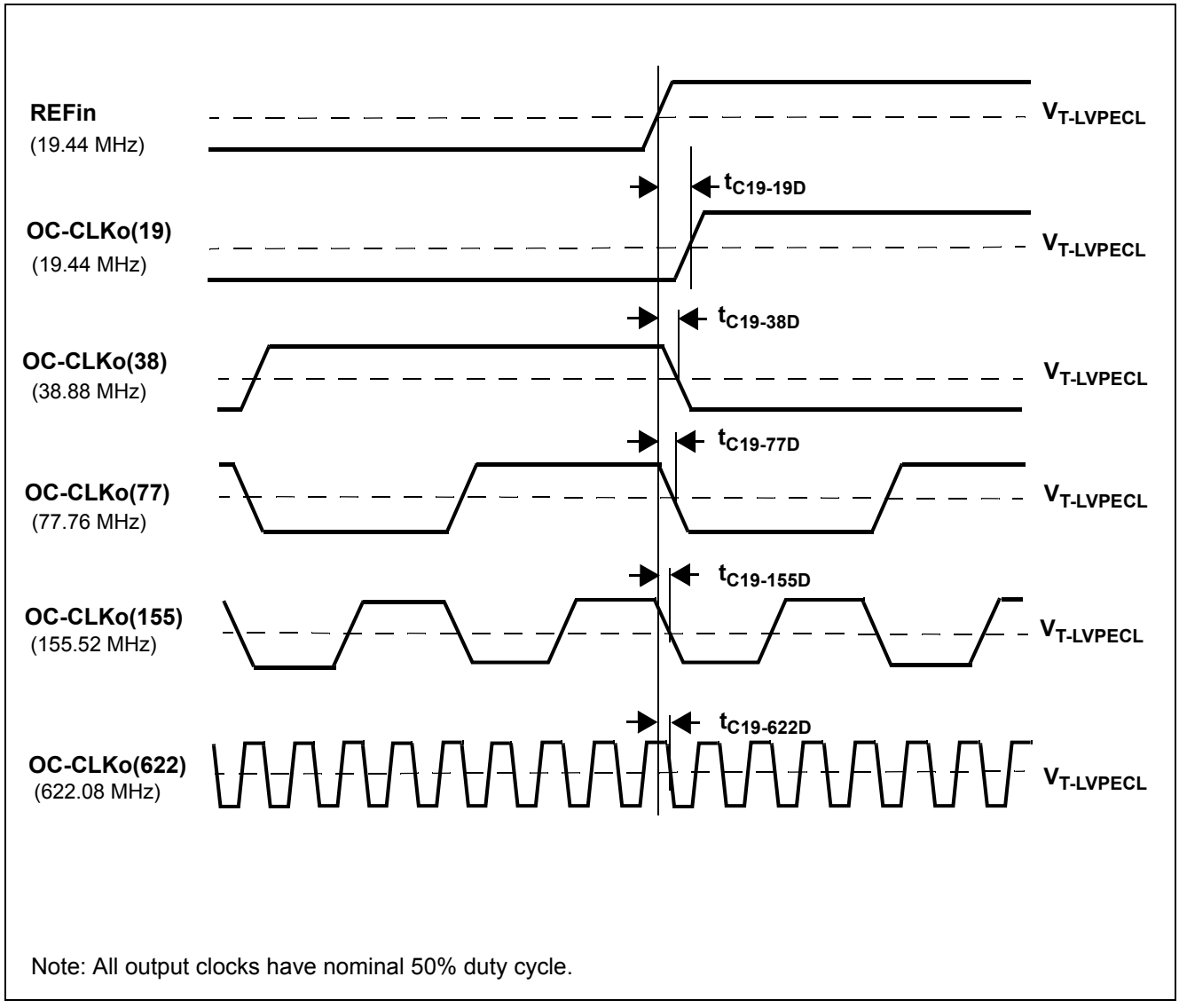


Figure 15 - REFin (19.44 MHz) Input to OC-CLKo Output Timing

AC Electrical Characteristics† - REFin (77.76 MHz) Input to OC-CLKo Output Timing

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	REFin(77.76 MHz) to OC-CLKo(19) delay	$t_{C77-19D}$	3.5	6.5	9.5	ns	
2	REFin(77.76 MHz) to OC-CLKo(38) delay	$t_{C77-38D}$	3.2	6.2	9.2	ns	
3	REFin(77.76 MHz) to OC-CLKo(77) delay	$t_{C77-77D}$	2.9	5.9	8.8	ns	
4	REFin(77.76 MHz) to OC-CLKo(155) delay	$t_{C77-155D}$	2.6	5.6	8.6	ns	
5	REFin(77.76 MHz) to OC-CLKo(622) delay	$t_{C77-622D}$	0	0.8	1.6	ns	

† Supply voltage and operating temperature are as per Recommended Operating Conditions.

‡ Typical figures are for design aid only: not guaranteed and not subject to production testing.

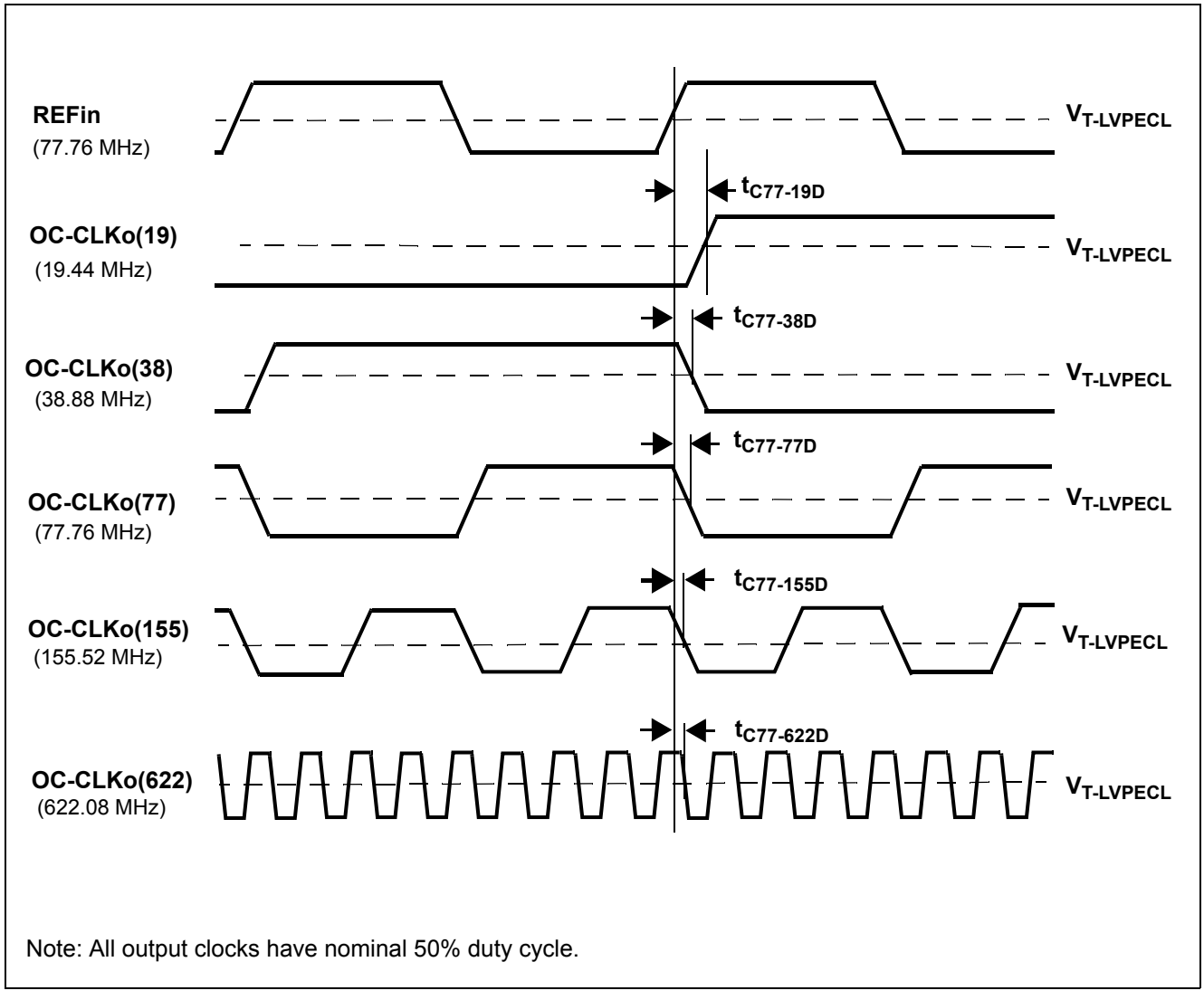


Figure 16 - REFin (77.76 MHz) Input to OC-CLKo Output Timing

Performance Characteristics - Functional (VCC = 3.3 V ±10%; TA = -40 to 85×C)

	Characteristics	Min.	Typ.	Max.	Units	Notes
1	Pull-in range	±1000			ppm	At nominal input reference frequency C19i = 19.44 MHz
2	Lock Time			300	ms	

Performance Characteristics: Output Jitter Generation (LVPECL: 19.44 MHz, 38.88 MHz, 77.76 MHz, 155.52 MHz, and 622.08 MHz and CMOS: 19.44 MHz) - GR-253-CORE conformance - (V_{CC} = 3.3 V ±10%; T_A = - 40 to 85°C)

GR-253-CORE Jitter Generation Requirements				ZL30415 Jitter Generation Performance			
	Interface (Category II)	Jitter Measurement Filter	Limit in UI	Equivalent limit in time domain	Typ.†	Max.‡	Units
1	OC-12 STS-12	12 kHz - 5 MHz	0.1 UIpp	161		35	ps_{P-P}
			0.01 UI_{RMS}	16.1	1.7	3.5	ps_{RMS}
2	OC-3 STS-3	12 kHz - 1.3 MHz	0.1 UIpp	643		33	ps_{P-P}
			0.01 UI_{RMS}	64.3	1.6	3.3	ps_{RMS}

† Typical figures are for design aid only: not guaranteed and not subject to production testing.

‡ Loop Filter components: R_F = 8.2 kΩ, C_F = 470 nF.

Performance Characteristics: Output Jitter Generation (LVPECL: 19.44 MHz, 38.88 MHz, 77.76 MHz, 155.52 MHz, and 622.08 MHz and CMOS: 19.44 MHz) - ETSI EN 300 462-7-1 conformance - (V_{CC} = 3.3 V ±10%; T_A = -40 to 85°C)

EN 300 462-7-1 Jitter Generation Requirements				ZL30415 Jitter Generation Performance			
	Interface	**Jitter Measurement Filter**	**Limit in UI**	**Equivalent limit in time domain**	**Typ.†**	**Max.‡**	**Units**
1	STM-4	250 kHz to 5 MHz	0.1 UIpp	161		30	ps_{P-P}
			-	-	1.5	3	ps_{RMS}
		1 kHz to 5 MHz	0.5 UIpp	804		80	ps_{P-P}
			-	-	4	8	ps_{RMS}
2	STM-1 optical	65 kHz to 1.3 MHz	0.1 UIpp	643		31	ps_{P-P}
			-	-	1.6	3.1	ps_{RMS}
		500 Hz to 1.3 MHz	0.5 UIpp	3215		100	ps_{P-P}
			-	-	5	10	ps_{RMS}
3	STM-1 electrical	65 kHz to 1.3 MHz	0.075 UIpp	482		31	ps_{P-P}
			-	-	1.6	3.1	ps_{RMS}
		500 Hz to 1.3 MHz	0.5 UIpp	3215		100	ps_{P-P}
			-	-	5	10	ps_{RMS}

† Typical figures are for design aid only: not guaranteed and not subject to production testing.

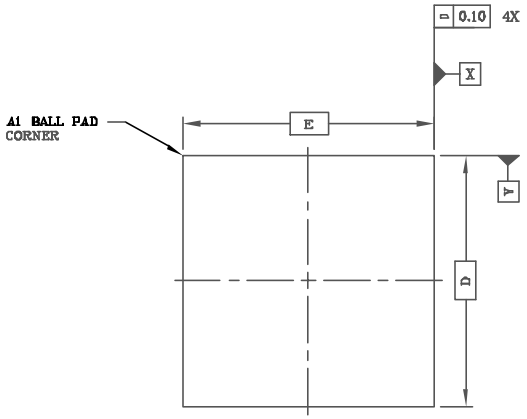
‡ Loop Filter components: R_F = 8.2 kΩ, C_F = 470 nF.

Performance Characteristics: Output Jitter Generation (LVPECL: 19.44 MHz, 38.88 MHz, 77.76 MHz, 155.52 MHz, and 622.08 MHz and CMOS: 19.44 MHz) - G.813 conformance (Option 1 and 2) - (V_{CC} = 3.3 V ±10%; T_A = -40 to 85°C)

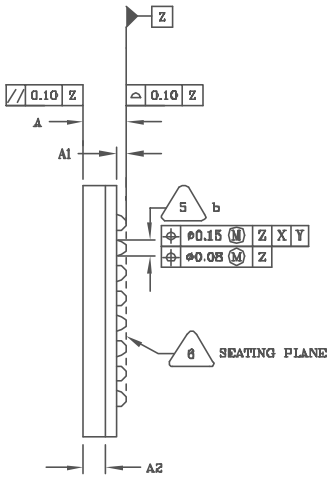
G.813 Jitter Generation Requirements				ZL30415 Jitter Generation Performance			
	Interface	**Jitter Measurement Filter**	**Limit in UI**	**Equivalent limit in time domain**	**Typ.†**	**Max.‡**	**Units**
Option 1							
1	STM-4	250 kHz to 5 MHz	0.1 UIpp	161		30	ps_{P-P}
			-	-	1.5	3	ps_{RMS}
		1 kHz to 5 MHz	0.5 UIpp	804		80	ps_{P-P}
			-	-	4	8	ps_{RMS}
2	STM-1	65 kHz to 1.3 MHz	0.1 UIpp	643		31	ps_{P-P}
			-	-	1.6	3.1	ps_{RMS}
		500 Hz to 1.3 MHz	0.5 UIpp	3215		100	ps_{P-P}
			-	-	5	10	ps_{RMS}
Option 2							
3	STM-4	12 kHz - 5 MHz	0.1 UIpp	161		35	ps_{P-P}
			-	-	1.7	3.5	ps_{RMS}
4	STM-1	12 kHz - 1.3 MHz	0.1 UIpp	643		33	ps_{P-P}
			-	-	1.6	3.3	ps_{RMS}

† Typical figures are for design aid only: not guaranteed and not subject to production testing.

‡ Loop Filter components: R_F = 8.2 kΩ, C_F = 470 nF.

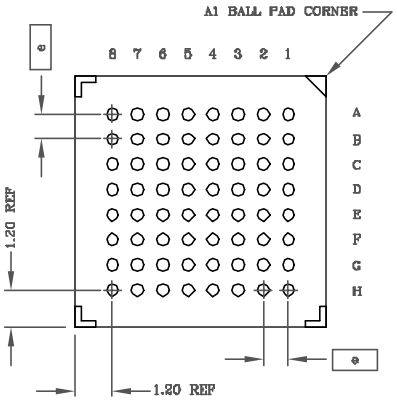


TOP VIEW



SIDE VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.39	1.40	1.41
A1	0.31	0.36	0.41
A2	0.65	0.70	0.75
b	0.46 Typ.		
D	8.00 Ref.		
E	8.00 Ref.		
e	0.80 Ref		
n	64		



BOTTOM VIEW

6 PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

5 DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM Z.

4. THE MAXIMUM ALLOWABLE NUMBER OF SOLDER BUMPS IS 64, FOR 8X8 BODY.

3. ALL DIMENSIONS ARE IN MILLIMETERS.

2. NOT TO SCALE.

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994.

NOTES: UNLESS OTHERWISE SPECIFIED

ISSUE	1			
ACN				
DATE	17 Jul. 03			
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes

Package Code GG

Package Outline for 64ball, 8x8mm. 0.8mm Pitch CABGA

100798

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