85C220/85C224-100, -80 AND -66 FAST REGISTERED SPEED T_{SU}, T_{SO} 8-MACROCELL PLDs

These register optimized timing PLDs offer superior design features:

- **Low-Power, High-Performance Upgrade for SSI/MSI Logic and Bipolar PALs* High-Performance Systems**
- **Replacement or Upgrade for 16V8/ 20V8 PAL and GAL Architecture**
- **8 Macrocells with Independently Programmable I/O Architecture**
- **Up to 18 Inputs (10 Dedicated and 8 I/O) and 8 Outputs**
- **Programmable "Security Bit" Allows Total Protection of Proprietary Designs**
- **100% Generally Tested Logic Array**

85C220-100 AND 85C224-100

- **100 MHz Max Frequency (External Feedback); 5.5 ns (Max) Clock to Output; 4.5 ns (Min) Set-Up Time**
- **Meets Critical Timing Requirements of Advanced Intel Microprocessor Systems**
- **7.5 ns (Max) Propagation Delay**
- **Typical I_{CC} = 90 mA**
- **Available in 20-Pin and 28-Pin PLCC Packages**
- **Low Power and Output Skew for Clock Device Applications**

85C220-80 AND 85C224-80

- **Quarter Power (I_{CC} = 40 mA); Programmable Zero Power Mode (50 μA Typical)**
- **80 MHz Max Frequency (External Feedback); 5.5 ns (Max) Clock to Output; 7 ns (Min) Set-Up Time**
- **10 ns Propagation Delay**
- **High-Speed Upgrade to EP320, EP330, and 5C032**
- **Available in 300-mil 20-Pin and 24-Pin CerDIP/PDIP Packages, and 20-Pin and 28-Pin PLCC Packages**

October 1993
Order Number: 290224-005

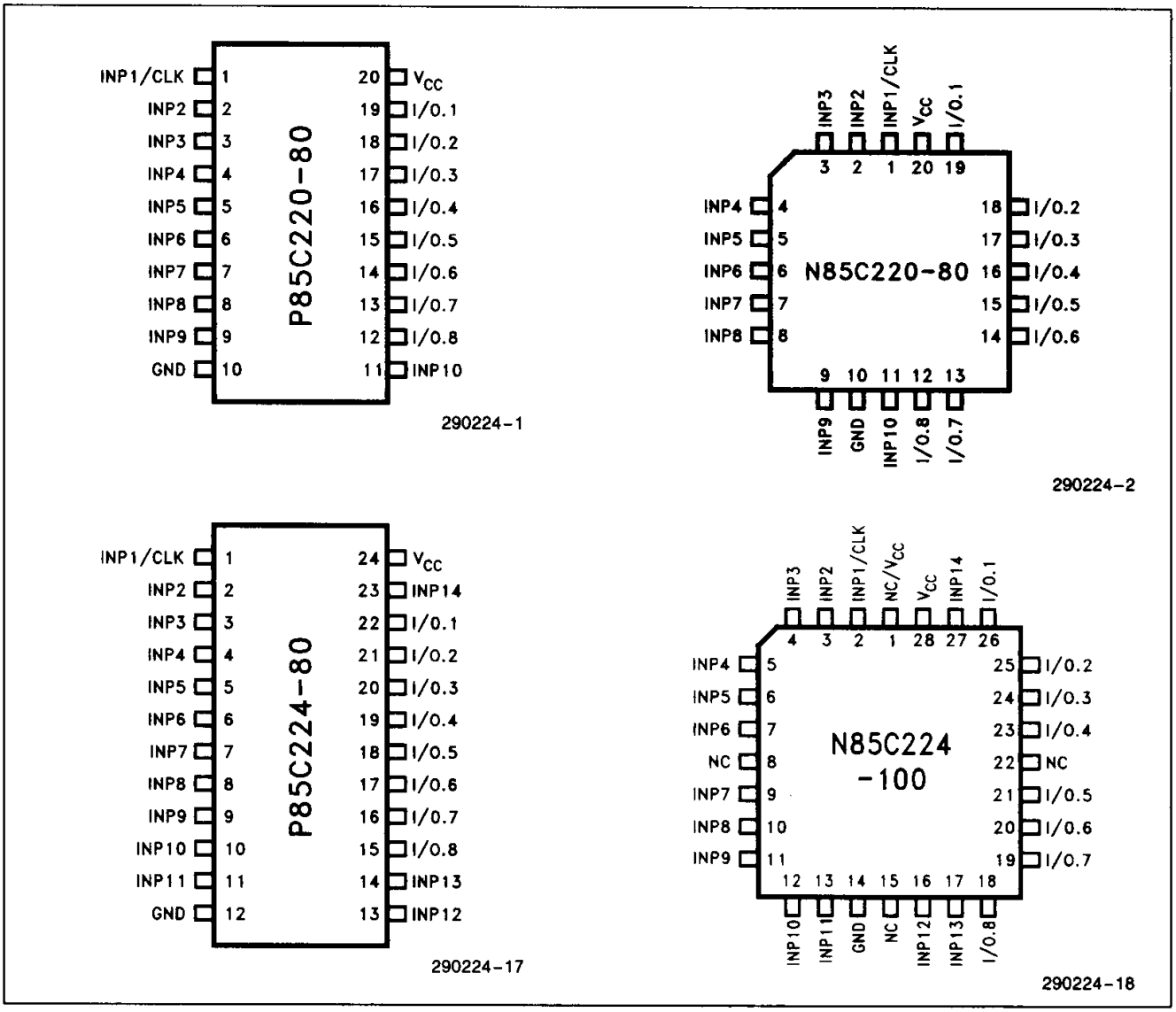


Figure 1. Pinout Diagrams

High Frequency/Low Output Skew Clock Driver

The 85C220 and 85C224-100 displays dramatically reduced output pin skew in comparison with industry clock driver products. With high performance systems relying on increasingly faster clocking frequencies, managing the timing of high frequency system clocks is now more important than ever. Whether the configuration is combinatorial (as with a clock driver) or registered (as with a frequency divider) the output skew (T_{OS}) is typically less than 300 pico seconds! The extremely low output skew of the 85C220 and 85C224 make the devices ideal for a variety of high frequency system clock related applications including Pentium™ microprocessor, Intel486 and PCI Bus designs. The 85C224-100 combines the flexibility of programmable logic with the industry's lowest output skew.

INTRODUCTION

The Intel 85C220/85C224 8-micron CHMOS μPLD (Microcomputer Programmable Logic Device) is capable of implementing over 300 equivalent gates of user-customized logic functions through programming. With its flexible I/O architecture and fast speeds, this device has functional capabilities that surpass those of typical programmable logic devices. This device can be used to upgrade high-speed bipolar programmable logic devices and 74-series LS and CMOS SSI and MSI logic devices in bus control and state-machine applications for Advanced Intel Microprocessors, i486™, Intel386™, and Intel i860™-based systems and other high-performance processors. The 85C220/85C224 can also be used as a direct, low-power replacement for almost all high-speed 20-pin and 24-pin fuse-based programmable logic devices.

The 85C220/85C224 uses advanced EPROM cells as architecture and logic control memory elements. Coupled with Intel's proprietary CHMOS IIIE technology, these devices offer a fast t_{PD} in combinatorial mode, with current consumption much lower than bipolar devices of equivalent speed. The maximum "count" frequencies of 100 MHZ and 80 MHz are optimized for high-performance state machines typically encountered in bus control applications. EPROM technology allows these devices to be 100% factory tested by programming and erasing all the EPROM logic control elements.

The inherent speed of the device together with its lower power demands and plastic package make the 85C220/85C224 an ideal production vehicle for high-volume manufacturing of high-performance systems. The 85C220/85C224 will improve performance and reliability, while decreasing system noise, power consumption and heat generation.

ARCHITECTURE DESCRIPTION

The architecture of the 85C220/85C224 is based on the SOP (Sum of Products) PAL structure with a programmable AND array feeding into a fixed OR array. Programmable macrocells allow the device to accommodate both combinatorial and sequential logic functions. Each macrocell is individually programmable for combinatorial or registered output. An invert option on the SOP allows each output to be configured as an active-high or active-low output.

As shown in Figures 2 and 3, the 85C220/85C224 contains 10/14 dedicated inputs and 8 I/O pins. Each I/O pin can be individually programmed to function as an input, output, or bidirectional I/O pin. Associated with each I/O pin is a programmable macrocell.

Figures 4 and 5 show the structure of the 85C220/85C224 macrocell. Each macrocell includes a p-term (product term) block with eight AND p-terms feeding the OR gate of the I/O control block and one additional p-term controlling the output buffer. The logic array is 36 rows wide, allowing each p-term in the device to connect to the true or complement of each input and I/O feedback signal. Each intersecting point in the logic array is connected or not connected based on the value programmed in the EPROM array. Initially (EPROM erased state), all p-terms are connected to all signals. Connections are broken by programming the appropriate EPROM cells. Connecting both the true and complement of a signal for a given p-term removes that p-term from the SOP for the macrocell (i.e., that p-term is a "don't care").

Figure 6 shows the architecture of each macrocell's I/O control block. The SOP input to the I/O control block can be inverted or non-inverted. The output can be registered or combinatorial. When registered output is selected, feedback to the logic array comes directly from the register (before the output buffer). When combinatorial output is selected, feedback comes from the I/O pin (after the output buffer) and can be used for bidirectional I/O. The register is a D-type register that clocks on the rising edge of CLK.

20-PIN AND 24-PIN PLD COMPATIBILITY

The 85C220/85C224 is designed to be a logical superset of most high-speed 20-pin and 24-pin bipolar PAL and GAL devices. The I/O and logic sections of the device can be configured to emulate any of the devices listed below. Designers can often replace multiple PALs with fewer 85C220/85C224 devices. Tables 1 and 2 include some of the devices with which the 85C220/85C224 are compatible.

Table 1. Replacement/Upgrade

10 ns—20-Pin and 24-Pin		
Company	**20-Pin Part**	**24-Pin Part**
Intel	**85C220-80**	**85C224-80**
AMD	PAL16L8D	PAL20L8-10
AMD	PAL16R8D	PAL20R8-10
AMD	PAL16R8-7	PAL20R8-7
AMD	PALCE16V8	PALCE20V8
National	GAL16V8A	GAL20V8A
National	PAL16L8D	PAL20L8D
National	PAL16R8D	PAL20R8D
National	PAL16R8-7	N/A
Signetics	PLUS16L8D	PLUS20L8D
Signetics	PLUS16R8D	PLUS20R8D
Signetics	PLUS16R8-7	PLUS20R8-7
TI	TIBPAL16L8-10	TIBPAL20L8-10
TI	TIBPAL16R8-10	TIBPAL20R8-10
TI	TIBPAL16R8-7	TIBPAL20R8-7

Table 2. Replacement/Upgrade

12 ns—20-Pin and 24-Pin		
Company	**20-Pin Part**	**24-Pin Part**
Intel	**85C220-66**	**85C224-66**
AMD	PAL16L8	PAL20L8
AMD	PAL16R8	PAL20R8
AMD	PALCE16V8	PALCE20V8
Cypress	PALC16L8	PALC20L8
Cypress	PALC16R8	PALC20R8
National	GAL16V8A	GAL20V8A
National	PAL16L8	PAL20L8
National	PAL16R8	PAL20R8
Signetics	PLUS16L8	PLUS20L8
Signetics	PLUS16R8	PLUS20R8
TI	TIBPAL16L8	TIBPAL20L8
TI	TIBPAL16R6	TIBPAL20R6
TI	TIBPAL16R8	TIBPAL20R8

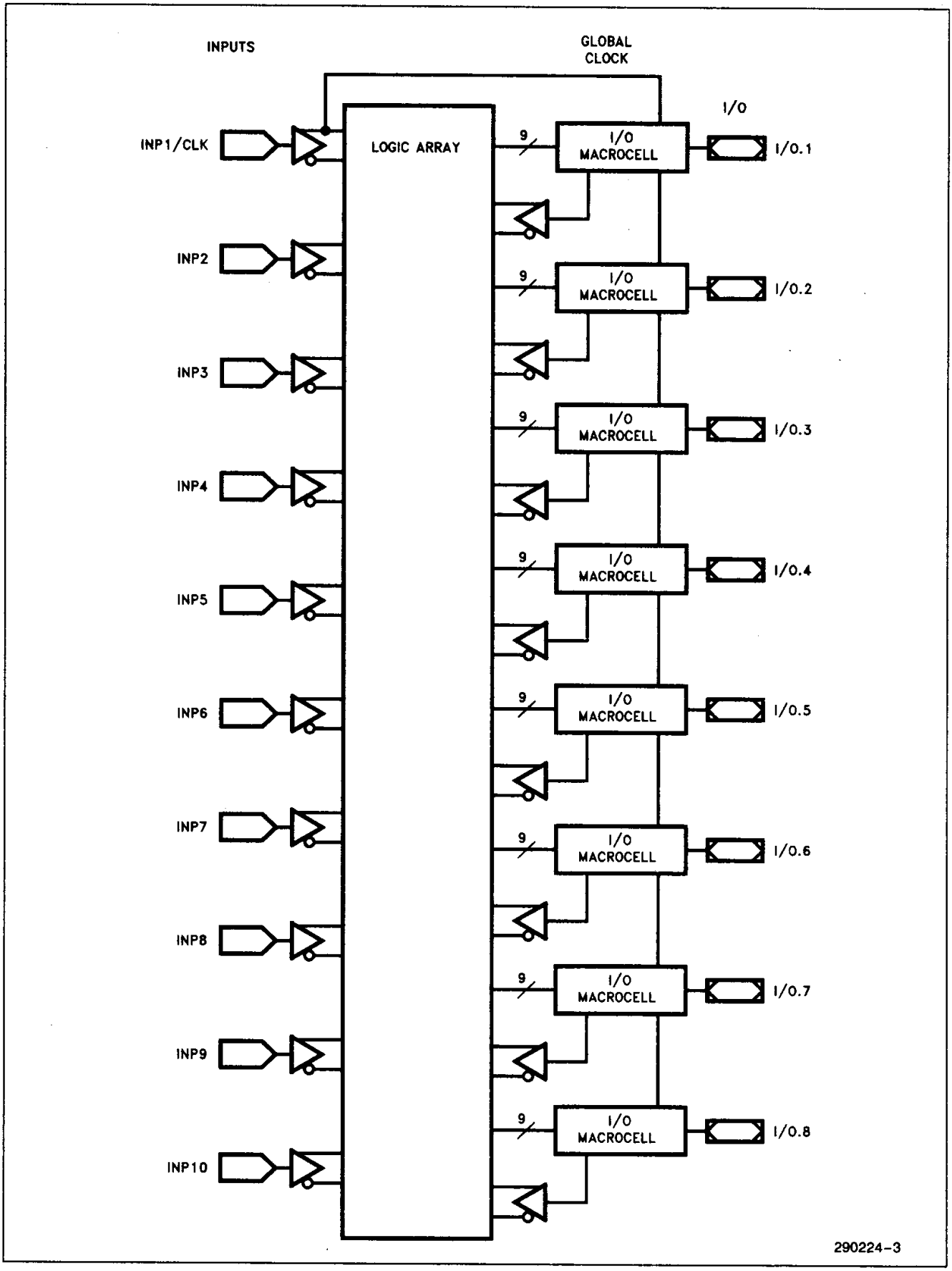


Figure 2. 85C220 Global Architecture

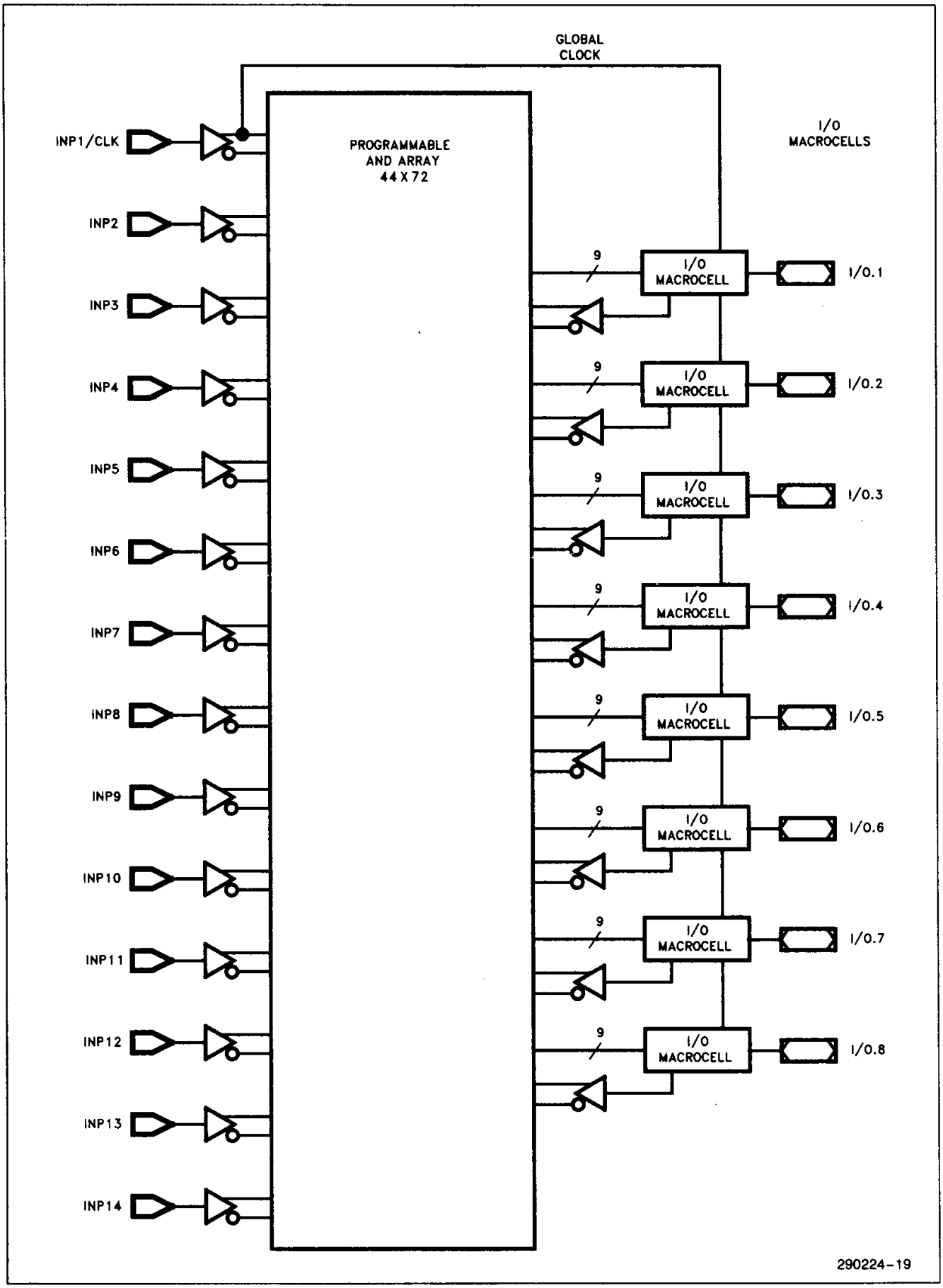


Figure 3. 85C224 Global Architecture

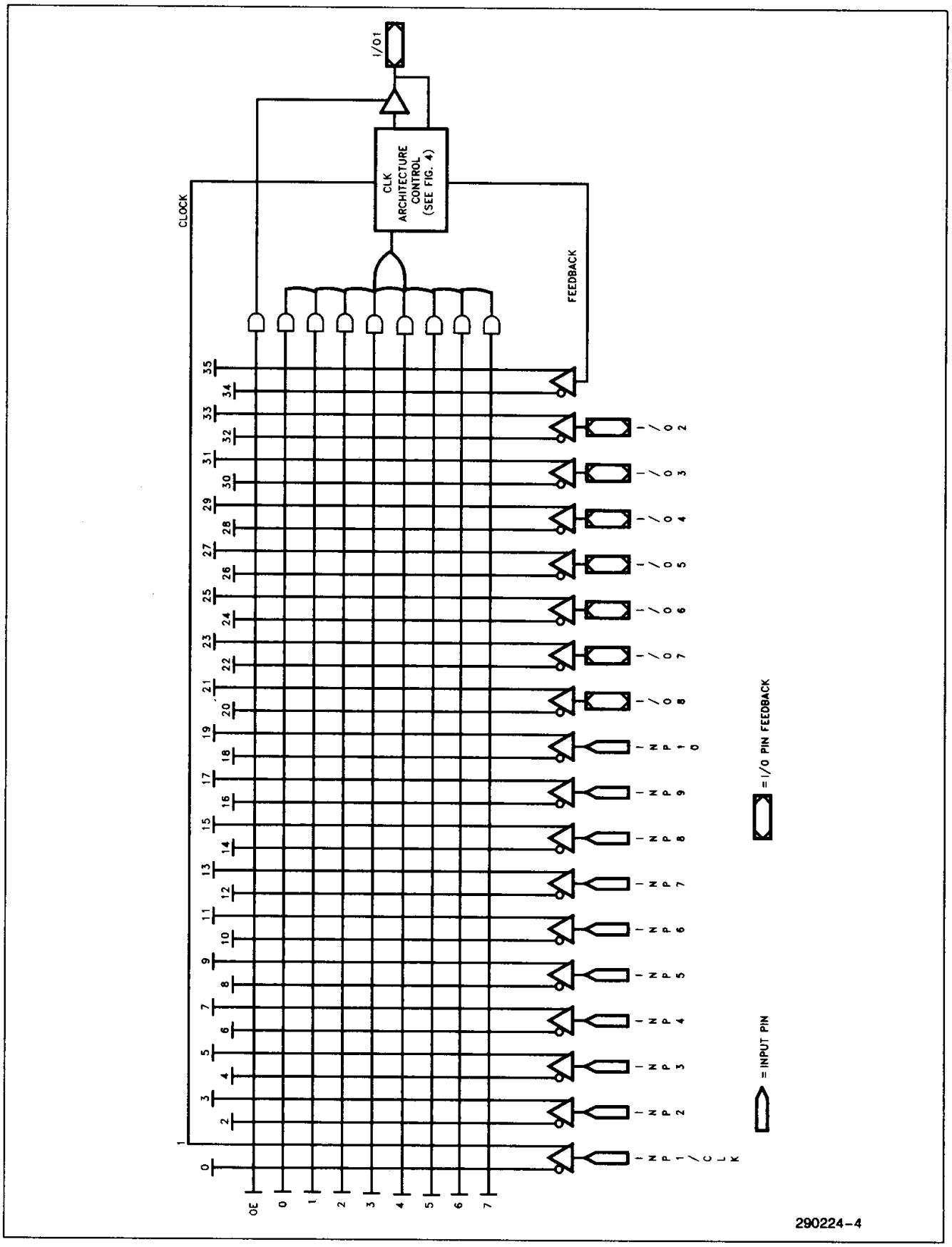


Figure 4. 85C220 Macrocell Architecture

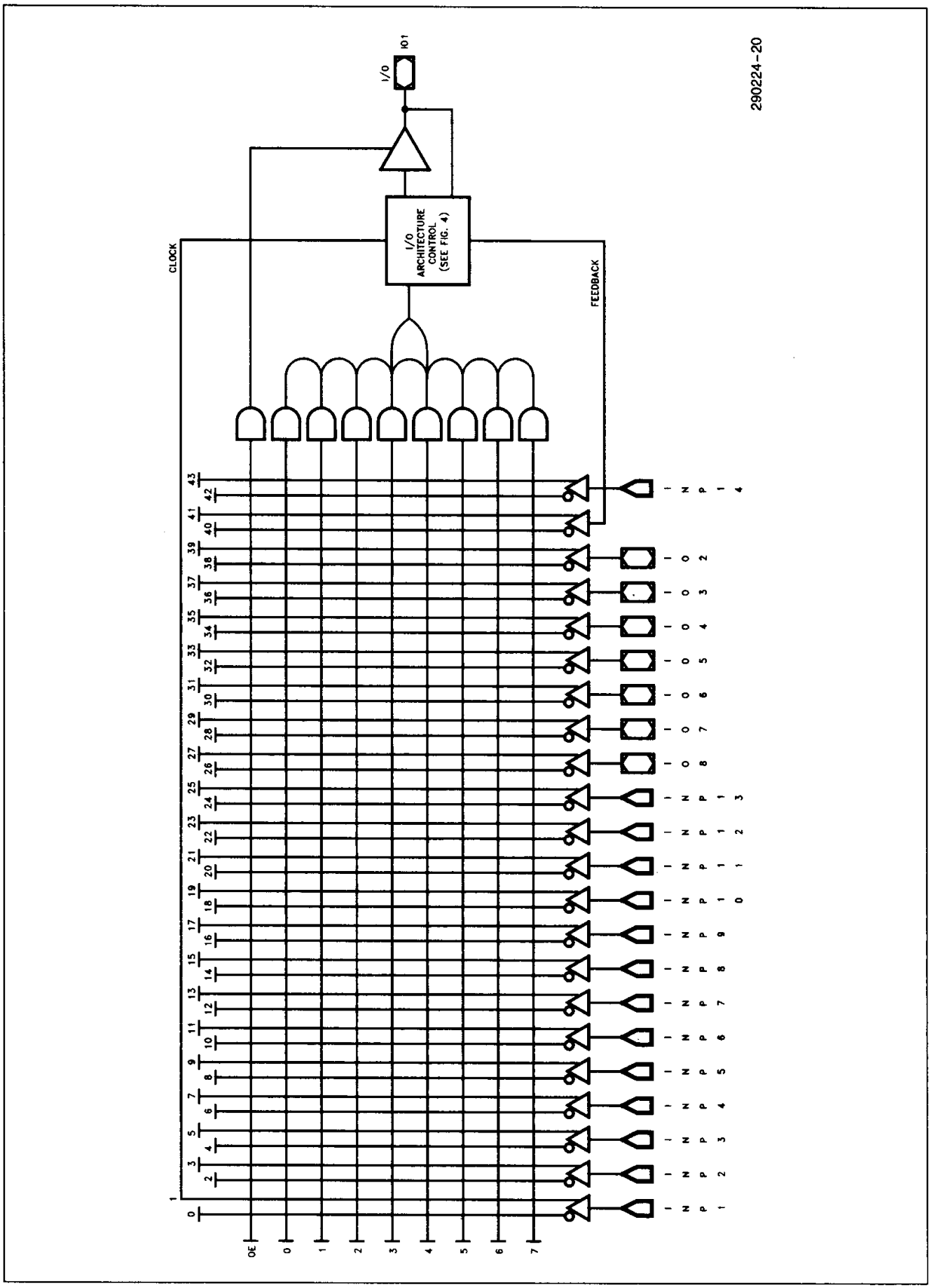


Figure 5. 85C224 Macrocell Architecture

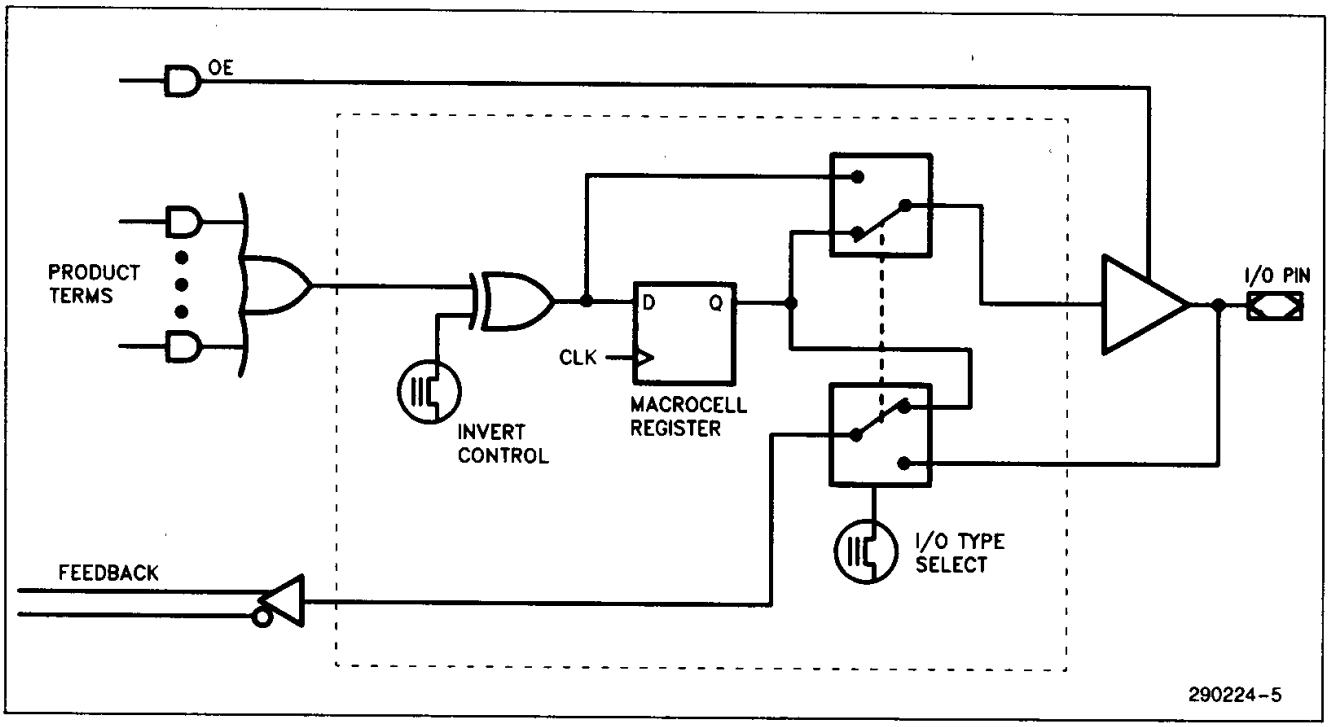


Figure 6. 85C220/85C224 I/O Control Architecture

AUTOMATIC STAND-BY MODE

The 85C220/85C224-80 and -66 contains a programmable bit, the Turbo Bit, that optimizes operation either for speed or for power savings. When the Turbo Bit is programmed (TURBO = ON), the device is optimized for maximum speed. When the Turbo Bit is not programmed (TURBO = OFF), the device is optimized for power savings by entering standby mode during periods of inactivity.

Figure 7 shows the device entering standby mode approximately 75 ns after the last input or I/O transition. When the next input or I/O transition is detected, the device returns to active mode. Wakeup time adds an additional 20 ns to the propagation delay through the device as measured from the first transition. No delay will occur if an output is dependent on more than one input and the last of the inputs changes after the device has returned to active mode.

After erasure, the Turbo Bit is unprogrammed (OFF); automatic standby mode is enabled. When the Turbo Bit is programmed (ON), the device never enters standby mode.

POWER-ON CHARACTERISTICS

85C220/85C224 inputs and outputs begin responding 1 μs (max.) after V_{CC} power-up (V_{CC} = 4.75V) or after a power-loss/power-up sequence. All macrocells programmed as registers will be set to a logic low.

ERASED STATE CHARACTERISTICS

Prior to programming or after erasure, the I/O structure is configured for combinatorial active low output with input (pin) feedback.

Erasure time for the 85C220/85C224 is 1 hour at 12,000 μWsec/cm^2 with a 2537Å UV lamp.

Erasure characteristics of the device are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000Å. It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range. Data shows that constant exposure to room level fluorescent lighting could erase the typi-

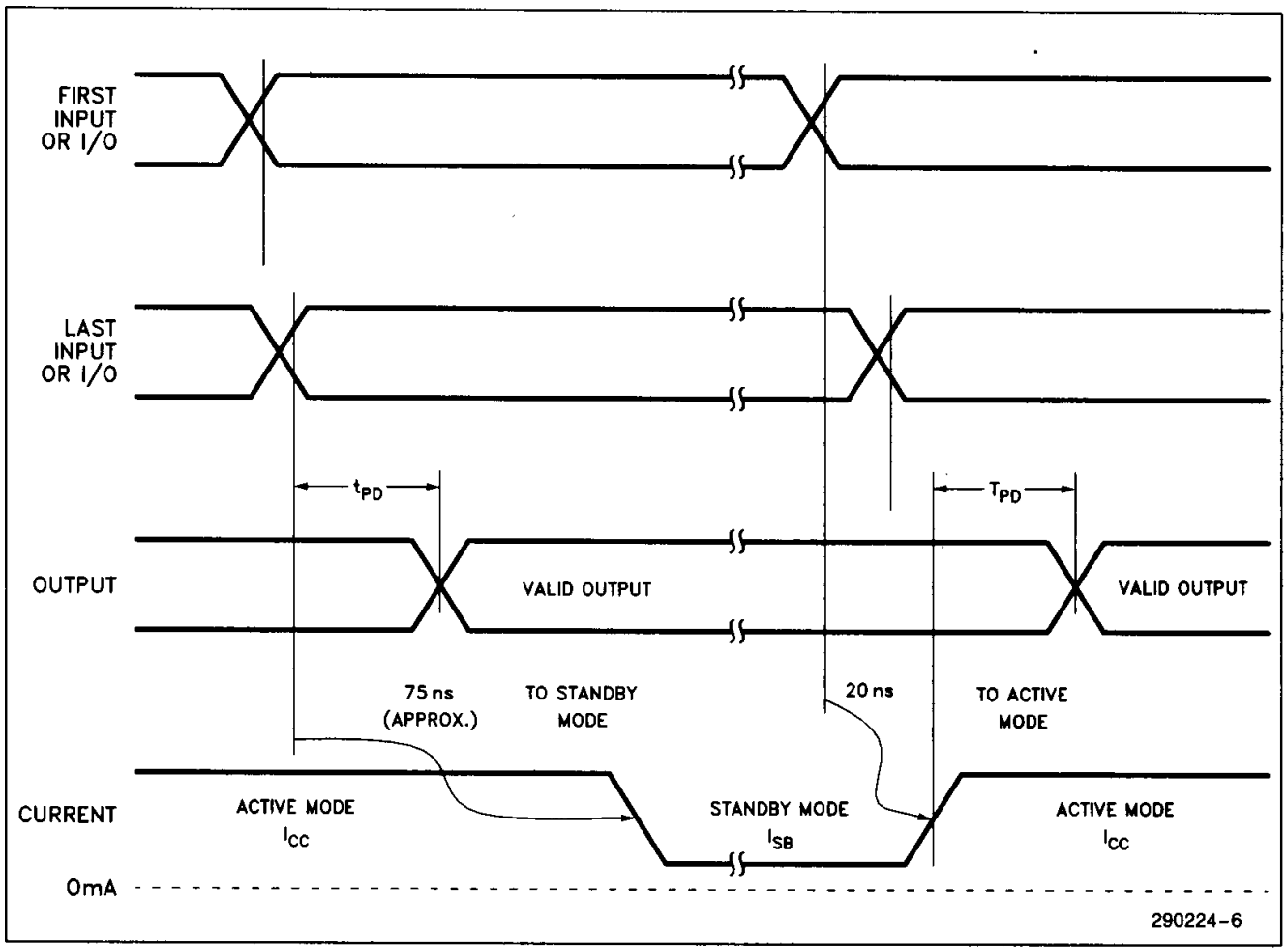


Figure 7. 85C220/85C224 Standby and Active Mode Transitions

cal 85C220/85C224 in approximately six years, while it would take approximately two weeks to erase the device when exposed to direct sunlight. If the device is to be exposed to these lighting conditions for extended periods of time, conductive opaque labels should be placed over the device window to prevent unintentional erasure.

The recommended erasure procedure for the 85C220/85C224 is exposure to shortwave utraviolet light with a wavelength 2537Å. The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of forty (40) Wsec/cm^2. The erasure time with this dosage is approximately 1 hour using an ultraviolet lamp with a 12,000 μW/cm^2 power rating. The device should be placed within 1 inch of the lamp tubes during exposure. The maximum integrated dose the 85C220/85C224 can be exposed to without damage is 7258 Wsec/cm^2 (1 week at 12,000 μW/cm^2). Exposure to high intensity UV light for longer periods may cause permanent damage to the device.

Intelligent Programming Algorithm

The 85C220/85C224 support the Intelligent Programming Algorithm, which rapidly programs Intel EPLDs, and many of Intel's microcontrollers and EPROMs while maintaining a high degree of reliability. It is particularly suited for production programming environments. This method decreases the overall programming time while reliability is ensured as the incremental programming margin of each bit has been verified during programming. Programming voltage and waveform specifications are available by request from Intel to support device programming.

LATCH-UP IMMUNITY

All of the input, output, and clock pins of the device have been designed to resist latch-up which is inherent in inferior CMOS structures. The 85C220/85C224 is designed with Intel's proprietary 1-micron

CHMOS IIIE EPROM process. Thus, each of the pins will not experience latch-up with currents up to ±100 mA and voltages ranging from −0.5V to (V_{CC} + 0.5V). The programming pin is designed to resist latch-up to the 13.5V maximum device limit.

DESIGN RECOMMENDATIONS

For proper operation, it is recommended that all input and output pins be constrained to the voltage range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}. All unused inputs and I/Os should be tied high or low to minimize power consumption (do not leave them floating). On the 85C224 PLCC package, the optional power pin (pin 1) and optional ground pins (8, 15, and 22) may be connected to power and ground, respectively, to reduce output switching noise. A high-speed power supply decoupling capacitor of at least 0.2 μF must be connected directly between the V_{CC} and GND pins.

As with all CMOS devices, ESD handling procedures should be used with the devices to prevent damage to the devices during programming, assembly, and test.

COMPILER SUPPORT

The 85C220 and 85C224 are supported by Intel's PLDshell Plus software as well as third-party logic compilers such as ABEL*, CUPL*, PLDDesigner*, Log/IC*, etc.

PLDshell Plus software is a free design package that accepts PALASM 2-compatible source files. PLDshell Plus software allows you to design in a familiar language and to functionally simulate your design. You can also invoke third-party design packages directly from the PLDshell Run menu.

iPLS II includes the LOC (Logic Optimizing Compiler) and APT (Advanced Programming Tool). For detailed information on iPLS II, refer to the iPLDS II Data Sheet, order number: 290134.

The following ADF primitives are supported by this device:

INP	RONF
CONF	RORF
COIF	NORF

PROGRAMMING SUPPORT

Programming for the 85C220 is supported by APT on the GUPI 20D20J Programming Adaptor using either an iUP-PC Personal Programmer or an iUP-200A/201A Universal Programmer. Programming for the 85C224 is supported by the same software/platforms using the GUPI 24D28J Programming Adaptor.

85C220/85C224 programming support is also provided by third-party programmer companies such as Data I/O, Logical Devices, STAG, etc. Please refer to the "Programming Support" lists in the *Programmable Logic* handbook for complete information and vendor contacts.

ORDERING INFORMATION

f_{CNT1} (MHz)	f_{MAX} (MHz)	t_{PD} (ns)	Order Code 20-Pin	Order Code 24-Pin	Package	Operating Range
100	115	7.5	N85C220-100	N85C224-100	PLCC	Commercial
80	111	10	D85C220-80	D85C224-80	†CerDIP	Commercial
			P85C220-80	P85C224-80	PDIP	
			N85C220-80	N85C224-80	PLCC	
66	90.9	12	D85C220-66	D85C224-66	†CerDIP	Commercial
			P85C220-66	P85C224-66	PDIP	
			N85C220-66	N85C224-66	PLCC	

†Windowed CerDIP package allows UV erase.

*ABEL is a trademark of Data I/O, Corporation. CUPL is a trademark of Logical Devices, Inc. PLDesigner is a trademark of MINC, Inc.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage (V_{CC})(1) ..... −2.0V to +7.0V

Programming Supply Voltage (V_{PP})(1) ..... −2.0V to +13.5V

D.C. Input Voltage (V_I)(1, 2) ... −0.5V to V_{CC} +0.5V

Storage Temperature (T_{STG}) .... −65°C to +150°C

Ambient Temperature (T_{AMB})(3) .. −10°C to +85°C

NOTES:
1. Voltages with respect to GND.
2. Minimum D.C. input is −0.5V. During transitions, the inputs may undershoot to −2.0V or overshoot to +7.0V for periods of less than 20 ns under no load conditions.
3. Under bias. Extended Temperature versions are also available.

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

2

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IN}	Input Voltage	0	V_{CC}	V
V_O	Output Voltage	0	V_{CC}	V
T_A	Operating Temperature	0	+70	°C
t_R	Input Rise Time		500	ns
t_F	Input Fall Time		500	ns

D.C. CHARACTERISTICS (T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%)

85C220/85C224-100

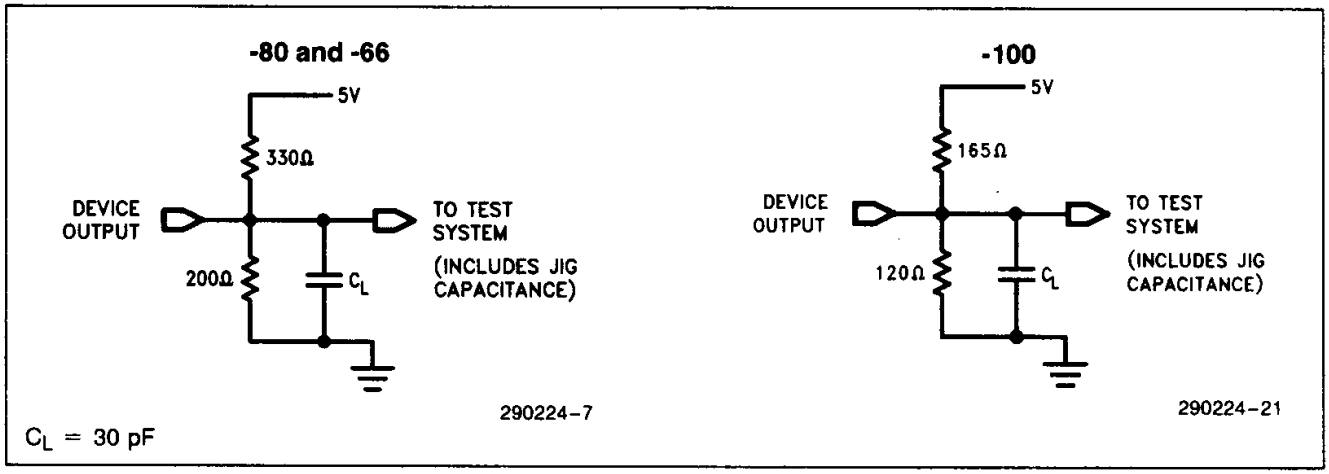
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}(4)	High Level Input Voltage	2.0		V_{CC} + 0.3	V	
V_{IL}(4)	Low Level Input Voltage	−0.3		0.8	V	
V_{OH}	High Level Output Voltage	2.4			V	I/O = −4.0 mA D.C., V_{CC} = Min
V_{OL}	Low Level Output Voltage			0.45	V	I/O = 24.0 mA D.C., V_{CC} = Min
I_I	Input Leakage Current			±10	µA	V_{CC} = Max, GND < V_{IN} < V_{CC}
I_{OZ}	Output Leakage Current			±10	µA	V_{CC} = Max, GND < V_{OUT} < V_{CC}
I_{SC}(6)	Output Short Circuit Current	−30		−120	mA	V_{CC} = Max, V_{OUT} = 0.5V
I_{CC}	Power Supply Current		60	90	mA	V_{CC} = Max, V_{IN} = V_{CC} or GND, No Load, f_{IN} = 25 MHz, Device Prog. as an 8-Bit Counter
			85	115	mA	f_{IN} = 100 MHz

85C220/85C224-80 and -66

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}(4)	High Level Input Voltage	2.0		$V_{CC}+0.3$	V	
V_{IL}(4)	Low Level Input Voltage	−0.3		0.8	V	
V_{OH}	High Level Output Voltage	2.4			V	I_O = −4.0 mA D.C., V_{CC} = Min
V_{OL}(5)	Low Level Output Voltage			0.45	V	I_O = 12.0 mA D.C., V_{CC} = Min
I_I	Input Leakage Current			±10	μA	V_{CC} = Max, GND < V_{IN} < V_{CC}
I_{OZ}	Output Leakage Current			±10	μA	V_{CC} = Max, GND < V_{OUT} < V_{CC}
I_{SC}(6)	Output Short Circuit Current	−30		−120	mA	V_{CC} = Max, V_{OUT} = 0.5V
I_{SB}(7)	Standby Current		50	500	μA	V_{CC} = Max, V_{IN} = V_{CC} or GND, Standby Mode
I_{CC}	Power Supply Current (see I_{CC} vs Frequency Graph)		2	5	mA	V_{CC} = Max, V_{IN} = V_{CC} or GND, No Load, f_{IN} = 1 MHz, Device Prog. as an 8-Bit Counter, Non-Turbo Mode
			35	50	mA	f_{IN} = 15 MHz, Active Mode
			45	60	mA	f_{IN} = 80 MHz, Active Mode

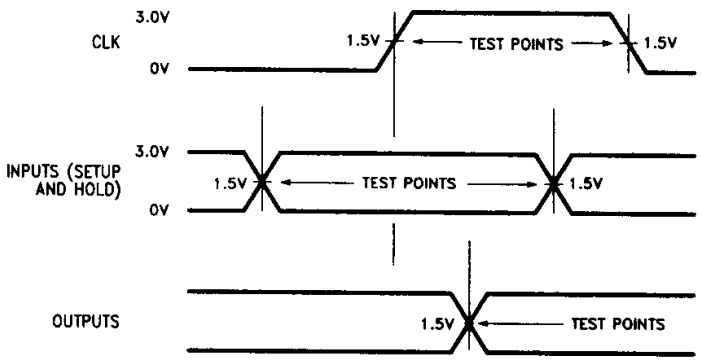
NOTES:
4. Absolute values with respect to device GND; all over and undershoots due to system or tester noise are included.
5. Maximum DC I_{OL} for the device (all 8 outputs) is 64 mA.
6. Not more than 1 output should be tested at a time. Duration of that test should not exceed 1 second.
7. In Non-Turbo Mode (TURBO=OFF), device enters standby mode approximately 75 ns after the last input transition.

A.C. TESTING LOAD CIRCUIT



C_L = 30 pF

A.C. TESTING WAVEFORM—SYNCHRONOUS INPUTS AND OUTPUTS



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A.C. Testing: Inputs (including CLK) are driven at 3.0V for a Logic "1" and 0V for a Logic "0". Setup and hold input measurements relative to CLK are made at 2.0V on CLK (low-to-high transition). Inputs are measured at 2.0V for a high and 0.8V for a low. Outputs are measured at 1.5V. Device input rise and fall times are less than 3 ns.

2

CAPACITANCE (T_A = 0°C to +70°C; V_{CC} = 5.0V ±5%)(8)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
C_{IN}	Input Capacitance		4	6	pF	V_{IN} = 0V, f = 1.0 MHz
C_{IO}	I/O Capacitance		5	8	pF	V_{OUT} = 0V, f = 1.0 MHz
C_{CLK}	CLK Capacitance		6	8	pF	V_{OUT} = 0V, f = 1.0 MHz
C_{VPP}	V_{PP} Pin Capacitance		8	10	pF	V_{PP} on Pin 11/13, f = 1.0 MHz

NOTES:
8. These values are evaluated during initial characterization and whenever design modifications occur that may affect capacitance.

A.C. CHARACTERISTICS (T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%)(9)

Symbol	Parameter	85C220-100/ 85C224-100			85C220-80/ 85C224-80			85C220-66/ 85C224-66			Non-Turbo(10) Mode	Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
t_{PD}(11)	Input or I/O to Output	3		7.5	4		10	4		12	+20	ns
t_{PZX}(12)	Input or I/O to Output Enable	3		9	4		12	4		12	+20	ns
t_{PXZ}(12)	Input or I/O to Output Disable	3		9	4		10	4		12	+20	ns
T_{os}	Registered Output Skew	150	250	300								ps
T_{os}	Comb. Output Skew	150	300	400								ps

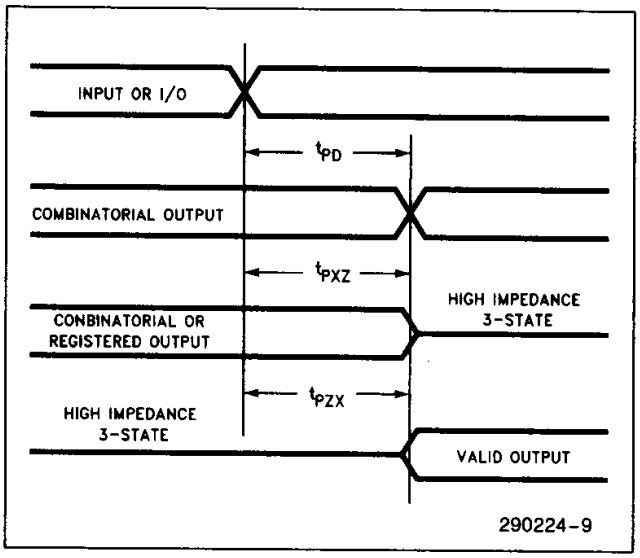
NOTES:
9. Typical values are at T_A = +25°C, V_{CC} = 5V, Active Mode.
10. If device is operated in Standby Mode (Standby bit = Low) and the device is inactive for approximately 75 ns, increase time by amount shown for -80 and -66 only.
11. Measured with all eight outputs switching.
12. t_{PZX} and t_{PXZ} are measured at ±0.5V from steady state voltage as driven by specification output load. t_{PXZ} is measured with C_L = 5 pF. Measured with all eight outputs switching.

SYNCHRONOUS CLOCK MODE (T_A = 0°C to 70°C, V_{CC} = 5V ±5%)[9]

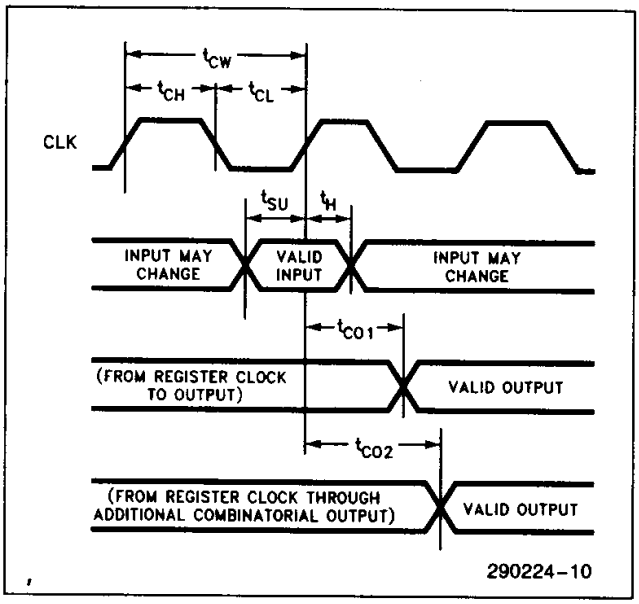
Symbol	Parameter	85C220-100/ 85C224-100			85C220-80/ 85C224-80			85C220-66 85C224-66			Non-Turbo[10] Mode	Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
f_{CNT1}[11]	Maximum Counter Frequency $1/(t_{SU} + t_{CO})$—External Feedback		111	100		100	80		80	66		MHz
f_{CNT2}[11]	Maximum Counter Frequency $1/(t_{CNT})$—Internal Feedback			115		111	100		90	83.3		MHz
f_{MAX}[11]	Maximum Frequency (Pipelined) $1/(t_{CW})$—No Feedback			115		125	111		100	90.9		MHz
t_{SU}	Input or I/O Setup Time to CLK	4.5			7			9			+ 20	ns
t_H	Input or I/O Hold Time from CLK	0			0			0				ns
t_{CO1}	CLK High to Output Valid	3		5.5	1.5[13]		5.5[11]	1.5[13]		6[11]		ns
t_{CO2}	CLK High to Output Valid Fed through Comb. Macrocell	4.5		10	4.5		13	4.5		15	+ 20	ns
t_{CNT}[11]	Macrocell Output Feedback to Macrocell Input—Internal Path	10			10			12			+ 20	ns
t_{CL}	CLK Low Time	4			4			5				ns
t_{CH}	CLK High Time	4			4			5				ns
t_{CW}	CLK Period	10			9			11				ns

NOTE:
13. t_{CO1} min. is measured with one output switching, T_A = 0°C, V_{CC} = 5.25V.

COMBINATORIAL MODE



REGISTERED MODE



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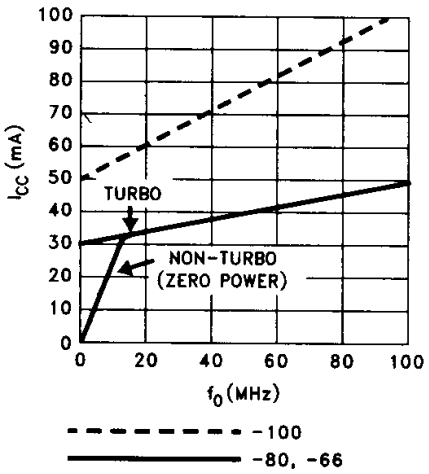
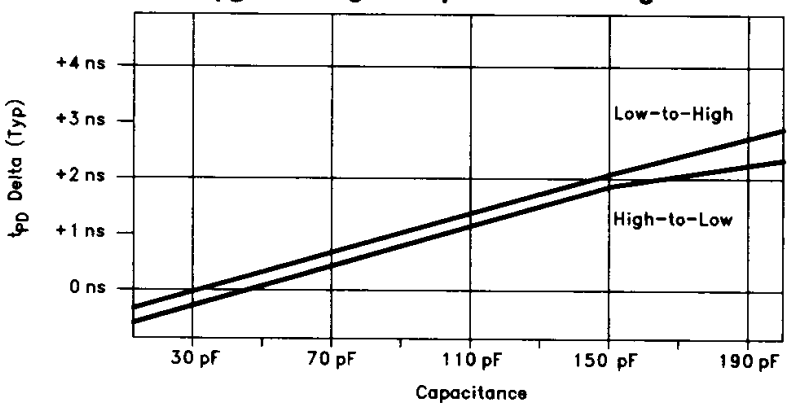
85C220/85224
I_{CC} vs Frequency



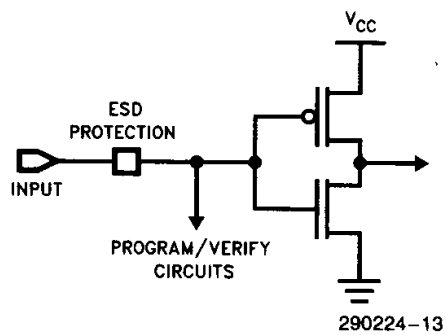
Conditions:
T_A = 25°C
V_{CC} = 5.25V

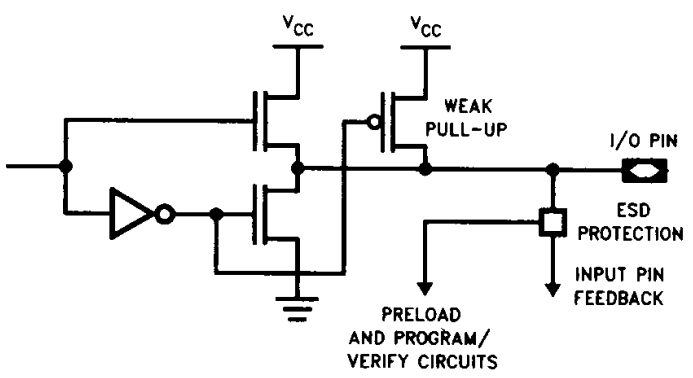
85C220/85C224
t_{PD} Derating vs Capacitive Loading



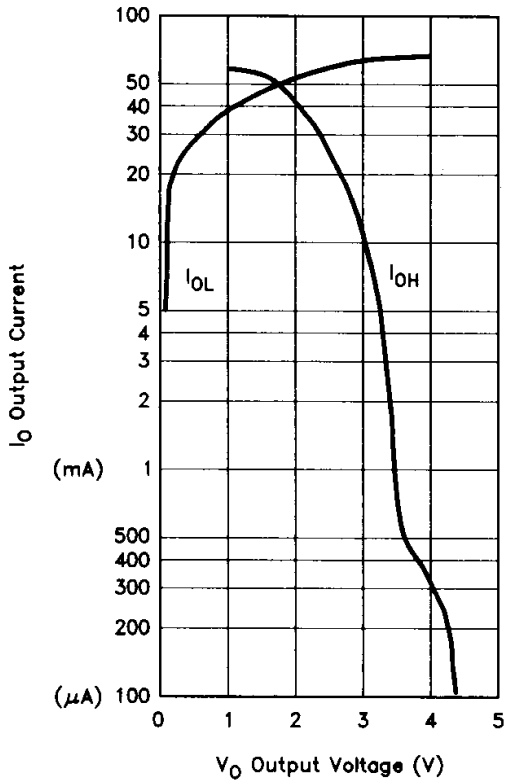
Conditions:
T_A = 70°C
V_{CC} = 4.75V

INPUT/OUTPUT EQUIVALENT SCHEMATICS





85C220/85C224 Output Drive Current in Relation to Voltage



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Conditions:
T_A = +80°C
V_{CC} = 4.75V

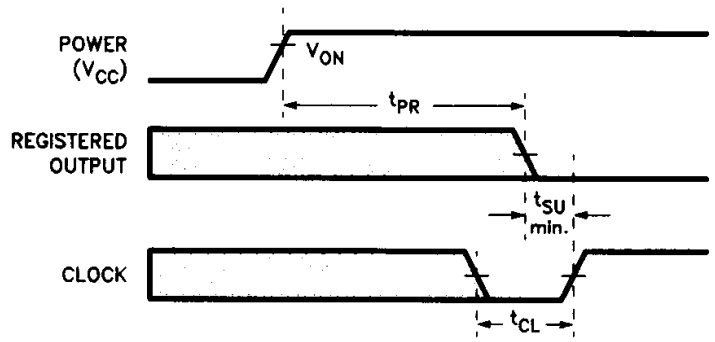
Power-Up Reset

Internal power-up reset circuits ensure that all flip-flops will be reset to a logic 0 after the device has powered up. Because V_{CC} rise can vary significantly from one application to another, V_{CC} rise must be monotonic.

POWER-UP RESET CHARACTERISTICS

Symbol	Parameter	Value
t_{PR}	Power-Up Reset Time	1000 ns Max.
V_{ON}	Turn-On Voltage	4.75V

POWER-UP RESET



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PACKAGE/TECHNOLOGY SPECIFICATIONS

Description	85C220	85C224
Θ_{Ja}—Junction-to-Ambient Thermal Resistance	68°C/W—CerDIP 90°C/W—PDIP 90°C/W—PLCC	55°C/W—CerDIP 65°C/W—PDIP 65°C—PLCC
Θ_{Jc}—Junction-to-Case Thermal Resistance	30°C/W—CerDIP 25°C/W—PDIP 25°C/W—PLCC	55°C/W—CerDIP 20°C/W—PDIP 20°C/W—PLCC
Process	CHMOS IIIE, PX29.5	CHMOS IIIE, PX29.5
I_{CC} Hot—Ambient @70°C	40 mA (-80 Only)	
I_{CC} Typical—Ambient @25°C	40 mA (-80 Only)	

REVISION HISTORY

-004 to -005

Addition of specification for clock driver.