

### FEATURES

#### IF Subsystem

Bandpass  $\Sigma\Delta$  Modulator

Variable-Gain Preamplifier with 13 dB of AGC Range

Mixer

AGC Detector

Op Amp for LNA Biasing

ECL-to-CMOS Level Translator

#### Ultralow Power Design

2.7 V Operating Voltage

4.8 mA Current Consumption

Power-Down Control

#### Small 20-Lead SSOP Package

### APPLICATIONS

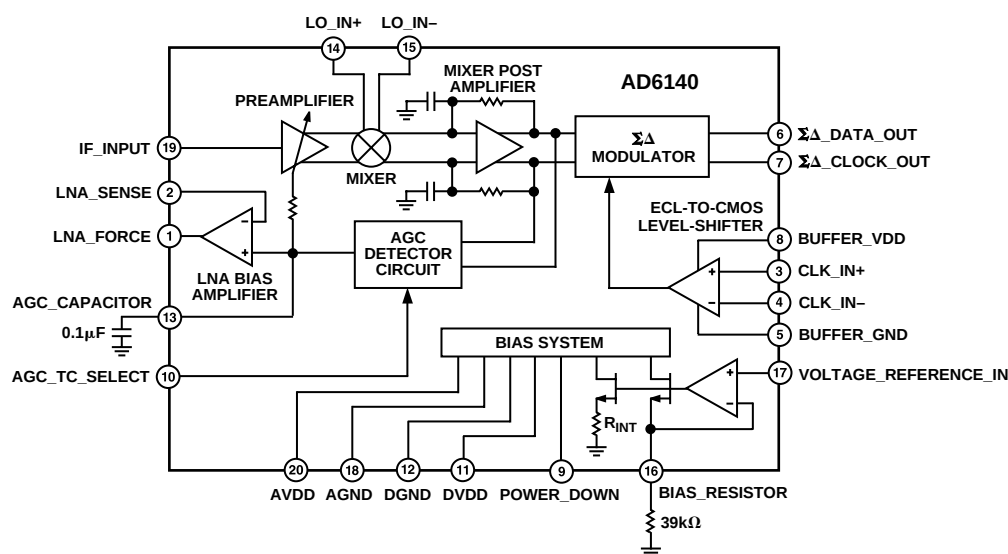
FLEX™, ReFLEX™ Receivers

Multimode Receivers

### GENERAL DESCRIPTION

The AD6140 is a bandpass  $\Sigma\Delta$  ADC IF IC for receivers requiring a high dynamic range and multiple filter bandwidths. With an external decimation filter, it creates a multibit analog-to-digital converter. The AD6140 consists of a variable gain, low noise preamplifier, mixer, AGC detector, bandpass  $\Sigma\Delta$  modulator, an ECL-to-CMOS level translator for the system clock, and an auxiliary amplifier for use in biasing a discrete LNA. It is designed to operate with Motorola's ReFLEX chipset solution. Contact Motorola directly for more information about the ReFLEX chipset solution. With data and clock outputs at CMOS logic levels, it interfaces to an external decimation filter. It comes in a 20-lead plastic SSOP and operates over the  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  industrial temperature range at 2.7 V.

### FUNCTIONAL BLOCK DIAGRAM



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### REV. 0

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# AD6140—SPECIFICATIONS (T<sub>A</sub> = +25°C, V<sub>CC</sub> = 2.7 V, VOLTAGE\_REFERENCE\_IN = 1 V, unless otherwise noted)

| Specification                     | Conditions                                                                                                                                                                                                      | Min | Typ  | Max       | Units |
|-----------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|------|-----------|-------|
| OVERALL                           | VOLTAGE_REFERENCE_IN = 1 V ± 5% dc,<br>IF = 49.6 MHz<br>LO = 49.792 MHz or 49.408 MHz, 200 mV p-p<br>Differential Input<br>Clock = 6.144 MHz, 800 mV p-p Differential ECL<br>Input, Clock Asymmetry = 50 ± 2.5% |     |      |           |       |
| Input Third Order Intercept Point | At Max Gain                                                                                                                                                                                                     | −27 | −19  |           | dBm   |
| Noise Figure                      | At Max Gain, External Termination                                                                                                                                                                               |     | 10.5 |           | dB    |
| Input Resistance                  | At IF_INPUT (Pin 19)                                                                                                                                                                                            |     | 2.5  |           | kΩ    |
| Input Capacitance                 | At IF_INPUT (Pin 19)                                                                                                                                                                                            |     | 12   |           | pF    |
| Dynamic Range                     | 6.25 kHz Bandwidth Centered at 192 kHz                                                                                                                                                                          | 76  | 83   |           | dB    |
| Maximum Gain                      |                                                                                                                                                                                                                 |     | 29.5 |           | dB    |
| Minimum Gain                      |                                                                                                                                                                                                                 |     | 16   |           | dB    |
| AGC DETECTOR                      |                                                                                                                                                                                                                 |     |      |           |       |
| AGC Threshold                     |                                                                                                                                                                                                                 |     | −24  |           | dBm   |
| Capacitor Charging Current        | AGC_TC_SELECT Input = Logic LOW (FAST AGC)                                                                                                                                                                      |     | 2.8  |           | μA    |
|                                   | AGC_TC_SELECT Input = Logic HIGH (SLOW AGC)                                                                                                                                                                     |     | 50   |           | nA    |
| ECL-TO-CMOS LEVEL<br>TRANSLATOR   | VDD (to VDD − 0.8 V) Differential Levels                                                                                                                                                                        |     |      |           |       |
| Clock Output Drive                | 5 pF Load                                                                                                                                                                                                       | 2.6 |      |           | V p-p |
| Clock Asymmetry                   | 5 pF Load                                                                                                                                                                                                       |     | ±2.5 |           | %     |
| LNA BIAS AMPLIFIER VOLTAGE        |                                                                                                                                                                                                                 |     |      |           |       |
| LNA_FORCE                         | 2.9 V LNA_SENSE, Minimum Gain                                                                                                                                                                                   | 1.7 |      |           | V     |
| LNA_SENSE Input Voltage Range     |                                                                                                                                                                                                                 | VDD |      | VDD − 0.3 | V     |
| POWER-DOWN INTERFACE              |                                                                                                                                                                                                                 |     |      |           |       |
| Logic Threshold                   |                                                                                                                                                                                                                 |     | 0.7  |           | V     |
| Turn-On Response Time             | To Valid Data Output                                                                                                                                                                                            |     | 100  |           | μs    |
| Turn-Off Response Time            | To Typical Power-Down Supply Current                                                                                                                                                                            |     | 100  |           | μs    |
| POWER SUPPLY                      |                                                                                                                                                                                                                 |     |      |           |       |
| Supply Voltage                    |                                                                                                                                                                                                                 | 2.5 |      | 2.9       | V     |
| Supply Current                    | Power-Down Input: Logic LOW = ON, IF_Input = 0 V                                                                                                                                                                |     | 4.8  | 5.75      | mA    |
| Power-Down Current                | Power-Down Input: Logic HIGH = OFF                                                                                                                                                                              |     | 3    |           | μA    |
| Operating Temperature Range       |                                                                                                                                                                                                                 | −40 |      | +85       | °C    |

Specifications subject to change without notice.

**ABSOLUTE MAXIMUM RATINGS<sup>1</sup>**

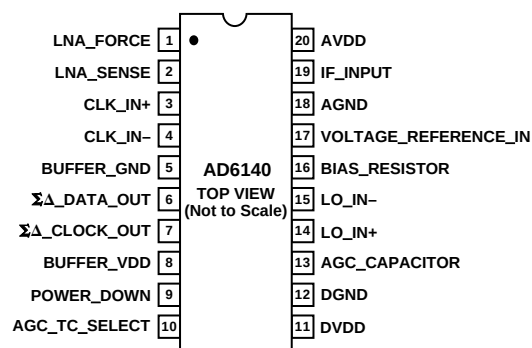
Supply Voltage to Ground . . . . . +5.5 V  
 Internal Power Dissipation<sup>2</sup> . . . . . 50 mW  
 Operating Temperature Range . . . . . -40°C to +85°C  
 Storage Temperature Range . . . . . -65°C to +150°C  
 Lead Temperature, Soldering (60 sec) . . . . . +300°C

**NOTES**

<sup>1</sup>Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended rating conditions for extended periods may affect device reliability.

<sup>2</sup>Thermal Characteristics:

20-Lead SSOP:  $\theta_{JA} = 126^{\circ}\text{C}/\text{W}$ .

**PIN CONFIGURATION****ORDERING GUIDE**

| Model       | Temperature Range | Package Description                   | Package Option |
|-------------|-------------------|---------------------------------------|----------------|
| AD6140ARS   | -40°C to +85°C    | Shrink Small Outline Package          | RS-20          |
| AD6140ARSRL | -40°C to +85°C    | 20-Lead Plastic SSOP on Tape-and-Reel |                |

**CAUTION**

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD6140 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



## PIN FUNCTION DESCRIPTION

| Pin No | Pin Name                  | Function                                                                                                                         | Applicable Signal Levels                                                                                  |
|--------|---------------------------|----------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------|
| 1      | LNA_FORCE                 | Output For Biasing Discrete LNA                                                                                                  | Output Ranges from 0 V (LNA OFF) to 2.7 V                                                                 |
| 2      | LNA_SENSE                 | Input For Biasing Discrete LNA                                                                                                   | VDD to VDD – 0.3 V Input                                                                                  |
| 3      | CLK_IN+                   | Positive 6.144 MHz ADC Clock Input                                                                                               | 800 mV p-p Differential Input<br>VDD to VDD – 0.8 V Levels<br>Direct Coupled into 1500 $\Omega$ Impedance |
| 4      | CLK_IN–                   | Negative 6.144 MHz ADC Clock Input                                                                                               | 800 mV p-p Differential Input<br>VDD to VDD – 0.8 V Levels<br>Direct Coupled into 1500 $\Omega$ Impedance |
| 5      | BUFFER_GND                | ECL-to-CMOS Level Translator Ground                                                                                              | Pin Connected to Ground                                                                                   |
| 6      | $\Sigma\Delta$ _DATA_OUT  | $\Sigma\Delta$ ADC Serial Data Output                                                                                            | CMOS Logic Levels                                                                                         |
| 7      | $\Sigma\Delta$ _CLOCK_OUT | 6.144 MHz ADC Clock Output                                                                                                       | CMOS Logic Levels                                                                                         |
| 8      | BUFFER_VDD                | ECL-to-CMOS Level Translator VDD                                                                                                 | Digital Supply Input                                                                                      |
| 9      | POWER_DOWN                | Turns IC Off and On                                                                                                              | CMOS Logic Levels; 0 V = ON, VPOS = OFF                                                                   |
| 10     | AGC_TC_SELECT             | AGC Time Constant Select; Changes AGC Capacitor Charging Current by 56:1, where FAST AGC Current is 56 $\times$ SLOW AGC Current | CMOS Logic Levels; 0 V = Fast Mode, VPOS = Slow Mode                                                      |
| 11     | DVDD                      | Digital Power Supply Input                                                                                                       | Pin Connected to Digital Supply                                                                           |
| 12     | DGND                      | Digital Ground                                                                                                                   | Pin Connected to Ground                                                                                   |
| 13     | AGC_CAPACITOR             | Charge/Discharge Current into AGC Integrator Capacitor                                                                           | AGC Integration Capacitor Connected to Ground                                                             |
| 14     | LO_IN+                    | Positive LO Input                                                                                                                | 200 mV p-p Differential Input; Internally AC-Coupled into 1500 $\Omega$ Impedance                         |
| 15     | LO_IN–                    | Negative LO Input                                                                                                                | 200 mV p-p Differential Input, Internally AC-Coupled into 1500 $\Omega$ Impedance                         |
| 16     | BIAS_RESISTOR             | Resistor to Ground Sets Overall Bias Current and Power Consumption                                                               | 39 k $\Omega$ Resistor Connected to Ground                                                                |
| 17     | VOLTAGE_REFERENCE_IN      | ADC Voltage Reference Input                                                                                                      | Regulated and Filtered 1.0 V $\pm$ 5% Input                                                               |
| 18     | AGND                      | Analog Ground                                                                                                                    | Pin Connected to Ground                                                                                   |
| 19     | IF_INPUT                  | IF Input                                                                                                                         | Typically 16.4 $\mu$ V p-p to 65.2 mV p-p                                                                 |
| 20     | AVDD                      | Analog Power Supply Input                                                                                                        | Pin Connected to Analog Supply                                                                            |

# Typical Performance Characteristics—AD6140

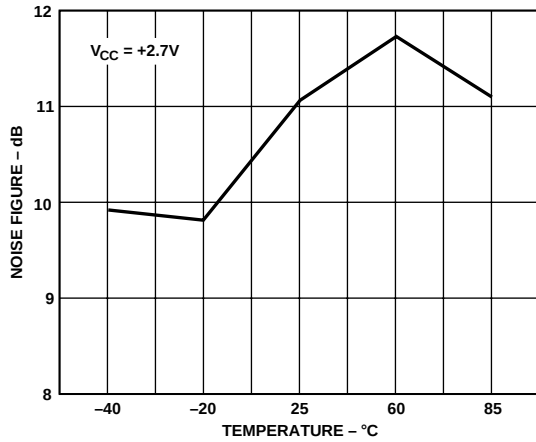


Figure 1. Noise Figure vs. Temperature

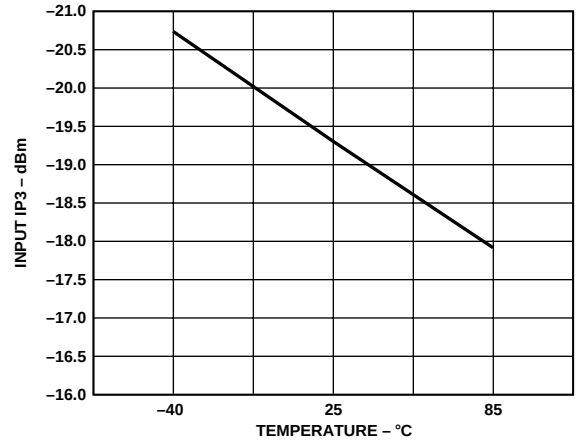


Figure 4. Input IP3 vs. Temperature

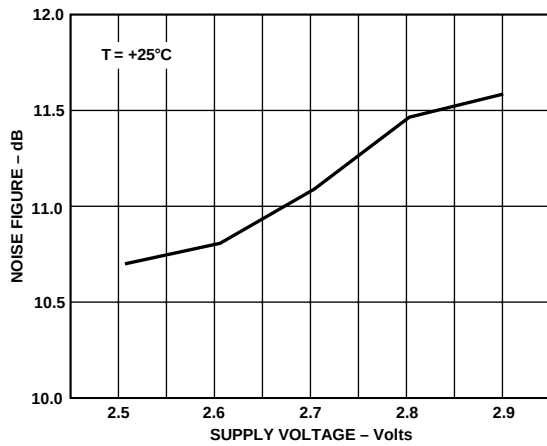


Figure 2. Noise Figure vs. Power Supply

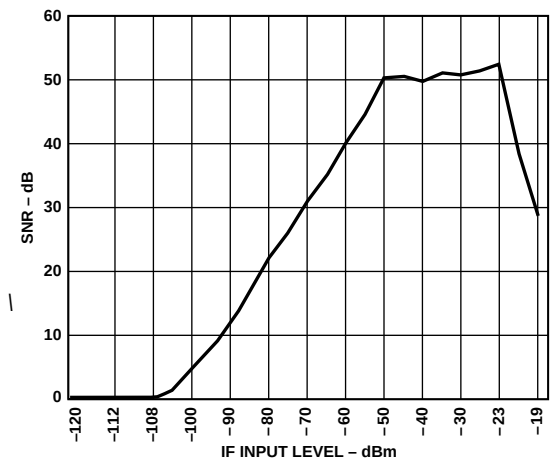


Figure 5. Signal to Noise Ratio vs. IF Input Level at  $T_A = +25^\circ\text{C}$

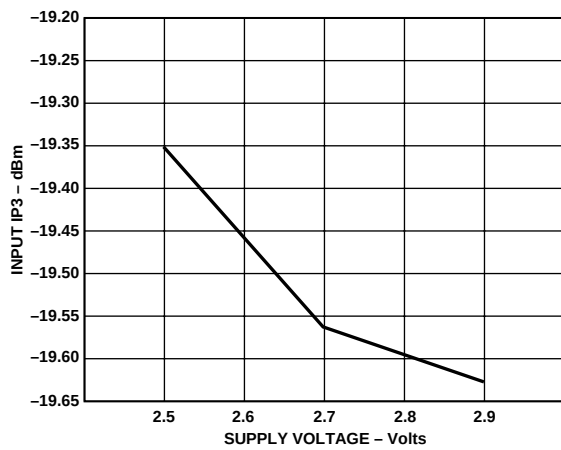


Figure 3. Input IP3 vs. Power Supply

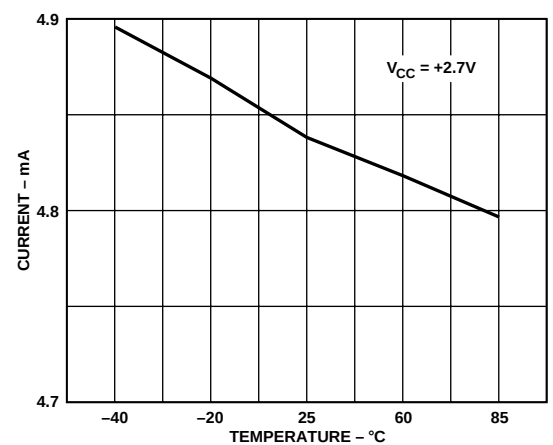


Figure 6. Supply Current vs. Temperature

# AD6140

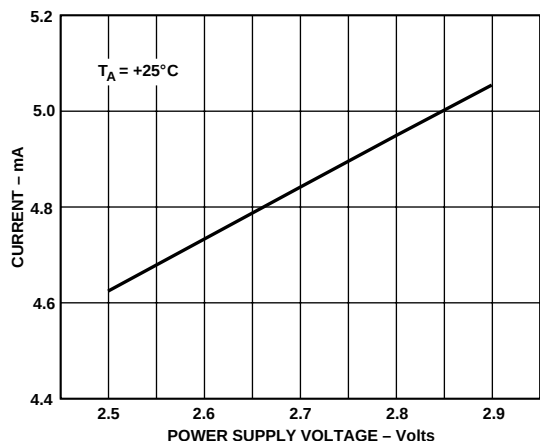


Figure 7. Supply Current vs. Power Supply Voltage

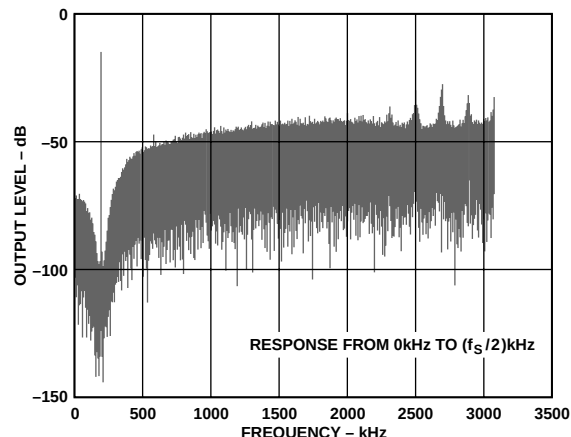


Figure 9. Output Spectrum of AD6140

## ΣΔ MODULATION

A ΣΔ modulator uses feedback around a low noise quantizer (1 bit in this case) in order to “shape” the spectrum of quantization noise. Using this technique, we can shape noise away from an arbitrary passband, within which we can place a modulated signal. A ΣΔ modulator reproduces the input, but adds quantization noise, which can be digitally removed with a filter, known as a decimation filter. Applying this technique to bandpass signals results in an analog-to-digital converter suitable for converting the IF signals in a digital radio.

The output of the AD6140’s ΣΔ modulator is shown in Figure 9. As can be seen, the noise is shaped away from a narrow bandwidth, within which we place a signal (a sine wave in this case) resulting in a narrowband, high dynamic range digital representation of the analog input.

## PRODUCT OVERVIEW

The AD6140 is a bandpass ΣΔ analog-to-digital converter IC for dual conversion receivers requiring a high dynamic range and multiple filter bandwidths. It consists of a variable gain, low noise preamplifier, mixer, automatic gain control (AGC) detector, bandpass ΣΔ modulator, an ECL to CMOS level translator and an auxiliary amplifier for use in biasing a discrete LNA.

The low noise preamplifier accepts a first IF input at 49.6 MHz from 16.4 μV p-p to 63.2 mV p-p. It provides a variable gain from 12 dB to 25 dB.

The mixer accepts an LO frequency of 49.792 MHz or 49.408 MHz, resulting in an IF frequency of 192 kHz. The LO level should be 200 mV p-p differential. It is ac-coupled to the AD6140. The mixer operates in the linear region, hence the gain of the mixer is a function of the LO level. As a result, special care must be taken to ensure that the LO level is 200 mV p-p,

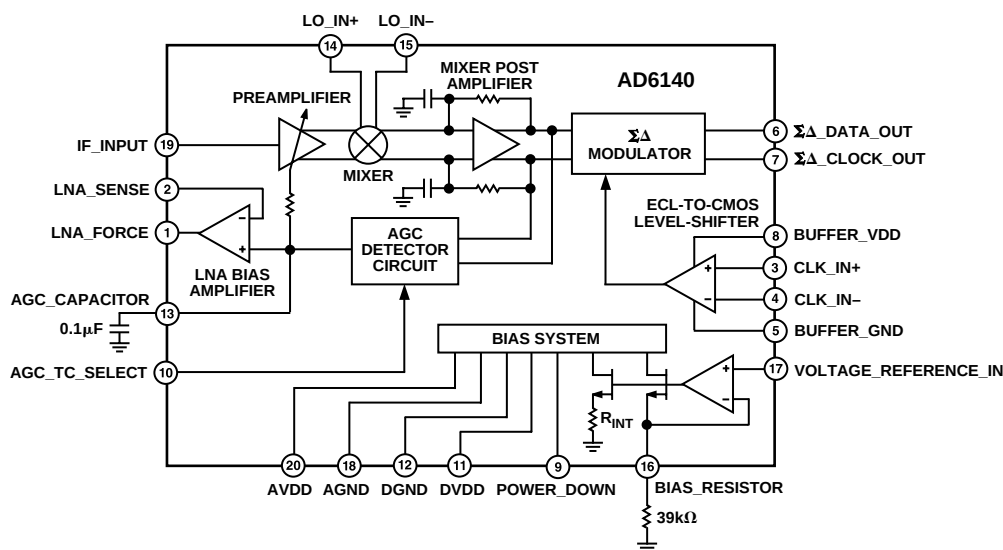


Figure 8. Functional Block Diagram

otherwise, the expected gain will not be obtained from the AD6140. In addition to the mixer, there is a mixer post-amplifier within the AD6140. The total gain from the mixer and mixer post-amplifier is 5 dB.

The  $\Sigma\Delta$  modulator uses a 6.144 MHz clock, which is a differential ECL input. There is an ECL-to-CMOS converter on the AD6140, which converts this differential ECL input into a single-ended CMOS signal. This 6.144 MHz single-ended CMOS clock is provided at Pin 7 ( $\Sigma\Delta\_CLOCK\_OUT$ ). The output data of the AD6140 is a 6.144 MHz single bitstream at Pin 6 ( $\Sigma\Delta\_DATA\_OUT$ ). The signal gain through the  $\Sigma\Delta$  modulator is -0.77 dB.

Within the  $\Sigma\Delta$  modulator, the data output digital bitstream is fed through a 1-bit D/A converter and is fed back to numerous internal points. The level of this feedback signal, known as the full-scale level, defines the  $\Sigma\Delta$  modulator input signal level, which would result in the output digital bitstream containing the maximum number of ones possible. This condition, known as maximum ones density, represents the maximum in-band output signal power of the  $\Sigma\Delta$  modulator. The full-scale level is set to 2 V p-p or -4.77 dBm (relative to 1500  $\Omega$ ). However, if a signal into the modulator is -4.77 dBm, the modulator will enter an unstable state. Consequently, the maximum input to the modulator is constrained to 5 dB less than the signal, which would produce maximum ones density. This level, defined as the clip level, is -9.77 dBm (relative to 1500  $\Omega$ ).

The maximum signal into the modulator does not correspond to maximum ones density. The entire dynamic range of the resulting analog to digital converter ( $\Sigma\Delta$  modulator plus decimation filter) is not realized. In order to relate the maximum signal into the modulator to the maximum signal out of the modulator, a gain of 5 dB should be applied in the decimation filter.

As can be seen in Figure 5, the output signal to noise ratio will increase until a point at which it rapidly degrades. This point represents the input signal level where the  $\Sigma\Delta$  modulator has become unstable. As a result, the maximum input signal level is constrained by the point at which it is so high that instability occurs in the modulator. Dynamic range is defined as the difference between the integrated noise floor (within a particular bandwidth) and the power in the output signal just before the  $\Sigma\Delta$  modulator has become unstable. For a typical 6.25 kHz bandwidth centered around 192 kHz, the AD6140 has 83 dB of dynamic range.

In order to increase the range of useful input signals of the AD6140, an AGC detector is employed which senses the input signal level to the  $\Sigma\Delta$  modulator and adjusts the gain in the preamplifier. The AGC circuitry provides 13 dB of automatic gain control range. The AGC operates when the internal AGC voltage is between 700 mV (minimum gain) and 1.55 V (maximum gain). This voltage can be measured on the AGC\_CAPACITOR pin (Pin 13).

The AD6140 can be configured with the chip powered up or down. In order to power the chip down, set pin POWER\_DOWN (Pin 9) high. In order to power it up, set pin POWER\_DOWN (Pin 9) low.

Finally, an auxiliary amplifier used for biasing an external discrete LNA is provided with the AD6140.

## FREQUENCY PLAN

The AD6140 and its  $\Sigma\Delta$  modulator are designed for a specific frequency plan: a 6.144 MHz master clock, a 49.6 MHz first IF input, and a 192 kHz center frequency in the bandpass  $\Sigma\Delta$  modulator. The local oscillator may use high-side or low-side injection. The specifications for the AD6140 are only valid for this frequency plan. Any deviation from this frequency plan may result in degradation of the specified performance. Furthermore, there are only specific frequency plans which will result in acceptable performance for most applications. To avoid problems, do not change the frequency plan.

## USING THE AD6140

In this section, we will examine a few areas of special importance and include a few general applications tips. As is true of any device operating in the IF frequency range, special care must be taken in PC board layout. The location of the particular grounding points must be considered, with the objective of minimizing any unwanted signal coupling. Specifically, care should be taken in the layout of the IF and LO signal paths as well as the data and clock digital bit-streams. Layout of these portions of the PC board require special attention in order to ensure that the high frequency portions of these signals do not couple into other signals in the system. In order to maintain balance in differential signal levels, be sure to keep short and equal length transmission lines.

The power supplies should be decoupled to ensure a clean dc signal. Special care should be taken with respect to ensuring that the BUFFER\_VDD is especially clean and at the appropriate levels since the output in-band noise floor is particularly sensitive to this supply.

The IF input signal should be impedance matched and ac coupled. The impedance looking into the IF input pin is typically a 2.5 k $\Omega$  resistance in parallel with a 12 pF capacitance. The 1 V reference signal should be regulated and filtered.

The value of the BIAS\_RESISTOR (Pin 16) is 39 k $\Omega$ . The bias resistor sets the current consumption of the AD6140. Because the AD6140 was characterized with a 39 k $\Omega$  bias resistor, this is the only value for which the AD6140 specifications are guaranteed. Maximum current consumption is measured when the AD6140 is operating at maximum gain.

The AGC integration capacitor should be large enough to bypass any externally-generated noise on the internal AGC line to ground in addition to providing a path for the charging and discharging of the AGC current. In the Motorola ReFLEX chipset solution, this capacitor is 0.1  $\mu$ F. The AGC time constant is switch-selectable with the AGC\_TC\_SELECT pin (Pin 10). The AGC time constant has a typical current ratio of 56:1 when in the fast mode relative to slow mode. The nominal AGC current in the fast (high current) position is 2.8  $\mu$ A and in the slow (low current) position is 50 nA. The AGC time constant may be calculated from Equation 1.

$$T = \frac{CV}{I} \quad (1)$$

where  $T$  is the AGC time constant in seconds,  $C$  is the value of the AGC capacitor in Farads,  $V$  is the full-scale change in the AGC voltage, and  $I$  is the charging current in amperes.

# AD6140

## LEVEL DIAGRAM

Figure 10 shows a simplified block diagram of the AD6140 with the expected signal levels for the minimum gain configuration.

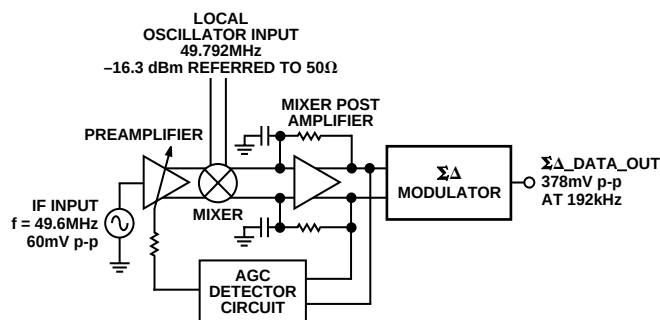


Figure 10. Level Diagram

## Motorola ReFLEX Transceiver

Figure 11 shows a block diagram of the Motorola ReFLEX chipset solution including the AD6140. As can be seen, the AD6140 accepts an IF input from a crystal filter at 49.6 MHz. The frequency synthesizer provides the 6.144 MHz clock, while the LO is also generated from the frequency synthesizer but is fed to the AD6140 via the I/Q modulator. The IF data output and the clock output both feed into the IF data processor. The LNA bias amplifier provides the AGC voltage for the first LNA in the receive path. The dc power is supplied from the power management chip.

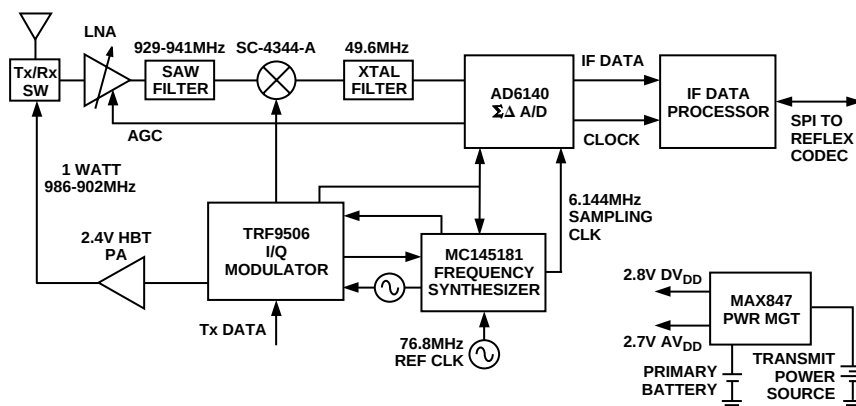


Figure 11. ReFLEX Transceiver Block Diagram

## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

### 20-Lead SSOP (RS-20)

