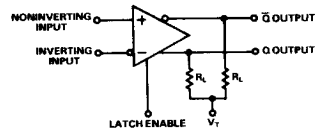
AD9685/AD9687

FEATURES
2.7ns Propagation Delay
0.5ns Latch Setup Time
90dB CMRR
+5V, −5.2V Supply Voltages

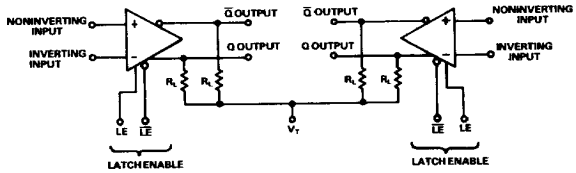
APPLICATIONS
High-Speed Triggers
High-Speed Line Receivers
Peak Detectors
Threshold Detectors

AD9685/AD9687 FUNCTIONAL BLOCK DIAGRAMS



THE OUTPUTS ARE OPEN EMITTERS, REQUIRING EXTERNAL PULL-DOWN RESISTORS. THESE RESISTORS MAY BE IN THE RANGE OF 50Ω–200Ω CONNECTED TO −2.0V; OR 200Ω–2000Ω CONNECTED TO −5.2V.

AD9685



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AD9687

GENERAL DESCRIPTION

The AD9685 and the AD9687 are high-speed voltage comparators. The AD9685 and the AD9687 are manufactured in a high performance bipolar process which allows improved speed and dc accuracy. The AD9685 is a single comparator with a 2.7ns propagation delay, and the AD9687 is a dual comparator of equal performance.

Both devices employ a high precision differential input stage with a common-mode range of ±2.5V. The AD9685 and the AD9687 provide complementary digital outputs which are fully ECL compatible. The output stage is capable of driving 50Ω terminated transmission lines given the 30mA output drive capacity. In addition to this, a latch enable input is provided, allowing operation in either a sample-hold mode or a track-hold mode.

The AD9685 and the AD9687 are both available as an industrial grade device, −25°C to +85°C, and as an extended temperature range device, −55°C to +125°C. The AD9685 is available in a 10-pin TO-100 metal can, or a 16-pin ceramic package. The AD9687 is available in a 16-pin ceramic package.

ORDERING INFORMATION

Device	Type	Temperature Range	Description	Package Options*
AD9685BD	Single	−25°C to +85°C	16-Pin DIP, Industrial	D-16
AD9685BH	Single	−25°C to +85°C	10-Pin Can, Industrial	H-10A
AD9685TD	Single	−55°C to +125°C	16-Pin DIP, Extended Temperature	D-16
AD9685TH	Single	−55°C to +125°C	10-Pin Can, Extended Temperature	H-10A
AD9687BD	Dual	−25°C to +85°C	16-Pin DIP, Industrial	D-16
AD9687TD	Dual	−55°C to +125°C	16-Pin DIP, Extended Temperature	D-16

*See Section 16 for package outline information.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Positive Supply Voltage ($+V_S$) . . . . . +6V
Negative Supply Voltage ($-V_S$) . . . . . −6V
Input Voltage . . . . . ±5V
Differential Input Voltage 5.5V
Latch Enable Voltage . . . . . $-V_S$ to 0V
Output Current 30mA
Power Dissipation AD9685 . . . . . 500mW
AD9687 . . . . . 600mW

Operating Temperature Range[2]
AD9685/87/BD/BH . . . . . −25°C to +85°C
AD9685/87/TD/TH . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −55°C to +150°C
Junction Temperature . . . . . +175°C
Lead Soldering Temperature (10sec) . . . . . +300°C

ELECTRICAL CHARACTERISTICS (Positive Supply Voltage = +5.0V; Negative Supply Voltage = −5.2V, unless otherwise stated)

		Industrial Temp. Range −25°C to +85°C						Military Temp. Range −55°C to +125°C						
		AD9685BD/BH			AD9687BD			AD9685TD/TH			AD9687TD			
Parameter	Temp	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
INPUT CHARACTERISTICS														
Input Offset Voltage[3]	+25°C		1	5		1	5		1	5		1	5	mV
	Full			7			7			7			7	mV
Input Offset Drift	Full		20			20			20			20		µV/°C
Input Bias Current	+25°C		3	15		3	15		3	15		3	15	µA
	Full			20			20			20			20	µA
Input Offset Current	+25°C		0.5	3		0.5	3		0.5	3		0.5	3	µA
	Full			5			5			5			5	µA
Input Resistance	+25°C		200			200			200			200		kΩ
Input Capacitance	+25°C		3			3			3			3		pF
Input Voltage Range	Full	−2.5		+2.5	−2.5		+2.5	−2.5		+2.5	−2.5		+2.5	V
Common-Mode Rejection Ratio	Full	75	90		75	90		80	90		80	90		dB
ENABLE INPUT														
Logic "1" Voltage	Full	−1.1			−1.1			−1.1			−1.1			V
Logic "0" Voltage	Full			−1.5			−1.5			−1.5			−1.5	V
Logic "1" Current	Full			60			60			60			60	µA
Logic "0" Current	Full			5			5			5			5	µA
DIGITAL OUTPUTS[4]														
Logic "1" Voltage	Full	−1.1			−1.1			−1.1			−1.1			V
Logic "0" Voltage	Full			−1.5			−1.5			−1.5			−1.5	V
SWITCHING PERFORMANCE[4]														
Propagation Delays[5]														
Input to Output HIGH	+25°C		2.7	3.0		2.7	4.0		2.7	3.0		2.7	4.0	ns
Input to Output LOW	+25°C		2.7	3.0		2.7	4.0		2.7	3.0		2.7	4.0	ns
Latch Enable to Output HIGH	+25°C		2.7	3.0		2.7	4.0		2.7	3.0		2.7	4.0	ns
Latch Enable to Output LOW	+25°C		2.7	3.0		2.7	4.0		2.7	3.0		2.7	4.0	ns
Latch Enable														
Minimum Pulse Width	+25°C		2.0	3.0		2.0	3.0		2.0	3.0		2.0	3.0	ns
Minimum Setup Time	+25°C		0.5	1.0		0.5	1.0		0.5	1.0		0.5	1.0	ns
Minimum Hold Time	+25°C		0.5	1.0		0.5	1.0		0.5	1.0		0.5	1.0	ns
POWER SUPPLY[6]														
Positive Supply Current (+5.0V)	Full		16	23		31	42		16	23		31	42	mA
Negative Supply Current (−5.2V)	Full		30	34		67	75		30	34		67	75	mA
Power Supply Rejection Ratio[7]	Full		60			60			60			60		dB

NOTES

[1]Absolute maximum ratings are limiting values, to be applied individually, and beyond which serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Typical thermal impedances . . .
AD9685 Metal Can $\theta_{ja} = 172°C/W$; $\theta_{jc} = 52°C/W$
AD9685 Ceramic $\theta_{ja} = 115°C/W$; $\theta_{jc} = 57°C/W$
AD9687 Ceramic $\theta_{ja} = 102°C/W$; $\theta_{jc} = 45°C/W$

[3]$R_S = 100\Omega$.

[4]Outputs terminated through 50Ω to −2.0V.

[5]Propagation delays measured with 100mV pulse; 5mV overdrive.

[6]Supply voltages should remain stable within ±5% for normal operation.

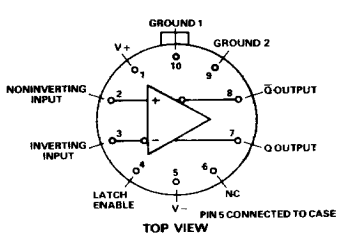
[7]Measured at ±5% of $+V_S$ and $-V_S$.

Specifications subject to change without notice.

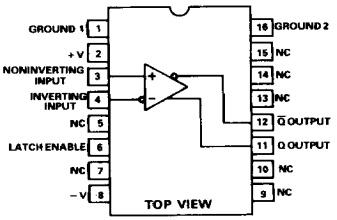
FUNCTIONAL DESCRIPTION

PIN NAME	DESCRIPTION
$+V_S$	– Positive supply terminal, nominally +5.0V.
NONINVERTING INPUT	– Noninverting analog input of the differential input stage. The NONINVERTING INPUT must be driven in conjunction with the INVERTING INPUT.
INVERTING INPUT	– Inverting analog input of the differential input stage. The INVERTING INPUT must be driven in conjunction with the NONINVERTING INPUT.
LATCH ENABLE	– In the "compare" mode (logic HIGH), the output will track changes at the input of the comparator. In the "latch" mode (logic LOW), the output will reflect the input state just prior to the comparator being placed in the "latch" mode. $\overline{\text{LATCH ENABLE}}$ must be driven in conjunction with LATCH ENABLE for the AD9687.
$\overline{\text{LATCH ENABLE}}$	– In the "compare" mode (logic LOW), the output will track changes at the input of the comparator. In the "latch" mode (logic HIGH), the output will reflect the input state just prior to the comparator being placed in the "latch" mode. $\overline{\text{LATCH ENABLE}}$ must be drive in conjunction with LATCH ENABLE for the AD9687.
$-V_S$	– Negative supply terminal, nominally −5.2V.
Q	– One of two complementary outputs, Q will be at logic HIGH, if the analog voltage at the NONINVERTING INPUT is greater than the analog voltage at the INVERTING INPUT (provided the comparator is in the "compare" mode). See LATCH ENABLE and $\overline{\text{LATCH ENABLE}}$ (AD9687 only) for additional information.
$\overline{Q}$	– One of two complementary outputs. $\overline{Q}$ will be at logic LOW, if the analog voltage at the NONINVERTING INPUT is greater than the analog voltage at the INVERTING INPUT (provided the comparator is in the "compare" mode). See LATCH ENABLE and $\overline{\text{LATCH ENABLE}}$ (AD9687 only) for additional information.
GROUND 1	– One of two grounds, but primarily associated with the digital ground. Both grounds should be connected together near the comparator.
GROUND 2	– One of two grounds, but primarily associated with the analog ground. Both grounds should be connected together near the comparator.

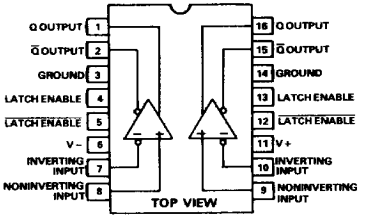
Pin Configuration



AD9685BH

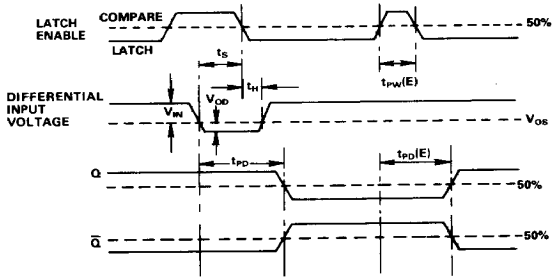


AD9685BD



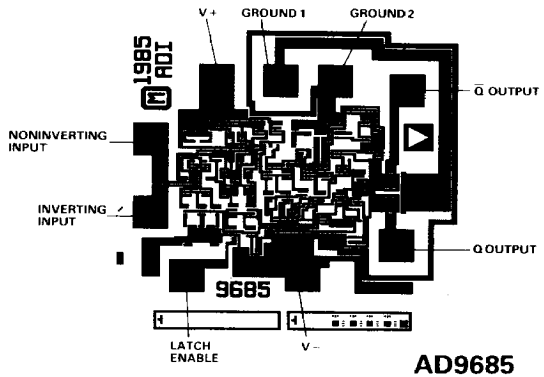
AD9687BD

SYSTEM TIMING DIAGRAM

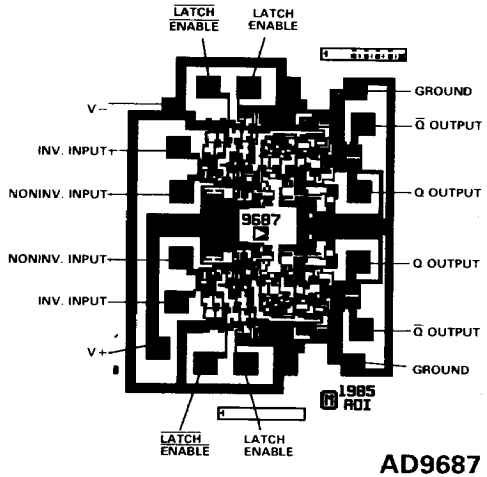


t_S	– Minimum Setup Time
t_H	– Minimum Hold Time
t_{PD}	– Input-to-Output Delay
$t_{PD}(E)$	– LATCH ENABLE to Output Delay
$t_{PW}(E)$	– Minimum LATCH ENABLE Pulse Width
V_{OS}	– Input Offset Voltage
V_{OD}	– Overdrive Voltage

DIE LAYOUT AND MECHANICAL INFORMATION



AD9685



AD9687

Die Dimensions	AD9685	54 × 50 × 15 (± 2) mils
	AD9687	84 × 62 × 15 (± 2) mils
Pad Dimensions		4 × 4 mils
Metalization		10,000Å, Aluminum
Backing		None
Substrate Potential		$-V_S$
Passivation		10,000Å, Nitride
Die Attach		Gold Eutectic
Bond Wire		1.25 mil, Aluminum, Ultrasonic Bonding or 1 mil, Gold, Gold Ball Bonding