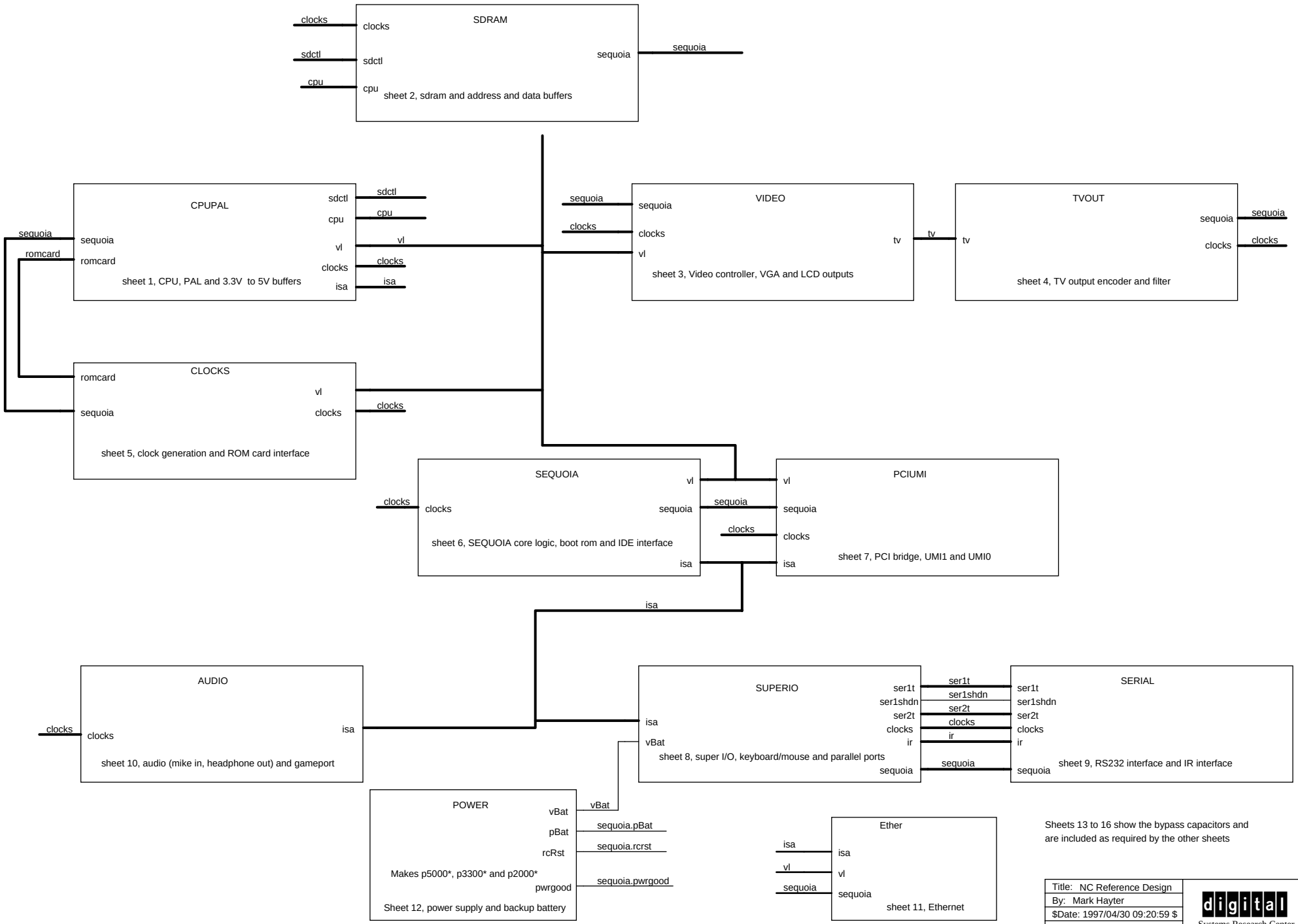
SDRAM
clocks
sdctl
cpu
sequoia
sheet 2, sdram and address and data buffers
CPUPAL
sequoia
romcard
vl
clocks
isa
sheet 1, CPU, PAL and 3.3V to 5V buffers
VIDEO
tv
sheet 3, Video controller, VGA and LCD outputs
TVOUT
sheet 4, TV output encoder and filter
CLOCKS
sheet 5, clock generation and ROM card interface
SEQUOIA
sheet 6, SEQUOIA core logic, boot rom and IDE interface
PCIUMI
sheet 7, PCI bridge, UMI1 and UMI0
AUDIO
sheet 10, audio (mike in, headphone out) and gameport
SUPERIO
vBat
ser1t
ser1shdn
ser2t
ir
sheet 8, super I/O, keyboard/mouse and parallel ports
SERIAL
sheet 9, RS232 interface and IR interface
POWER
pBat
rcRst
pwrgood
Makes p5000*, p3300* and p2000*
Sheet 12, power supply and backup battery
Ether
sheet 11, Ethernet
Sheets 13 to 16 show the bypass capacitors and are included as required by the other sheets
Title: NC Reference Design
By: Mark Hayter
$Date: 1997/04/30 09:20:59 $
RCS $Revision: 1.19 $
Version: Rev 4
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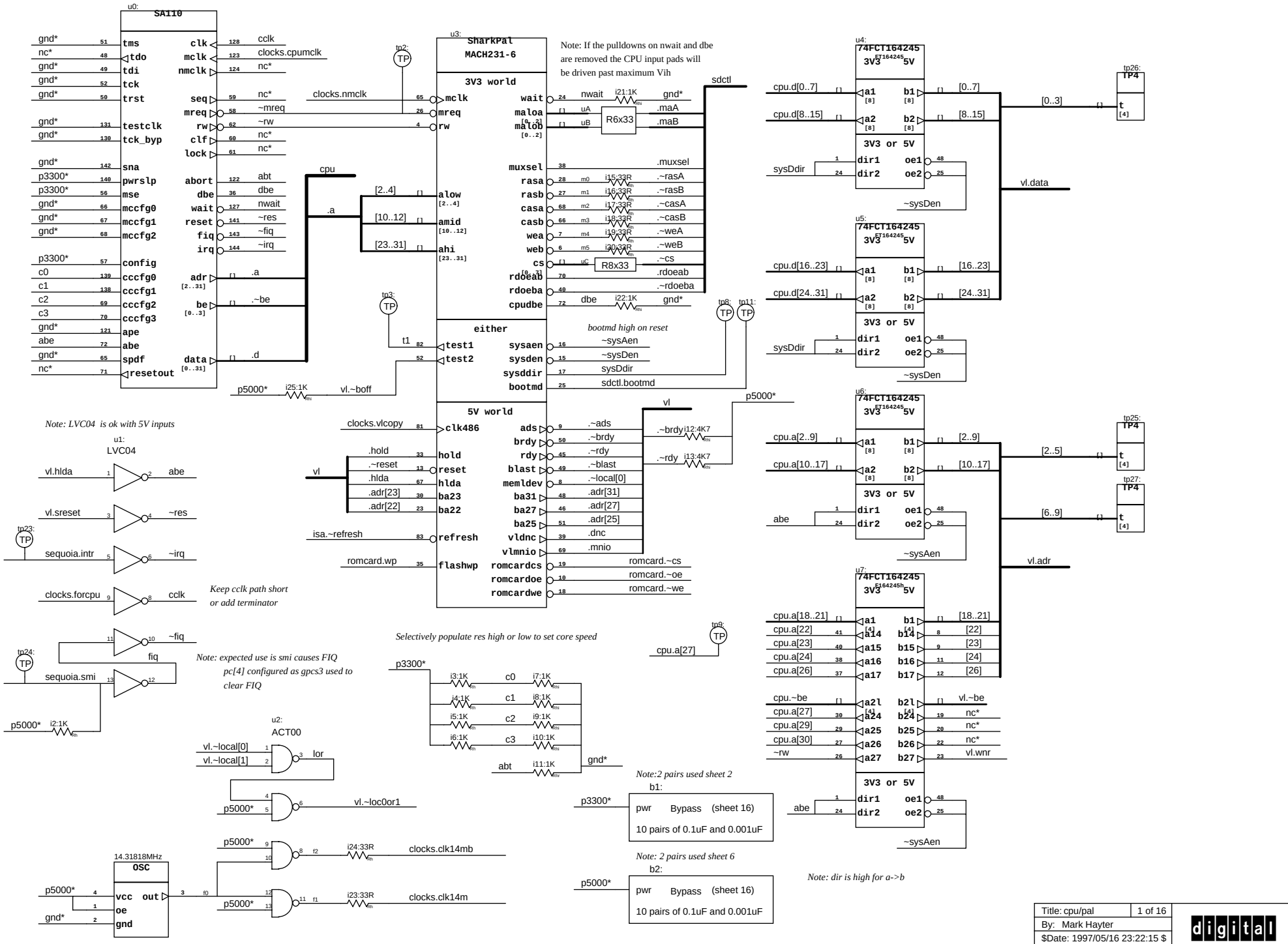
Systems Research Center
Palo Alto, CA


u0:
SA110
u3:
SharkPal
MACH231-6
3V3 world
either
5V world
Note: If the pulldowns on nwait and dbe are removed the CPU input pads will be driven past maximum Vih
bootmd high on reset
u4:
74FCT164245
3V3 or 5V
u5:
u6:
u7:
vl.data
vl.adr
Note: LVC04 is ok with 5V inputs
u1:
LVC04
Keep cclk path short or add terminator
Selectively populate res high or low to set core speed
Note: expected use is smi causes FIQ
pc[4] configured as gpcs3 used to clear FIQ
u2:
ACT00
14.31818MHz
OSC
Note:2 pairs used sheet 2
b1:
pwr Bypass (sheet 16)
10 pairs of 0.1uF and 0.001uF
Note: 2 pairs used sheet 6
b2:
Note: dir is high for a->b
Title: cpu/pal
1 of 16
By: Mark Hayter
$Date: 1997/05/16 23:22:15 $
RCS $Revision: 1.36 $
Version: Rev 4
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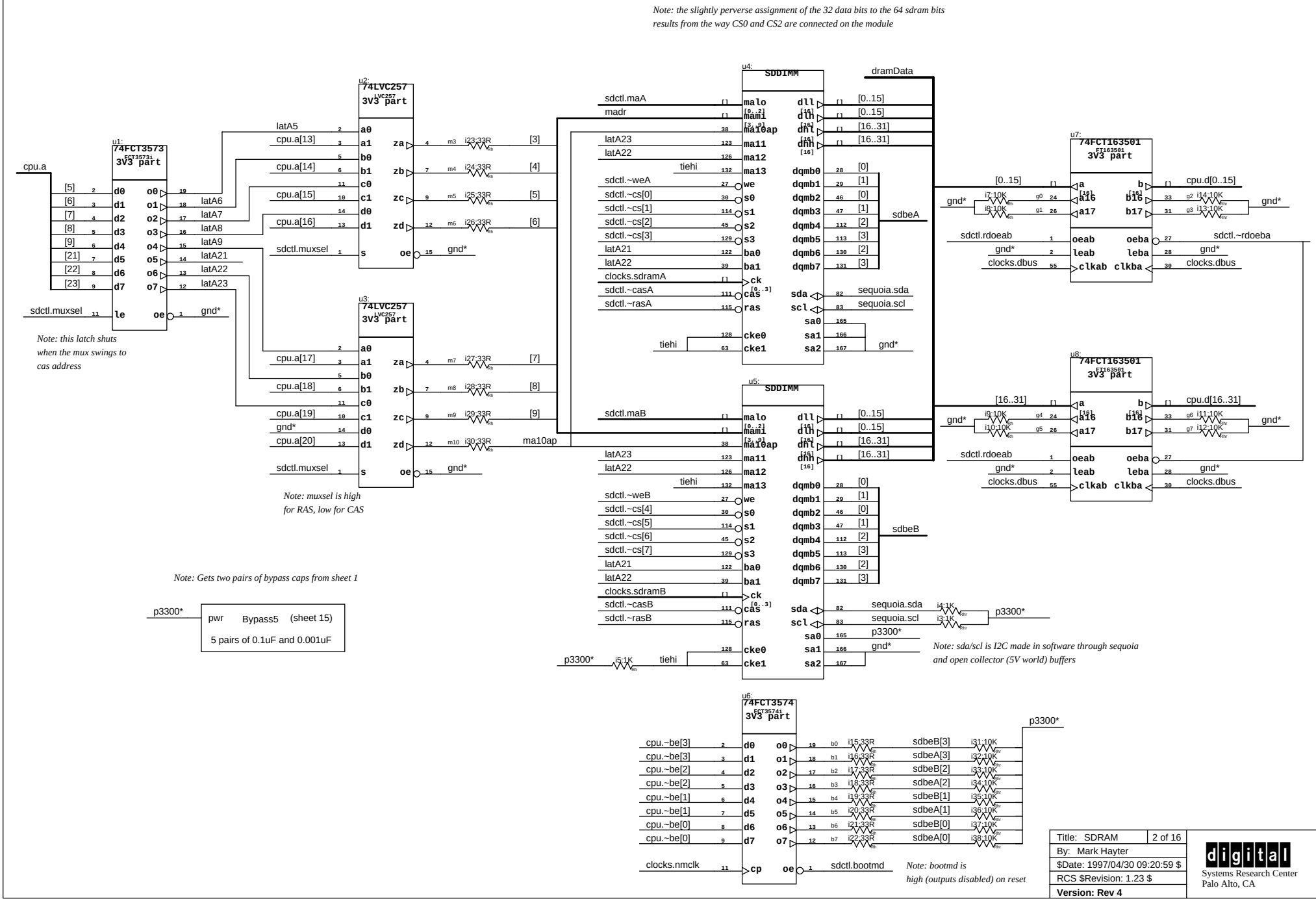
Note: the slightly perverse assignment of the 32 data bits to the 64 sdram bits results from the way CS0 and CS2 are connected on the module
u1: 74FCT3573 3V3 part
u2: 74LVC257 3V3 part
u3: 74LVC257 3V3 part
u4: SDDIMM
u5: SDDIMM
u6: 74FCT3574 3V3 part
u7: 74FCT163501 3V3 part
u8: 74FCT163501 3V3 part
dramData
cpu.a
latA5
latA6
latA7
latA8
latA9
latA21
latA22
latA23
sdctl.muxsel
gnd*
Note: this latch shuts when the mux swings to cas address
Note: muxsel is high for RAS, low for CAS
ma10ap
sdctl.maA
sdctl.maB
madr
sdctl.~weA
sdctl.~weB
sdctl.~cs[0]
sdctl.~cs[1]
sdctl.~cs[2]
sdctl.~cs[3]
sdctl.~cs[4]
sdctl.~cs[5]
sdctl.~cs[6]
sdctl.~cs[7]
sdctl.~casA
sdctl.~casB
sdctl.~rasA
sdctl.~rasB
clocks.sdramA
clocks.sdramB
sdbeA
sdbeB
sequoia.sda
sequoia.scl
Note: sda/scl is I2C made in software through sequoia and open collector (5V world) buffers
Note: Gets two pairs of bypass caps from sheet 1
p3300*
pwr Bypass5 (sheet 15)
5 pairs of 0.1uF and 0.001uF
cpu.~be[3]
cpu.~be[2]
cpu.~be[1]
cpu.~be[0]
clocks.nmclk
sdctl.bootmd
Note: bootmd is high (outputs disabled) on reset
cpu.d[0..15]
cpu.d[16..31]
sdctl.rdoeab
sdctl.~rdoeba
Title: SDRAM
2 of 16
By: Mark Hayter
$Date: 1997/04/30 09:20:59 $
RCS $Revision: 1.23 $
Version: Rev 4
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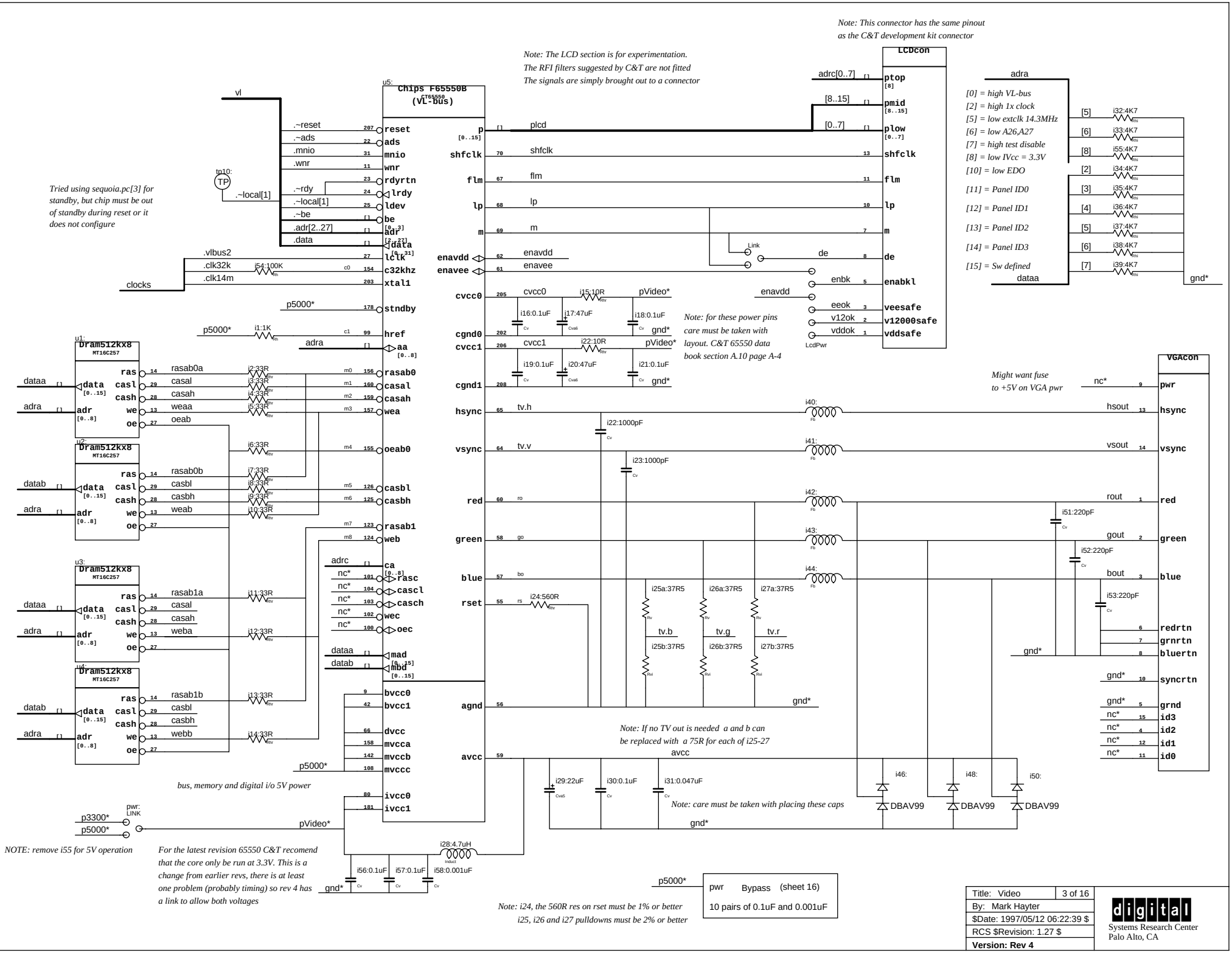
Palo Alto, CA


Note: This connector has the same pinout as the C&T development kit connector
Note: The LCD section is for experimentation.
The RFI filters suggested by C&T are not fitted
The signals are simply brought out to a connector
LCDcon
adrc[0..7]
[8..15]
[0..7]
ptop
pmid
plow
adra
[0] = high VL-bus
[2] = high 1x clock
[5] = low extclk 14.3MHz
[6] = low A26,A27
[7] = high test disable
[8] = low IVcc = 3.3V
[10] = low EDO
[11] = Panel ID0
[12] = Panel ID1
[13] = Panel ID2
[14] = Panel ID3
[15] = Sw defined
dataa
gnd*
Tried using sequoia.pc[3] for standby, but chip must be out of standby during reset or it does not configure
u5:
Chips F65550B
(VL-bus)
LT65550
vl
tp10:
TP
.~local[1]
.~reset
.~ads
.mnio
.wnr
.~rdy
.~local[1]
.~be
.adr[2..27]
.data
reset
ads
mnio
wnr
rdyrtn
lrdy
ldev
be
adr
data
lclk
.vlbus2
.clk32k
.clk14m
clocks
i54:100K
c32khz
xtal1
p5000*
stndby
i1:1K
href
adra
aa
u1:
u2:
u3:
u4:
Dram512kx8
MT16C257
ras
casl
cash
we
oe
data
adr
dataa
datab
rasab0a
casal
casah
weaa
oeab
rasab0
casal
casah
wea
oeab0
rasab0b
casbl
casbh
weab
casbl
casbh
rasab1
web
rasab1a
weba
rasab1b
webb
adrc
nc*
rasc
cascl
casch
wec
oec
mad
mbd
bvcc0
bvcc1
dvcc
mvcca
mvccb
mvccc
ivcc0
ivcc1
p
shfclk
flm
lp
m
enavdd
enavee
cvcc0
cvcc1
cgnd0
cgnd1
hsync
vsync
red
green
blue
rset
agnd
avcc
plcd
Link
de
enbk
eeok
v12ok
vddok
LcdPwr
enabkl
veesafe
v12000safe
vddsafe
pVideo*
i15:10R
i22:10R
i16:0.1uF
i17:47uF
i18:0.1uF
i19:0.1uF
i20:47uF
i21:0.1uF
Note: for these power pins care must be taken with layout. C&T 65550 data book section A.10 page A-4
tv.h
tv.v
i22:1000pF
i23:1000pF
ro
go
bo
rs
i24:560R
i25a:37R5
i26a:37R5
i27a:37R5
tv.b
tv.g
tv.r
i25b:37R5
i26b:37R5
i27b:37R5
Note: If no TV out is needed a and b can be replaced with a 75R for each of i25-27
i29:22uF
i30:0.1uF
i31:0.047uF
Note: care must be taken with placing these caps
i40:
i41:
i42:
i43:
i44:
i46:
i48:
i50:
DBAV99
VGAcon
Might want fuse to +5V on VGA pwr
nc*
pwr
hsout
hsync
vsout
vsync
rout
red
gout
green
bout
blue
redrtn
grnrtn
bluertn
syncrtn
grnd
id3
id2
id1
id0
i51:220pF
i52:220pF
i53:220pF
bus, memory and digital i/o 5V power
p3300*
p5000*
pwr:
LINK
NOTE: remove i55 for 5V operation
For the latest revision 65550 C&T recomend that the core only be run at 3.3V. This is a change from earlier revs, there is at least one problem (probably timing) so rev 4 has a link to allow both voltages
i28:4.7uH
i56:0.1uF
i57:0.1uF
i58:0.001uF
Note: i24, the 560R res on rset must be 1% or better
i25, i26 and i27 pulldowns must be 2% or better
pwr Bypass (sheet 16)
10 pairs of 0.1uF and 0.001uF
Title: Video
3 of 16
By: Mark Hayter
$Date: 1997/05/12 06:22:39 $
RCS $Revision: 1.27 $
Version: Rev 4
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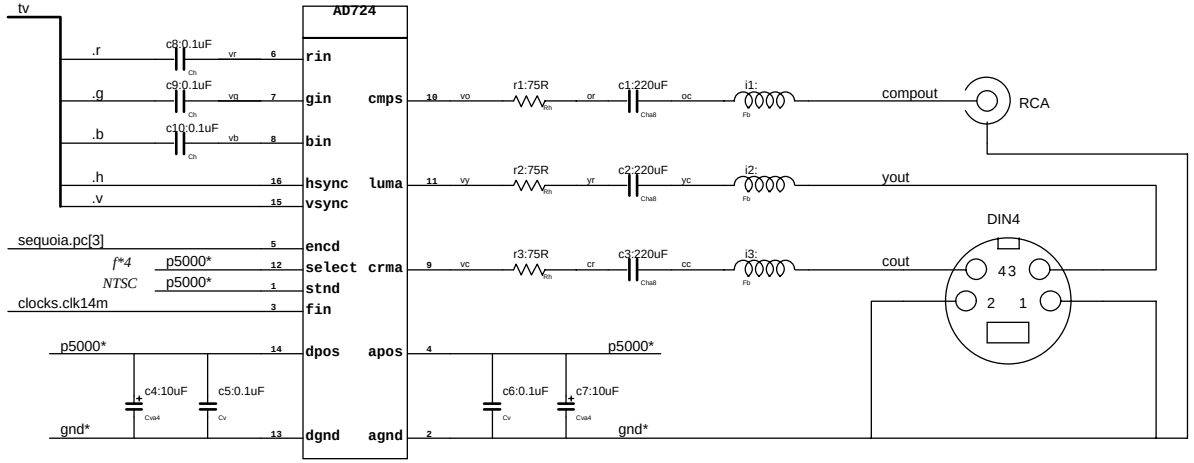
Palo Alto, CA



Title: TV out	4 of 16
By: Mark Hayter	
$Date: 1997/04/30 09:20:59 $	
RCS $Revision: 1.10 $	
Version: Rev 4	

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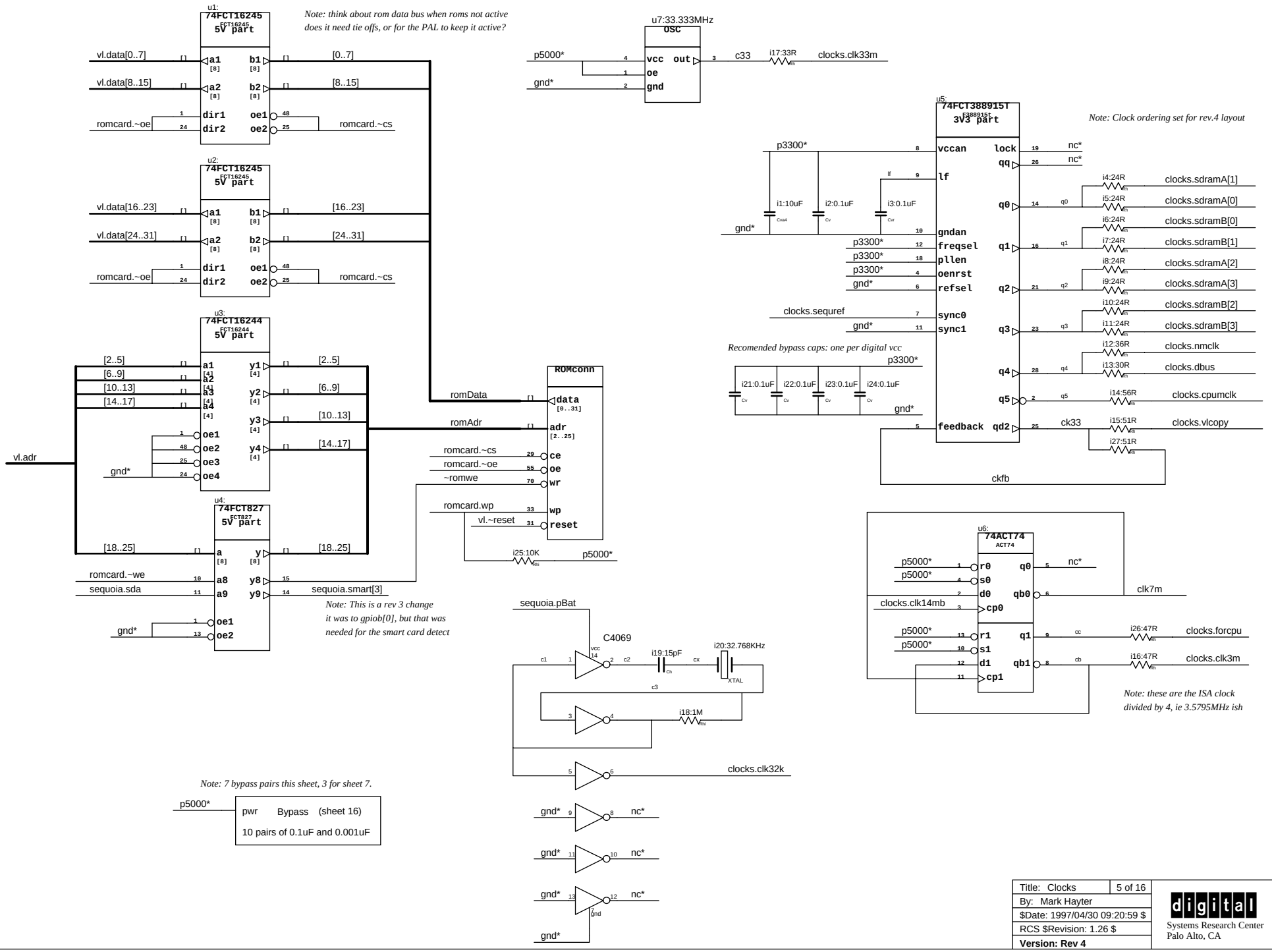
Systems Research Center
Palo Alto, CA



Title: Clocks	5 of 16
By: Mark Hayter	
$Date: 1997/04/30 09:20:59 $	
RCS $Revision: 1.26 $	
Version: Rev 4	

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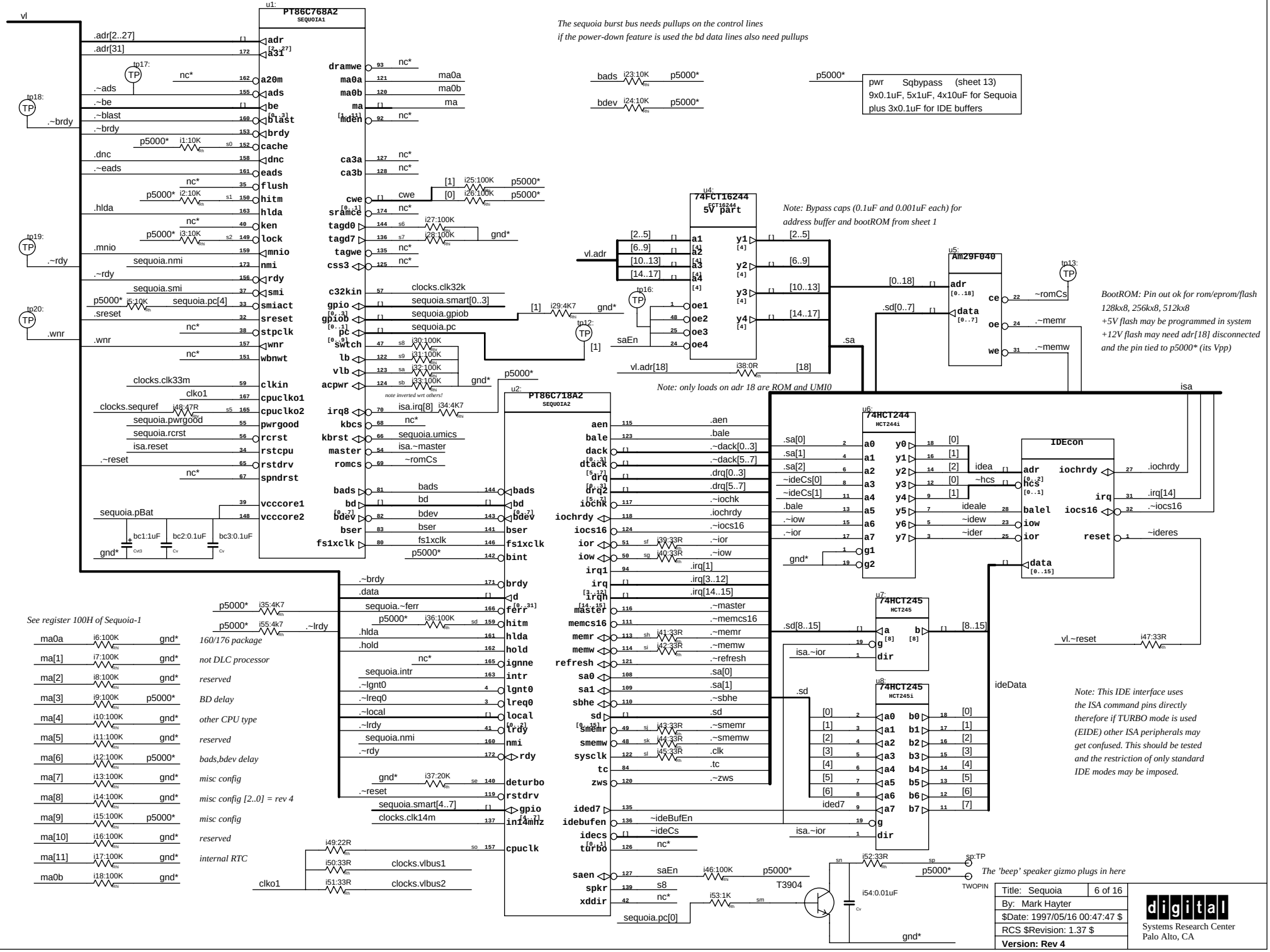
Palo Alto, CA


u1:
PT86C768A2
SEQUOIA1
vl
.adr[2..27]
.adr[31]
adr
a31
tp17:
nc*
a20m
.~ads
ads
.~be
be
tp18:
.~brdy
.~blast
blast
brdy
p5000*
i1:10K
cache
.dnc
dnc
.~eads
eads
flush
p5000*
i2:10K
hitm
.hlda
hlda
ken
p5000*
i3:10K
lock
tp19:
.mnio
mnio
.~rdy
sequoia.nmi
nmi
.~rdy
rdy
sequoia.smi
smi
p5000*
i5:10K
sequoia.pc[4]
smiact
tp20:
.sreset
sreset
stpclk
.wnr
wnr
wbnwt
clocks.clk33m
clkin
clko1
cpuclko1
clocks.sequref
i48:47R
cpuclko2
sequoia.pwrgood
pwrgood
sequoia.rcrst
rcrst
isa.reset
rstcpu
.~reset
rstdrv
spndrst
vcccore1
sequoia.pBat
vcccore2
bc1:1uF
bc2:0.1uF
bc3:0.1uF
gnd*
dramwe
nc*
ma0a
ma0b
ma
mden
ca3a
ca3b
cwe
sramce
tagd0
tagd7
tagwe
css3
c32kin
clocks.clk32k
gpio
sequoia.smart[0..3]
gpiob
sequoia.gpiob
pc
sequoia.pc
switch
lb
vlb
acpwr
note inverted wrt others!
irq8
isa.irq[8]
i34:4K7
kbcs
kbrst
sequoia.umics
master
isa.~master
romcs
~romCs
bads
bd
bdev
bser
fs1xclk
p5000*
bint
.~brdy
brdy
.data
d
sequoia.~ferr
ferr
p5000*
i35:4K7
p5000*
i55:4k7
.~lrdy
p5000*
i36:100K
hitm
.hlda
hlda
.hold
hold
nc*
ignne
sequoia.intr
intr
.~lgnt0
lgnt0
.~lreq0
lreq0
.~local
local
.~lrdy
lrdy
sequoia.nmi
nmi
.~rdy
rdy
gnd*
i37:20K
deturbo
.~reset
rstdrv
sequoia.smart[4..7]
gpio
clocks.clk14m
in14mhz
cpuclk
i49:22R
i50:33R
clocks.vlbus1
clko1
i51:33R
clocks.vlbus2
so
The sequoia burst bus needs pullups on the control lines
if the power-down feature is used the bd data lines also need pullups
bads
i23:10K
p5000*
bdev
i24:10K
p5000*
p5000*
pwr Sqbypass (sheet 13)
9x0.1uF, 5x1uF, 4x10uF for Sequoia
plus 3x0.1uF for IDE buffers
u4:
74FCT16244
FCT16244
5V part
Note: Bypass caps (0.1uF and 0.001uF each) for
address buffer and bootROM from sheet 1
vl.adr
[2..5]
[6..9]
[10..13]
[14..17]
a1
a2
a3
a4
y1
y2
y3
y4
oe1
oe2
oe3
oe4
tp16:
saEn
tp12:
vl.adr[18]
i38:0R
[18]
[0..18]
.sd[0..7]
.sa
u5:
Am29F040
adr
data
ce
oe
we
~romCs
.~memr
.~memw
tp13:
BootROM: Pin out ok for rom/eprom/flash
128kx8, 256kx8, 512kx8
+5V flash may be programmed in system
+12V flash may need adr[18] disconnected
and the pin tied to p5000* (its Vpp)
Note: only loads on adr 18 are ROM and UMI0
u2:
PT86718A2
SEQUOIA2
aen
bale
dack
dtack
drq
drq2
iochk
iochrdy
iocs16
ior
iow
irq1
irq
irqh
master
memcs16
memr
memw
refresh
sa0
sa1
sbhe
sd
smemr
smemw
sysclk
tc
zws
.aen
.bale
.~dack[0..3]
.~dack[5..7]
.drq[0..3]
.drq[5..7]
.~iochk
.iochrdy
.~iocs16
.~ior
.~iow
.irq[1]
.irq[3..12]
.irq[14..15]
.~master
.~memcs16
.~memr
.~memw
.~refresh
.sa[0]
.sa[1]
.~sbhe
.sd
.~smemr
.~smemw
.clk
.tc
.~zws
ided7
idebufen
idecs
turbo
saen
spkr
xddir
~ideBufEn
~ideCs
nc*
saEn
s8
nc*
sequoia.pc[0]
i46:100K
p5000*
T3904
i53:1K
i54:0.01uF
i52:33R
sp:TP
TWOPIN
The 'beep' speaker gizmo plugs in here
u6:
74HCT244
HCT244i
a0
a1
a2
a3
a4
a5
a6
a7
g1
g2
y0
y1
y2
y3
y4
y5
y6
y7
.sa[0]
.sa[1]
.sa[2]
~ideCs[0]
~ideCs[1]
.bale
.~iow
.~ior
idea
~hcs
ideale
~idew
~ider
IDEcon
adr
hcs
balel
iow
ior
data
iochrdy
irq
iocs16
reset
.iochrdy
.irq[14]
.~iocs16
~ideres
isa
u7:
74HCT245
HCT245
.sd[8..15]
isa.~ior
vl.~reset
i47:33R
u8:
74HCT245
HCT245i
.sd
ideData
[0]
[1]
[2]
[3]
[4]
[5]
[6]
[7]
ided7
Note: This IDE interface uses
the ISA command pins directly
therefore if TURBO mode is used
(EIDE) other ISA peripherals may
get confused. This should be tested
and the restriction of only standard
IDE modes may be imposed.
See register 100H of Sequoia-1
ma0a
ma[1]
ma[2]
ma[3]
ma[4]
ma[5]
ma[6]
ma[7]
ma[8]
ma[9]
ma[10]
ma[11]
ma0b
i6:100K
i7:100K
i8:100K
i9:100K
i10:100K
i11:100K
i12:100K
i13:100K
i14:100K
i15:100K
i16:100K
i17:100K
i18:100K
160/176 package
not DLC processor
reserved
BD delay
other CPU type
reserved
bads,bdev delay
misc config
misc config [2..0] = rev 4
misc config
reserved
internal RTC
Title: Sequoia
6 of 16
By: Mark Hayter
$Date: 1997/05/16 00:47:47 $
RCS $Revision: 1.37 $
Version: Rev 4
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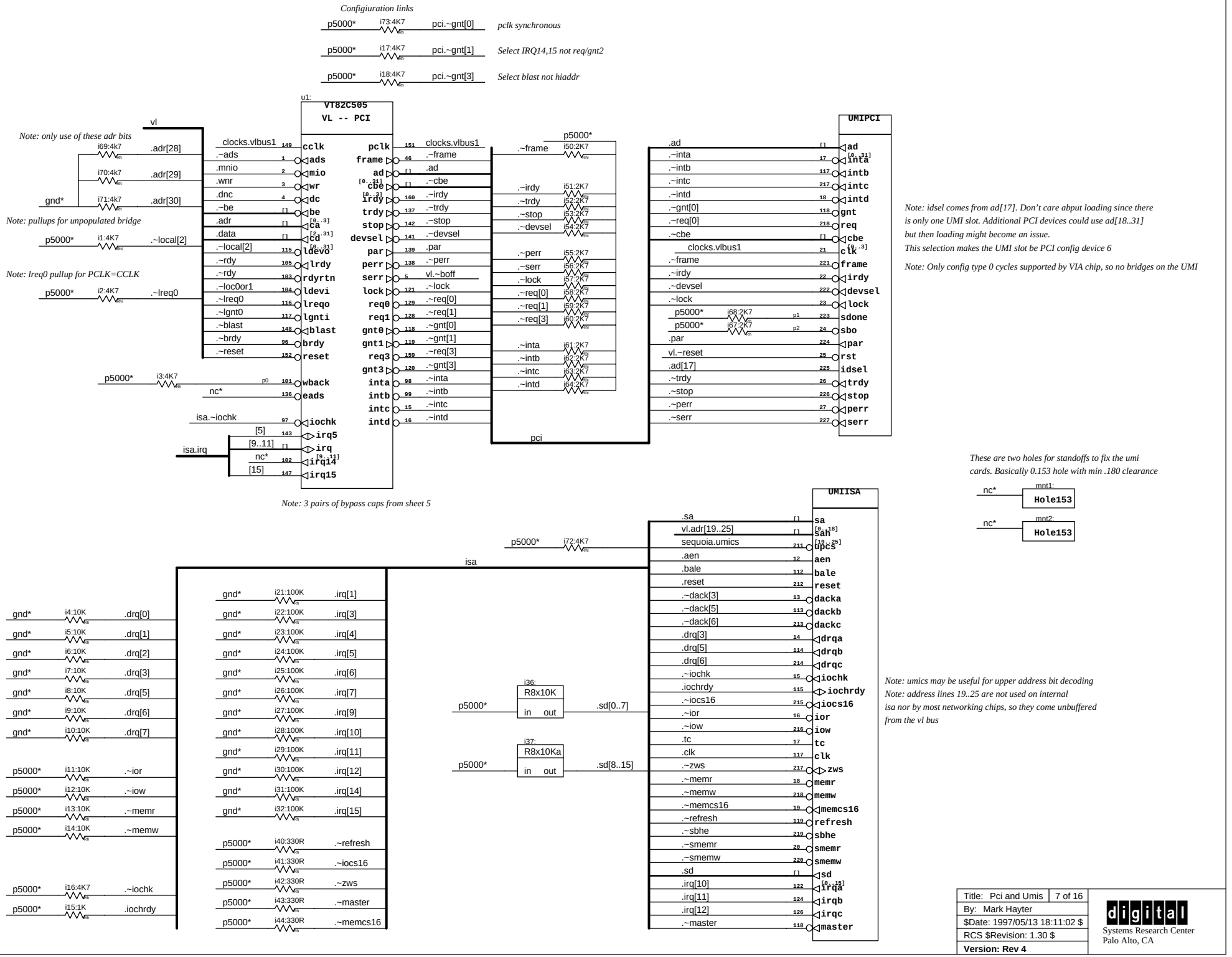
Palo Alto, CA



Title: Pci and Umis	7 of 16
By: Mark Hayter	
$Date: 1997/05/13 18:11:02 $	
RCS $Revision: 1.30 $	
Version: Rev 4	

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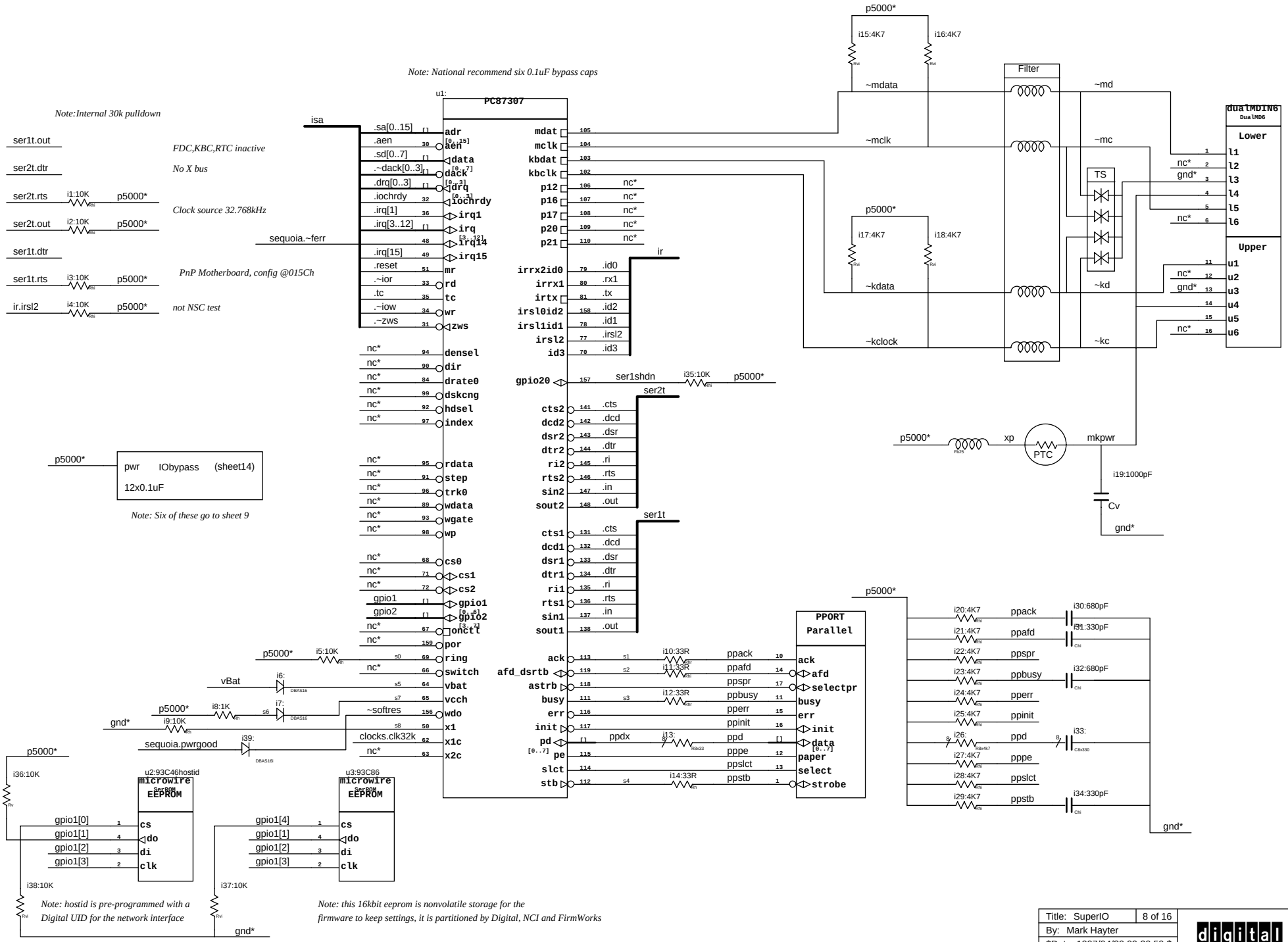

Title: SuperIO	8 of 16
By: Mark Hayter	
$Date: 1997/04/30 09:20:59 $	
RCS $Revision: 1.28 $	
Version: Rev 4	

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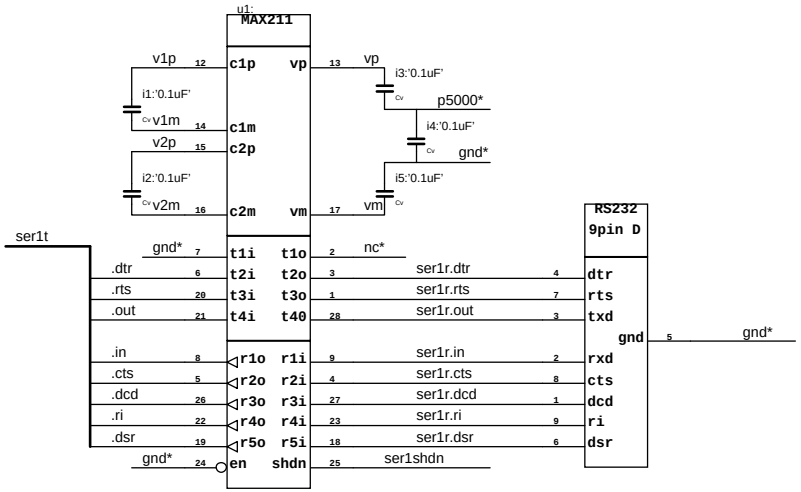
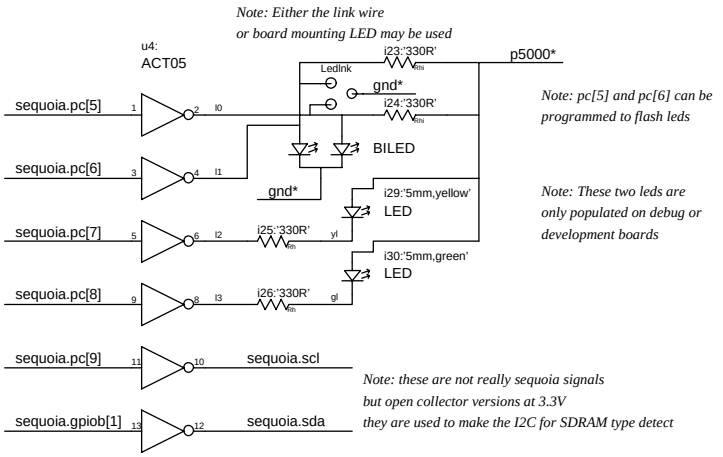
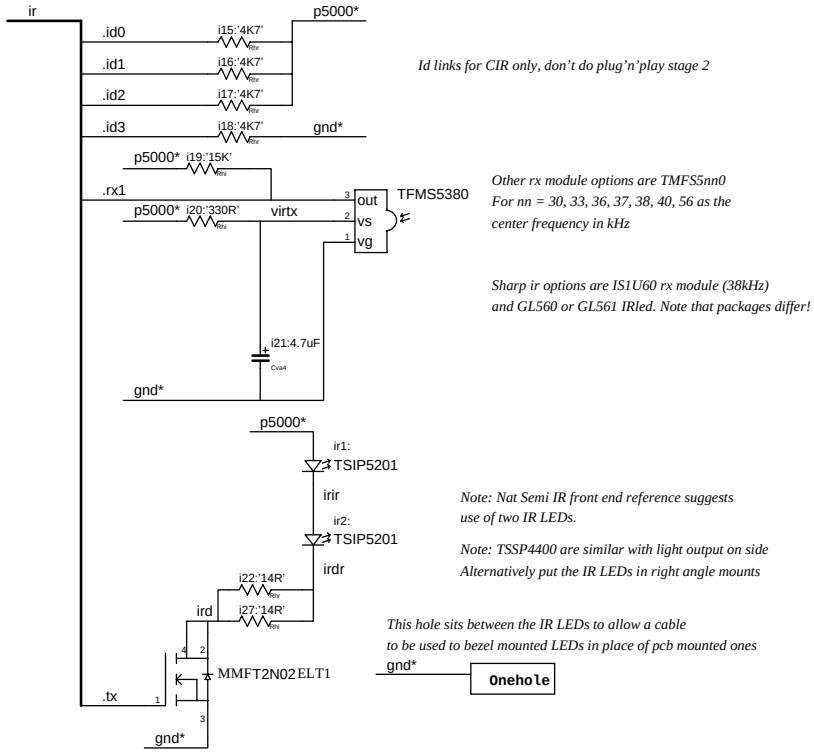


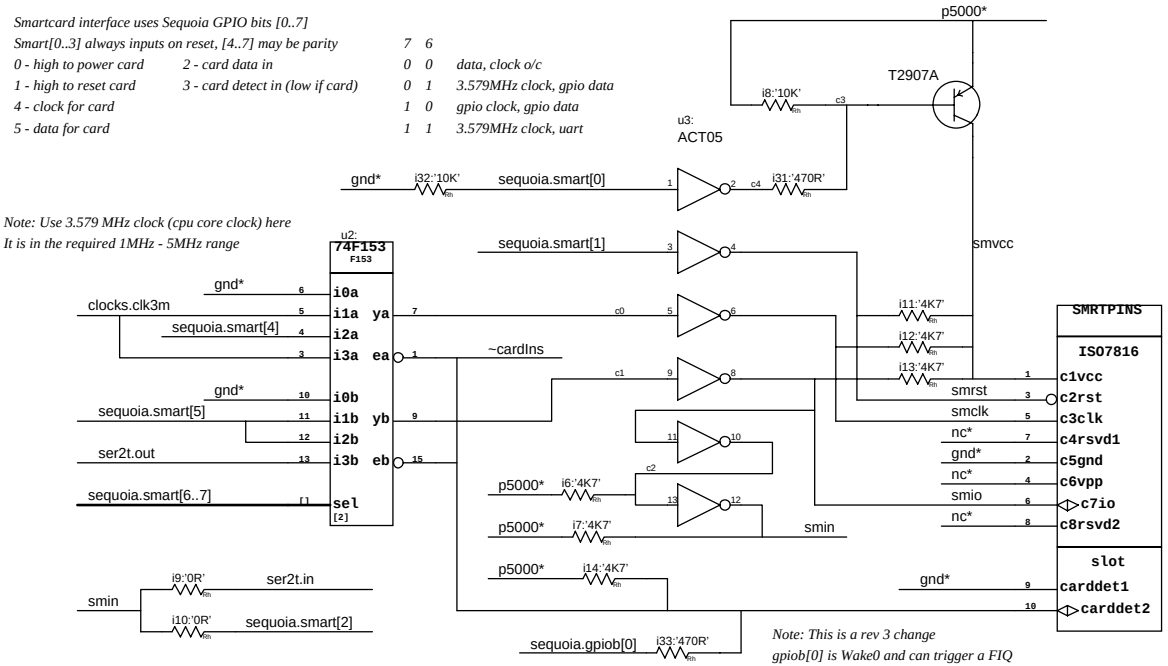


The IR from the SuperIO supports IRDA and Consumer IR
Only 38kHz consumer IR is provided here
TX frequency is set by software, but receiver module is tuned

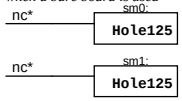


Smartcard interface uses Sequoia GPIO bits [0..7]
Smart[0..3] always inputs on reset, [4..7] may be parity
0 - high to power card
1 - high to reset card
4 - clock for card
5 - data for card
2 - card data in
3 - card detect in (low if card)

7	6	
0	0	data, clock o/c
0	1	3.579MHz clock, gpio data
1	0	gpio clock, gpio data
1	1	3.579MHz clock, uart



These holes are for supports for the smartcard reader when a bare board is used



Title: Serial I/O	9 of 16
By: Mark Hayter	
$Date: 1997/05/12 00:28:29 $	
RCS $Revision: 1.29 $	
Version: Rev 4	

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Note: four 0.1uF bypass capacitors (as suggested by ESS) shown on sheet 11

The audio is designed to use either the ES888 or ES1887 codec
The main difference is that the 1887 includes FM synth, it is also more expensive (about $3 more)
The 1887 is also slightly more configurable
Software for the 888 should work with the 1887 apart from a few lines of setup code (and the lack of synth)

:'ES888 or ES1887'

ES888

isa

.reset 78 **reset** — **msi** 56 mi — i11:2K2 — miout 15 **midii**
.~ior 72 **iorb** — **mso** 55 mo — i12:2K2 — moout 12 **midio**
.~iow 73 **iowb**
.sa[0..11] [] **adr** [0..11]
.aen 9 **aen**
.sd[0..7] [] **datal** [0..7]
.sd[8..15] [] **datah** [8..15]

p5000*
i14:2K2 i15:2K2 i16:2K2 i17:2K2 i13: pg PTC pGame 1 **pwr1**
i18:150pF 8 **pwr2** 9 **pwr3**

swa 32 sa — 2 **sw1**
swb 31 sb — 7 **sw2**
swc 30 sc — 10 **sw3**
swd 29 sd — 14 **sw4**

i19:0.01uF i20:0.01uF i21:0.01uF i22:0.01uF gnd*

Note: Use xtal here if the clk14m is not accurate enough

nc* 76 **xo**
clocks.clk14m 77 **xi**

.irq[9] 71 **irqa**
.irq[5] 70 **irqb**
.irq[7] 69 **irqc**
.irq[10] 68 **irqd**
.irq[15] 67 **irqe**

ta 28 ta — i22:2K2 x1 — 3 **x1**
tb 27 tb — i24:2K2 y1 — 6 **y1**
tc 26 tc — i25:2K2 x2 — 11 **x2**
td 25 td — i26:2K2 y2 — 13 **y2**

i27:1M i28:0.01uF i29:1M i30:0.01uF i31:1M i32:0.01uF i33:1M i34:0.01uF gnd* 5 **gnd1** 4 **gnd2**

.drq[0] 65 **drqa**
.~dack[0] 66 **dackba**
.drq[1] 63 **drqb**
.~dack[1] 64 **dackbb**
.drq[3] 61 **drqc**
.~dack[3] 62 **dackbc**
.drq[5] 59 **drqd**
.~dack[5] 60 **dackbd**

fmcsb 18 nc*
frmstb 79 nc*
fs 80 nc*
dclk 81 nc*
dr 82 nc*
dx 83 nc*
fmsel 86 fmsel — i35:4K7 — gnd*

p5000* i1:1K amode 22 **amode**
gnd* 52 **pcspki**

Note: Slight difference between 888 and 1887 for the DSP serial port. This arrangement should be fine for not using the port

The frmsrb out from the 888 becomes fsr in on the 1887
The fs in on the 888 becomes fsx in on the 1887
For using the port on both chips these would have to be linked in the 1887 case and not in the 888 case.
For never using leave unlinked and rely on the internal pulldowns

nc* 19 **voldn**
nc* 20 **volup**
nc* 21 **mute**

msd 84 nc*
mclk 85 nc*

gpo0 54 nc*
gpo1 53 nc*

AudioGm
GamePort

15 pin (2 row) female D over three 3.5mm jacks

Below this line is the analog power/ground domain

Below this line is the analog power/ground domain

Right Jack
nc* 302 **rsig3**
nc* 310 **rsw3**
miin 303 **lsig3**
311 **lsw3**
agnd 301 **com3**

Mono mike input

Center Jack
rl 202 **rsig2**
nc* 210 **rsw2**
ll 203 **lsig2**
nc* 211 **lsw2**
agnd 201 **com2**

Stereo line output

Left Jack
ro 102 **rsig1**
nc* 110 **rsw1**
lo 103 **lsig1**
nc* 111 **lsw1**
101 **com1**

Stereo headphone output

Note: Care with layout Need single connection point for agnd to gnd

p5000* i2: avcc 41 **vdda1**
i3:10uF i4:0.1uF agnd

vref 44 vref — i36:0.1uF
foutl 33 fl — i37:0.22uF i38:1000pF
cinl 42 cil
foutr 34 fr — i39:0.22uF i40:1000pF
cinr 43 cir
pcspko 50 nc*
aoutr 49 rl — i51:0.22uF
aoutl 48 ll — i52:0.22uF

i53:0.22uF i0 46 **linel**
i54:0.22uF i1 47 **liner**
i55:0.22uF i2 37 **auxl**
i56:0.22uF i3 38 **auxr**
i57:0.22uF i4 36 **fdxo**
i58:0.22uF i5 35 **fdxi**

Note: rev 4 change tie off unused inputs

agnd

Note: output amp is directly (not cap) coupled since vref/cmr is used as the reference

avcc
i41:10uF i42:0.1uF
cmr
aord
i45:8K6
SSM2135
ramp i43:330uF
aor
i44:10K
aol
i46:10K
i47:8K6
aold
lamp i48:330uF
cmr
i50:0.1uF
Had 10uF here

Mike input is on combo connector on right of this page

miin i5:0.1uF mic 39 **mic**
i6:7K5 i7:7K5 avcc cmr 45 **cmr**
avccm
i8:10uF i9:47uF i10:0.1uF
40 **gnda**
agnd

Title: Audio	10 of 16
By: Mark Hayter	
$Date: 1997/05/17 00:51:49 $	
RCS $Revision: 1.32 $	
Version: Rev 4	

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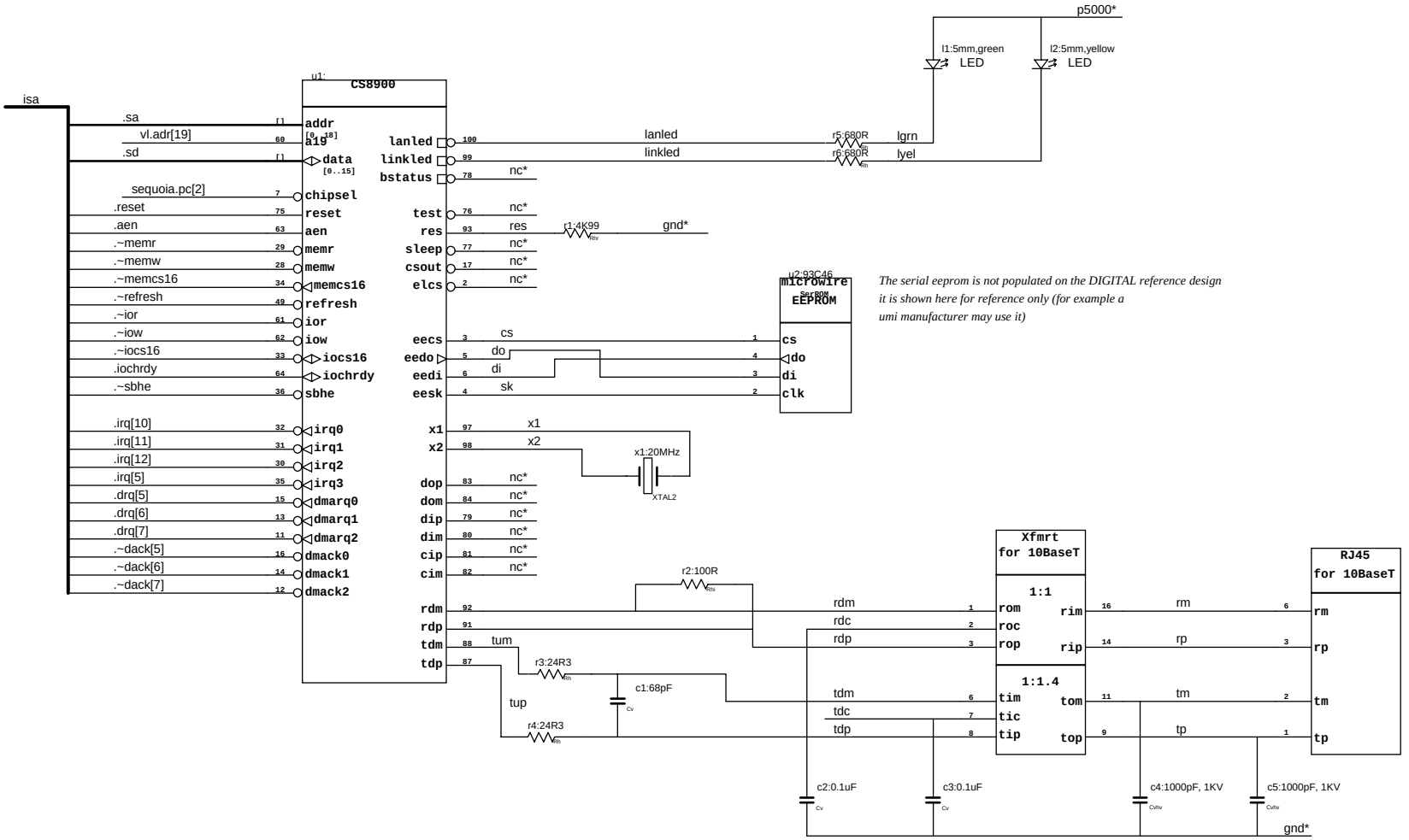

The serial eeprom is not populated on the DIGITAL reference design it is shown here for reference only (for example a umi manufacturer may use it)

Four digital, three analog recomended by Crystal
One for serial eeprom, four for audio (sheet 10)

p5000* — pwr IObypass (sheet14) — 12x0.1uF

R2, R3, and R4 are setup for 100 ohm twisted pair.
Other values are possible. See CS8900 data sheet, page 123.

Note: Changed these caps from 10n to 1n

Title: Ethernet	11 of 16
By: Hal Murray	
$Date: 1997/04/30 09:20:59 $	
RCS $Revision: 1.16 $	
Version: Rev 4	

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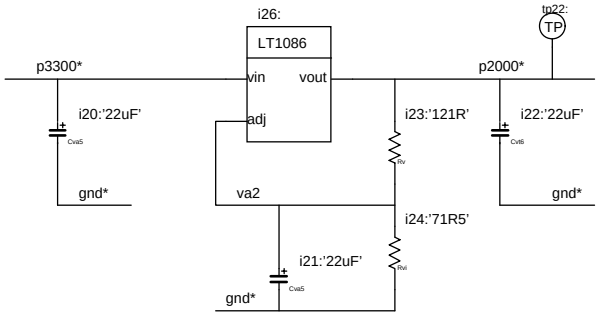
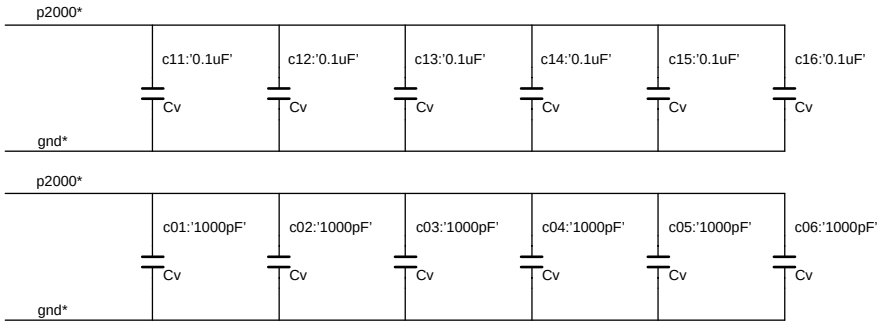
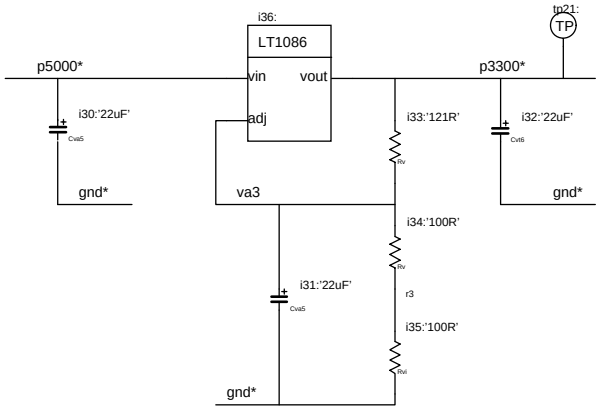
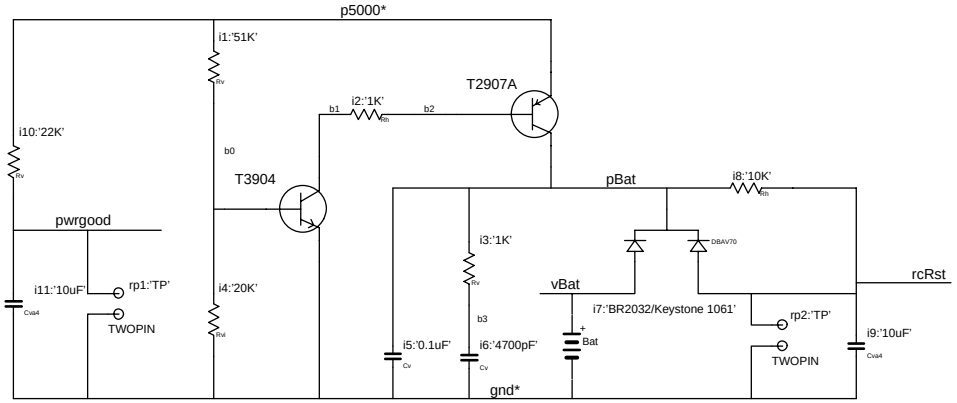
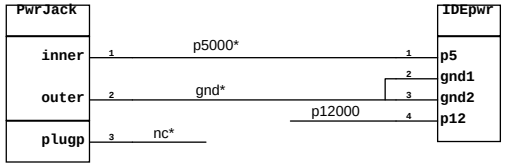




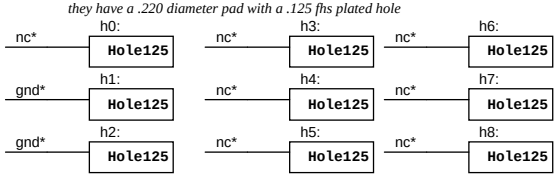




Note: Battery is 3V Li coin cell BR2032 in a smt holder



Note: These are the mounting holes, with the two near the connectors grounded they have a .220 diameter pad with a .125 fhs plated hole



Title: Power	12 of 16
By: Mark Hayter	
$Date: 1997/05/14 03:07:47 $	
RCS $Revision: 1.28 $	
Version: Rev 4	

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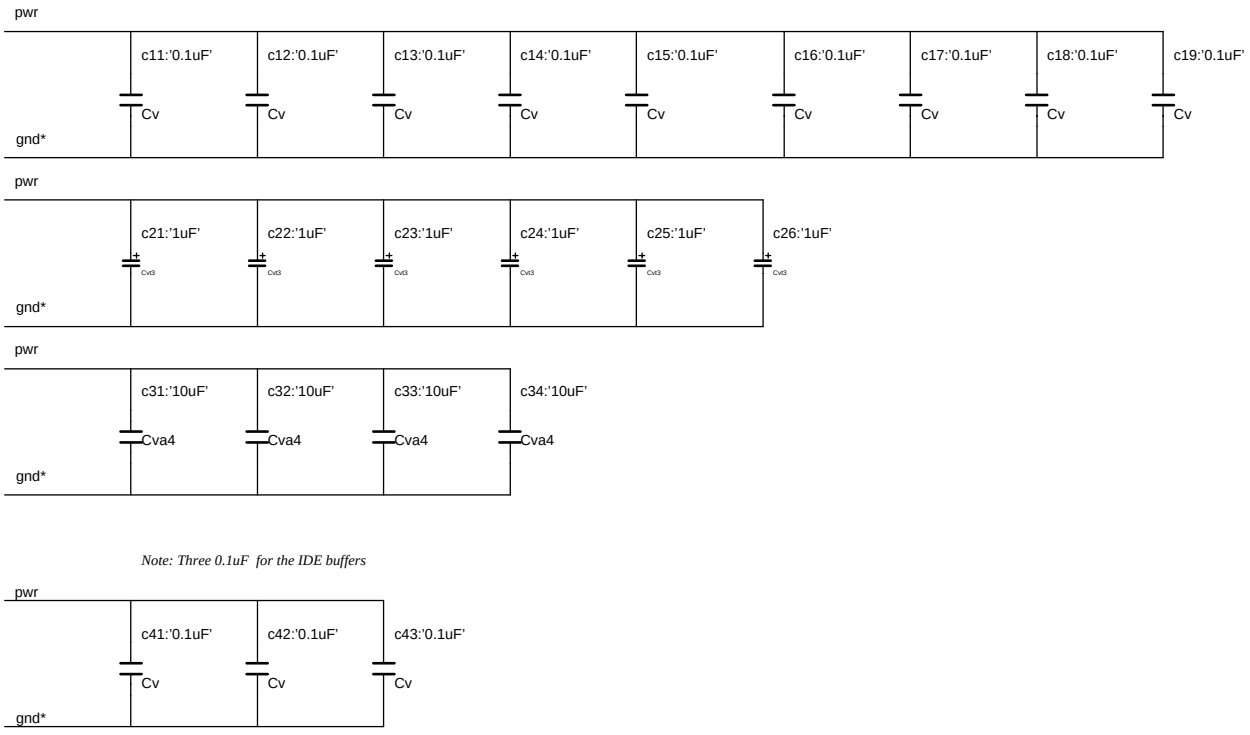
Note: Sequoia1 gets 0.1uF + 1uF for each of the five power groups plus 1uF extra
Note: Sequoia2 gets 0.1uF + 10uF for each of the four power groups



Note: Three 0.1uF for the IDE buffers

Title: Sequoia bypass	13 of 16
By: Mark Hayter	
$Date: 1997/04/30 09:20:59 $	
RCS $Revision: 1.8 $	
Version: Rev 4	

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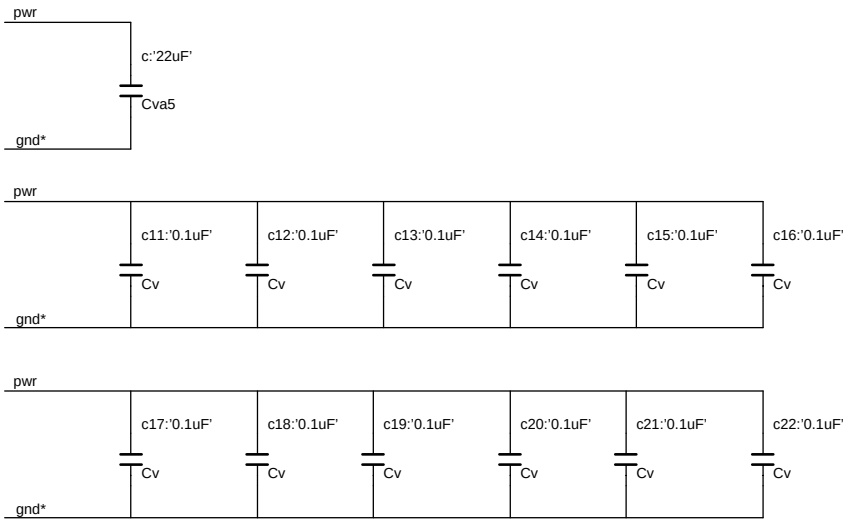

Title: I/O bypass	14 of 16
By: Mark Hayter	
$Date: 1997/04/30 09:20:59 $	
RCS $Revision: 1.8 $	
Version: Rev 4	

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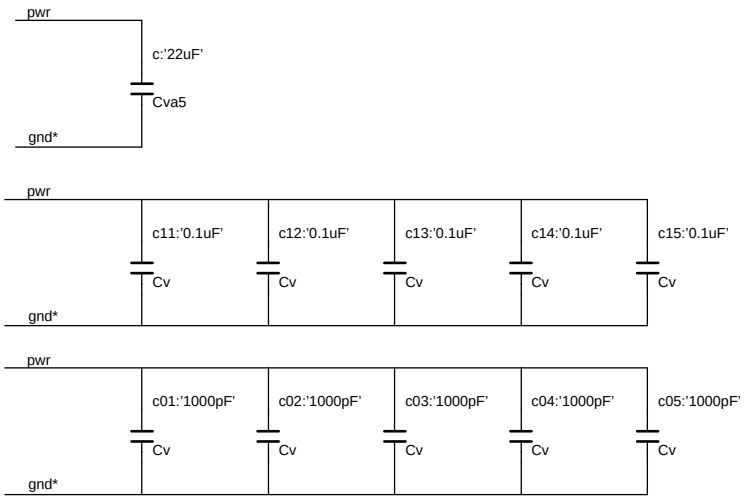

Title: Bypass (5)	15 of 16
By: Hal Murray	
$Date: 1997/04/30 09:20:59 $	
RCS $Revision: 1.8 $	
Version: Rev 4	

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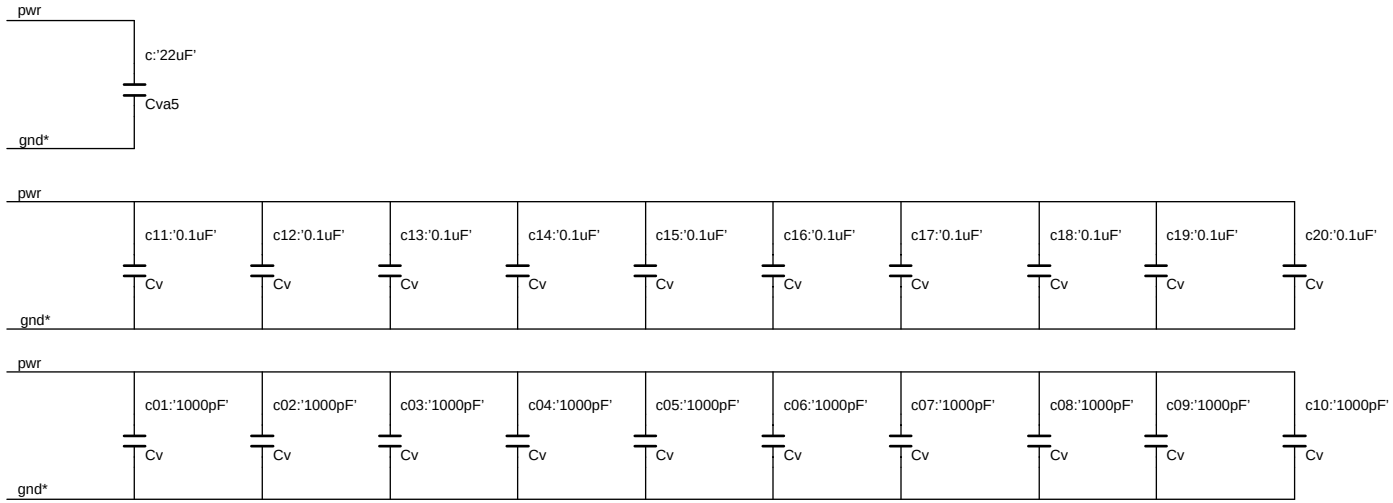

Title: Bypass (10)	16 of 16
By: Hal Murray	
$Date: 1997/04/30 09:20:59 $	
RCS $Revision: 1.10 $	
Version: Rev 4	

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