EMBEDDED ULTRA-LOW POWER Intel486™ GX PROCESSOR

- **Ultra-Low Power Member of the Intel486 Processor Family**
  - **— 32-Bit RISC Technology Core**
  - **— 8-Kbyte Write-Through Cache**
  - **— Four Internal Write Buffers**
  - **— Burst Bus Cycles**
  - **— Data Bus Parity Generation and Checking**
  - **— Intel System Management Mode (SMM)**
  - **— Boundary Scan (JTAG)**
- **16-Bit External Data Bus**
- **176-Lead Thin Quad Flat Pack (TQFP)**
- **Separate Voltage Supply for Core Circuitry**
- **Fast Core-Clock Restart**
- **Auto Clock Freeze**
- **Ideal for Embedded Battery-Operated and Hand-Held Applications**

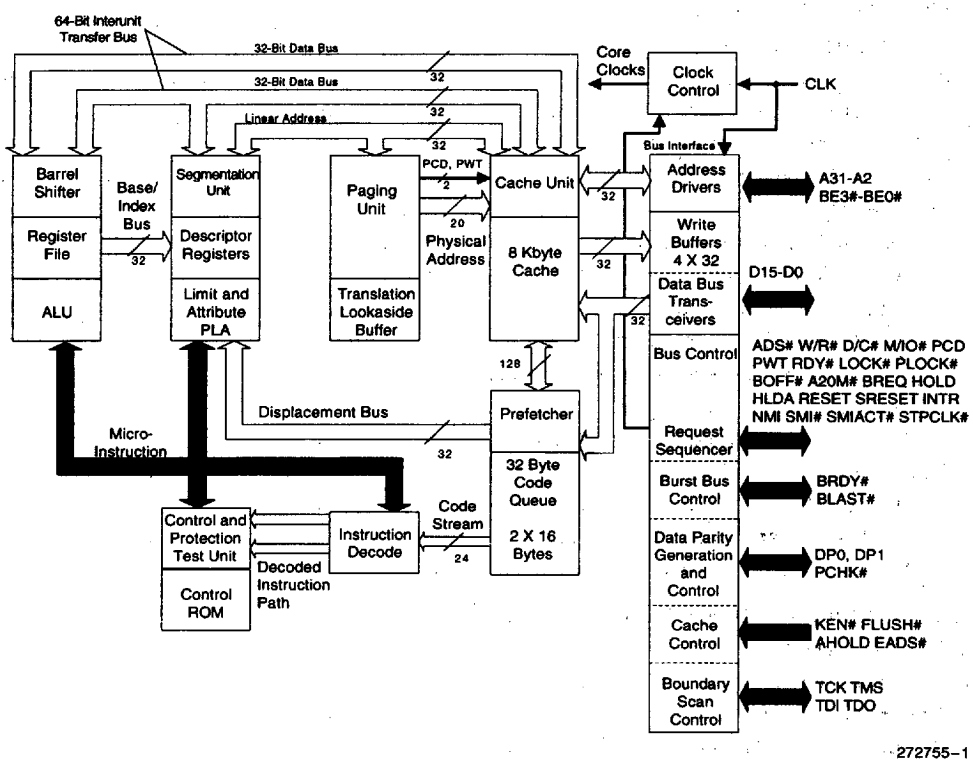

Figure 1. Embedded ULP Intel486™ GX Processor Block Diagram

Embedded Ultra-Low Power Intel486™ GX Processor

CONTENTS

PAGE

CONTENTS

FIGURES

CONTENTS

PAGE

TABLES

1.0 INTRODUCTION

This data sheet describes the embedded Ultra-Low Power (ULP) Intel486™ GX processor. It is intended for embedded battery-operated and hand-held applications. The embedded ULP Intel486 GX processor provides all of the features of the Intel486 SX processor except for the 8-bit bus sizing logic and the processor-upgrade pin. The processor typically uses 20% to 50% less power than the Intel486 SX processor. Additionally, the embedded ULP Intel486 GX processor external data bus and parity signals have level-keeper circuitry and a fast-recovery core clock which are vital for ultra-low-power system designs. The processor is available in a Thin Quad Flat Package (TQFP) enabling low-profile component implementation.

The embedded ULP Intel486 GX processor consists of a 32-bit integer processing unit, an on-chip cache, and a memory management unit. The design ensures full instruction-set compatibility with the 8086, 8088, 80186, 80286, Intel386™ SX, Intel386 DX, and all versions of Intel486 processors.

1.1 Features

The embedded ULP Intel486 GX processor offers these features of the Intel486 SX processor:

- **32-bit RISC-Technology Core**—The embedded ULP Intel486 GX processor performs a complete set of arithmetic and logical operations on 8-, 16-, and 32-bit data types using a full-width ALU and eight general purpose registers.
- **Single Cycle Execution**—Many instructions execute in a single clock cycle.
- **Instruction Pipelining**—Overlapped instruction fetching, decoding, address translation and execution.
- **On-Chip Cache with Cache Consistency Support**—An 8-Kbyte, write-through, internal cache is used for both data and instructions. Cache hits provide zero wait-state access times for data within the cache. Bus activity is tracked to detect alterations in the memory represented by the internal cache. The internal cache can be invalidated or flushed so that an external cache controller can maintain cache consistency.
- **External Cache Control**—Write-back and flush controls for an external cache are provided so the processor can maintain cache consistency.
- **On-Chip Memory Management Unit**—Address management and memory space protection mechanisms maintain the integrity of memory in a multitasking and virtual memory environment. Both segmentation and paging are supported.
- **Burst Cycles**—Burst transfers allow a new 16-bit data word to be read from memory on each bus clock cycle. This capability is especially useful for instruction prefetch and for filling the internal cache. Burst transfers also occur on some memory write and some I/O data transfers.
- **Write Buffers**—The processor contains four write buffers to enhance the performance of consecutive writes to memory. The processor can continue internal operations after a write to these buffers, without waiting for the write to be completed on the external bus.
- **Bus Backoff**—When another bus master needs control of the bus during a processor initiated bus cycle, the embedded ULP Intel486 GX processor floats its bus signals, then restarts the cycle when the bus becomes available again.
- **Instruction Restart**—Programs can continue execution following an exception generated by an unsuccessful attempt to access memory. This feature is important for supporting demand-paged virtual memory applications.
- **Boundary Scan (JTAG)**—Boundary Scan provides in-circuit testing of components on printed circuit boards. The Intel Boundary Scan implementation conforms with the IEEE Standard Test Access Port and Boundary Scan Architecture.

- **Intel System Management Mode (SMM)**—A unique Intel architecture operating mode provides a dedicated special purpose interrupt and address space that can be used to implement intelligent power management and other enhanced functions in a manner that is completely transparent to the operating system and applications software.
- **I/O Restart**—An I/O instruction interrupted by a System Management Interrupt (SMI#) can automatically be restarted following the execution of the RSM instruction.
- **Stop Clock**—The embedded ULP Intel486 GX processor has a stop clock control mechanism that provides two low-power states: a Stop Grant state (40–85 mW typical, depending on input clock frequency) and a Stop Clock state (~60 μW typical, with input clock frequency of 0 MHz).
- **Auto HALT Power Down**—After the execution of a HALT instruction, the embedded ULP Intel486 GX processor issues a normal Halt bus cycle and the clock input to the processor core is automatically stopped, causing the processor to enter the Auto HALT Power Down state (40–85 mW typical, depending on input clock frequency).

The embedded ULP Intel486 GX processor differs from the Intel486 SX processor in the following areas:

- **16-Bit External Data Bus**—The embedded ULP Intel486 GX processor is designed for 16-bit embedded systems, yet internally provides the 32-bit architecture of the Intel486 processor family. Two data parity bits are provided.
- **Processor Upgrade Removed**—The UP# signal is not provided.
- **Dynamic Bus-Sizing Removed**—The BS8# signal is not provided.
- **Separate Processor-Core Power**—While the embedded ULP Intel486 GX processor requires a supply voltage of 3.3V, the processor core has dedicated V_{CC} pins and operates with a supply voltage as low as 2.0V.
- **Small, Low-Profile Package**—The 176-Lead Thin Quad Flat Pack (TQFP) package is approximately 26mm square and only 1.5mm in height. This is approximately the diameter and thickness of a U.S. quarter. The embedded ULP Intel486 GX processor is ideal for embedded hand-held and battery-powered applications.
- **Level Keeper Circuits**—The embedded ULP Intel486 GX processor has level-keeper circuits for its 16-bit external data bus and parity signals. They retain valid high and low logic voltage levels when the processor is in the Stop Grant and Stop Clock states. The level-keeper circuits for the parity signals are always enabled. This is a power-saving improvement from the floating data bus of the Intel486 SX processor.
- **Auto Clock Freeze**—The embedded ULP Intel486 GX processor monitors bus events and internal activity. The Auto Clock Freeze feature automatically controls internal clock distribution, turning off clocks to internal units when they are idle. This power-saving function is transparent to the embedded system.
- **Fast Clock Restart**—The embedded ULP Intel486 GX processor requires only eight clock periods to synchronize its internal clock with the CLK input signal. This provides for faster transition from the Stop Clock State to the Normal State. For 33-MHz operation, this synchronization time is only 240 ns compared with 1 ms (PLL startup latency) for the Intel486 processor.

1.2 Family Members

Table 1 shows the embedded ULP Intel486 GX processor and briefly describes its characteristics.

Table 1. The Embedded Ultra-Low Power Intel486™ GX Processor

Product	Supply Voltage (V_{CCP})	Processor Core Supply Voltage (V_{CC})	Processor Frequency (MHz)	Package
FA80486GXSF-33	3.3V	2.0V to 3.3V	16	176-Lead TQFP
		2.2V to 3.3V	20	
		2.4V to 3.3V	25	
		2.7V to 3.3V	33	

2.0 HOW TO USE THIS DOCUMENT

Even though it has a 16-bit external data bus, the embedded ULP Intel486 GX processor has characteristics similar to the 32-bit Intel486 SX processor. This document describes the new features of the embedded ULP Intel486 GX processor. Some Intel486 SX processor information is also included to minimize the dependence on the reference documents.

For a complete set of documentation related to the embedded ULP Intel486 GX processor, use this document in conjunction with the following reference documents:

- *Intel486™ Processor Family* datasheet—Order No. 242202
- *Intel486 Microprocessor Family Programmer's Reference Manual*—Order No. 240486
- Intel Application Note AP-485—*Intel Processor Identification with the CPUID Instruction*—Order No. 241618

3.0 PIN DESCRIPTIONS

3.1 Pin Assignments

The following figures and tables show the pin assignments for the 176-pin Thin Quad Flat Pack (TQFP) package of the embedded ULP Intel486 GX processor. Included are:

- Figure 2, Package Diagram for 176-Lead TQFP Package Embedded ULP Intel486™ GX Processor
- Table 2, Pin Assignment for 176-Lead TQFP Package Embedded ULP Intel486™ GX Processor
- Table 3, Pin Cross Reference for 176-Lead TQFP Package Embedded ULP Intel486™ GX Processor
- Table 4, Embedded ULP Intel486™ GX Processor Pin Descriptions
- Table 5, Output Pins
- Table 6, Input/Output Pins
- Table 7, Test Pins
- Table 8, Input Pins

The tables and figures show "no-connects" as "N/C." These pins should always remain unconnected. Connecting N/C pins to V_{CC}, V_{CCP}, V_{SS}, or any other signal pin can result in component malfunction or incompatibility with future steppings of the embedded ULP Intel486 GX processor.

4

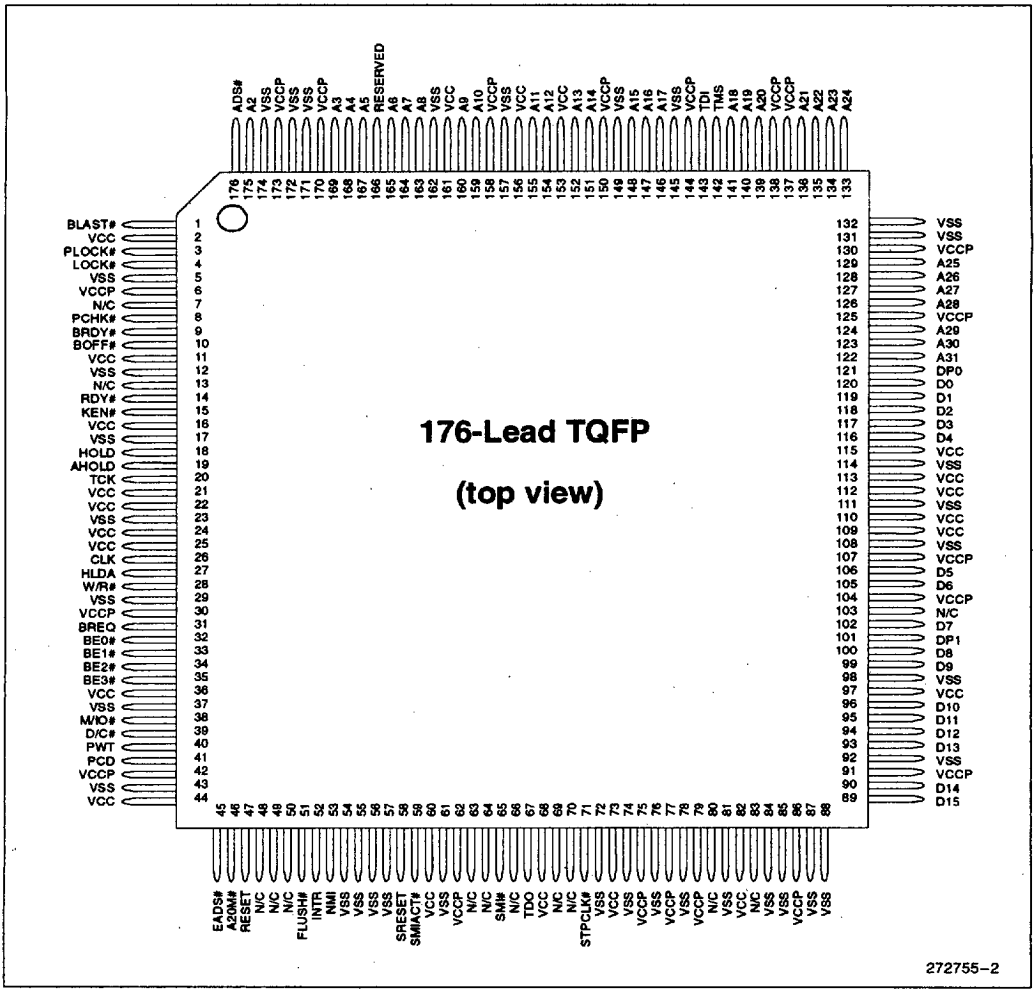

Figure 2. Package Diagram for 176-Lead TQFP Package Embedded ULP Intel486™ GX Processor

Table 2. Pin Assignment for 176-Lead TQFP Package
Embedded ULP Intel486™ GX Processor

Pin #	Description	Pin #	Description	Pin #	Description	Pin #	Description
1	BLAST#	31	BREQ	61	V_{SS}	91	V_{CCP}
2	V_{CC}	32	BE0#	62	V_{CCP}	92	V_{SS}
3	PLOCK#	33	BE1#	63	N/C	93	D13
4	LOCK#	34	BE2#	64	N/C	94	D12
5	V_{SS}	35	BE3#	65	SMI#	95	D11
6	V_{CCP}	36	V_{CC}	66	N/C	96	D10
7	N/C	37	V_{SS}	67	TDO	97	V_{CC}
8	PCHK#	38	M/IO#	68	V_{CC}	98	V_{SS}
9	BRDY#	39	D/C#	69	N/C	99	D9
10	BOFF#	40	PWT	70	N/C	100	D8
11	V_{CC}	41	PCD	71	STPCLK#	101	DP1
12	V_{SS}	42	V_{CCP}	72	V_{SS}	102	D7
13	N/C	43	V_{SS}	73	V_{CC}	103	N/C
14	RDY#	44	V_{CC}	74	V_{SS}	104	V_{CCP}
15	KEN#	45	EADS#	75	V_{CCP}	105	D6
16	V_{CC}	46	A20M#	76	V_{SS}	106	D5
17	V_{SS}	47	RESET	77	V_{CCP}	107	V_{CCP}
18	HOLD	48	N/C	78	V_{SS}	108	V_{SS}
19	AHOLD	49	N/C	79	V_{CCP}	109	V_{CC}
20	TCK	50	N/C	80	N/C	110	V_{CC}
21	V_{CC}	51	FLUSH#	81	V_{SS}	111	V_{SS}
22	V_{CC}	52	INTR	82	V_{CC}	112	V_{CC}
23	V_{SS}	53	NMI	83	N/C	113	V_{CC}
24	V_{CC}	54	V_{SS}	84	V_{SS}	114	V_{SS}
25	V_{CC}	55	V_{SS}	85	V_{SS}	115	V_{CC}
26	CLK	56	V_{SS}	86	V_{CCP}	116	D4
27	HLDA	57	V_{SS}	87	V_{SS}	117	D3
28	W/R#	58	SRESET	88	V_{SS}	118	D2
29	V_{SS}	59	SMIACT#	89	D15	119	D1
30	V_{CCP}	60	V_{CC}	90	D14	120	D0

Table 2. Pin Assignment for 176-Lead TQFP Package
Embedded ULP Intel486™ GX Processor (Continued)

Pin #	Description	Pin #	Description	Pin #	Description	Pin #	Description
121	DP0	135	A22	149	V_{SS}	163	A8
122	A31	136	A21	150	V_{CCP}	164	A7
123	A30	137	V_{CCP}	151	A14	165	A6
124	A29	138	V_{CCP}	152	A13	166	RESERVED
125	V_{CCP}	139	A20	153	V_{CC}	167	A5
126	A28	140	A19	154	A12	168	A4
127	A27	141	A18	155	A11	169	A3
128	A26	142	TMS	156	V_{CC}	170	V_{CCP}
129	A25	143	TDI	157	V_{SS}	171	V_{SS}
130	V_{CCP}	144	V_{CCP}	158	V_{CCP}	172	V_{SS}
131	V_{SS}	145	V_{SS}	159	A10	173	V_{CCP}
132	V_{SS}	146	A17	160	A9	174	V_{SS}
133	A24	147	A16	161	V_{CC}	175	A2
134	A23	148	A15	162	V_{SS}	176	ADS#

Table 3. Pin Cross Reference for 176-Lead TQFP Package
Embedded ULP Intel486™ GX Processor

Address	Pin #	Data	Pin #	Control	Pin #	N/C	V_{CCP}	V_{CC}	V_{SS}
A2	175	D0	120	A20M#	46	7	6	2	5
A3	169	D1	119	ADS#	176	13	30	11	12
A4	168	D2	118	AHOLD	19	48	42	16	17
A5	167	D3	117	BE0#	32	49	62	21	23
A6	165	D4	116	BE1#	33	50	75	22	29
A7	164	D5	106	BE2#	34	63	77	24	37
A8	163	D6	105	BE3#	35	64	79	25	43
A9	160	D7	102	BLAST#	1	66	86	36	54
A10	159	D8	100	BOFF#	10	69	91	44	55
A11	155	D9	99	BRDY#	9	70	104	60	56
A12	154	D10	96	BREQ	31	80	107	68	57
A13	152	D11	95	CLK	26	83	125	73	61

Table 3. Pin Cross Reference for 176-Lead TQFP Package
Embedded ULP Intel486™ GX Processor (Continued)

Address	Pin #	Data	Pin #	Control	Pin #	N/C	V_{CCP}	V_{CC}	V_{SS}
A14	151	D12	94	D/C#	39	103	130	82	72
A15	148	D13	93	DP0	121		137	97	74
A16	147	D14	90	DP1	101		138	109	76
A17	146	D15	89	EADS#	45		144	110	78
A18	141			FLUSH#	51		150	112	81
A19	140			HLDA	27		158	113	84
A20	139			HOLD	18		170	115	85
A21	136			INTR	52		173	153	87
A22	135			KEN#	15			156	88
A23	134			LOCK#	4			161	92
A24	133			M/IO#	38				98
A25	129			NMI	53				108
A26	128			PCD	41				111
A27	127			PCHK#	8				114
A28	126			PLOCK#	3				131
A29	124			PWT	40				132
A30	123			RDY#	14				145
A31	122			RESERVED	166				149
				RESET	47				157
				SMI#	65				162
				SMIACT#	59				171
				SRESET	58				172
				STPCLK#	71				174
				TCK	20				
				TDI	143				
				TDO	67				
				TMS	142				
				W/R#	28				

4

3.2 Pin Quick Reference

The following is a brief pin description. For detailed signal descriptions refer to "Signal Description" in section 9 of the *Intel486™ Processor Family* datasheet.

Table 4. Embedded ULP Intel486™ GX Processor Pin Descriptions (Sheet 1 of 6)

Symbol	Type	Name and Function
CLK	I	**Clock** provides the fundamental timing and internal operating frequency for the embedded ULP Intel486 GX processor. All external timing parameters are specified with respect to the rising edge of CLK.
ADDRESS BUS		
A31–A4 **A3–A2**	I/O O	**Address Lines** A31–A2, together with the byte enable signals, BE3#–BE0#, define the physical area of memory or input/output space accessed. Address lines A31–A4 are used to drive addresses into the embedded ULP Intel486 GX processor to perform cache line invalidation. Input signals must meet setup and hold times t_{22} and t_{23}. A31–A2 are not driven during bus or address hold.
BE3# **BE2#** **BE1#** **BE0#**	O O O O	**Byte Enable** signals indicate active bytes during read and write cycles. During the first cycle of a cache fill, the external system should assume that all byte enables are active. BE3#–BE0# are active LOW and are not driven during bus hold. BE3# applies to processor data bits D31–D24 BE2# applies to processor data bits D23–D16 BE1# applies to processor data bits D15–D8 BE0# applies to processor data bits D7–D0 The byte enables can be used by the external system to generate address bits A1 and A0, as well as byte-high (D15–D8) and byte-low (D7–D0) enables. These are needed to interpret the 16-bit external data bus.
DATA BUS		
D15–D0	I/O	**Data Lines.** D7–D0 define the least significant byte of the data bus; D15–D8 define the most significant byte of the data bus. These signals must meet setup and hold times t_{22} and t_{23} for proper operation on reads. These pins are driven during the second and subsequent clocks of write cycles.
DP1 **DP0**	I/O	There is one **Data Parity** pin for each byte of the data bus. Data parity is generated on all write data cycles with the same timing as the data driven by the embedded ULP Intel486 GX processor. Even parity information must be driven back into the processor on the data parity pins with the same timing as read information to ensure that the correct parity check status is indicated by the processor. The signals read on these pins do not affect program execution. Input signals must meet setup and hold times t_{22} and t_{23}. DP1 and DP0 must be connected to V_{CCP} through a pull-up resistor in systems that do not use parity. DP1 and DP0 are active HIGH and are driven during the second and subsequent clocks of write cycles.

Table 4. Embedded ULP Intel486™ GX Processor Pin Descriptions (Sheet 2 of 6)

Symbol	Type	Name and Function
PCHK#	O	**Parity Status** is driven on the PCHK# pin the clock after ready for read operations. The parity status is for data sampled at the end of the previous clock. A parity error is indicated by PCHK# being LOW. Parity status is only checked for enabled bytes as indicated by the byte enable signals. PCHK# is valid only in the clock immediately after read data is returned to the processor. At all other times PCHK# is inactive (HIGH). PCHK# is never floated.
BUS CYCLE DEFINITION		
M/IO# **D/C#** **W/R#**	O O O	**Memory/Input-Output, Data/Control** and **Write/Read** lines are the primary bus definition signals. These signals are driven valid as the ADS# signal is asserted. **M/IO# D/C# W/R# Bus Cycle Initiated** 0 0 0 Interrupt Acknowledge 0 0 1 HALT/Special Cycle (see details below) 0 1 0 I/O Read 0 1 1 I/O Write 1 0 0 Code Read 1 0 1 Reserved 1 1 0 Memory Read 1 1 1 Memory Write **HALT/Special Cycle** **Cycle Name — BE3#–BE0# — A4–A2** Shutdown — 1110 — 000 HALT — 1011 — 000 Stop Grant bus cycle — 1011 — 100
LOCK#	O	**Bus Lock** indicates that the current bus cycle is locked. The embedded ULP Intel486 GX processor does not allow a bus hold when LOCK# is asserted (address holds are allowed). LOCK# goes active in the first clock of the first locked bus cycle and goes inactive after the last clock of the last locked bus cycle. The last locked cycle ends when Ready is returned. LOCK# is active LOW and not driven during bus hold. Locked read cycles are not transformed into cache fill cycles when KEN# is returned active.
PLOCK#	O	**Pseudo-Lock** indicates that the current bus transaction requires more than one bus cycle to complete. For the embedded ULP Intel486 GX processor, examples of such operations are segment table descriptor reads (64 bits) and cache line fills (128 bits). The embedded ULP Intel486 GX processor drives PLOCK# active until the addresses for the last bus cycle of the transaction are driven, regardless of whether RDY# or BRDY# have been returned. PLOCK# should be sampled only in the clock in which Ready is returned. PLOCK# is active LOW and is not driven during bus hold.
BUS CONTROL		
ADS#	O	**Address Status** output indicates that a valid bus cycle definition and address are available on the cycle definition lines and address bus. ADS# is driven active in the same clock in which the addresses are driven. ADS# is active LOW and not driven during bus hold.

4

Table 4. Embedded ULP Intel486™ GX Processor Pin Descriptions (Sheet 3 of 6)

Symbol	Type	Name and Function
RDY#	I	**Non-burst Ready** input indicates that the current bus cycle is complete. RDY# indicates that the external system has presented valid data on the data pins in response to a read or that the external system has accepted data from the embedded ULP Intel486 GX processor in response to a write. RDY# is ignored when the bus is idle and at the end of the first clock of the bus cycle. RDY# is active during address hold. Data can be returned to the embedded ULP Intel486 GX processor while AHOLD is active. RDY# is active LOW and is not provided with an internal pull-up resistor. RDY# must satisfy setup and hold times t_{16} and t_{17} for proper chip operation.
BURST CONTROL		
BRDY#	I	**Burst Ready** input performs the same function during a burst cycle that RDY# performs during a non-burst cycle. BRDY# indicates that the external system has presented valid data in response to a read or that the external system has accepted data in response to a write. BRDY# is ignored when the bus is idle and at the end of the first clock in a bus cycle. BRDY# is sampled in the second and subsequent clocks of a burst cycle. Data presented on the data bus is strobed into the embedded ULP Intel486 GX processor when BRDY# is sampled active. If RDY# is returned simultaneously with BRDY#, BRDY# is ignored and the burst cycle is prematurely aborted. BRDY# is active LOW and is provided with a small pull-up resistor. BRDY# must satisfy the setup and hold times t_{16} and t_{17}.
BLAST#	O	**Burst Last** signal indicates that the next time BRDY# is returned, the burst bus cycle is complete. BLAST# is active for both burst and non-burst bus cycles. BLAST# is active LOW and is not driven during bus hold.
INTERRUPTS		
RESET	I	**Reset** input forces the embedded ULP Intel486 GX processor to begin execution at a known state. The processor cannot begin executing instructions until at least 1ms after V_{CC}, V_{CCP}, and CLK have reached their proper DC and AC specifications. The RESET pin must remain active during this time to ensure proper processor operation. However, for warm resets, RESET should remain active for at least 15 CLK periods. RESET is active HIGH. RESET is asynchronous but must meet setup and hold times t_{20} and t_{21} for recognition in any specific clock.
INTR	I	**Maskable Interrupt** indicates that an external interrupt has been generated. When the internal interrupt flag is set in EFLAGS, active interrupt processing is initiated. The embedded ULP Intel486 GX processor generates two locked interrupt acknowledge bus cycles in response to the INTR pin going active. INTR must remain active until the interrupt acknowledges have been performed to ensure processor recognition of the interrupt. INTR is active HIGH and is not provided with an internal pull-down resistor. INTR is asynchronous, but must meet setup and hold times t_{20} and t_{21} for recognition in any specific clock.

Table 4. Embedded ULP Intel486™ GX Processor Pin Descriptions (Sheet 4 of 6)

Symbol	Type	Name and Function
NMI	I	**Non-Maskable Interrupt** request signal indicates that an external non-maskable interrupt has been generated. NMI is rising-edge sensitive and must be held LOW for at least four CLK periods before this rising edge. NMI is not provided with an internal pull-down resistor. NMI is asynchronous, but must meet setup and hold times t_{20} and t_{21} for recognition in any specific clock.
SRESET	I	**Soft Reset** pin duplicates all functionality of the RESET pin except that the SMBASE register retains its previous value. For soft resets, SRESET must remain active for at least 15 CLK periods. SRESET is active HIGH. SRESET is asynchronous but must meet setup and hold times t_{20} and t_{21} for recognition in any specific clock.
SMI#	I	**System Management Interrupt** input invokes System Management Mode (SMM). SMI# is a falling-edge triggered signal which forces the embedded ULP Intel486 GX processor into SMM at the completion of the current instruction. SMI# is recognized on an instruction boundary and at each iteration for repeat string instructions. SMI# does not break LOCKed bus cycles and cannot interrupt a currently executing SMM. The embedded ULP Intel486 GX processor latches the falling edge of one pending SMI# signal while it is executing an existing SMI#. The nested SMI# is not recognized until after the execution of a Resume (RSM) instruction.
SMIACT#	O	**System Management Interrupt Active**, an active LOW output, indicates that the embedded ULP Intel486 GX processor is operating in SMM. It is asserted when the processor begins to execute the SMI# state save sequence and remains active LOW until the processor executes the last state restore cycle out of SMRAM.
STPCLK#	I	**Stop Clock Request** input signal indicates a request was made to turn off or change the CLK input frequency. When the embedded ULP Intel486 GX processor recognizes a STPCLK#, it stops execution on the next instruction boundary (unless superseded by a higher priority interrupt), empties all internal pipelines and write buffers, and generates a Stop Grant bus cycle. STPCLK# is active LOW. **STPCLK# is an asynchronous signal, but must remain active until the embedded ULP Intel486 GX processor issues the Stop Grant bus cycle. STPCLK# may be de-asserted at any time after the processor has issued the Stop Grant bus cycle.**
BUS ARBITRATION		
BREQ	O	**Bus Request** signal indicates that the embedded ULP Intel486 GX processor has internally generated a bus request. BREQ is generated whether or not the processor is driving the bus. BREQ is active HIGH and is never floated.
HOLD	I	**Bus Hold Request** allows another bus master complete control of the embedded ULP Intel486 GX processor bus. In response to HOLD going active, the processor floats most of its output and input/output pins. HLDA is asserted after completing the current bus cycle, burst cycle or sequence of locked cycles. The embedded ULP Intel486 GX processor remains in this state until HOLD is de-asserted. HOLD is active HIGH and is not provided with an internal pull-down resistor. HOLD must satisfy setup and hold times t_{18} and t_{19} for proper operation.

Table 4. Embedded ULP Intel486™ GX Processor Pin Descriptions (Sheet 5 of 6)

Symbol	Type	Name and Function
HLDA	O	**Hold Acknowledge** goes active in response to a hold request presented on the HOLD pin. HLDA indicates that the embedded ULP Intel486 GX processor has given the bus to another local bus master. HLDA is driven active in the same clock that the processor floats its bus. HLDA is driven inactive when leaving bus hold. HLDA is active HIGH and remains driven during bus hold.
BOFF#	I	**Backoff** input forces the embedded ULP Intel486 GX processor to float its bus in the next clock. The processor floats all pins normally floated during bus hold but HLDA is not asserted in response to BOFF#. BOFF# has higher priority than RDY# or BRDY#; if both are returned in the same clock, BOFF# takes effect. The embedded ULP Intel486 GX processor remains in bus hold until BOFF# is negated. If a bus cycle is in progress when BOFF# is asserted the cycle is restarted. BOFF# is active LOW and must meet setup and hold times t_{18} and t_{19} for proper operation.
CACHE INVALIDATION		
AHOLD	I	**Address Hold** request allows another bus master access to the embedded ULP Intel486 GX processor's address bus for a cache invalidation cycle. The processor stops driving its address bus in the clock following AHOLD going active. Only the address bus is floated during address hold, the remainder of the bus remains active. AHOLD is active HIGH and is provided with a small internal pull-down resistor. For proper operation, AHOLD must meet setup and hold times t_{18} and t_{19}.
EADS#	I	**External Address** - This signal indicates that a *valid* external address has been driven onto the embedded ULP Intel486 GX processor address pins. This address is used to perform an internal cache invalidation cycle. EADS# is active LOW and is provided with an internal pull-up resistor. EADS# must satisfy setup and hold times t_{12} and t_{13} for proper operation.
CACHE CONTROL		
KEN#	I	**Cache Enable** pin is used to determine whether the current cycle is cacheable. When the embedded ULP Intel486 GX processor generates a cycle that can be cached and KEN# is active one clock before RDY# or BRDY# during the first transfer of the cycle, the cycle becomes a cache line fill cycle. Returning KEN# active one clock before RDY# during the last read in the cache line fill causes the line to be placed in the on-chip cache. KEN# is active LOW and is provided with a small internal pull-up resistor. KEN# must satisfy setup and hold times t_{14} and t_{15} for proper operation.
FLUSH#	I	**Cache Flush** input forces the embedded ULP Intel486 GX processor to flush its entire internal cache. FLUSH# is active LOW and need only be asserted for one clock. FLUSH# is asynchronous but setup and hold times t_{20} and t_{21} must be met for recognition in any specific clock.

Table 4. Embedded ULP Intel486™ GX Processor Pin Descriptions (Sheet 6 of 6)

Symbol	Type	Name and Function
PAGE CACHEABILITY		
PWT **PCD**	O O	**Page Write-Through** and **Page Cache Disable** pins reflect the state of the page attribute bits, PWT and PCD, in the page table entry, page directory entry or control register 3 (CR3) when paging is enabled. When paging is disabled, the embedded ULP Intel486 GX processor ignores the PCD and PWT bits and assumes they are zero for the purpose of caching and driving PCD and PWT pins. PWT and PCD have the same timing as the cycle definition pins (M/IO#, D/C#, and W/R#). PWT and PCD are active HIGH and are not driven during bus hold. PCD is masked by the cache disable bit (CD) in Control Register 0.
ADDRESS MASK		
A20M#	I	**Address Bit 20 Mask** pin, when asserted, causes the embedded ULP Intel486 GX processor to mask physical address bit 20 (A20) before performing a lookup to the internal cache or driving a memory cycle on the bus. A20M# emulates the address wraparound at 1Mbyte, which occurs on the 8086 processor. A20M# is active LOW and should be asserted only when the embedded ULP Intel486 GX processor is in real mode. This pin is asynchronous but should meet setup and hold times t_{20} and t_{21} for recognition in any specific clock. For proper operation, A20M# should be sampled HIGH at the falling edge of RESET.
TEST ACCESS PORT		
TCK	I	**Test Clock**, an input to the embedded ULP Intel486 GX processor, provides the clocking function required by the JTAG Boundary scan feature. TCK is used to clock state information (via TMS) and data (via TDI) into the component on the rising edge of TCK. Data is clocked out of the component (via TDO) on the falling edge of TCK. TCK is provided with an internal pull-up resistor.
TDI	I	**Test Data Input** is the serial input used to shift JTAG instructions and data into the processor. TDI is sampled on the rising edge of TCK, during the SHIFT-IR and SHIFT-DR TAP controller states. During all other Test Access Port (TAP) controller states, TDI is a "don't care." TDI is provided with an internal pull-up resistor.
TDO	O	**Test Data Output** is the serial output used to shift JTAG instructions and data out of the component. TDO is driven on the falling edge of TCK during the SHIFT-IR and SHIFT-DR TAP controller states. At all other times TDO is driven to the high impedance state.
TMS	I	**Test Mode Select** is decoded by the JTAG TAP to select test logic operation. TMS is sampled on the rising edge of TCK. To guarantee deterministic behavior of the TAP controller, TMS is provided with an internal pull-up resistor.
RESERVED PINS		
RESERVED	I	**Reserved** is reserved for future use. This pin MUST be connected to an external pull-up resistor circuit. The recommended resistor value is 10 KΩ.

Table 5. Output Pins

Name	Active Level	Output Signal		
		Floated During Address Hold	Floated During Bus Hold	During Stop Grant and Stop Clock States(1)
BREQ	HIGH			Previous State
HLDA	HIGH			As per HOLD
BE3#–BE0#	LOW		•	Previous State
PWT, PCD	HIGH		•	Previous State
W/R#, M/IO#, D/C#	HIGH/LOW		•	Previous State
LOCK#	LOW		•	HIGH (inactive)
PLOCK#	LOW		•	HIGH (inactive)
ADS#	LOW		•	HIGH (inactive)
BLAST#	LOW		•	Previous State
PCHK#	LOW			Previous State
A3–A2	HIGH	•	•	Previous State
SMIACT#	LOW			Previous State

NOTE:
1. The term "Previous State" means that the processor maintains the logic level applied to the signal pin just before the processor entered the Stop Grant state. This conserves power by preventing the signal pin from floating.

Table 6. Input/Output Pins

Name	Active Level	Output Signal		
		Floated During Address Hold	Floated During Bus Hold	During Stop Grant and Stop Clock States(1,2)
D15–D0	HIGH		•	Level-Keeper
DP1, DP0	HIGH		•	Level-Keeper
A31–A4	HIGH	•	•	Previous State

NOTE:
1. The term "Level-Keeper" means that the processor maintains the most recent logic level applied to the signal pin. This conserves power by preventing the signal pin from floating. If a system component, other than the processor, temporarily drives these signal pins and then floats them, the processor forces and maintains the most recent logic levels that were applied by the system component. The level keepers for DP1 and DP0 are always enabled.
2. The term "Previous State" means that the processor maintains the logic level applied to the signal pin just before the processor entered the Stop Grant state. This conserves power by preventing the signal pin from floating.

Table 7. Test Pins

Name	Input or Output	Sampled/ Driven On
TCK	Input	N/A
TDI	Input	Rising Edge of TCK
TDO	Output	Failing Edge of TCK
TMS	Input	Rising Edge of TCK

Table 8. Input Pins

Name	Active Level	Synchronous/ Asynchronous	Internal Pull-Up/ Pull-Down
CLK			
RESET	HIGH	Asynchronous	
SRESET	HIGH	Asynchronous	Pull-Down
HOLD	HIGH	Synchronous	
AHOLD	HIGH	Synchronous	Pull-Down
EADS#	LOW	Synchronous	Pull-Up
BOFF#	LOW	Synchronous	Pull-Up
FLUSH#	LOW	Asynchronous	Pull-Up
A20M#	LOW	Asynchronous	Pull-Up
KEN#	LOW	Synchronous	Pull-Up
RDY#	LOW	Synchronous	
BRDY#	LOW	Synchronous	Pull-Up
INTR	HIGH	Asynchronous	
NMI	HIGH	Asynchronous	
RESERVED			
SMI#	LOW	Asynchronous	Pull-Up
STPCLK#	LOW	Asynchronous	Pull-Up
TCK	HIGH		Pull-Up
TDI	HIGH		Pull-Up
TMS	HIGH		Pull-Up

4.0 ARCHITECTURAL AND FUNCTIONAL OVERVIEW

The embedded ULP Intel486 GX processor architecture is essentially the same as the 3.3V Intel486 SX processor with a 1X clock (CLK) input. Refer to the *Intel486™ Processor Family* datasheet (242202) for a description of the Intel486 SX processor. With some minor exceptions, the following datasheet sections apply to the embedded ULP Intel486 GX processor:

- Architectural Overview
- Real Mode Architecture
- Protected Mode Architecture
- On-Chip Cache
- System Management Mode (SMM) Architectures
- Hardware Interface
- Bus Operation
- Testability
- Debugging Support
- Instruction Set Summary
- Differences Between Intel486 Processors and Intel386™ Processors

Exceptions to these sections of the datasheet are:

- The embedded ULP Intel486 GX processor has a 16-bit external data bus and two data parity signals. While it has four byte-enable signals (BE3# – BE0#), the external system must generate address bits A1, A0 as well as enables for each byte of the 16-bit external data bus. More information about byte enables is provided in this datasheet.
- The information pertaining to dynamic bus sizing of the external data bus does not apply. The embedded ULP Intel486 GX processor does not have the BS8# signal pin.

- The embedded ULP Intel486 GX processor bursts data cycles similar to an Intel486 SX processor with bus-sizing BS16# active.
- References to the Upgrade Power Down Mode do not apply. The embedded ULP Intel486 GX processor does not have the UP# signal pin and does not support the Intel OverDrive® processor.
- References to "V_{CC}" are called "V_{CCP}" by the embedded ULP Intel486 GX processor when the supply voltage pertains to the processor's external interface drivers and receivers. The term "V_{CC}" pertains only to the processor core supply voltage of the embedded ULP Intel486 GX processor. Information about the split-supply voltage is provided in this datasheet.
- The Phase-Locked Loop (PLL) circuit of the 1X clock (CLK) input has been replaced by a proprietary Differential Delay Line (DDL) circuit that has a faster recovery time. Datasheet references to the PLL and its 1 ms recovery time are replaced with the DDL circuit and its eight-CLK recovery time. Information about the DDL circuit and recovery time is provided in this datasheet.
- The embedded ULP Intel486 GX processor has level-keeper circuits for its external 16-bit data bus (D15–D0) and data parity (DP1, DP0) signals. The Intel486 SX processor floats these signals instead. More information about the level-keeper circuitry is provided in this datasheet.
- The datasheet describes the processor supply-current consumption for the Auto HALT Power Down, Stop Grant, and Stop Clock states. This supply-current consumption for the embedded ULP Intel486 GX processor is much less than that of the Intel486 SX processor. Information about power consumption and these states is provided in this datasheet.
- The CPU ID, Boundary-Scan (JTAG) ID, and boundary-scan register bits for the embedded ULP Intel486 GX processor are in this datasheet.
- The embedded ULP Intel486 GX processor has one pin reserved for possible future use. This pin is an input signal, pin 166. It is called RESERVED and must be connected to a 10-KΩ pull-up resistor.

4.1 Separate Supply Voltages

The embedded ULP Intel486 GX processor has separate voltage-supply planes for its internal core-processor circuits and its external driver/receiver circuits. The supply voltage for the internal core processor is named V_{CC} and the supply voltage for the external circuits is named V_{CCP}.

For a single-supply voltage design, the embedded ULP Intel486 GX processor is functional at 3.3V ± 0.3V. In this type of system design, the processor's V_{CC} and V_{CCP} pins must be tied to the same power plane.

Even though V_{CCP} must be 3.3V ± 0.3V, the processor's external-output circuits can drive TTL-compatible components. However, the processor's external-input circuits do not allow connection to TTL-compatible components. **Section 5.2, DC Specifications** contains the DC specifications for the processor's input and output signals.

For lower-power operation, a separate, lower voltage for V_{CC} can be chosen, but V_{CCP} must be 3.3V ± 0.3V. Any voltage value between 2.0V and 3.3V can be chosen for V_{CC} for guaranteed processor operation up to 16 MHz. The embedded ULP Intel486 GX processor can also operate at 33 MHz, provided the V_{CC} value chosen is between 2.7V and 3.3V. **Section 5.2, DC Specifications** defines supply voltage specifications.

In systems with separate V_{CC} and V_{CCP} power planes, the processor-core voltage supply must always be less than or equal to the processor's external-interface voltage supply; e.g., the system design must guarantee:

$$V_{CC} \leq V_{CCP}$$

Violating this relationship causes excessive power consumption. Limited testing has shown no component damage when this relationship is violated. However, prolonged violation is not recommended and component integrity is not guaranteed.

The $V_{CC} \leq V_{CCP}$ relationship must also be guaranteed by the system design during power-up and power-down sequences. Refer to Figure 3.

Even though V_{CC} must be less than or equal to V_{CCP}, it is recommended that the system's power-on sequence allows V_{CC} to quickly achieve its op-

erational level once V_{CCP} achieves its operational level. Similarly, the power-down sequence should allow V_{CCP} to power down quickly after V_{CC} is below the operational voltage level. These recommendations are given to keep power consumption at a minimum. Deviating from the recommendations does not create a component reliability problem, but power consumption of the processor's external interface circuits increases beyond normal operating values.

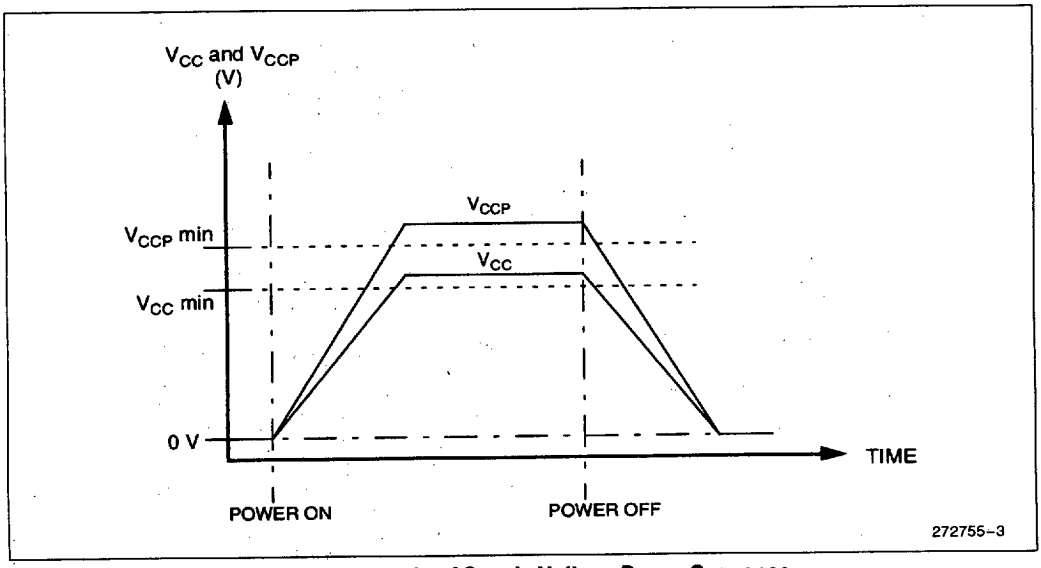

Figure 3. Example of Supply Voltage Power Sequence

4.2 Fast Clock Restart

The embedded ULP Intel486 GX processor has an integrated proprietary differential delay line (DDL) circuit for internal clock generation. The DDL is driven by the CLK input signal provided by the external system. During normal operation, the external system must guarantee that the CLK signal maintains its frequency so that the clock period deviates no more than 250 ps/CLK. This state, called the Normal State, is shown in Figure 4.

To increase or decrease the CLK frequency more quickly than this, the system must interrupt the processor with the STPCLK# signal. Once the processor indicates that it is in the Stop Grant State, the system can adjust the CLK signal to the new frequency, wait a minimum of eight CLK periods, then force the processor to return to the normal operational state by deactivating the STPCLK# interrupt.

This wait of eight CLK periods is much faster than the 1ms wait required by earlier Intel486 SX processor products.

While in the Stop Grant State, the external system may deactivate the CLK signal to the processor. This forces the processor to the Stop Clock State—the state in which the processor consumes the least power. Once the system reactivates the CLK signal, the processor transitions to the Stop Grant State within eight CLK periods.

Normal operation can be resumed by deactivating the STPCLK# interrupt signal. Here again, the embedded ULP Intel486 GX processor recovers from the Stop Clock State much faster than the 1ms PLL recovery of earlier Intel486 SX processors.

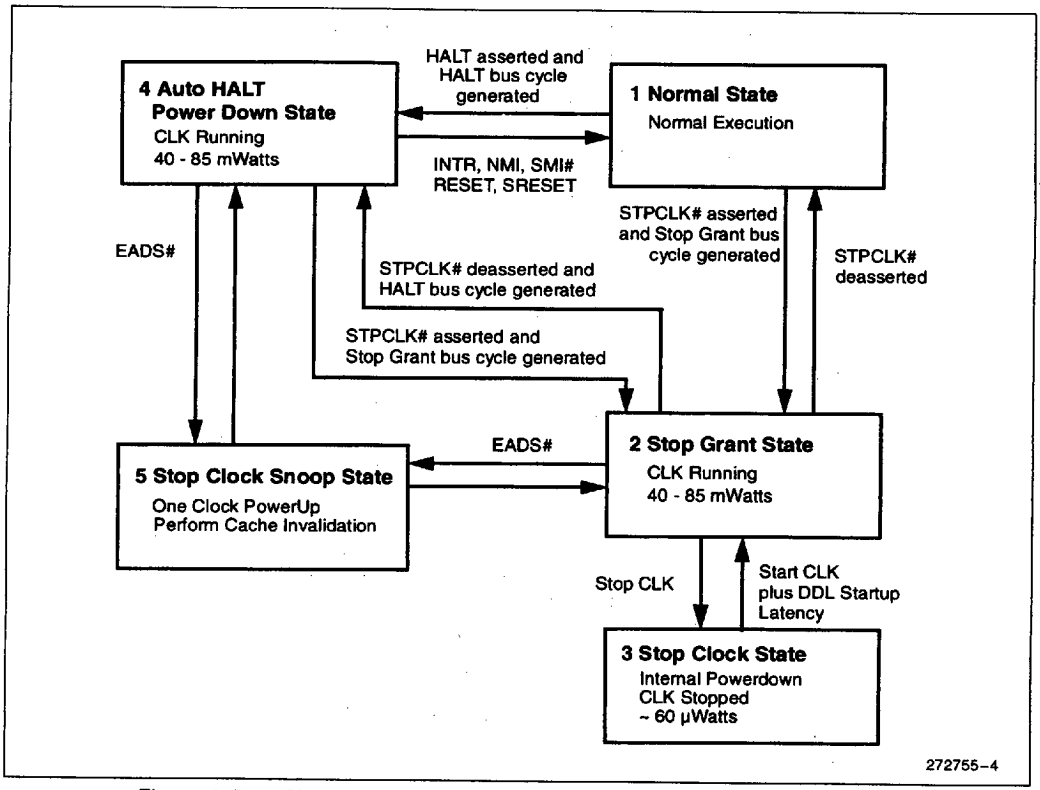

Figure 4. Stop Clock State Diagram with Typical Power Consumption Values

4.3 Level-Keeper Circuits

To obtain the lowest possible power consumption during the Stop Grant and Stop Clock states, system designers must ensure that:

- input signals with pull-up resistors are not driven LOW
- input signals with pull-down resistors are not driven HIGH

See Table 8, Input Pins for the list of signals with internal pull-up and pull-down resistors.

All other input pins except A31–A4, D15–D0, DP1, and DP0 must be driven to the power supply rails to ensure lowest possible current consumption.

During the Stop Grant and Stop Clock states, most processor output signals maintain their previous condition, which is the level they held when entering the Stop Grant state. In response to HOLD driven active during the Stop Grant state when the CLK input is running, the embedded ULP Intel486 GX processor generates HLDA and floats all output and input/output signals which are floated during the HOLD/HLDA state. When HOLD is deasserted, processor signals which maintain their previous state return to the state they were in prior to the HOLD/HLDA sequence.

The data bus (D15–D0) and parity bits also maintain their previous states during the Stop Grant and Stop Clock states, but do so differently, as described in the following paragraphs.

The embedded ULP Intel486 GX processor's data bus pins (D15–D0) and data parity pins have level keepers which maintain their previous states while in the Stop Grant and Stop Clock states. In response to HOLD driven active during the Stop Grant state when the CLK input is running, the embedded ULP Intel486 GX processor generates HLDA and floats D15–D0, DP1 and DP0 throughout the HOLD/HLDA cycles. When HOLD is deasserted, the processor's D15–D0, DP1 and DP0 signals return to the states they were in prior to the HOLD/HLDA sequence.

At all other times during the Stop Grant and Stop Clock states, the processor maintains the logic levels of D15–D0, DP1 and DP0. When the external system circuitry drives D15–D0, DP1 and DP0 to different logic levels, the processor flips its D15–D0, DP1 and DP0 logic levels to match the ones driven by the external system. The processor maintains (keeps) these new levels even after the external circuitry stops driving D15–D0, DP1 and DP0.

For some system designs, external resistors may not be required on D15–D0, DP1 and DP0 (they are required on previous Intel486 SX processor designs). System designs that never request Bus Hold during the Stop Grant and Stop Clock states might not require external resistors. If the system design uses Bus Hold during these states, the processor disables the level-keepers and floats the data bus. This type of design would require some kind of data bus termination to minimize power consumption. It is strongly recommended that the D15–D0, DP1 and DP0 pins do not have network resistors connected. External resistors used in the system design must be of a sufficient resistance value to "flip" the level-keeper circuitry and eliminate potential DC paths.

The level-keeper circuits for DP1 and DP0 are always enabled, while the level-keeper circuits for D15–D0 are enabled only during the Stop Grant and Stop Clock states.

The level-keeper circuit is designed to allow an external 27-KΩ pull-up resistor to switch the D15–D0, DP1 and DP0 circuits to a logic-HIGH level even though the level-keeper attempts to keep a logic-LOW level. In general, pull-up resistors smaller than 27 KΩ can be used as well as those greater than or equal to 1 MΩ. Pull-down resistors, when connected to D15–D0, DP1 and DP0, should be least 800 KΩ.

4.4 Low-Power Features

As with other Intel486 processors, the embedded ULP Intel486 GX processor minimizes power consumption by providing the Auto HALT Power Down, Stop Grant, and Stop Clock states (see Figure 4). The embedded ULP Intel486 GX processor has an Auto Clock Freeze feature that further conserves power by judiciously deactivating its internal clocks while in the Normal Execution Mode. The power-conserving mechanism is designed such that it does not degrade processor performance or require changes to AC timing specifications.

4.4.1 Auto Clock Freeze

To reduce power consumption, during the following bus cycles—under certain conditions—the processor slows-up or freezes some internal clocks:

- Data-Read Wait Cycles (Memory, I/O and Interrupt Acknowledge)
- Data-Write Wait Cycles (Memory, I/O)
- HOLD/HLDA Cycles
- AHOLD Cycles
- BOFF Cycles

Power is conserved during the wait periods in these cycles until the appropriate external-system signals are sent to the processor. These signals include:

- READY
- NMI, SMI#, INTR, and RESET
- BOFF#
- FLUSH#
- EADS#
- KEN# transitions

The embedded ULP Intel486 GX processor also reduces power consumption by temporarily freezing the clocks of its internal logic blocks. When a logic block is idle or in a wait state, its clock is frozen.

4.5 Bus Interface and Operation

4.5.1 16-Bit Data Bus

The bi-directional lines, D15–D0, form the data bus for the embedded ULP Intel486 GX processor. D7–D0 define the least-significant byte and D15–D8 the most-significant byte. Data transfers are possible only to 16-bit devices. Bus-sizing for 8-bit devices (BS8# signal pin) is not supported by the processor. In some cases, external circuitry is needed for the processor to interface with 8-bit devices. An example of when external circuitry is not needed is an 8-bit I/O port that is mapped to a byte address. Here only part of the 16-bit data word is meant for the device and BS8# is not needed.

D15–D0 are active HIGH. For reads, D15–D0 must meet the setup and hold times, t_{22} and t_{23}. D15–D0 are not driven during read cycles and bus hold.

4.5.2 Parity

Parity operation is the same as it is for the rest of the Intel486 processor family, with these exceptions:

- DP0 and DP1 are the data parity pins for the processor. There is one parity signal for each byte of the external data bus. Input signals on DP0 and DP1 must meet the setup and hold times, t_{22} and t_{23}. In systems not using parity, DP0 and DP1 must be connected to V_{CCP} through a pull-up resistor.
- The data parity pins have level-keeper circuits which are described later.

4.5.3 Data Transfer Mechanism

Data transfers operate in a manner similar to data transfers on the 32-bit data bus members of the Intel486 processor family with the BS16# pin driven active. For 32-bit data-bus family members, such 16-bit data transfers involve all 32 bits of their external data busses and all four parity bits. Since the embedded ULP Intel486 GX processor has a 16-bit external data bus, all data transfers occur on the low order data bits, D0 through D15. Parity is generated and checked on DP0 and DP1. Dynamic Data Bus Sizing (BS16#, and BS8#) is not supported. All address bits (A31–A2) and byte enables (BE0#, BE1#, BE2#, and BE3#) are supported. Address bits A1 and A0 can be generated from the byte-enable signals in the same manner as the other Intel486 processors. Typically in 16-bit data bus designs, A1, byte-low enable (BLE), and byte-high enable (BHE) are needed and can be generated from the four byte-enable signals. Figure 5 shows the logic that can be used to generate A1, BHE#, and BLE#.

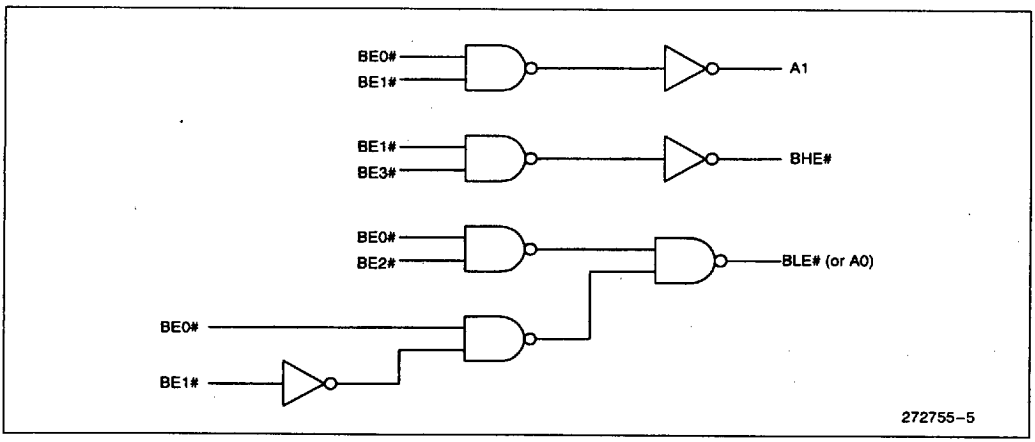

Figure 5. Logic to Generate A1, BHE# and BLE#

Table 9 contains the list of valid byte-enable combinations and how the 16-bit external data bus is interpreted.

Table 9. Valid Byte-Enable Cycles

Case	Byte Enables				From External Circuitry (Note 1)				External Data Bus	
	BE3#	BE2#	BE1#	BE0#	A1	A0	BHE#	BLE# (A0)	D15–D8, DP1	D7–D0 DP0
1	1	1	1	0	0	0	1	0	-	valid
2	1	1	0	0	0	0	0	0	valid	valid
3	1	0	0	0	0	0	0	0	valid	valid
4	0	0	0	0	0	0	0	0	valid	valid
5	1	1	0	1	0	1	0	1	valid	-
6	1	0	0	1	0	1	0	1	valid	-
7	0	0	0	1	0	1	0	1	valid	-
8	1	0	1	1	1	0	1	0	-	valid
9	0	0	1	1	1	0	0	0	valid	valid
10	0	1	1	1	1	1	0	1	valid	-

NOTE:
1. If the external system indicates to the processor that a read is cacheable, the processor initiates a cache-line fill. In this case, the external system should ignore BE3#, BE2#, BE1#, and BE0# and force A1, A0, and BHE# to a low logic level (0) for the first cycle of the transfer. This forces a memory read to start from a data address having its least significant digit 0, 4, 8, or C (hex). The byte-enable decodes for subsequent cycles of the line fill follow the table information as listed.

Except for the initial transfer of a cache-line fill, the Byte Enables BE3#, BE2#, BE1#, and BE0# for cases 1, 2, 5, 8, 9, and 10 indicate either a one-, or two-byte data transfer that can be accomplished in one 16-bit data cycle.

Except for the initial transfer of a cache-line fill, the Byte Enables BE3#, BE2#, BE1#, and BE0# for cases 3, 4, 6, and 7 indicate the transfer of two, three, or four data bytes that cannot be accomplished in one 16-bit data cycle. In these cases, the processor attempts to complete the partial transfer using an additional data cycle. The additional cycle could be burst by the processor (processor could respond with BLAST# unasserted for case 3, 4, 6, or 7). This is true for both memory and I/O reads and writes. There is more information about bursting in later sections.

During write cycles, valid data is only driven onto the external data bus pins corresponding to active byte enables. Other pins of the data bus are driven but do not contain valid data.

NOTE:
Unlike the Intel386™ processor, the embedded ULP Intel486 GX processor does not duplicate write data onto the parts of the data bus for which the corresponding byte enable is inactive.

4.5.3.1 Multiple and Burst Cycle Bus Transfers

The embedded ULP Intel486 GX processor, like all other Intel486 processors, requires more than one data cycle to read or write data having bit widths greater than 32. Examples of this data are cache lines (128 bits) and instruction prefetches (128 bits). In addition, the embedded ULP Intel486 GX processor requires multiple data cycles to transfer data having bit widths greater than 16. An example is a doubleword operand (32 bits). Transferring misaligned 16-bit words also requires multiple data cycles.

If a multiple data cycle is a memory-read or I/O-read data transfer, the processor could use burst cycles to perform the transfer. The processor could also burst misaligned 16-bit and 32-bit memory-write or I/O-write data transfers.

In designing a memory and I/O port controller for the embedded ULP Intel486 GX processor, knowledge of the address sequence for burst cycles can be used to provide high-speed data access (minimal number of wait states). The following sections describe this sequence.

4.5.3.2 Cacheable Cycles

The embedded ULP Intel486 GX processor uses burst cycles to perform a cache line fill. Because of its 16-bit external data bus, the processor bursts eight data cycles to read a 128-bit (16-byte) cache line from system memory. During the first cycle of the cache line transfer, the external system must ignore BE3#, BE2#, BE1#, and BE0# presented by the processor and proceed as if A1, A0, and BHE# were logic-low levels (0). This forces the memory read to start from a data address having its least significant hexadecimal digit 0, 4, 8, or C. The byte enables presented by the processor for subsequent cycles are decoded in the usual way by the external system. The sequences of data addresses are shown in Table 10. Like the rest of the Intel486 processor family, the initial value of A31–A4, M/IO#, W/R#, and D/C# are presented by the processor throughout the cache line fill. Also, the burst sequence can be terminated by the processor at any time by with an active BLAST# signal.

Table 10. Address Sequence for Cache Line Transfers and Instruction Prefetches

Starting Address (Least significant hexadecimal digit)	Data Cycle	Signals from the Processor				Address of Expected Read Data	
		A3 A2	Byte Enables BE3#–BE0#	A3–A0 (Hex)	BLAST#	D15–D8, DP1	D7–D0, DP0
0, 1, 2, 3	1	00	0000	0	1	1	0
	2	00	0011	2	1	3	2
	3	01	0000	4	1	5	4
	4	01	0011	6	1	7	6
	5	10	0000	8	1	9	8
	6	10	0011	A	1	B	A
	7	11	0000	C	1	D	C
	8	11	0011	E	0	F	E
4, 5, 6, 7	1	01	0000	4	1	5	4
	2	01	0011	6	1	7	6
	3	01	0000	0	1	1	0
	4	00	0011	2	1	3	2
	5	11	0000	C	1	D	C
	6	11	0011	E	1	F	E
	7	10	0000	8	1	9	8
	8	10	0011	A	0	B	A
8, 9, A, B	1	10	0000	8	1	9	8
	2	10	0011	A	1	B	A
	3	11	0000	C	1	D	C
	4	11	0011	E	1	F	E
	5	00	0000	0	1	1	0
	6	00	0011	2	1	3	2
	7	01	0000	4	1	5	4
	8	01	0011	6	0	7	6
C, D, E, F	1	11	0000	C	1	D	C
	2	11	0011	E	1	F	E
	3	10	0000	8	1	9	8
	4	10	0011	A	1	B	A
	5	01	0000	4	1	5	4
	6	01	0011	6	1	7	6
	7	00	0000	0	1	1	0
	8	00	0011	2	0	3	2

Whenever its cache circuitry is not busy, the processor uses this same bursting mechanism for prefetching instructions (128 bits, 16 bytes), even if the instructions are not indicated as cacheable by the external system. Instruction prefetches can occur that use the address sequencing shown in Table 10. The initial value of A31–A4, M/IO#, W/R#, and D/C# are presented by the processor throughout the 128-bit prefetch burst. It is possible for the processor to prefetch instructions not needed. The burst sequence can be terminated by the processor at any time with an active BLAST# signal.

4.5.3.3 Non-Cacheable Cycles

For memory and I/O data transfers, the embedded ULP Intel486 GX processor determines how many data cycles are required for the transfer based on its internal information. This information includes the byte-length of the data, the transfer's starting data address, and data alignment. For memory reads, the processor resorts to the 128-bit cache-line address sequence described above if the external system indicates the data is cacheable. Otherwise, the processor uses its internal information to determine whether to burst the data cycles of a multiple-cycle transfer. In some cases, the transfer can be performed entirely by burst cycles. In other cases, a combination of burst cycles and single cycles are required to perform the data transfer. There are also cases for which burst cycles cannot be used and the transfer consists of multiple cycles, each beginning with the ADS# signal.

I/O Writes, I/O Reads, and Memory Writes

If the processor initiates bursting (BLAST# inactive) during an I/O Write, I/O Read or Memory Write, the duration of the burst is a maximum of four bytes (32 bits). All of the possible burst situations are listed in Table 11. In all cases, the burst is two data cycles. The control signals M/IO#, D/C#, W/R#, address bits A31–A4 as well as A3 and A2 remain constant throughout each two-cycle burst.

Table 11. Valid Burst Cycle Sequences—I/O Reads and All Writes

Starting Address (Least significant hexadecimal digit)	Data Cycle	Signals from the Processor				Address of Expected Read Data	
		A3 A2	Byte Enables BE3#–BE0#	A3–A0 (Hex)	BLAST#	D15–D8, DP1	D7–D0, DP0
0, 4, 8, C	1	A3 A2	0 0 0 0	0, 4, 8, C	1	2nd	1st
	2	A3 A2	0 0 1 1	2, 6, A, E	0	4th	3rd
1, 5, 9, D	1	A3 A2	0 0 0 1	1, 5, 9, D	1	1st	-
	2	A3 A2	0 0 1 1	2, 6, A, E	0	3rd	2nd
1, 5, 9, D	1	A3 A2	1 0 0 1	1, 5, 9, D	1	1st	-
	2	A3 A2	1 0 1 1	2, 6, A, E	0	-	2nd
2, 6, A, E	1	A3 A2	1 0 0 0	0, 4, 8, C	1	2nd	1st
	2	A3 A2	1 0 1 1	2, 6, A, E	0	-	3rd

Non-Cacheable Memory Reads

When the processor initiates bursting, the duration of the burst is a maximum of 16 bytes (128 bits).

Non-cacheable instruction prefetches can be 16 bytes in duration. The possible burst sequences are the same as for cache-line transfers listed in Table 11. The burst sequence can be terminated at any time with an active BLAST# signal.

The length of a burst transfer can be 16, eight, or fewer than eight bytes.

For burst lengths of eight or less, the entire burst transfer is confined to a quad-word (eight-byte) data boundary of system memory. A31–A3 remain constant throughout this type of burst transfer.

4.5.3.4 Burst Transfer Address Prediction

The processor provides the data address (A31–A2) and byte enables (BE3#–BE0#) for the first data cycle while ADS# is inactive. The initial values for A1, BHE# and BLE# (A0) can be derived from the byte enables. If bursting is anticipated, the next data address can be predicted at this time and can be used by the memory controller to perform burst data transfers with minimal wait states. Rather than list all of the burst mode address combinations, a general algorithm is provided in Figure 6. This algorithm holds true for all burst transfers including cache-line fills, instruction prefetches, I/O and memory-write data transfers described in earlier sections.

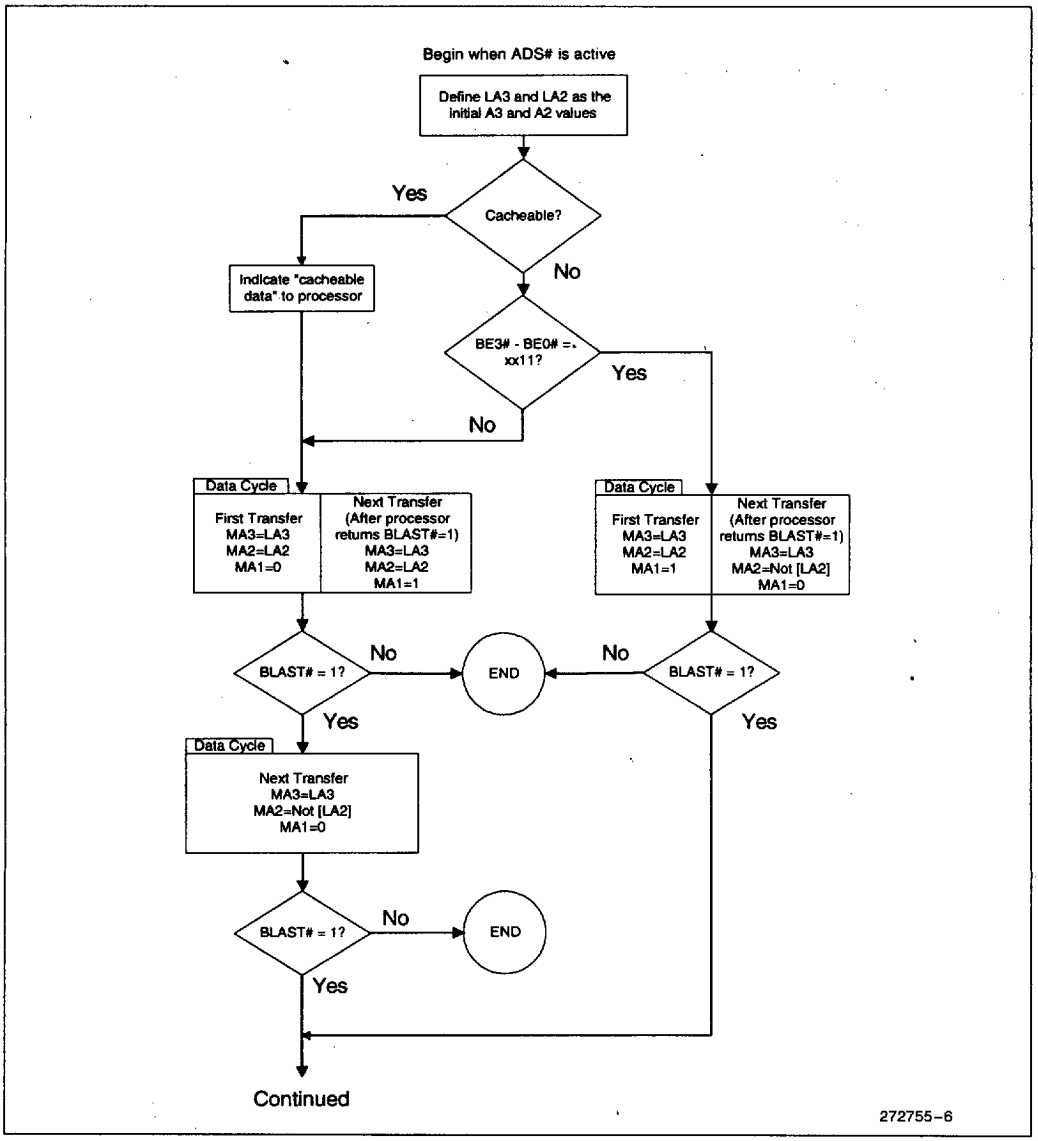

Figure 6. Address Prediction for Burst Transfers (1 of 3)

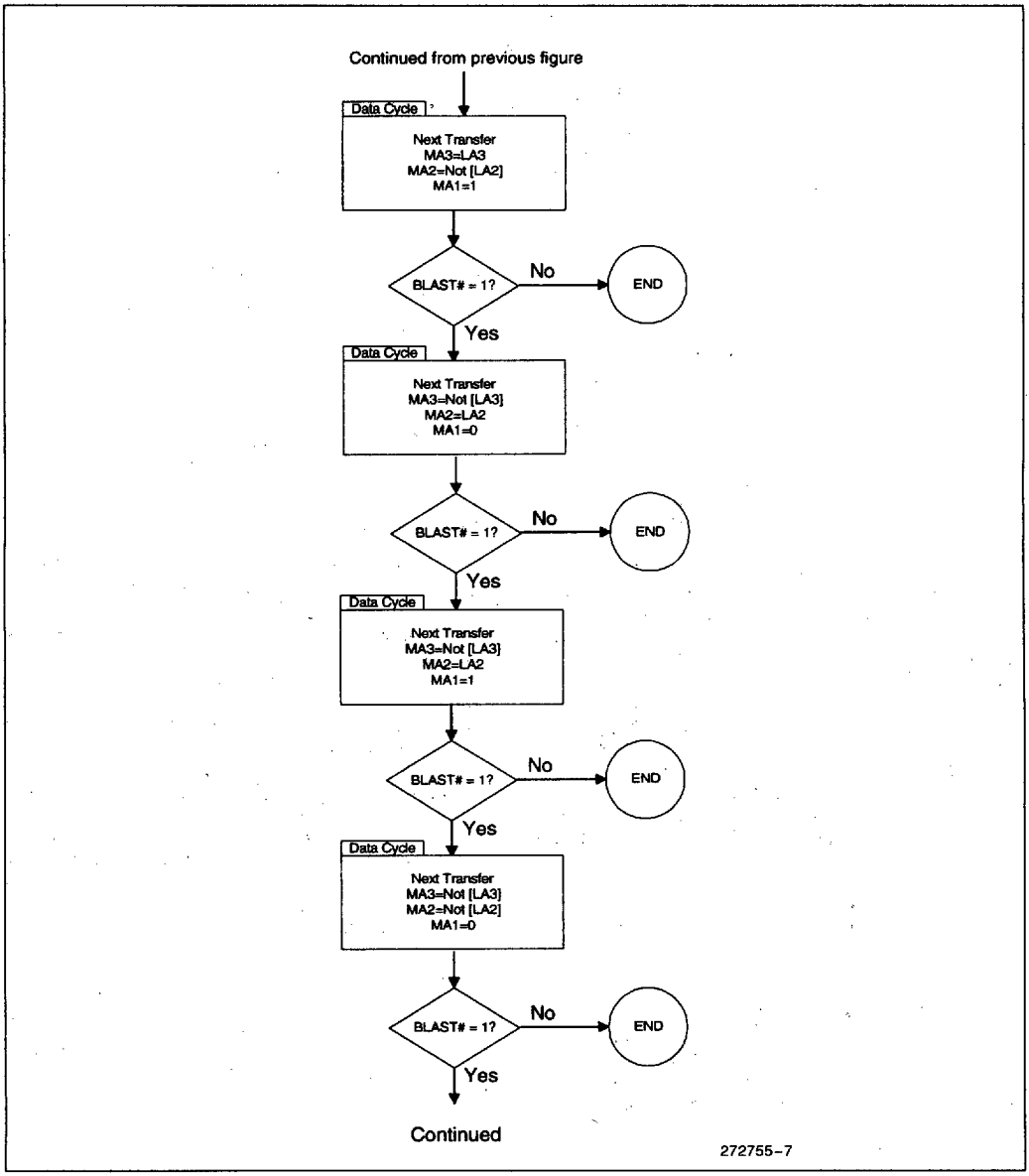

Figure 7. Address Prediction for Burst Transfers (2 of 3)

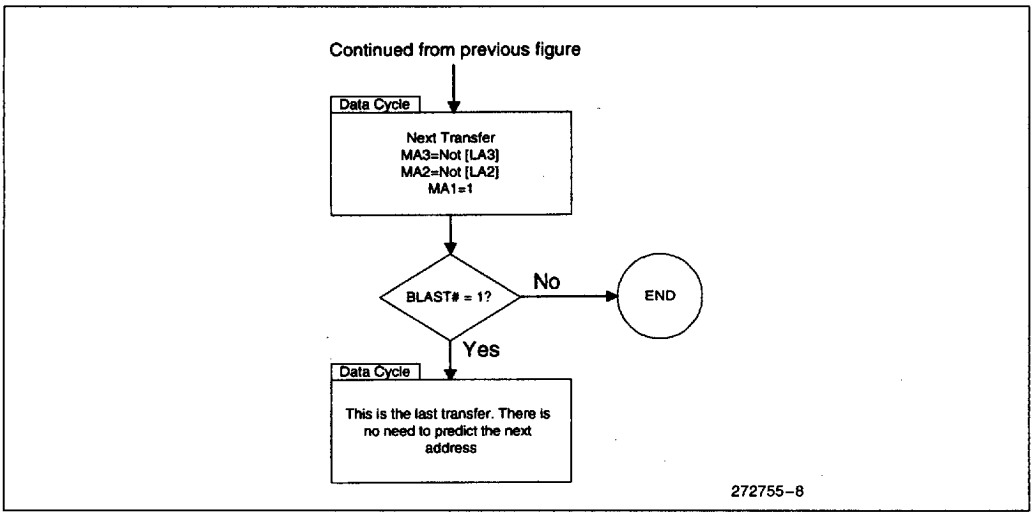

Figure 8. Address Prediction for Burst Transfers (3 of 3)

In the figure, MA3, MA2, and MA1 are memory address bits. LA3 and LA2 are the saved, initial values of A3 and A2 respectively. The term "MA2 = NOT [LA2]" means that MA2 is the opposite logic state as the saved initial A2 value. MA31–MA4 are derived directly from A31–A4, which remain constant throughout the burst transfer. M/IO#, W/R#, and D/C# also remain constant. BLE# (A0) is not shown, but is always active (LOW) throughout the transfer. BHE#, also not shown, cannot be predicted for the last data cycle of a burst transfer and must be decoded from the byte enable bits for the last burst cycle (follows BLAST# = 0). Otherwise BHE# is always active (LOW) throughout the burst. The processor defines "cacheable data" as the case where PCD is inactive (LOW) and LOCK# is inactive (HIGH) and KEN# is active (LOW).

4.6 CPUID Instruction

The embedded ULP Intel486 GX processor supports the CPUID instruction (see Table 12). Because not all Intel processors support the CPUID instruction, a simple test can determine if the instruction is supported. The test involves the processor's ID Flag, which is bit 21 of the EFLAGS register. If software can change the value of this flag, the CPUID instruction is available. The actual state of the ID Flag bit is irrelevant and provides no significance to the hardware. This bit is cleared (reset to zero) upon device reset (RESET or SRESET) for compatibility with Intel486 processor designs that do not support the CPUID instruction.

CPUID-instruction details are provided here for the embedded ULP Intel486 GX processor. Refer to Intel Application Note AP-485 *Intel Processor Identification with the CPUID Instruction* (Order No. 241618) for a description that covers all aspects of the CPUID instruction and how it pertains to other Intel processors.

4.6.1 Operation of the CPUID Instruction

The CPUID instruction requires the software developer to pass an input parameter to the processor in the EAX register. The processor response is returned in registers EAX, EBX, EDX, and ECX.

Table 12. CPUID Instruction Description

OP CODE	Instruction	Processor Core Clocks	Parameter passed in EAX (Input Value)	Description
0F A2	CPUID	9	0	Vendor (Intel) ID String
		14	1	Processor Identification
		9	> 1	Undefined (Do Not Use)

Vendor ID String—When the parameter passed in EAX is 0 (zero), the register values returned upon instruction execution are shown in the following table.

		31 – – – – – – 24	23 – – – – – – 16	15 – – – – – – 8	7 – – – – – – 0
High Value (= 1)	**EAX**	0000	0000	0000	0001
Vendor ID String	**EBX**	u (75)	n (6E)	e (65)	G (47)
(ASCII	**EDX**	I (49)	e (65)	n (6E)	i (69)
Characters)	**ECX**	l (6C)	e (65)	t (74)	n (6E)

The values in EBX, EDX and ECX indicate an Intel processor. When taken in the proper order, they decode to the string "GenuineIntel."

Processor Identification—When the parameter passed to EAX is 1 (one), the register values returned upon instruction execution are:

		31 – – – – 14	13, 12	11 – – – 8	7 – – – 4	3 – – – 0
Processor Signature	**EAX**	(Do Not Use) Intel Reserved	00 Processor Type	0100 Family	0010 Model	XXXX Stepping

(Intel releases information about stepping numbers as needed)

		31 – 0
Intel Reserved	**EBX**	Intel Reserved
(Do Not Use)	**ECX**	Intel Reserved

		31 – – – – – – – – – – – – – – – – 2	1	0
Feature Flags	**EDX**	0 0	1 VME	0 FPU

4.7 Identification After Reset

Processor Identification—Upon reset, the EDX register contains the processor signature:

		31 – – – – 14	13, 12	11 – – – 8	7 – – – 4	3 – – – 0
Processor Signature	**EDX**	(Do Not Use) Intel Reserved	00 Processor Type	0100 Family	0010 Model	XXXX Stepping

(Intel releases information about stepping numbers as needed)

4.8 Boundary Scan (JTAG)

4.8.1 Device Identification

Table 13 shows the 32-bit code for the embedded ULP Intel486 GX processor which is loaded into the Device Identification Register.

Table 13. Boundary Scan Component Identification Code

Version	Part Number				Mfg ID	1
	V_{CC} 0=5V 1=3.3V	Intel Architecture Type	Family 0100 = Intel486 CPU Family	Model 00100 = embedded ULP Intel486 SX processor	009H = Intel	
31 - - - 28	27	26 - - - - - 21	20 - - - - 17	16 - - - - - 12	11 - - - - - 1	0
XXXX	1	000001	0100	00010	00000001001	1

(Intel releases information about version numbers as needed)
Boundary Scan Component Identification Code = x828 4013 (Hex)

4.8.2 Boundary Scan Register Bits and Bit Order

The boundary scan register contains a cell for each pin as well as cells for control of bidirectional and three-state pins. There are "Reserved" bits which correspond to no-connect (N/C) signals of the embedded ULP Intel486 GX processor. Control registers WRCTL, ABUSCTL, BUSCTL, and MISCCTL are used to select the direction of bidirectional or three-state output signal pins. A "1" in these cells designates that the associated bus or bits are floated if the pins are three-state, or selected as input if they are bidirectional.

- WRCTL controls D15–D0, DP1 and DP0
- ABUSCTL controls A31–A2
- BUSCTL controls ADS#, BLAST#, PLOCK#, LOCK#, W/R#, BE0#, BE1#, BE2#, BE3#, M/IO#, D/C#, PWT, and PCD
- MISCCTL controls PCHK#, HLDA, and BREQ

The following is the bit order of the embedded ULP Intel486 GX processor boundary scan register:

TDO ← A2, A3, A4, A5, RESERVED, A6, A7, A8, A9, A10, A11, A12, A13, A14, A15, A16, A17, A18, A19, A20, A21, A22, A23, A24, A25, A26, A27, A28, A29, A30, A31, DP0, D0, D1, D2, D3, D4, D5, D6, D7, DP1, D8, D9, D10, D11, D12, D13, D14, D15, Reserved, Reserved, Reserved, Reserved, Reserved, Reserved, Reserved, Reserved, Reserved, Reserved, Reserved, Reserved, Reserved, Reserved, Reserved, Reserved, Reserved, STPCLK#, Reserved, Reserved, SMI#, SMIACT#, SRESET, NMI, INTR, FLUSH#, RESET, A20M#, EADS#, PCD, PWT, D/C#, M/IO#, BE3#, BE2#, BE1#, BE0#, BREQ, W/R#, HLDA, CLK, Reserved, AHOLD, HOLD, KEN#, RDY#, Reserved, Reserved, BOFF#, BRDY#, PCHK#, LOCK#, PLOCK#, BLAST#, ADS#, MISCCTL, BUSCTL, ABUSCTL, WRCTL ← **TDI**

5.0 ELECTRICAL SPECIFICATIONS

5.1 Maximum Ratings

Table 14 is a stress rating only. Extended exposure to the Maximum Ratings may affect device reliability.

Furthermore, although the embedded ULP Intel486 GX processor contains protective circuitry to resist damage from electrostatic discharge, always take precautions to avoid high static voltages or electric fields.

Functional operating conditions are given in **Section 5.2, DC Specifications** and **Section 5.3, AC Specifications.**

Table 14. Absolute Maximum Ratings

Case Temperature under Bias	−65°C to +110°C
Storage Temperature	−65°C to +150°C
DC Voltage on Any Pin with Respect to Ground	−0.5V to V_{CCP} + 0.5V
Supply Voltage V_{CC} with Respect to V_{SS}	−0.5V to +4.6V
Supply Voltage V_{CCP} with Respect to V_{SS}	−0.5V to +4.6V

5.2 DC Specifications

The following tables show the operating supply voltages, DC I/O specifications, and component power consumption for the embedded ULP Intel486 GX processor.

Table 15. Operating Supply Voltages

Product	V_{CCP} Range(1)	Max. CLK Frequency	V_{CC} Range(2)	V_{CC} Fluctuation
FA80486GXSF-33	3.3V ± 0.3V	16	2.0V min 3.3V max	±0.2V at 2.0V ≤ V_{CC} ≤ 2.7V +0.3V/−0.2V at 2.7V < V_{CC} < 3.0V ±0.3V at 3.0V ≤ V_{CC} ≤ 3.3V
		20	2.2V min 3.3V max	
		25	2.4V min 3.3V max	
		33	2.7V min 3.3V max	

NOTES:
1. In all cases, V_{CCP} must be ≥ VCC.
2. V_{CC} may be set to any voltage within the V_{CC} Range. The setting determines the allowed V_{CC} Fluctuation.

Table 16. DC Specifications

T_{CASE} = 0°C to +85°C

Symbol	Parameter	Min.	Max.	Unit	Notes
V_{IL}	Input LOW Voltage	−0.3	+0.8	V	
V_{IH}	Input HIGH Voltage	2.0	V_{CCP} +0.3	V	(Note 1)
V_{IHC}	Input HIGH Voltage of CLK	V_{CCP} −0.6	V_{CCP} +0.3	V	
V_{OL}	Output LOW Voltage I_{OL} = 2.0 mA I_{OL} = 100 μA		 0.4 0.2	 V V	
V_{OH}	Output HIGH Voltage I_{OH} = −2.0 mA I_{OH} = −100 μA	 2.4 V_{CCP} −0.2		 V V	
I_{LI}	Input Leakage Current		±15	μA	(Note 2)
I_{IH}	Input Leakage Current		200	μA	(Note 3)
I_{IL}	Input Leakage Current		−400	μA	(Note 4)
I_{LO}	Output Leakage Current		±15	μA	
C_{IN}	Input Capacitance		10	pF	(Note 5)
C_{OUT}	I/O or Output Capacitance		10	pF	(Note 5)
C_{CLK}	CLK Capacitance		6	pF	(Note 5)

NOTES:
1. All inputs except CLK.
2. This parameter is for inputs without pull-up or pull-down resistors and $0V \leq V_{IN} \leq V_{CCP}$.
3. This parameter is for inputs with pull-down resistors and V_{IH} = 2.4V, and for level-keeper pins at V = 0.4V.
4. This parameter is for inputs with pull-up resistors and V_{IL} = 0.4V, and for level-keeper pins at V = 2.4V.
5. F_C = 1 MHz. Not 100% tested.

Table 17. Active I_{CC} Values

T_{CASE} = 0°C to +85°C

Symbol	Parameter	Frequency	Supply Voltage	Typical I_{CC}	Max. I_{CC}	Notes
I_{CC1}	I_{CC} Active (V_{CC} pins)	16 MHz	V_{CC} = 2.0 ± 0.2V	65 mA	105 mA	
			V_{CC} = 3.3 ± 0.3V	105 mA	170 mA	
		20 MHz	V_{CC} = 2.2 ± 0.2V	85 mA	140 mA	
			V_{CC} = 3.3±0.3V	130 mA	210 mA	
		25 MHz	V_{CC} = 2.4 ± 0.2V	120 mA	195 mA	
			V_{CC} = 3.3 ± 0.3V	165 mA	260 mA	
		33 MHz	V_{CC} = 2.7 ± 0.2V	180 mA	280 mA	
			V_{CC} = 3.3 ± 0.3V	220 mA	345 mA	
I_{CC2}	I_{CC} Active (V_{CCP} pins)	16 MHz	V_{CCP} = 3.3 ± 0.3V	5 mA	16 mA	1
		20 MHz	V_{CCP} = 3.3 ± 0.3V	6 mA	20 mA	1
		25 MHz	V_{CCP} = 3.3 ± 0.3V	7 mA	25 mA	1
		33 MHz	V_{CCP} = 3.3 ± 0.3V	9 mA	32 mA	1

NOTE:
1. These parameters are for C_L = 50 pF

4

Table 18. Clock Stop, Stop Grant, and Auto HALT Power Down I_{CC} Values

T_{CASE} = 0°C to +85°C

Symbol	Parameter	Frequency	Supply Voltage	Typical I_{CC}	Max. I_{CC}	Notes
I_{CCS0}	I_{CC} Stop Clock (V_{CC} pins)	0 MHz	V_{CC} = 2.0 ± 0.2V	3 μA	105 μA	Note 1
			V_{CC} = 2.2 ± 0.2V	3 μA	110 μA	
			V_{CC} = 2.4 ± 0.2V	4 μA	120 μA	
			V_{CC} = 2.7 ± 0.2V	4 μA	130 μA	
			V_{CC} = 3.3 ± 0.3V	5 μA	150 μA	
I_{CCS2}	I_{CC} Stop Clock (V_{CCP} pins)	0 MHz	V_{CCP} = 3.3 ± 0.3V	3 μA	80 μA	
I_{CCS1}	I_{CC} Stop Grant, Auto HALT Power Down (V_{CC} pins)	16 MHz	V_{CC} = 2.0 ± 0.2V	8 mA	15 mA	
			V_{CC} = 3.3 ± 0.3V	12 mA	20 mA	
		20 MHz	V_{CC} = 2.2 ± 0.2V	10 mA	20 mA	
			V_{CC} = 3.3 ± 0.3V	15 mA	25 mA	
		25 MHz	V_{CC} = 2.4 ± 0.2V	14 mA	25 mA	
			V_{CC} = 3.3 ± 0.3V	20 mA	30 mA	
		33 MHz	V_{CC} = 2.7 ± 0.2V	20 mA	30 mA	
			V_{CC} = 3.3 ± 0.3V	25 mA	35 mA	
I_{CCS3}	I_{CC} Stop Grant, Auto HALT Power Down (V_{CCP} pins)	16 MHz	V_{CCP} = 3.3 ± 0.3V	270 μA	1.0 mA	
		20 MHz	V_{CCP} = 3.3 ± 0.3V	340 μA	1.2 mA	
		25 MHz	V_{CCP} = 3.3 ± 0.3V	425 μA	1.5 mA	
		33 MHz	V_{CCP} = 3.3 ± 0.3V	610 μA	2.0 mA	

NOTE:

1. The I_{CC} Stop Clock specification refers to the I_{CC} value once the processor enters the Stop Clock state. For all input signals, the V_{IH} and V_{IL} levels must be equal to V_{CCP} and 0V, respectively, to meet the I_{CC} Stop Clock specifications.

5.3 AC Specifications

The AC specifications for the embedded ULP Intel486 GX processor are given in this section.

Table 19. AC Characteristics (Sheet 1 of 2)

valid over the operating supply voltages listed in Table 15, Operating Supply Voltages.
T_{CASE} = 0°C to +85°C; C_L = 50 pF

Symbol	Parameter	2.0V ≤ V_{CC} < 2.2V		2.2V ≤ V_{CC} < 2.4V		2.4V ≤ V_{CC} < 2.7V		2.7V ≤ V_{CC} ≤ 3.3V		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
	Frequency	0	16	0	20	0	25	0	33	MHz	(Note 1)
t_1	CLK Period	62.5		50		40		30		ns	(Note 1)
t_{1a}	CLK Period Stability		250		250		250		250	ps/CLK	(Note 2)
t_2	CLK High Time	23		18		14		11		ns	at 2V
t_3	CLK Low Time	23		18		14		11		ns	at 0.8V
t_4	CLK Fall Time		4		4		4		3	ns	2V to 0.8V (Note 3)
t_5	CLK Rise Time		4		4		4		3	ns	0.8V to 2V (Note 3)
t_6	A2–A31, PWT, PCD, BE0#–BE3#, M/IO#, D/C#, W/R#, ADS#, LOCK#, BREQ, HLDA, SMIACT# Valid Delay	3	30	3	24	3	19	3	16	ns	
t_7	A2–A31, PWT, PCD, BE0#–BE3#, M/IO#, D/C#, W/R#, ADS#, LOCK#, BREQ, Float Delay		36		30		28		20	ns	(Note 3)
t_8	PCHK# Valid Delay	3	34	3	29	3	24	3	22	ns	
t_{8a}	BLAST#, PLOCK# Valid Delay	3	34	3	29	3	24	3	20	ns	
t_9	BLAST#, PLOCK# Float Delay		36		30		28		20	ns	(Note 3)
t_{10}	D0–D15, DP0, DP1 Write Delay	3	31	3	26	3	20	3	19	ns	
t_{11}	D0–D15, DP0, DP1 Float Delay		36		30		28		20	ns	(Note 3)
t_{12}	EADS# Setup Time	13		11		8		6		ns	
t_{13}	EADS# Hold Time	4		4		3		3		ns	
t_{14}	KEN# Setup Time	13		11		8		6		ns	
t_{15}	KEN# Hold Time	4		4		3		3		ns	
t_{16}	RDY#, BRDY# Setup Time	13		11		8		6		ns	
t_{17}	RDY#, BRDY# Hold Time	4		4		3		3		ns	
t_{18}	HOLD, AHOLD Setup Time	15		13		10		6		ns	

Table 19. AC Characteristics (Sheet 2 of 2)

valid over the operating supply voltages listed in Table 15, Operating Supply Voltages.
T_{CASE} = 0°C to +85°C; C_L = 50 pF (Continued)

Symbol	Parameter	2.0V ≤ V_{CC} < 2.2V		2.2V ≤ V_{CC} < 2.4V		2.4V ≤ V_{CC} < 2.7V		2.7V ≤ V_{CC} ≤ 3.3V		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
t_{18a}	BOFF# Setup Time	15		13		10		9		ns	
t_{19}	HOLD, AHOLD, BOFF# Hold Time	4		4		3		3		ns	
t_{20}	FLUSH#, A20M#, NMI, INTR, SMI#, STPCLK#, SRESET, RESET Setup Time	15		13		10		6		ns	
t_{21}	FLUSH#, A20M#, NMI, INTR, SMI#, STPCLK#, SRESET, RESET Hold Time	4		4		3		3		ns	
t_{22}	D0–D15, DP0, DP1, A4–A31 Read Setup Time	11		8		6		6		ns	
t_{23}	D0–D15, DP0, DP1, A4–A31 Read Hold Time	4		4		3		3		ns	

NOTES:
1. 0 Hz operation is tested and guaranteed by the STPCLK# and Stop Grant bus cycle protocol. 0 Hz < CLK < 8 MHz operation is confirmed by design characterization, but not 100% tested in production.
2. Specification t_{1a} is available only when CLK frequency is changed without STPCLK#/STOP GRANT bus cycle protocol.
3. Not 100% tested, guaranteed by design characterization.
4. CLK reference voltage for timing measurement is 1.5V except t_2 through t_5. Other signals are measured at 1.5V.

Table 20. AC Specifications for the Test Access Port

Symbol	Parameter	$1.8V \leq V_{CC} < 3.0V$		$V_{CC} = 3.3 \pm 0.3V$		Unit	Figure	Notes
		Min	Max	Min	Max			
t_{24}	TCK Frequency		5		8	MHz	15	
t_{25}	TCK Period	200		125		ns	15	Note 1
t_{26}	TCK High Time	65		40		ns	15	@ 2.0V
t_{27}	TCK Low Time	65		40		ns	15	@ 0.8V
t_{28}	TCK Rise Time		15		8	ns	15	Note 2
t_{29}	TCK Fall Time		15		8	ns	15	Note 2
t_{30}	TDI, TMS Setup Time	16		8		ns	16	Note 3
t_{31}	TDI, TMS Hold Time	20		10		ns	16	Note 3
t_{32}	TDO Valid Delay	3	46	3	30	ns	16	Note 3
t_{33}	TDO Float Delay		52		36	ns	16	Notes 3, 4
t_{34}	All Outputs (except TDO) Valid Delay	3	80	3	30	ns	16	Note 3
t_{35}	All Outputs (except TDO) Float Delay		88		36	ns	16	Notes 3, 4
t_{36}	All Inputs (except TDI, TMS, TCK) Setup Time	16		8		ns	16	Note 3
t_{37}	All Inputs (except TDI, TMS, TCK) Hold Time	35		15		ns	16	Note 3

NOTES:
1. TCK period ≥ CLK period.
2. Rise/Fall Times are measured between 0.8V and 2.0V. Rise/Fall times can be relaxed by 1 ns per 10 ns increase in TCK period.
3. Parameter measured from TCK.
4. Not 100% tested, guaranteed by design characterization.

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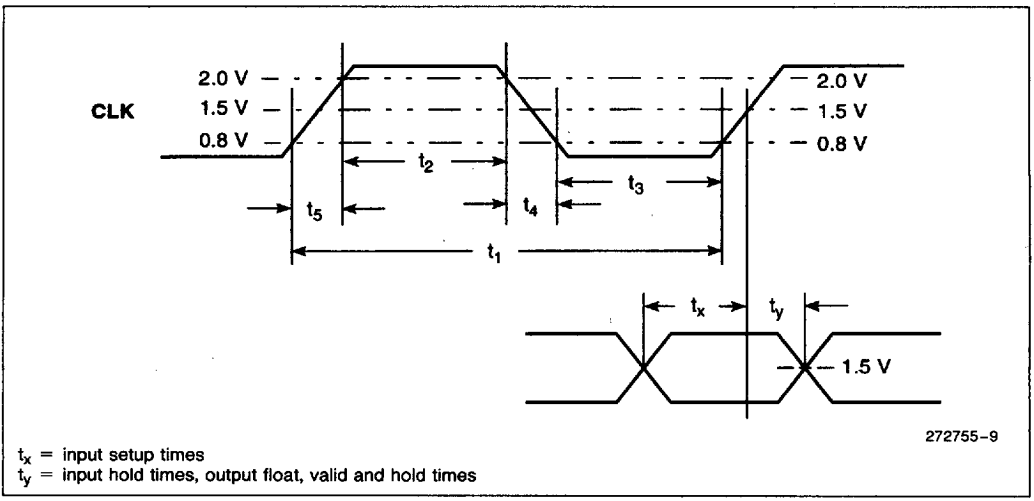

t_x = input setup times
t_y = input hold times, output float, valid and hold times

Figure 9. CLK Waveform

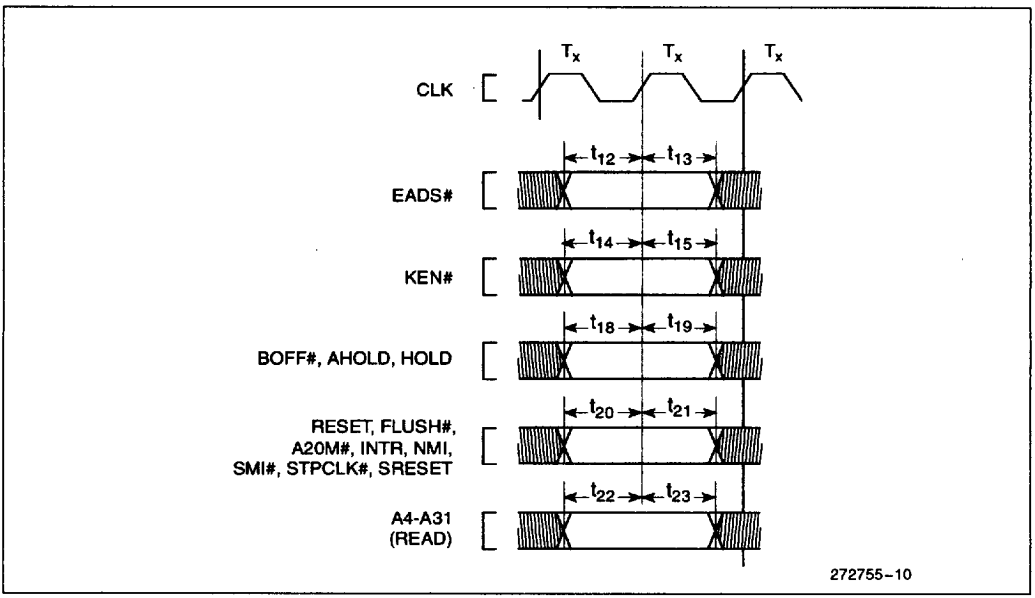

Figure 10. Input Setup and Hold Timing

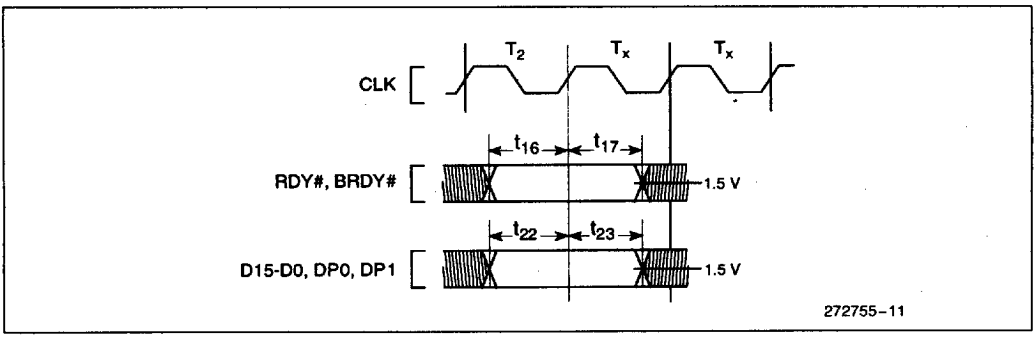

Figure 11. Input Setup and Hold Timing

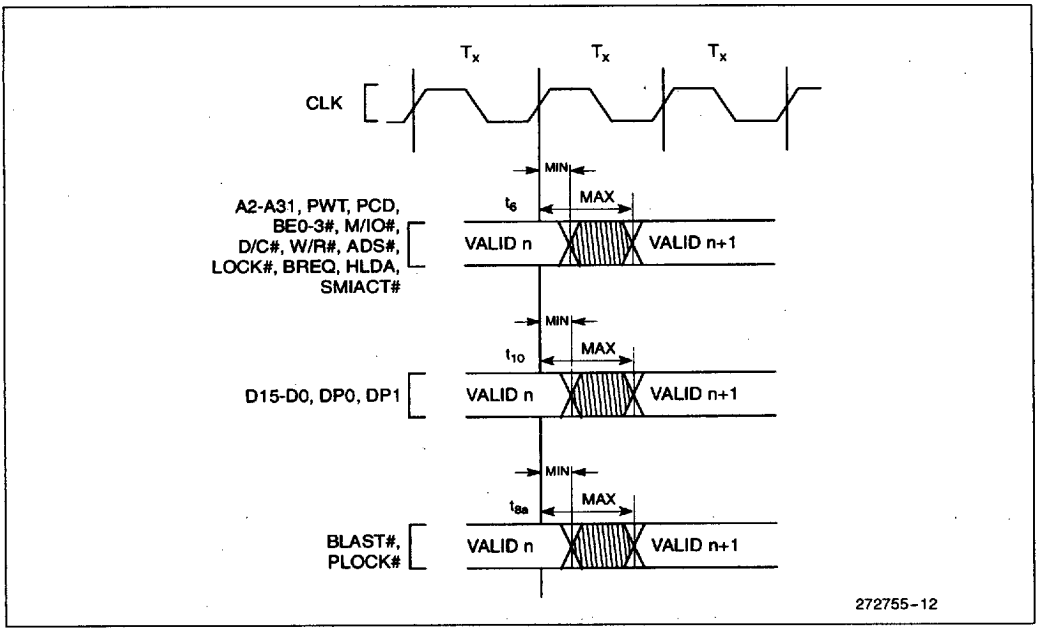

Figure 12. Output Valid Delay Timing

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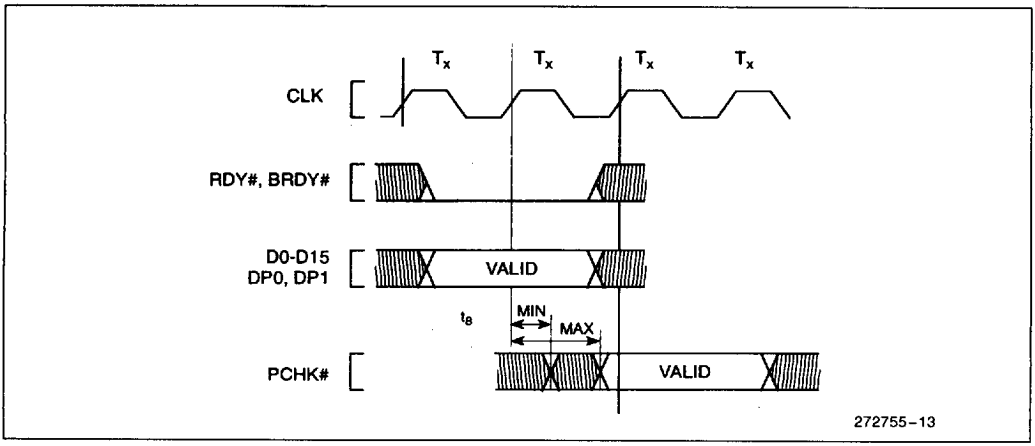


Figure 13. PCHK# Valid Delay Timing

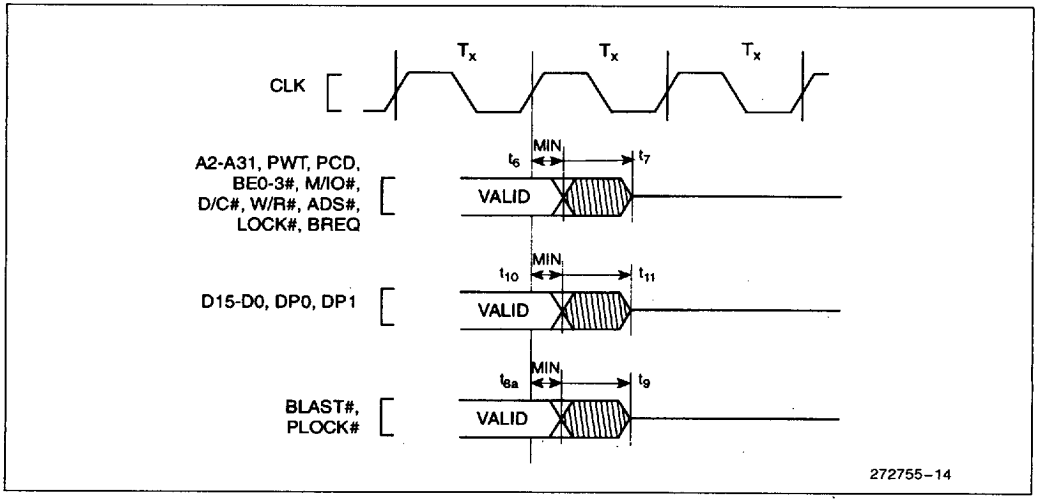


Figure 14. Maximum Float Delay Timing

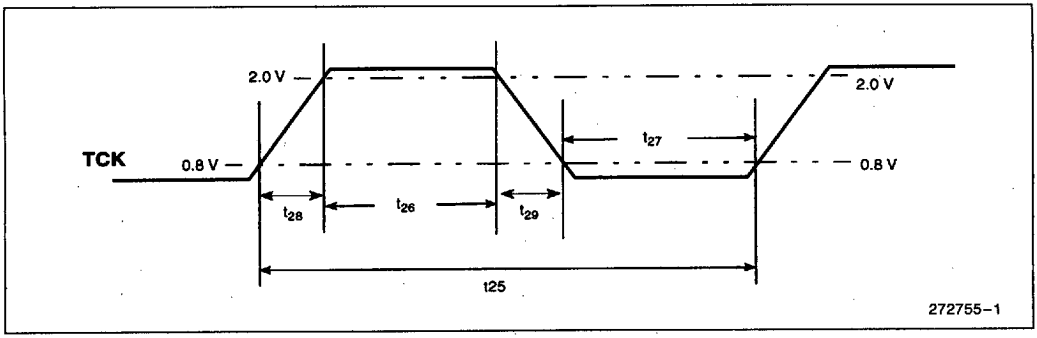


Figure 15. TCK Waveform

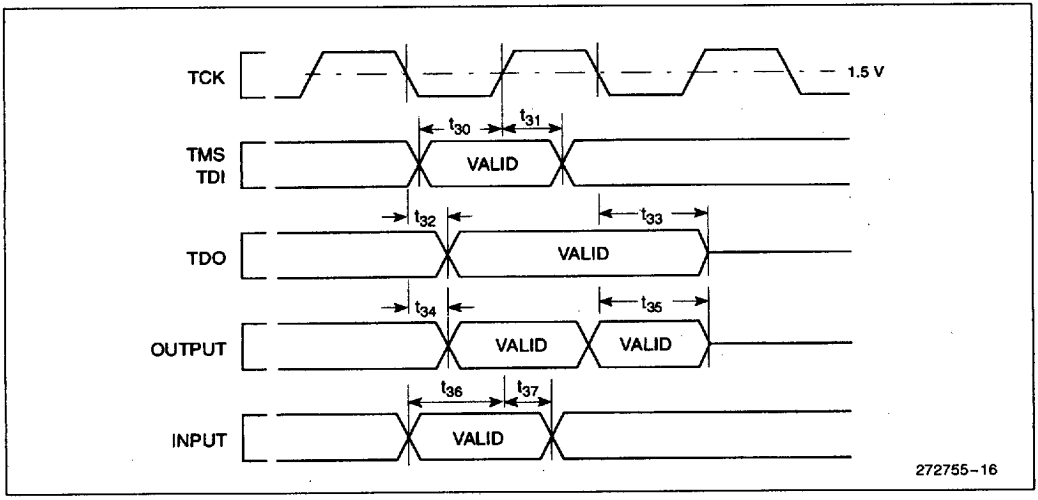
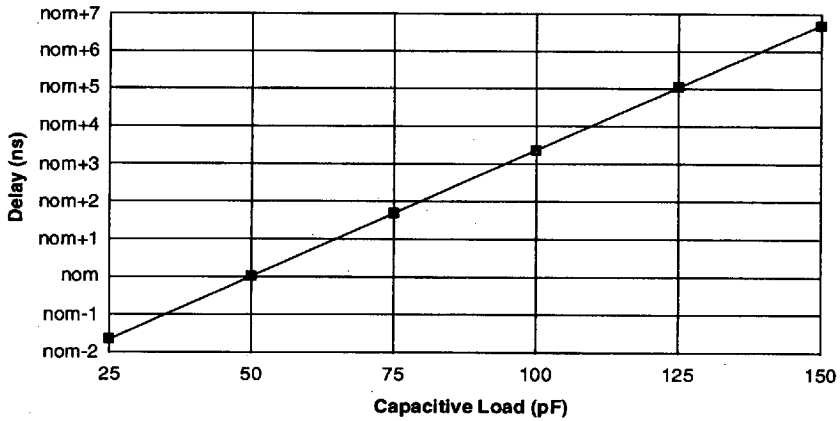


Figure 16. Test Signal Timing Diagram

4

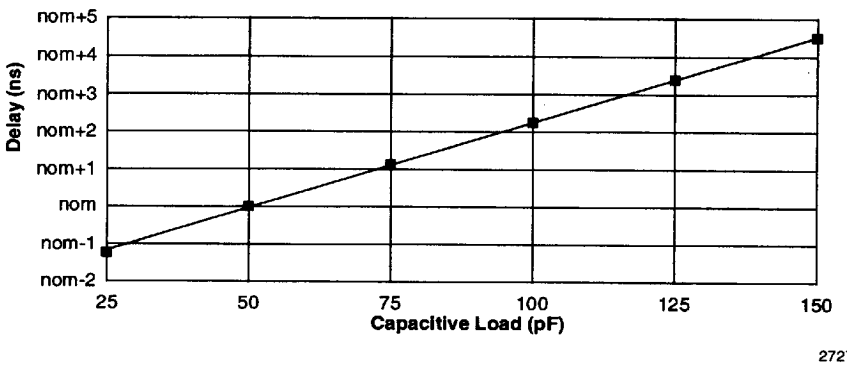
5.4 Capacitive Derating Curves

The following graphs are the capacitive derating curves for the embedded ULP Intel486 GX processor.



NOTE:
This graph will not be linear outside of the capacitive range shown.
nom = nominal value from the AC Characteristics table.

Figure 17. Typical Loading Delay versus Load Capacitance under Worst-Case Conditions for a Low-to-High Transition



NOTE:
This graph will not be linear outside of the capacitive range shown.
nom = nominal value from the AC Characteristics table.

Figure 18. Typical Loading Delay versus Load Capacitance under Worst-Case Conditions for a High-to-Low Transition

6.0 MECHANICAL DATA

This section describes the packaging dimensions and thermal specifications for the embedded ULP Intel486 GX processor.

6.1 Package Dimensions

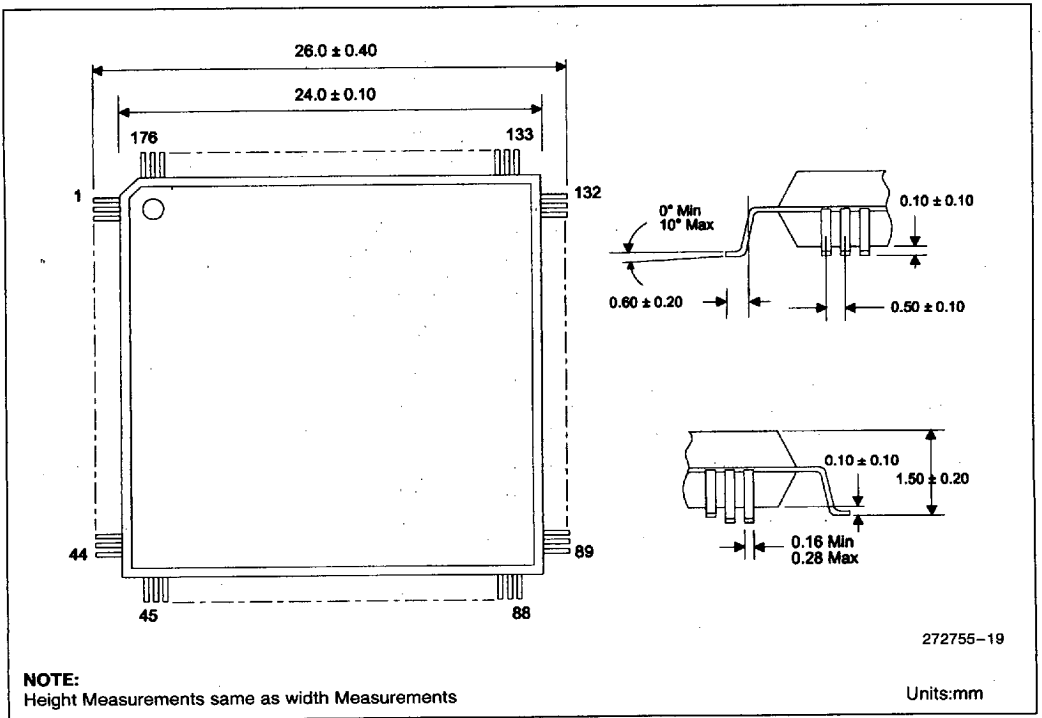


Figure 19. Package Mechanical Specifications for the 176 Lead TQFP Package

6.2 Package Thermal Specifications

The embedded ULP Intel486 GX processor is specified for operation when the case temperature (T_C) is within the range of 0°C to 85°C. T_C may be measured in any environment to determine whether the processor is within the specified operating range.

The ambient temperature (T_A) can be calculated from θ_{JC} and θ_{JA} from the following equations:

$$T_J = T_C + P * \theta_{JC}$$
$$T_A = T_J - P * \theta_{JA}$$
$$T_C = T_A + P * [\theta_{JA} - \theta_{JC}]$$
$$T_A = T_C - P * [\theta_{JA} - \theta_{JC}]$$

Where T_J, T_A, T_C equals Junction, Ambient and Case Temperature respectively. θ_{JC}, θ_{JA} equals Junction-to-Case and Junction-to-Ambient thermal Resistance, respectively. Maximum Power Consumption (P) is defined as

$$P = V\ (typ) * I_{CC}\ (max)$$
$$P = [V_{CC}\ (typ) * I_{CC1}\ (max)] + [V_{CCP}\ (typ) * I_{CC2}\ (max)]$$

where: I_{CC1} is the V_{CC} supply current
I_{CC2} is the V_{CCP} supply current

Values for θ_{JA} and θ_{JC} are given in the following tables for each product at its maximum operating frequencies.

Table 21. Thermal Resistance

(°C/W) θ_{JC} and θ_{JA} for the 176-Lead TQFP Package

θ_{JC} (°C/W)	θ_{JA} (°C/W) with no airflow
4.3	33.6

The following table shows maximum ambient temperatures of the embedded ULP Intel486 GX processor for each product and maximum operating frequencies. These temperatures are calculated using I_{CC1} and I_{CC1} values measured during component-validation testing using V_{CCP} = 3.6V and worst-case V_{CC} values.

Table 22. Maximum Ambient Temperature (T_A)

176-Lead TQFP Package

Frequency	V_{CC}	T_A (°C) with no airflow
16 MHz	2.0V	83
	3.3V	73
20 MHz	2.2V	80
	3.3V	70
25 MHz	2.4V	77
	3.3V	66
33 MHz	2.7V	70
	3.3V	60