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# HM628512B Series

4 M SRAM (512-kword × 8-bit)

# HITACHI

ADE-203-903D (Z)

Rev. 3.0

Aug. 24, 1999

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## Description

The Hitachi HM628512B is a 4-Mbit static RAM organized 512-kword × 8-bit. It realizes higher density, higher performance and low power consumption by employing 0.35 μm Hi-CMOS process technology. The device, packaged in a 525-mil SOP (foot print pitch width) or 400-mil TSOP TYPE II or 600-mil plastic DIP, is available for high density mounting. The HM628512B is suitable for battery backup system.

## Features

- Single 5 V supply
- Access time: 55/70 ns (max)
- Power dissipation
  - Active: 50 mW/MHz (typ)
  - Standby: 10 μW (typ)
- Completely static memory. No clock or timing strobe required
- Equal access and cycle times
- Common data input and output: Three state output
- Directly TTL compatible: All inputs and outputs
- Battery backup operation

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## HM628512B Series

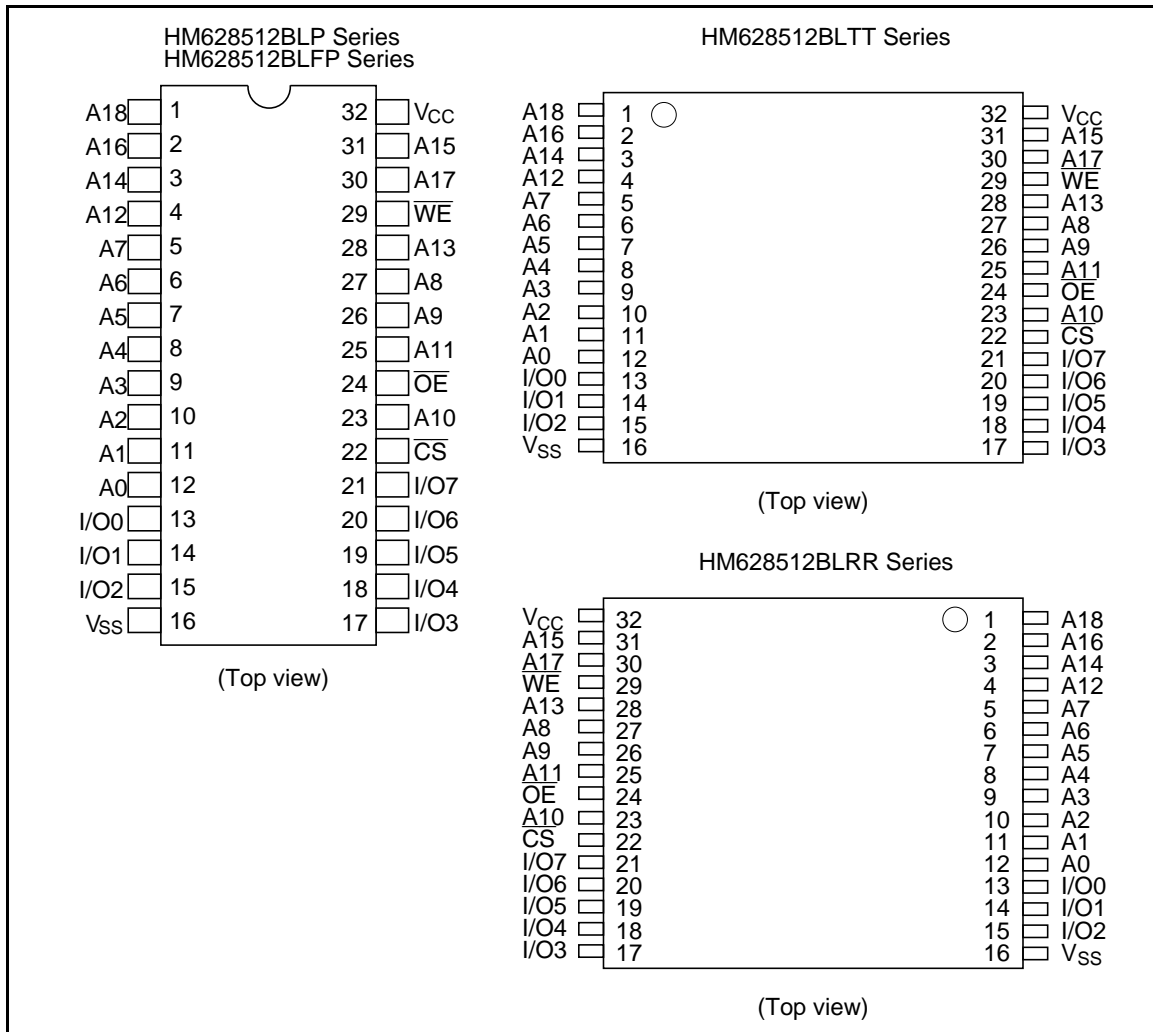
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### Ordering Information

Type No.	Access time	Package
HM628512BLP-5	55 ns	600-mil 32-pin plastic DIP (DP-32)
HM628512BLP-7	70 ns	
HM628512BLP-5SL	55 ns	
HM628512BLP-7SL	70 ns	
HM628512BLP-5UL	55 ns	
HM628512BLP-7UL	70 ns	
HM628512BLFP-5	55 ns	525-mil 32-pin plastic SOP (FP-32D)
HM628512BLFP-7	70 ns	
HM628512BLFP-5SL	55 ns	
HM628512BLFP-7SL	70 ns	
HM628512BLFP-5UL	55 ns	
HM628512BLFP-7UL	70 ns	
HM628512BLTT-5	55 ns	400-mil 32-pin plastic TSOP II (TTP-32D)
HM628512BLTT-7	70 ns	
HM628512BLTT-5SL	55 ns	
HM628512BLTT-7SL	70 ns	
HM628512BLTT-5UL	55 ns	
HM628512BLTT-7UL	70 ns	
HM628512BLRR-5	55 ns	400-mil 32-pin plastic TSOP II reverse (TTP-32DR)
HM628512BLRR-7	70 ns	
HM628512BLRR-5SL	55 ns	
HM628512BLRR-7SL	70 ns	
HM628512BLRR-5UL	55 ns	
HM628512BLRR-7UL	70 ns	

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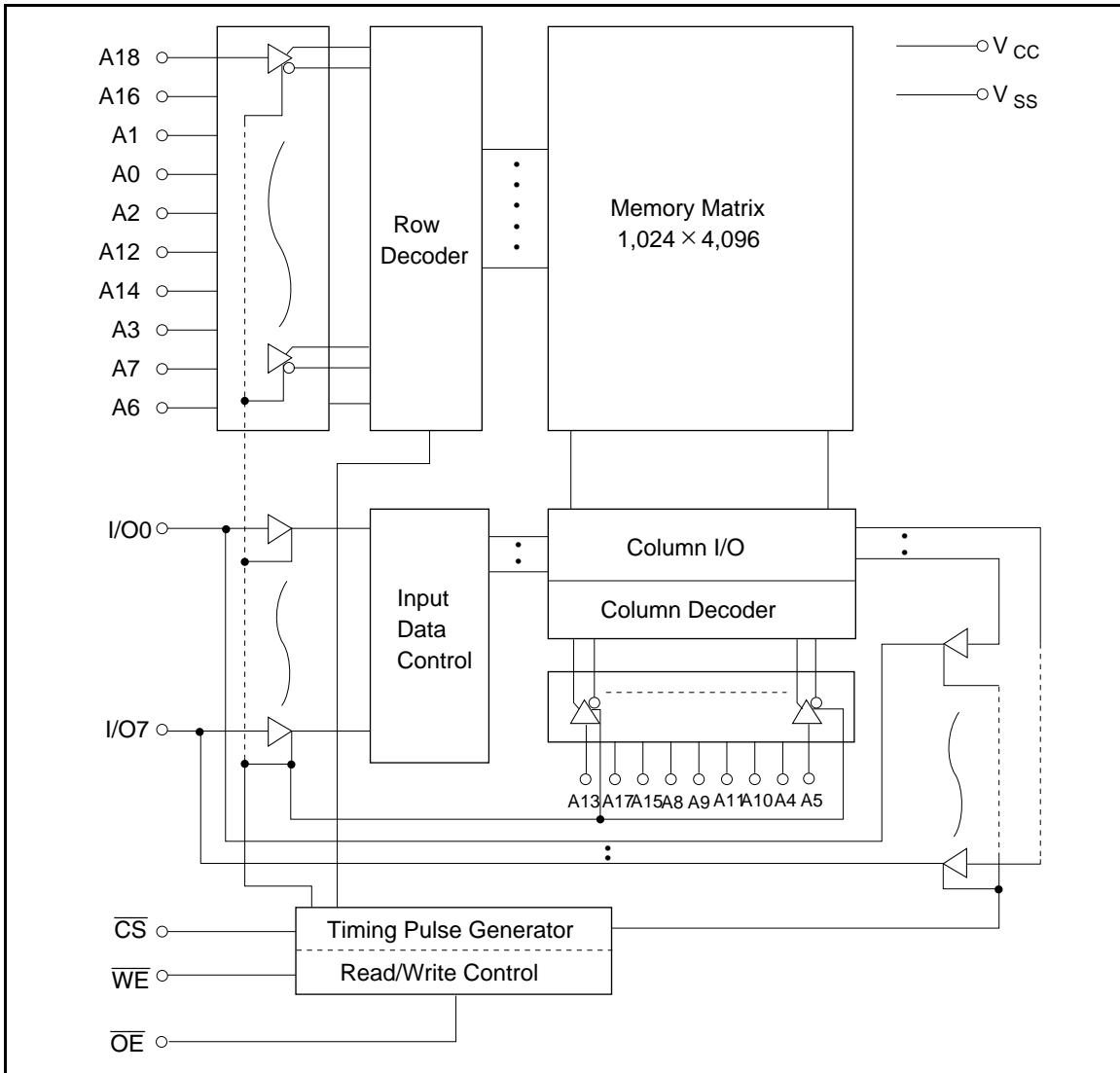
Pin Arrangement



Pin Description

Pin name	Function
A0 to A18	Address input
I/O0 to I/O7	Data input/output
CS	Chip select
OE	Output enable
WE	Write enable
V <sub>CC</sub>	Power supply
V <sub>SS</sub>	Ground

Block Diagram



Function Table

$\overline{WE}$	$\overline{CS}$	$\overline{OE}$	Mode	$V_{CC}$ current	Dout pin	Ref. cycle
x	H	x	Not selected	$I_{SB}, I_{SB1}$	High-Z	—
H	L	H	Output disable	$I_{CC}$	High-Z	—
H	L	L	Read	$I_{CC}$	Dout	Read cycle
L	L	H	Write	$I_{CC}$	Din	Write cycle (1)
L	L	L	Write	$I_{CC}$	Din	Write cycle (2)

Note: x: H or L

## Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage	$V_{CC}$	-0.5 to +7.0	V
Voltage on any pin relative to $V_{SS}$	$V_T$	-0.5 <sup>*1</sup> to $V_{CC} + 0.3$ <sup>*2</sup>	V
Power dissipation	$P_T$	1.0	W
Operating temperature	$T_{opr}$	-20 to +70	°C
Storage temperature	$T_{stg}$	-55 to +125	°C
Storage temperature under bias	$T_{bias}$	-20 to +85	°C

Notes: 1. -3.0 V for pulse half-width  $\leq 30$  ns  
 2. Maximum voltage is 7.0 V

## Recommended DC Operating Conditions ( $T_a = -20$ to $+70^\circ\text{C}$ )

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{CC}$	4.5	5.0	5.5	V
	$V_{SS}$	0	0	0	V
Input high voltage	$V_{IH}$	2.2	—	$V_{CC} + 0.3$	V
Input low voltage	$V_{IL}$	-0.3 <sup>*1</sup>	—	0.8	V

Note: 1. -3.0 V for pulse half-width  $\leq 30$  ns

## DC Characteristics ( $T_a = -20$ to $+70^\circ\text{C}$ , $V_{CC} = 5\text{ V} \pm 10\%$ , $V_{SS} = 0\text{ V}$ )

Parameter	Symbol	Min	Typ <sup>*1</sup>	Max	Unit	Test conditions
Input leakage current	$ I_{LI} $	—	—	1	$\mu\text{A}$	$V_{in} = V_{SS}$ to $V_{CC}$
Output leakage current	$ I_{LO} $	—	—	1	$\mu\text{A}$	$\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$ , $V_{I/O} = V_{SS}$ to $V_{CC}$
Operating power supply current: DC	$I_{CC}$	—	8	15	mA	$\overline{CS} = V_{IL}$ , others = $V_{IH}/V_{IL}$ , $I_{I/O} = 0\text{ mA}$
Operating power supply current	$I_{CC1}$	—	40	60	mA	Min cycle, duty = 100% $\overline{CS} = V_{IL}$ , others = $V_{IH}/V_{IL}$ $I_{I/O} = 0\text{ mA}$
Operating power supply current	$I_{CC2}$	—	10	20	mA	Cycle time = 1 $\mu\text{s}$ , duty = 100% $I_{I/O} = 0\text{ mA}$ , $\overline{CS} \leq 0.2\text{ V}$ $V_{IH} \geq V_{CC} - 0.2\text{ V}$ , $V_{IL} \leq 0.2\text{ V}$
Standby power supply current: DC	$I_{SB}$	—	1	3	mA	$\overline{CS} = V_{IH}$
Standby power supply current (1): DC	$I_{SB1}$	—	2 <sup>*2</sup>	100 <sup>*2</sup>	$\mu\text{A}$	$V_{in} \geq 0\text{ V}$ , $\overline{CS} \geq V_{CC} - 0.2\text{ V}$
		—	2 <sup>*3</sup>	50 <sup>*3</sup>	$\mu\text{A}$	
		—	2 <sup>*4</sup>	20 <sup>*4</sup>	$\mu\text{A}$	
Output low voltage	$V_{OL}$	—	—	0.4	V	$I_{OL} = 2.1\text{ mA}$
Output high voltage	$V_{OH}$	2.4	—	—	V	$I_{OH} = -1.0\text{ mA}$

Notes: 1. Typical values are at  $V_{CC} = 5.0\text{ V}$ ,  $T_a = +25^\circ\text{C}$  and specified loading, and not guaranteed.  
 2. This characteristics is guaranteed only for L version.  
 3. This characteristics is guaranteed only for L-SL version.

## HM628512B Series

4.This characteristics is guaranteed only for L-UL version.

### Capacitance (Ta = +25°C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit	Test conditions
Input capacitance*1	C <sub>in</sub>	—	8	pF	V <sub>in</sub> = 0 V
Input/output capacitance*1	C <sub>I/O</sub>	—	10	pF	V <sub>I/O</sub> = 0 V

Note: 1.This parameter is sampled and not 100% tested.

### AC Characteristics (Ta = -20 to +70°C, V<sub>CC</sub> = 5 V ± 10%, unless otherwise noted.)

#### Test Conditions

- Input pulse levels: 0.8 V to 2.4 V
- Input rise and fall time: 5 ns
- Input and output timing reference levels: 1.5 V
- Output load: 1 TTL Gate + C<sub>L</sub> (100 pF) (HM628512B-7)  
1 TTL Gate + C<sub>L</sub> (50 pF) (HM628512B-5)  
(Including scope & jig)

#### Read Cycle

HM628512B							
		-5		-7			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Read cycle time	t <sub>RC</sub>	55	—	70	—	ns	
Address access time	t <sub>AA</sub>	—	55	—	70	ns	
Chip select access time	t <sub>CO</sub>	—	55	—	70	ns	
Output enable to output valid	t <sub>OE</sub>	—	25	—	35	ns	
Chip selection to output in low-Z	t <sub>LZ</sub>	10	—	10	—	ns	2
Output enable to output in low-Z	t <sub>OLZ</sub>	5	—	5	—	ns	2
Chip deselection to output in high-Z	t <sub>HZ</sub>	0	20	0	25	ns	1, 2
Output disable to output in high-Z	t <sub>OHZ</sub>	0	20	0	25	ns	1, 2
Output hold from address change	t <sub>OH</sub>	10	—	10	—	ns	

Write Cycle

HM628512B							
		-5		-7			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Write cycle time	$t_{WC}$	55	—	70	—	ns	
Chip selection to end of write	$t_{CW}$	50	—	60	—	ns	4
Address setup time	$t_{AS}$	0	—	0	—	ns	5
Address valid to end of write	$t_{AW}$	50	—	60	—	ns	
Write pulse width	$t_{WP}$	40	—	50	—	ns	3, 12
Write recovery time	$t_{WR}$	0	—	0	—	ns	6
$\overline{WE}$ to output in high-Z	$t_{WHZ}$	0	20	0	25	ns	1, 2, 7
Data to write time overlap	$t_{DW}$	25	—	30	—	ns	
Data hold from write time	$t_{DH}$	0	—	0	—	ns	
Output active from output in high-Z	$t_{OW}$	5	—	5	—	ns	2
Output disable to output in high-Z	$t_{OHZ}$	0	20	0	25	ns	1, 2, 7

- Notes:
- $t_{HZ}$ ,  $t_{OHZ}$  and  $t_{WHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
  - This parameter is sampled and not 100% tested.
  - A write occurs during the overlap ( $t_{WP}$ ) of a low  $\overline{CS}$  and a low  $\overline{WE}$ . A write begins at the later transition of  $\overline{CS}$  going low or  $\overline{WE}$  going low. A write ends at the earlier transition of  $\overline{CS}$  going high or  $\overline{WE}$  going high.  $t_{WP}$  is measured from the beginning of write to the end of write.
  - $t_{CW}$  is measured from  $\overline{CS}$  going low to the end of write.
  - $t_{AS}$  is measured from the address valid to the beginning of write.
  - $t_{WR}$  is measured from the earlier of  $\overline{WE}$  or  $\overline{CS}$  going high to the end of write cycle.
  - During this period, I/O pins are in the output state so that the input signals of the opposite phase to the outputs must not be applied.
  - If the  $\overline{CS}$  low transition occurs simultaneously with the  $\overline{WE}$  low transition or after the  $\overline{WE}$  transition, the output remain in a high impedance state.
  - Dout is the same phase of the write data of this write cycle.
  - Dout is the read data of next address.
  - If  $\overline{CS}$  is low during this period, I/O pins are in the output state. Therefore, the input signals of the opposite phase to the outputs must not be applied to them.
  - In the write cycle with  $\overline{OE}$  low fixed,  $t_{WP}$  must satisfy the following equation to avoid a problem of data bus contention.  $t_{WP} \geq t_{DW} \text{ min} + t_{WHZ} \text{ max}$

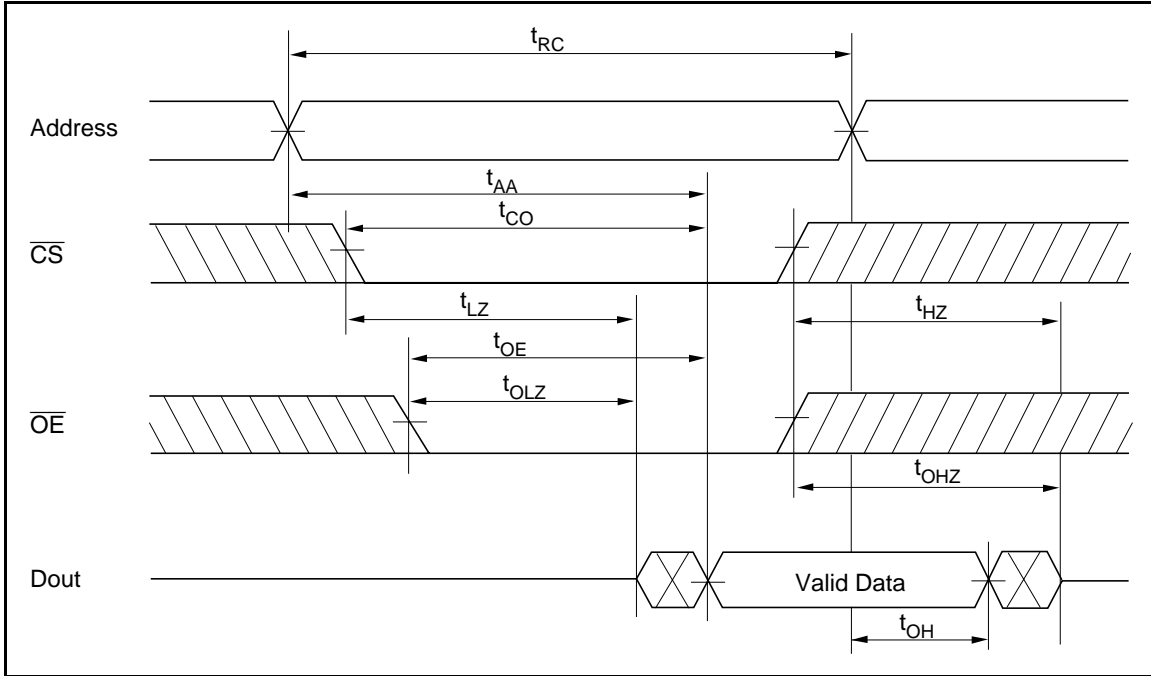
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# HM628512B Series

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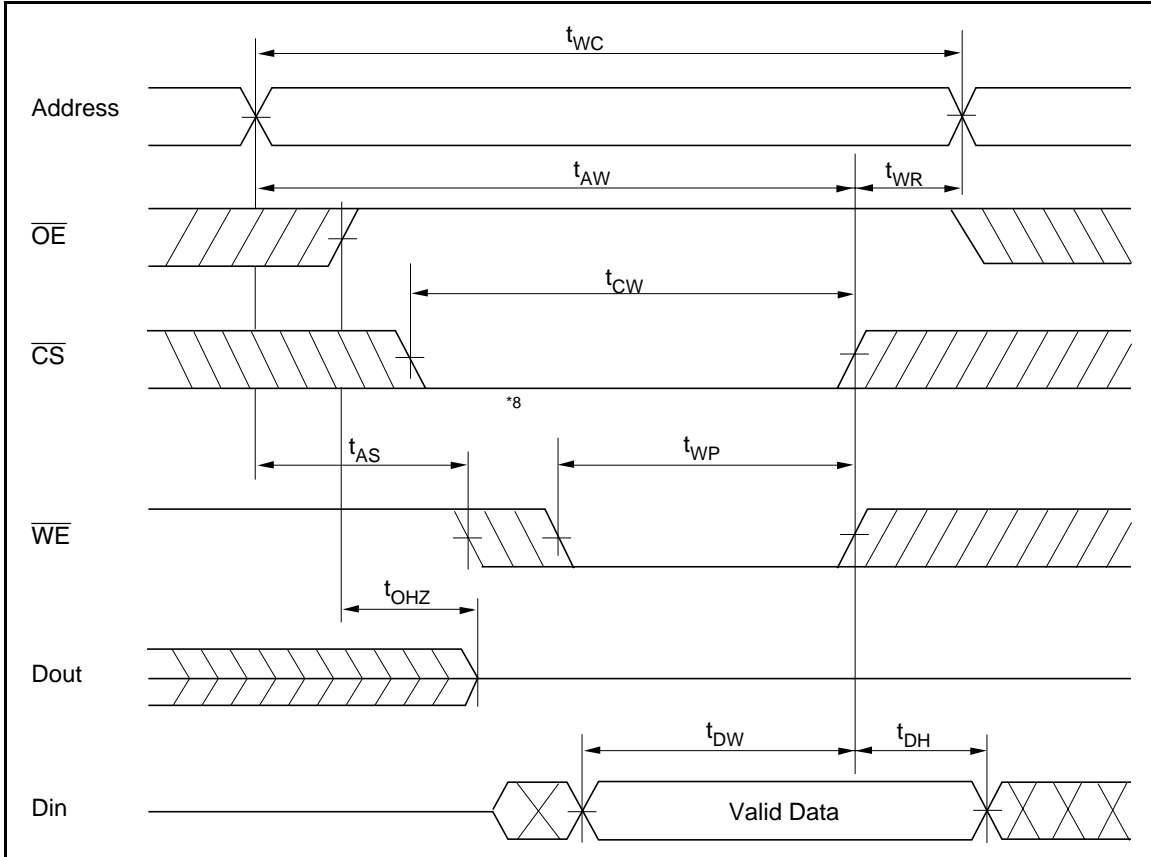
## Timing Waveforms

### Read Timing Waveform ( $\overline{WE} = V_{IH}$ )



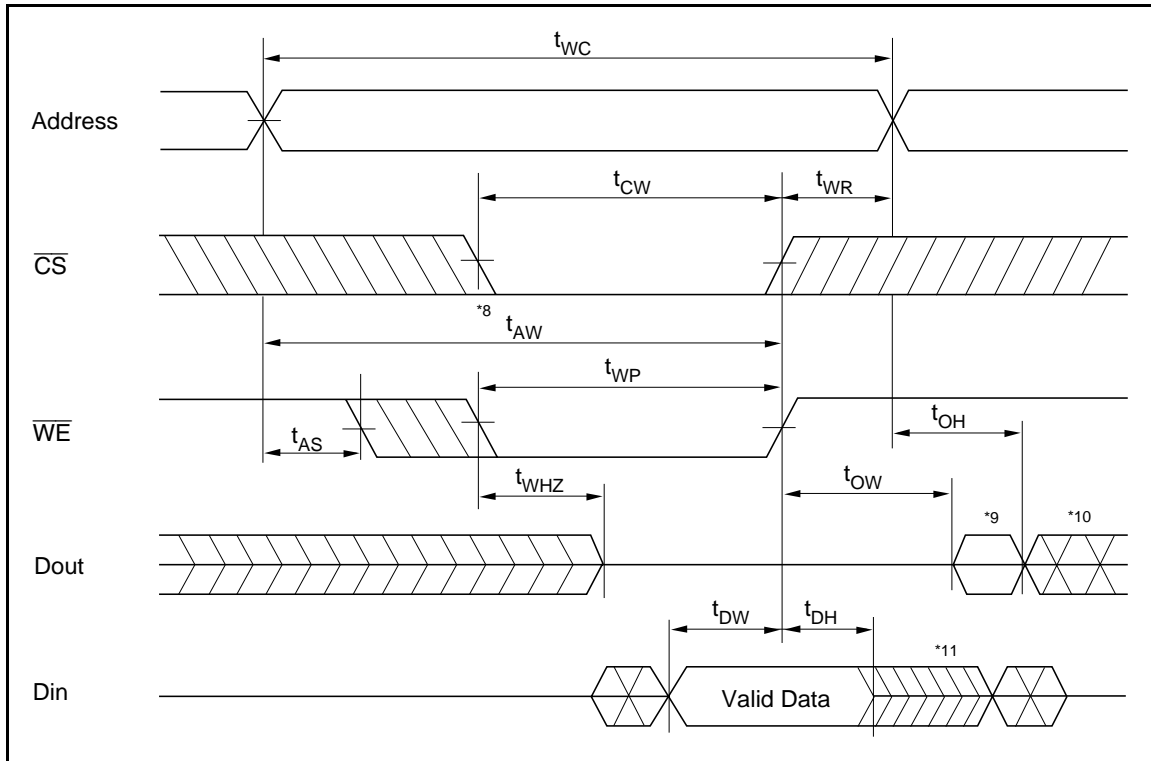


Write Timing Waveform (1) ( $\overline{\text{OE}}$  Clock)



## HM628512B Series

### Write Timing Waveform (2) ( $\overline{\text{OE}}$ Low Fixed)

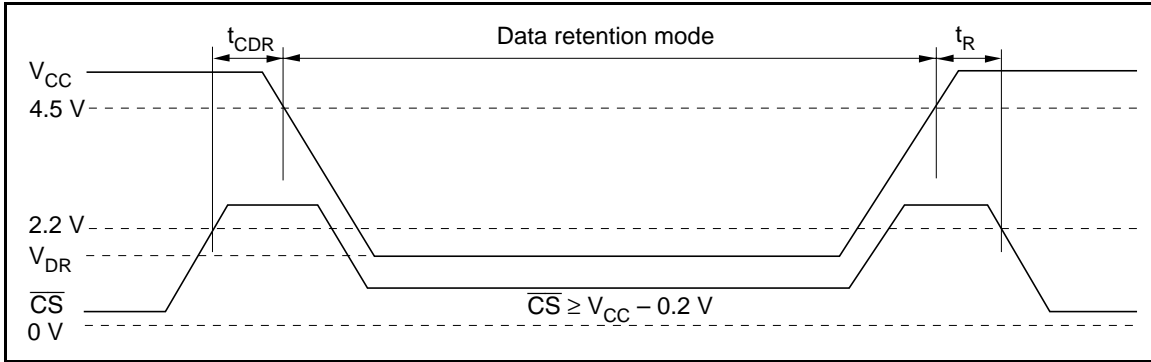


### Low $V_{CC}$ Data Retention Characteristics ( $T_a = -20$ to $+70^\circ\text{C}$ )

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions*4
$V_{CC}$ for data retention	$V_{DR}$	2	—	—	V	$\overline{\text{CS}} \geq V_{CC} - 0.2 \text{ V}$ , $V_{in} \geq 0 \text{ V}$
Data retention current	$I_{CCDR}$	—	$1^{*5}$	$50^{*1}$	$\mu\text{A}$	$V_{CC} = 3.0 \text{ V}$ , $V_{in} \geq 0 \text{ V}$
		—	$1^{*5}$	$15^{*2}$	$\mu\text{A}$	$\overline{\text{CS}} \geq V_{CC} - 0.2 \text{ V}$
		—	$1^{*5}$	$10^{*3}$	$\mu\text{A}$	
Chip deselect to data retention time	$t_{CDR}$	0	—	—	ns	See retention waveform
Operation recovery time	$t_R$	$t_{RC}^{*6}$	—	—	ns	

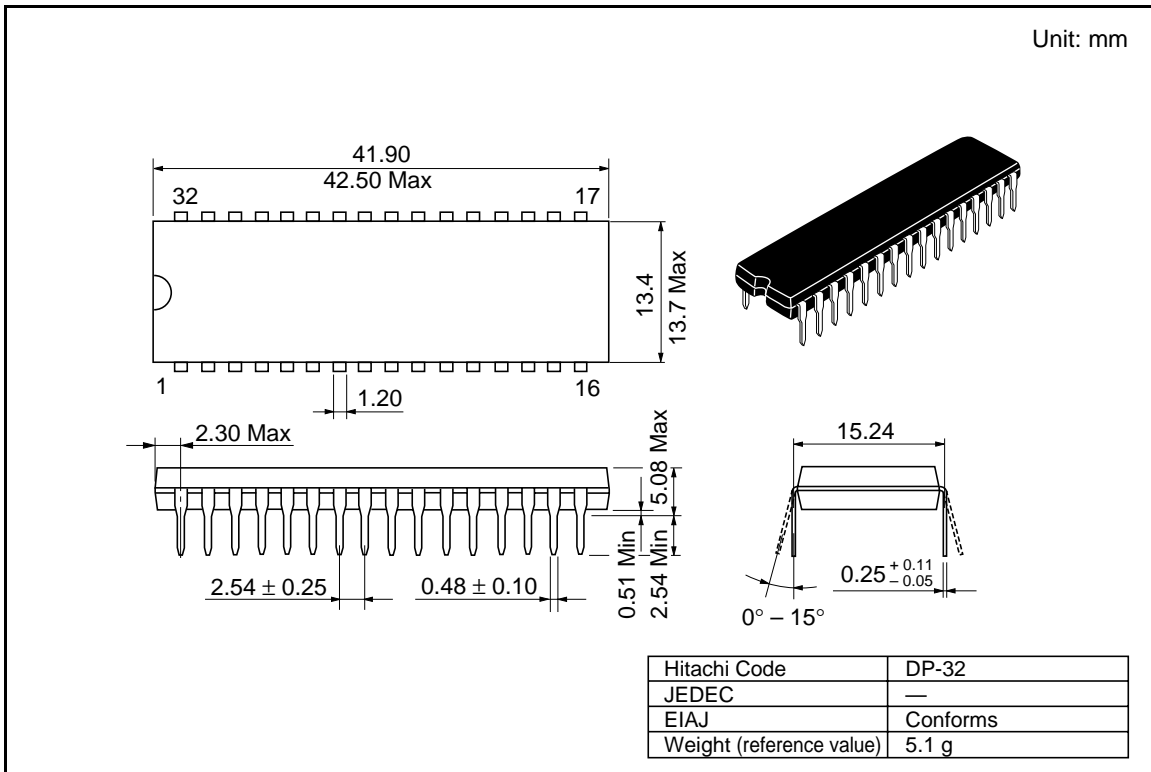
- Notes:
1. For L-version and  $20 \mu\text{A}$  (max.) at  $T_a = -20$  to  $+40^\circ\text{C}$ .
  2. For L-SL-version and  $3 \mu\text{A}$  (max.) at  $T_a = -20$  to  $+40^\circ\text{C}$ .
  3. For L-UL-version and  $3 \mu\text{A}$  (max.) at  $T_a = -20$  to  $+40^\circ\text{C}$ .
  4.  $\overline{\text{CS}}$  controls address buffer,  $\overline{\text{WE}}$  buffer,  $\overline{\text{OE}}$  buffer, and  $\text{Din}$  buffer. In data retention mode,  $V_{in}$  levels (address,  $\overline{\text{WE}}$ ,  $\overline{\text{OE}}$ , I/O) can be in the high impedance state.
  5. Typical values are at  $V_{CC} = 3.0 \text{ V}$ ,  $T_a = +25^\circ\text{C}$  and specified loading, and not guaranteed.
  6.  $t_{RC}$  = read cycle time.

Low  $V_{CC}$  Data Retention Timing Waveform ( $\overline{CS}$  Controlled)



Package Dimensions

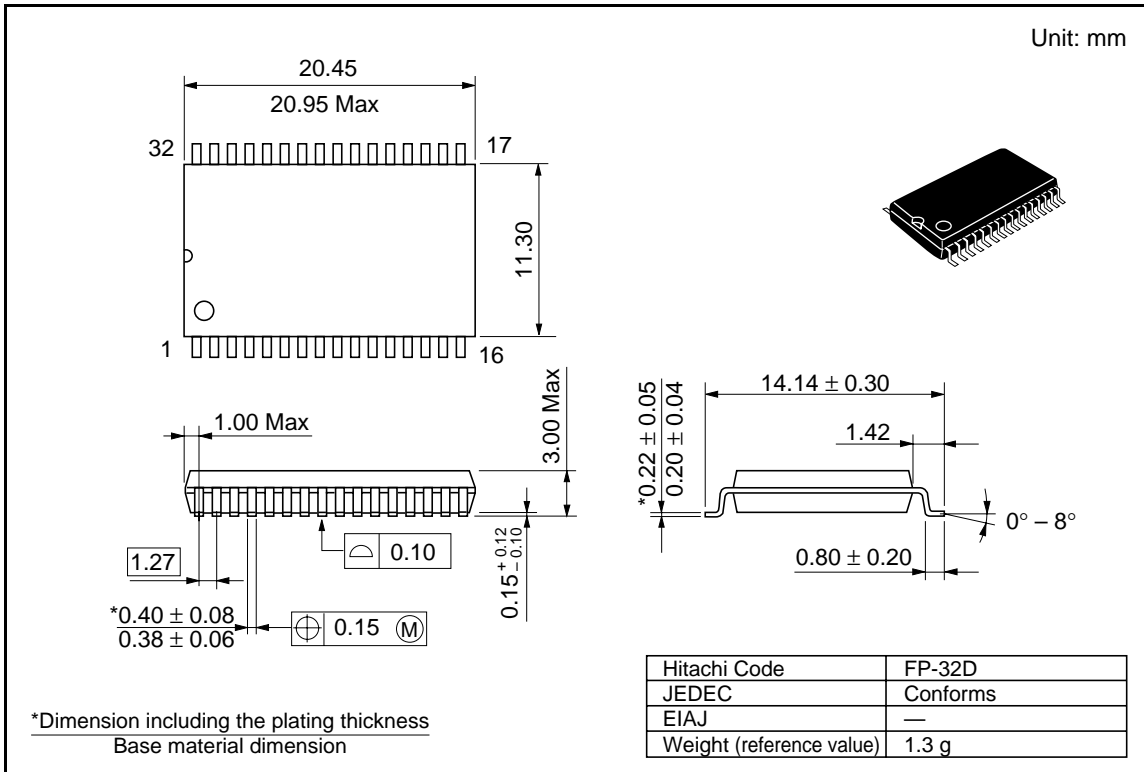
HM628512BLP Series (DP-32)



# HM628512B Series

## Package Dimensions (cont.)

### HM628512BLFP Series (FP-32D)

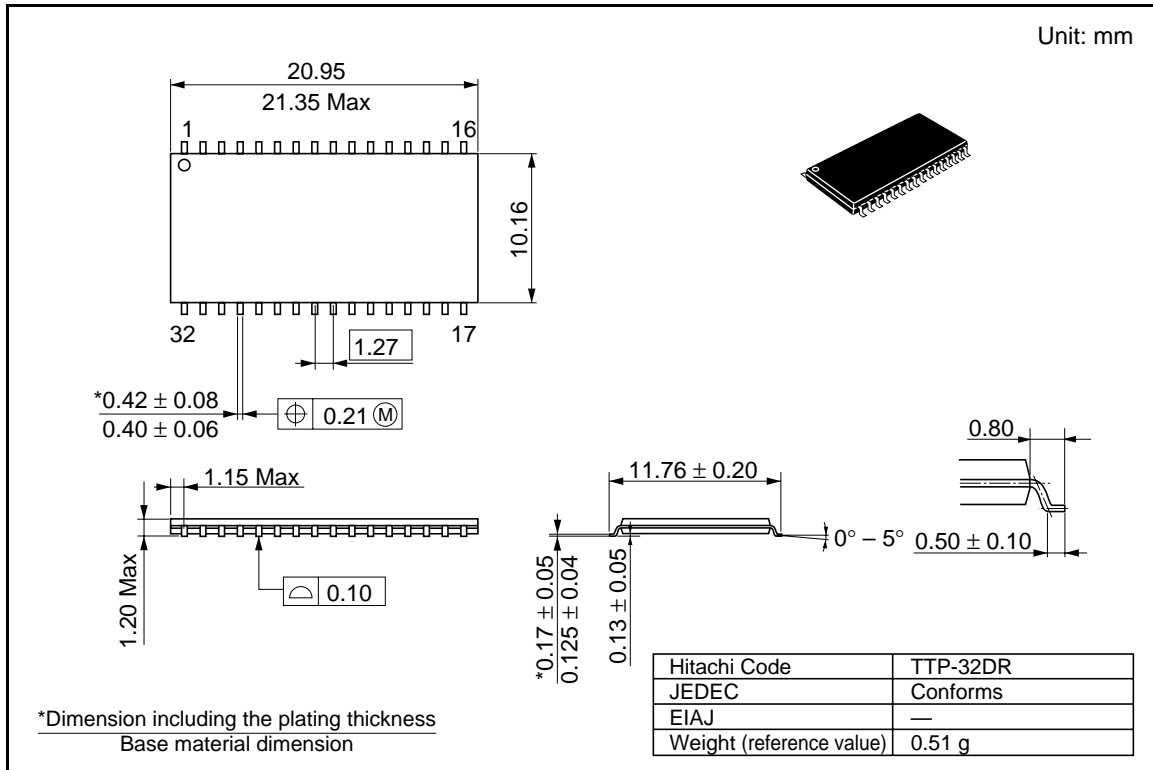




# HM628512B Series

## Package Dimensions (cont.)

### HM628512BLRR Series (TTP-32DR)



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## HM628512B Series

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### Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.0	Apr. 24, 1998	Initial issue	M. Higuchi	K. Imato
0.1	Nov. 19, 1998	DC Characteristics $I_{SB1}$ max: 40/20 $\mu$ A to 100/50 $\mu$ A Low $V_{CC}$ Data Retention Characteristics $I_{CCDR}$ max: 20/10 $\mu$ A to 50/15 $\mu$ A Change of note1 and 2	S. kunito	K. Imato
1.0	Jan. 13, 1999	Deletion of Preliminary Features Change of Power dissipation Standby: TBD (typ) to 10 $\mu$ W (typ) DC Characteristics $I_{SB1}$ typ: TBD/TBD to 2/2 $\mu$ A Low $V_{CC}$ Data Retention Characteristics $I_{CCDR}$ typ: TBD/TBD to 1/1 $\mu$ A	S. kunito	K. Imato
2.0	Apr. 8, 1999	Addition of L-UL-version DC Characteristics $I_{SB1}$ typ: 2/2 $\mu$ A to 2/2/2 $\mu$ A $I_{SB1}$ max: 100/50 $\mu$ A to 100/50/20 $\mu$ A Addition of note4 Low $V_{CC}$ Data Retention Characteristics $I_{CCDR}$ typ: 1/1 $\mu$ A to 1/1/1 $\mu$ A $I_{CCDR}$ max: 50/15 $\mu$ A to 50/15/10 $\mu$ A Addition of note3	S. kunito	K. Makuta
3.0	Aug. 24, 1999	Low $V_{CC}$ Data Retention Characteristics Correct error: $t_R$ unit ms to ns		