Integrated Device Technology, Inc.

128KB/256KB SECONDARY CACHE MODULE FOR THE INTEL® i486™

ADVANCE INFORMATION
IDT7MP6118
IDT7MP6119

FEATURES

- 128KB/256KB direct mapped, non-sectored, zero-wait-state secondary cache module
- Write-through and write-back functions supported
- Concurrent snooping is supported
- Software Instruction flushing is supported
- Ideal for use with i486-based systems
- Uses the IDT71589 32K x 9 CacheRAM™ with burst counter and self-timed write and the IDT71B74 cache-tag RAM
- Operates with external i486™ speeds of 33MHz
- 64 position dual read-out SIMM (Single In-line Memory Module) with 128 leads
- Single 5V (±5%) power supply
- Multiple GND pins and decoupling capacitors for maximum noise immunity
- Inputs/outputs directly TTL-compatible

DESCRIPTION

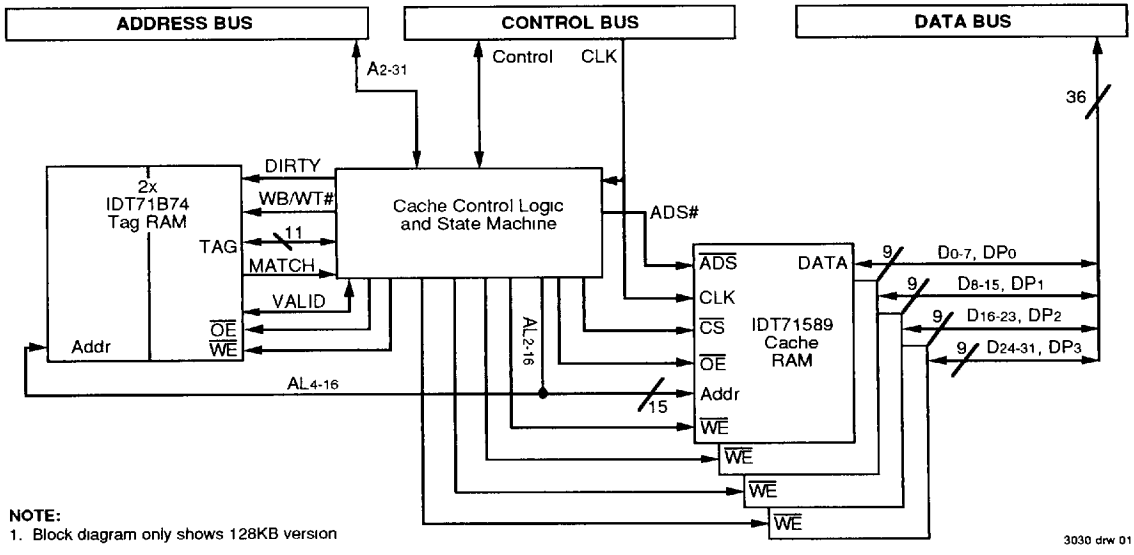
The IDT7MP6118/19 is a 128KB/256KB direct-mapped, non-sectored, zero-wait-state secondary cache supporting write-through, write-back functions and is ideal for use with many i486-based systems. The IDT7MP6118/19 uses IDT71589 32K x 9 CacheRAMs, IDT71B74 8K x 8 cache-tag RAMs along with cache control logic in plastic surface mount packages mounted on a multilayer epoxy laminate (FR-4) board. Extremely high speeds are achieved using IDT's high-performance, high-reliability BiCMOS and CMOS technologies.

The IDT7MP6118/19 supports zero-wait-state operation (2-1-1-1 cycles) at 33MHz during read and write cycles if the data is in the cache.

The dual read-out SIMM package configuration allows 128 signal leads to be placed on a package 3.85" x 1.5" (L x W) and is intended for use with dual read-out SIMM sockets. The IDT7MP6118 module thickness is 0.210" and the IDT7MP6119 module thickness is 0.365".

All inputs and outputs of the IDT7MP6118/19 are TTL-compatible and operate from a single 5V power supply. Multiple GND pins and on-board decoupling capacitors ensure maximum protection from noise.

FUNCTIONAL BLOCK DIAGRAM(1)



NOTE:
1. Block diagram only shows 128KB version

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PIN CONFIGURATION[1,2]

GND	65	1	GND
RESET	66	2	CLK
Vcc	67	3	Vcc
INV	68	4	CBOFF#
M/IO#	69	5	D/C#
FLUSH#	70	6	BLAST#
EADS#	71	7	SBOFF#
GND	72	8	GND
ADS#	73	9	W/R#
BE#0	74	10	BE#1
BE#2	75	11	BE#3
PWT	76	12	CS#
CRDY#	77	13	CKEN#
GND	78	14	GND
BRDY#	79	15	PULL_UP
SKEN#	80	16	START#
(See Note 2)	81	17	CHITM#
PRSN#	82	18	HITM#
WB/WT#	83	19	LOCK#
ID2	84	20	PCD
A2	85	21	A3
Vcc	86	22	Vcc
A4	87	23	A5
A6	88	24	A7
A8	89	25	A9
A10	90	26	A11
A12	91	27	A13
A14	92	28	A15
A16	93	29	A17
GND	94	30	GND
A18	95	31	A19
A20	96	32	A21
A22	97	33	A23
A24	98	34	A25
A26	99	35	A27
A28	100	36	A29
A30	101	37	A31
GND	102	38	GND
D0	103	39	D1
D2	104	40	D3
D4	105	41	D5
Vcc	106	42	Vcc
D6	107	43	D7
GND	108	44	GND
DP0	109	45	DP1
D8	110	46	D9
D10	111	47	D11
D12	112	48	D13
GND	113	49	GND
D14	114	50	D15
D16	115	51	D17
D18	116	52	D19
D20	117	53	D21
GND	118	54	GND
D22	119	55	D23
DP2	120	56	DP3
D24	121	57	D25
D26	122	58	D27
GND	123	59	GND
D28	124	60	D29
D30	125	61	D31
Vcc	126	62	Vcc
ID1	127	63	ID0
GND	128	64	GND

SIMM TOP VIEW

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ID TRUTH TABLE

ID2	ID1	ID0	Description
1	1	1	128KB, write-through
1	1	0	256KB, write-through
1	0	1	512KB, write-through
1	0	0	1MB, write-through
0	1	1	128KB, write-back
0	1	0	256KB, write-back
0	0	1	512KB, write-back
0	0	0	1MB, write-back

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NOTES:
1. Module pins 63, 84 and 127 are used to identify the size of the cache present in the socket. Consult the ID Truth Table for more details.
2. Pin 81 must be connected to VCC for proper operation of the module.

PIN DEFINITION

Symbol	Pin Function	I/O	Level	Description
CLK	Clock	I	N/A	This is the clock input to the cache. All timing references for the cache are made with respect to this input.
RESET	Reset	I	HIGH	If RESET is sampled HIGH by the cache, the cache control logic is reset to a known state. In addition, when RESET is sampled HIGH, the entire cache contents is invalidated.
FLUSH#	Flush	I	LOW	If FLUSH# is sampled LOW, the cache control logic goes into a flush pending state. While the cache is in a flush pending state, it will continue to service CPU cycles until it detects an I/O cycle. After detecting an I/O cycle, the cache invalidates its entire contents as it searches through the cache for dirty lines. If a line is not dirty, that line is invalidated and all associated flags are cleared. If a line is dirty, that line is written back by the cache and then it is invalidated and the associated flags cleared.
SBOFF#	System Backoff	I	LOW	This input forces the cache off of the CPU address and data buses. When SBOFF# is asserted, the cache will only recognize invalidation and snoop cycles; however, the cache will not write the data back for an invalidation/snoop hit to a dirty line until SBOFF# is deasserted.
CBOFF#	Cache Backoff	O	LOW	This output is asserted by the cache to force the CPU off the bus when the cache detects that a dirty line must be evicted from the cache. If SBOFF# is asserted the cache will not assert CBOFF#, except when the cache detects an invalidation/snoop hit to a dirty line and it does not sample HITM# LOW.
EADS#	External Address Strobe	I	LOW	This input is used in conjunction with INV by external devices to snoop, or invalidate, a cache line. If EADS# is sampled LOW simultaneous with ADS# LOW during a memory write cycle to a write through line, the cache invalidates the line. If EADS# is sampled LOW simultaneous with ADS# LOW during either a memory write cycle to a write back line or a memory read cycle, the cache ignores EADS#.
INV	Invalidate	I	HIGH	This input is used in conjunction with EADS# to snoop, or invalidate, a cache line. If INV is HIGH the cache will consider the access as an invalidation. If INV is LOW when EADS# is asserted the cache will consider the access as a snoop.
ADS#	Address Strobe	I/O	LOW	This pin is used by external devices to inform the cache that a valid address is present on the input of the cache. This pin is driven by the cache, while the cache is asserting CBOFF#, to evict a dirty line from the cache or to supply dirty data for a snoop hit.
M/IO#	Memory/IO	I/O	N/A	This pin is used by external devices to inform the cache that a memory access is being made when this pin is HIGH, or that an I/O access is being made when this pin is LOW. I/O cycles are not considered cacheable. This pin is driven HIGH by the cache, while the cache is asserting CBOFF#, to evict a dirty line from the cache or to supply dirty data for a snoop hit.
W/R#	Write/Read	I/O	N/A	This pin is used by external devices to inform the cache that either a write is being performed when this pin is HIGH, or that a read is being performed if this pin is LOW. This pin is driven HIGH by the cache, while the cache is asserting CBOFF#, to evict a dirty line from the cache or to supply dirty data for a snoop hit.
D/C#	Data/Control	I/O	N/A	This pin is used by the cache in conjunction with the M/IO#, W/R#,

				BE#(0:3) and A(2) to determine when a special bus cycle is being executed, and the type of special bus cycle being executed. This pin is driven HIGH by the cache, while the cache is asserting CBOFF#, to evict a dirty line from the cache or to supply dirty data for a snoop hit.
START#	Memory Start	O	LOW	This output is asserted by the cache to inform the system that it must service the current memory access. This output is also asserted during write/snoop cycles when ADS# and EADS# are sampled LOW simultaneously and the line is marked write through. START# is driven HIGH if the cache samples SBOFF# LOW.
BRDY#	Burst Data Ready	I/O	LOW	This pin is asserted by the cache when either a read hit is detected, or a write hit is detected and the line is marked as write back. This pin is an input to the cache when the cache detects a read miss, a write miss, or during locked bus cycles. This pin is also an input during write through write cycles. A write cycle is defined as write through if a hit occurs on a line that is marked write through. A write cycle is also considered write through if the cache samples either PCD or PWT HIGH at the initiation of the write cycle.
RDY#	Data Ready	I/O	LOW	This pin is asserted by the cache during the fourth word transfer of a burst cycle being serviced by the cache. This pin is an input to the cache when the cache detects a read miss, a write miss, or during locked bus cycles. This pin is also an input during write through write cycles. A write cycle is defined as write through if a hit occurs on a line that is marked write through. A write cycle is also considered write through if the cache samples either PCD or PWT HIGH at the initiation of the write cycle.
BLAST#	Burst Last	I/O	LOW	This pin is used by the cache to determine the last cycle of a burst cycle. This pin is driven by the cache during a line write, while the cache is asserting CBOFF#, when either evicting a line from the cache, or to supply dirty data for a snoop hit. The cache asserts BLAST# concurrent with the fourth word transfer from the cache.
A(2:31)	Address	I/O	N/A	These are the address lines to the cache. They are inputs to the cache, except when the cache is performing a write cycle for either a line eviction or to supply dirty data for a snoop hit.
BE#(0:3)	Byte Enable	I/O	LOW	These are the byte enable inputs to the cache. These inputs are sampled during write cycles to control byte writes, and they are used in conjunction with M/IO#, W/R#, D/C# and A(2) to determine when a special bus cycle is being executed. These pins are driven LOW when the cache is performing a write cycle for either a line eviction, or to supply dirty data for a snoop hit.
CS#	Chip Select	I	LOW	This input is sampled at the beginning of all bus cycles and invalidation cycles. If CS# is sampled high at the beginning of the cycle, the cache will not recognize the cycle.
D(0:31)	Data	I/O	N/A	These are the data lines of the cache. The cache will place valid data on these lines during read hits, and when the cache is performing a write cycle for either a line eviction, or to supply dirty data for a snoop hit.
DP(0:3)	Data Parity	I/O	N/A	These are the data parity lines of the cache. Functionality is the same as the data lines described above.
WB/WT#	Write Back/ Write Through	I/O	N/A	WB/WT# is an input to the cache when a line of data is loaded into the cache. If PWT is sampled HIGH at the beginning of a read cycle that results in a cache miss, the value of this pin is ignored and the line returned is considered write through. If PWT is sampled LOW at the beginning of a read cycle, and WB/WT# is sampled HIGH during the first word transfer of a line fill, the line is marked as write back. If PWT is sampled LOW at the beginning of

				a read cycle, and WB/WT# is sampled LOW during the first word transfer of a line fill, the line is marked as write through. If the line is marked as write back, the cache will update its memory contents without passing the cycle on to other devices during a memory write cycle. If the line is marked as write through, the cache will update its memory contents when the write cycle is serviced by the system. The cache drives this pin when servicing read hit cycles, and when servicing write hit cycles to write back lines. The cache floats this pin during write miss cycles, and during write through write cycles.
HITM#	Hit-Modified Input	I	LOW	This input is used to indicate to the cache that a dirty line is present in the CPU level 1 cache during snoop or invalidation cycles.
CHITM#	Hit-Modified Output	O	LOW	This output is asserted by the cache to indicate that a dirty line is being accessed in the cache during a memory read bus cycles. The cache also asserts this output when a dirty line is present in the cache during a snoop or invalidation cycle.
CKEN#	Cacheable Data Output	O	LOW	This output is asserted by the cache to indicate whether data from the cache is considered cacheable by the CPU. The cache will assert CKEN# for read hit cycles.
SKEN#	Cacheable Data Input	I	LOW	This input is sampled by the cache to determine whether the data being returned during a read miss is cacheable. SKEN# must be sampled LOW at least one cycle before the first word is transferred to the cache, and SKEN# must also be sampled LOW at least one cycle before the last word is transferred. This input is ignored if either PCD is sampled HIGH, or LOCK# is sampled LOW at the beginning of a read cycle.
PWT	Page Write Through	I/O	HIGH	This input is sampled by the cache at the initiation of memory read and write cycles. If PWT is sampled HIGH at the initiation of a memory read that results in a cache miss, the line returned is automatically considered write through. If PWT is sampled HIGH at the initiation of memory write cycle, the cache ignores the value of its internal write back/write through flag, and it is forced to treat the write cycle as write through. The cache drives this pin LOW, while CBOFF# is asserted, when the cache executes a write cycle to evict a dirty line from the cache or to supply dirty data for a snoop hit.
PCD	Page Cache Disable	I/O	HIGH	If PCD is sampled HIGH at the beginning of a read cycle and the data is contained in the cache, the cache ignores the value of PCD and treats the cycle as a normal cycle. If the data is not contained in the cache, the cache considers the data returned as non-cacheable. If PCD is sampled HIGH at the beginning of a write cycle, the cache ignores its internal write back/write through flag, and it treats the write cycle as write through. The cache drives this pin LOW while CBOFF# is asserted, when the cache executes a write cycle to evict a dirty line from the cache or to supply dirty data for a snoop hit.
LOCK#	Lock	I/O	LOW	If LOCK# is sampled LOW at the beginning of a read cycle and the data in the cache is not dirty, the read cycle is treated as a non-cacheable read miss. If the cache contains dirty data at the read address location requested by the locked cycle, the cache performs a coordinated read cycle. In a coordinated read, the cache supplies data to the CPU, but the memory controller drives RDY# or BRDY# to complete the cycle. If LOCK# is sampled LOW at the beginning of a write cycle, the cache ignores its internal write back/write through flag, and it treats the write cycle as write through. LOCK# assertion is only recognized by the cache if LOCKEN is

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				sampled HIGH simultaneously. The cache drives this pin HIGH, while CBOFF# is asserted, when the cache executes a write cycle to evict a dirty line from the cache or to supply dirty data for a snoop hit.
ID(0:2)	ID pins	O	N/A	These pins are used to identify the cache configuration to the system. These pins should be tied to pull-up resistors external to the cache. To produce a logic HIGH level on any ID pin, the pin is a no connect on the module. To produce a logic LOW level on any pin, the pin is hard-wired to ground on the module
PRSN#	Presence	O	LOW	This output informs the system that a cache module is present in the system. This pin is hard-wired to ground on the cache module.
PULL_UP	Pull up	O	HIGH	This output pin corresponds to the BRDYO# output of the IDT7MP6104, and it is tied to VCC through a pull up resistor.

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RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
GND	Supply Voltage	0	0	0 0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	–0 5[1]	—	0.8	V

NOTE:
1. VIL = –3 0V for pulse width less than 5ns.

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ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

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NOTE:
Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE[1, 2]

(T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter[1]	Condition	7MP6118/9	Unit
C_{IN}	Input Capacitance (Address, Control)	V_{IN} = 0V	15/15	pF
C_{IN}	Input Capacitance (CLK)	V_{IN} = 0V	45/75	pF
C_{OUT}	Output Capacitance (Control)	V_{IN} = 0V	15/15	pF
$C_{I/O}$	Data I/O Capacitance	V_{OUT} = 0V	10/20	pF

NOTES:
1 These parameters are guaranteed by design but not tested
2. These parameters are maximum values.

3030 tbl 04

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 5%

3030 tbl 06

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 5%, T_A = 0°C to 70°C)

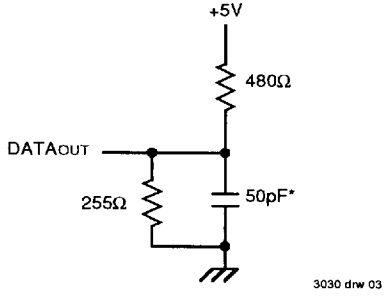
Symbol	Parameter	Test Condition	Min.	7MP6118 Max.	7MP6119 Max.	Unit
$\|I_{LI}\|$	Input Leakage Current (Data)	V_{CC} = Max, V_{IN} = GND to V_{CC}	—	10	20	µA
$\|I_{LI}\|$	Input Leakage Current (Address)	V_{CC} = Max, V_{IN} = GND to V_{CC}	—	10	10	µA
$\|I_{LI}\|$	Input Leakage Current (Control)	V_{CC} = Max, V_{IN} = GND to V_{CC}	—	10	10	µA
$\|I_{LI}\|$	Input Leakage Current (CLK)	V_{CC} = Max, V_{IN} = GND to V_{CC}	—	50	90	µA
$\|I_{LO}\|$	Output Leakage Current	V_{OUT} = 0V to V_{CC}, V_{CC} = Max	—	10	20	µA
V_{OLD}	Output Low Voltage (Data)	I_{OL} = 8mA, V_{CC} = Min	—	0 4	0.4	V
V_{OLC}	Output Low Voltage (Control)	I_{OL} = 12mA, V_{CC} = Min	—	0 5	0 5	V
V_{OH}	Output High Voltage (Data and Control)	I_{OH} = –4mA, V_{CC} = Min	2 4	—	—	V
I_{CC}	Operating Power Supply Current	V_{CC} = Max., $\overline{CS} \le V_{IL}$, f = f_{MAX}, Outputs Open	—	1250	2400	mA

3030 tbl 06

AC TEST CONDITIONS

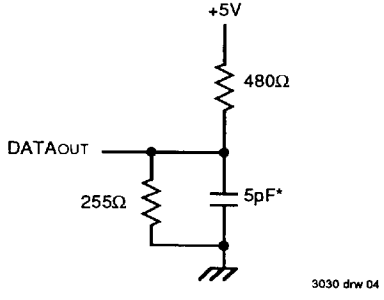
Input Pulse Levels	GND to 3 0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1 5V
Output Reference Levels	1 5V
Output Load	See Figures 1 and 2

3030 tbl 07



*including scope and jig capacitances

Figure 1. Output Load



*including scope and jig capacitances

Figure 2. Output Load (for t_{OHZ}, t_{CHZ}, t_{OLZ} and t_{CLZ})

AC ELECTRICAL CHARACTERISTICS[1, 2]

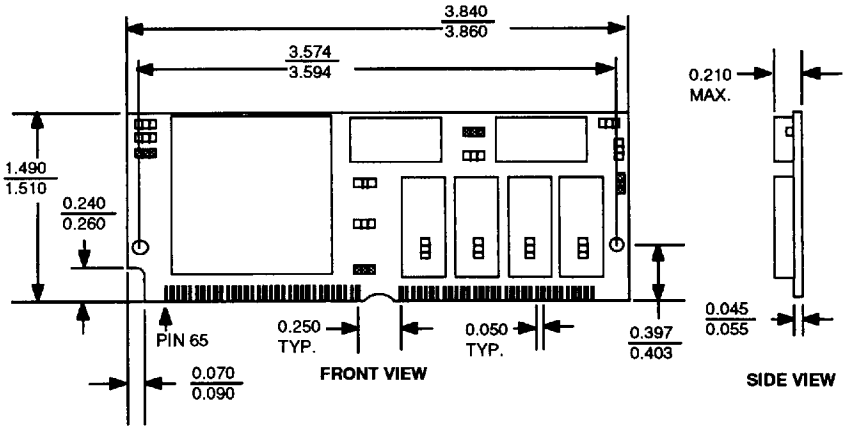
(V_{CC} = 5.0V ± 5%, T_A = 0° to +70°C)

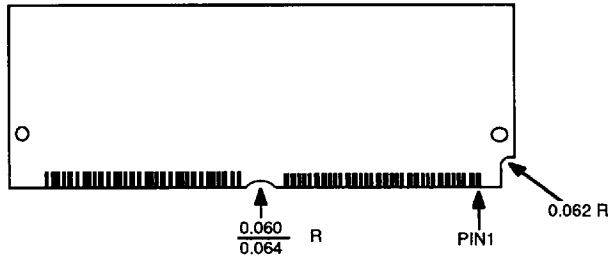
Symbol	Parameter	33MHz Min.	33MHz Max.	Unit
t_1	Clock Period	30	—	ns
t_2	Clock HIGH Time	11	—	ns
t_3	Clock LOW Time	11	—	ns
t_4	A_{2}-A_{31}, $BE\#_{0\text{-}3}$ Set-up Time	13	—	ns
t_5	A_{2}-A_{31}, $BE\#_{0\text{-}3}$ Hold Time	10	—	ns
t_6	ADS#, M/IO#, W/R#, D/C# LOCK#, PCD, PWT Set-up Time	10	—	ns
t_7	ADS#, M/IO#, W/R#, D/C# LOCK#, PCD, PWT Hold Time	3	—	ns
t_8	BLAST#, CS# Set-up Time	8	—	ns
t_9	BLAST#, CS# Hold Time	3	—	ns
t_{10}	CRDY#, CBRDY# Set-up Time	10	—	ns
t_{11}	CRDY#, CBRDY# Hold Time	3	—	ns
t_{12}	SKEN# Set-up Time	8	—	ns
t_{13}	SKEN# Hold Time	3	—	ns
t_{14}	D_0-D_{31}, DP_0-DP_3 Set-up Time	5	—	ns
t_{15}	D_0-D_{31}, DP_0-DP_3 Hold Time	3	—	ns
t_{16}	EADS#, INV Set-up Time	8	—	ns
t_{17}	EADS#, INV Hold Time	3	—	ns
t_{18}	A_4-A_{31} Set-up Time (Snoop)	6	—	ns
t_{19}	A_4-A_{31} Hold Time (Snoop)	10	—	ns
t_{20}	RESET, FLUSH# Set-up Time	8	—	ns
t_{21}	RESET, FLUSH# Hold Time	3	—	ns
t_{22}	RESET, FLUSH# Pulse Width	80	—	ns
t_{23}	RDY#, BRDY#, START#, CHITM#, WB/WT#, CKEN# Valid	—	18	ns
t_{24}[3]	RDY#, BRDY#, WB/WT# Float Delay	—	11	ns
t_{25}	A_{2}-A_{31}, $BE\#_{0\text{-}3}$ S, ADS#, M/IO#, D/C#, BLAST#, LOCK#, PCD, PWT Valid (Writeback)	—	16	ns
t_{26}	A_{2}-A_{31}, $BE\#_{0\text{-}3}$ S, ADS#, M/IO#, D/C#, BLAST#, LOCK#, PCD, PWT Float Delay (Writeback)	—	20	ns
t_{27}	D_0-D_{31}, DP_0-DP_3 Valid (Read Hit/Writeback)	—	22	ns
t_{28}	WB/WT# Set-up Time	9	—	ns
t_{29}	WB/WT# Hold Time	3	—	ns
t_{30}	CBOFF# Valid Time	—	18	ns
t_{31}	SBOFF# Set-up Time	9	—	ns
t_{32}	SBOFF# Hold Time	3	—	ns

3030 tbl 08

NOTES:
1 Please consult the factory for 50MHz versions
2. AC parameters guaranteed by design.
3. RDY#, BRDY#, WB/WT# Float Delay time is measured from the falling edge of the CLK input

PACKAGE DIMENSIONS
7MP6118





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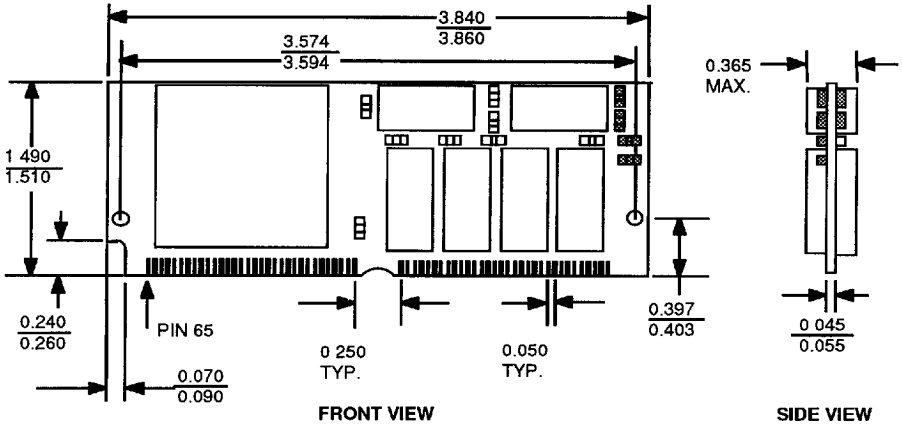
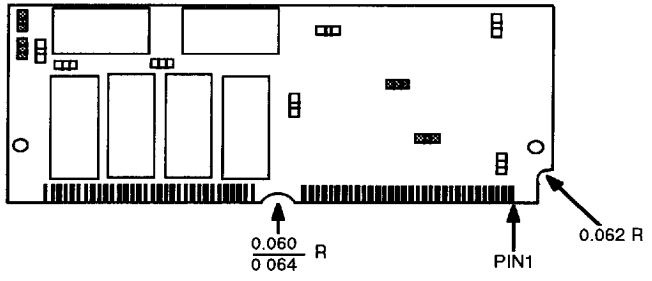
PACKAGE DIMENSIONS
7MP6119





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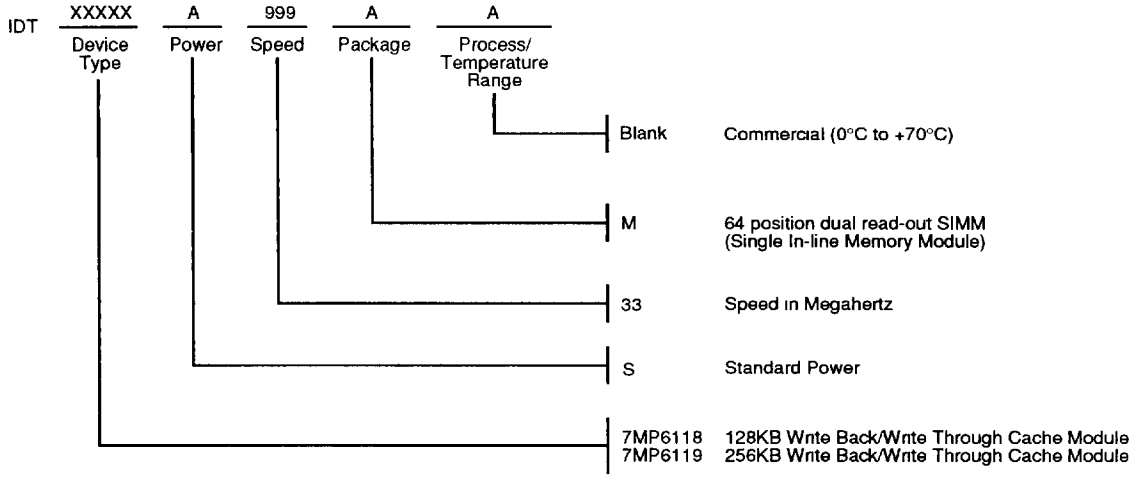
ORDERING INFORMATION



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