TAIWAN SEMICONDUCTOR

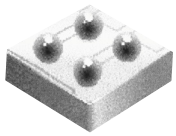
PRELIMINARY DATA SHEET

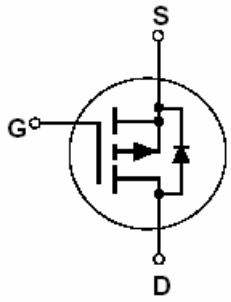
For information only

TS4405P - Single P-Channel 1.8V Specified MicroSURF™

General Description

Taiwan Semiconductor's new low cost, state of the art MicroSURF™ lateral MOSFET process technology in chipscale bondwireless packaging minimizes PCB space and $R_{DS(ON)}$ plus provides an ultra-low Qg X $R_{DS(ON)}$ figure of merit.



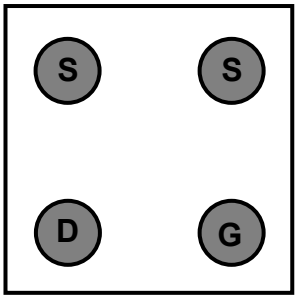


Features

- -4.9A, -12V $R_{DS(ON)}$ = 50mΩ at -4.5 Volts
- -4.4A, -12V $R_{DS(ON)}$ = 70mΩ at -2.5 Volts
- -4.0A, -12V $R_{DS(ON)}$ = 90mΩ at -1.8 Volts
- Low profile package: less than 0.8mm height when mounted on PCB.
- Occupies only 1.21 mm^2 of PCB area.
  Less than 30% of the area of a SC-70.
- Excellent thermal characteristics.
- Lead free solder bumps available.

MicroSURF™ for Load Switching and PA Switch

Patent Pending



Bump Side View

Absolute Maximum Ratings

T_A=25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain-Source Voltage	-12	V
V_{GSS}	Gate-Source Voltage	±8	V
I_D	Drain Current – Continuous	-4.9	A
	– Pulsed	-10	
P_D	Power Dissipation (Steady State)	1.5	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

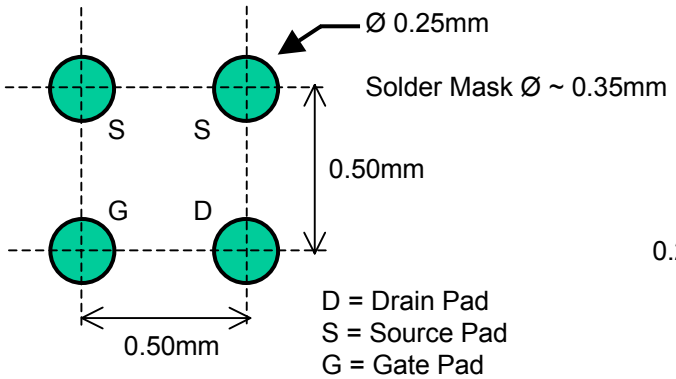
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	85	°C/W
$R_{\theta JR}$	Thermal Resistance, Junction-to-Ball	20	
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1.8	

Electrical Characteristics

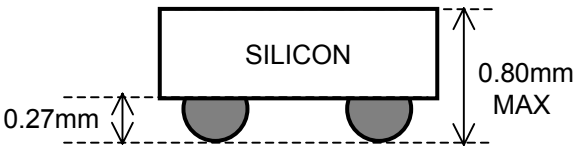
T_A=25°C unless otherwise specified

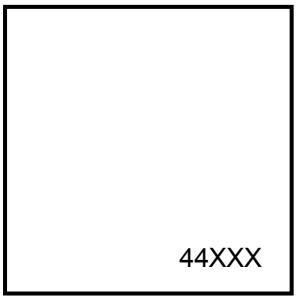
Symbol	Parameter	Test Condition	Min	Typ	Max	Units
$V_{(BD)SS}$	Drain-Source Breakdow n Voltage	V_{GS}=0V, I_D=-250μA			-11	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-12V, V_{GS}=0V			-1	μA
	Zero Gate Voltage Drain Current	V_{DS}=-12V, V_{GS}=0V, T=70°C			-5	μA
I_{GSS}	Gate-Body Leakage	V_{GS}=±8V, V_{DS}=0V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250μA		-0,58		V
$r_{DS(on)}$	Drain-Source On-State Resistance	V_{GS}=-4.5V, I_D=-1A			50	mΩ
	Drain-Source On-State Resistance	V_{GS}=-2.5V, I_D=-1A			70	mΩ
	Drain-Source On-State Resistance	V_{GS}=-1.8V, I_D=-1A			90	mΩ
C_{iss}	Input Capacitance	V_{DS}=-12V, V_G=0V, F=1MHZ		300		pF
C_{oss}	Output Capacitance	V_{DS}=-12V, V_G=0V, F=1MHZ		200		pF
C_{rss}	Reverse Transfer Capacitance	V_{DS}=-12V, V_G=0V, F=1MHZ		80		pF
Q_g	Total Gate Charge	V_{GS}=-4.5V, I_D=-4A, V_{DS}=-8V		10		nC
Q_{gs}	Gate Source-Charge	V_{GS}=-4.5V, I_D=-4A, V_{DS}=-8V		2		nC
Q_{gd}	Gate Drain-Charge	V_{GS}=-4.5V, I_D=-4A, V_{DS}=-8V		1		nC
V_{SD}	Diode Forw ard Voltage	I_S=-4A, V_{GS}=0V		0.7		V

Dimensional Outline and Pad Layout



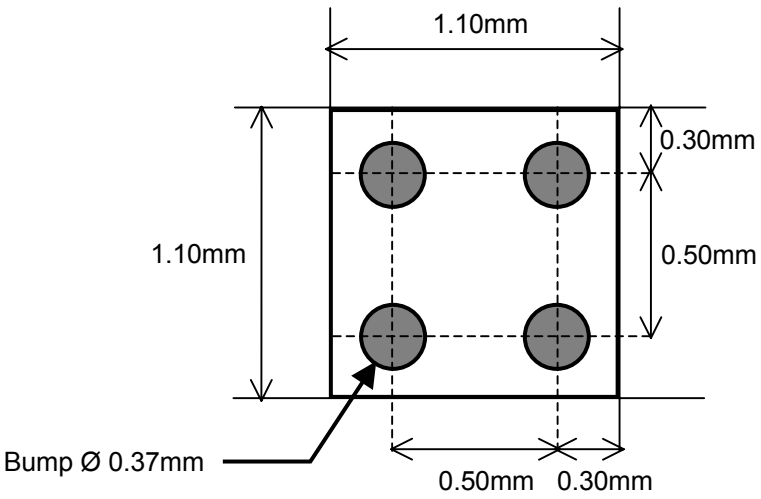
LAND PATTERN
RECOMMENDATION





MARK ON BACKSIDE OF DIE

XXX = Date/Lot Traceability Code



Bumps are Eutectic solder 63/37 Sn/Pb