



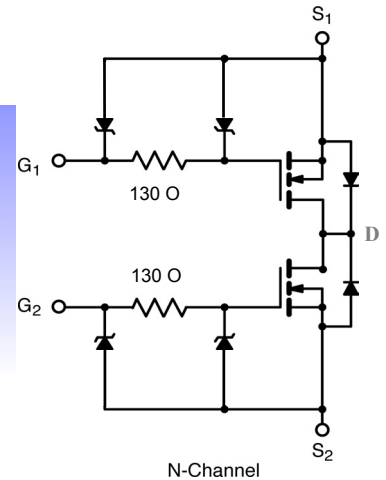
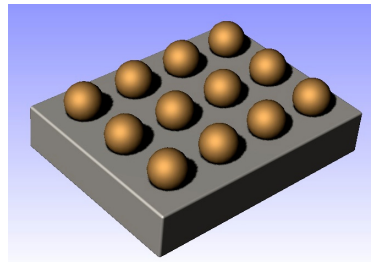
For information only

Battery Protection MicroSURF™

TS8314 – Bi-directional N-Channel 2.5V Specified MicroSURF™

General Description

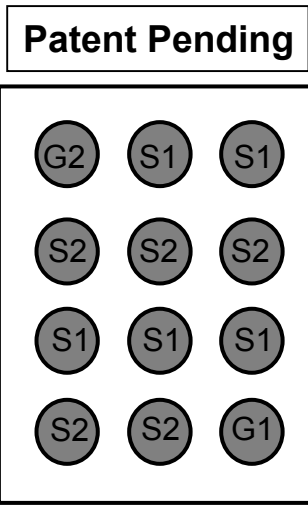
Taiwan Semiconductor's new low cost, state of the art MicroSURF™ lateral MOSFET process technology in chip-scale bondwireless packaging minimizes PCB space and $R_{DS(ON)}$ plus provides an ultra-low $Q_g \times R_{DS(ON)}$ figure of merit.



Features

- 6.5A, 20V $R_{DS1(ON)}$ equivalent = 15mΩ at 4.5 Volts
- 5.5A, 20V $R_{DS1(ON)}$ equivalent = 22mΩ at 2.5 Volts
- Low profile package: less than 0.8mm height when mounted on PCB.
- Occupies less than 1/5 the area of TSSOP-8.
- Excellent thermal characteristics.
- Integrated gate diodes provide ElectroStatic Discharge (ESD) protection of 4000V Human Body Model (HBM).
- Lead free solder bumps available.

MicroSURF™ for Battery Protection



Bottom: Bump Side

Absolute Maximum Ratings

$T_A=25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{S1S2}	Source1-Source2 Voltage	20	V
V_{GS}	Gate-Source Voltage	+12 / -0.5	V
I_{S1S2}	Source1-Source2 Current – Continuous – Pulsed	6.5	A
		13	
P_D	Power Dissipation (Steady State)	1.3	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	82	$^\circ\text{C/W}$
$R_{\theta JR}$	Thermal Resistance, Junction-to-Balls	7	

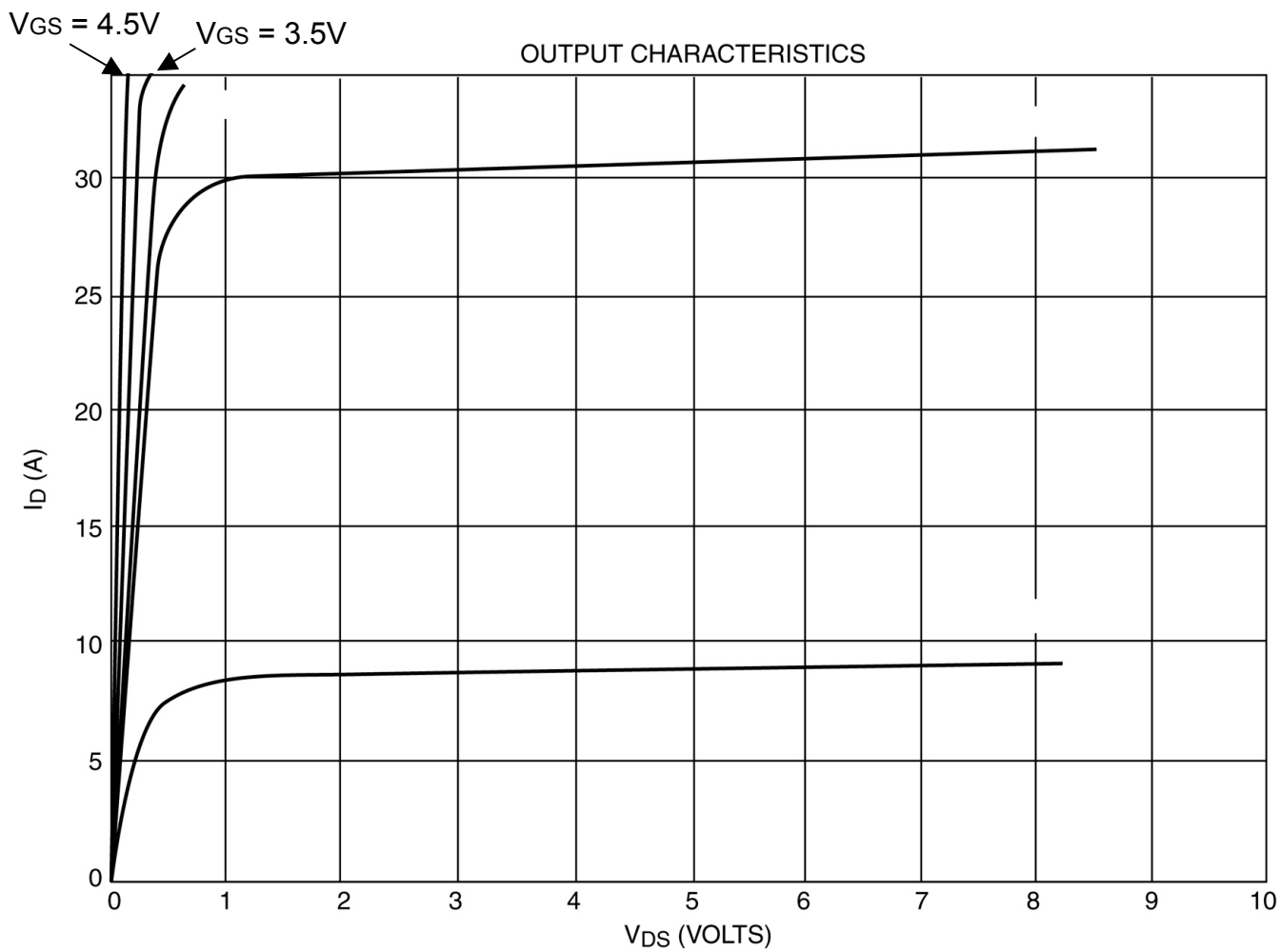
Electrical Characteristics

TS8314

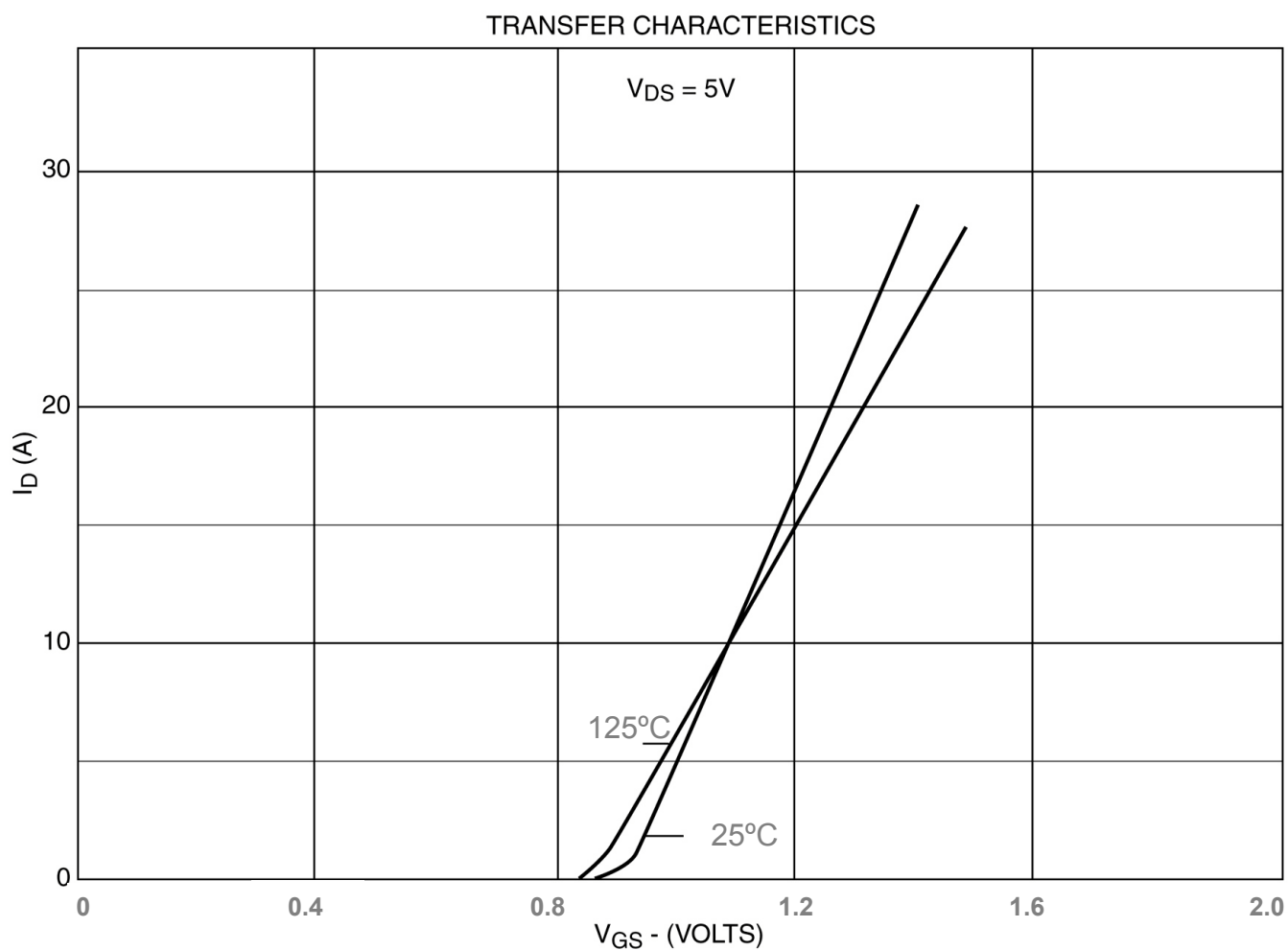
Electrical Characteristics

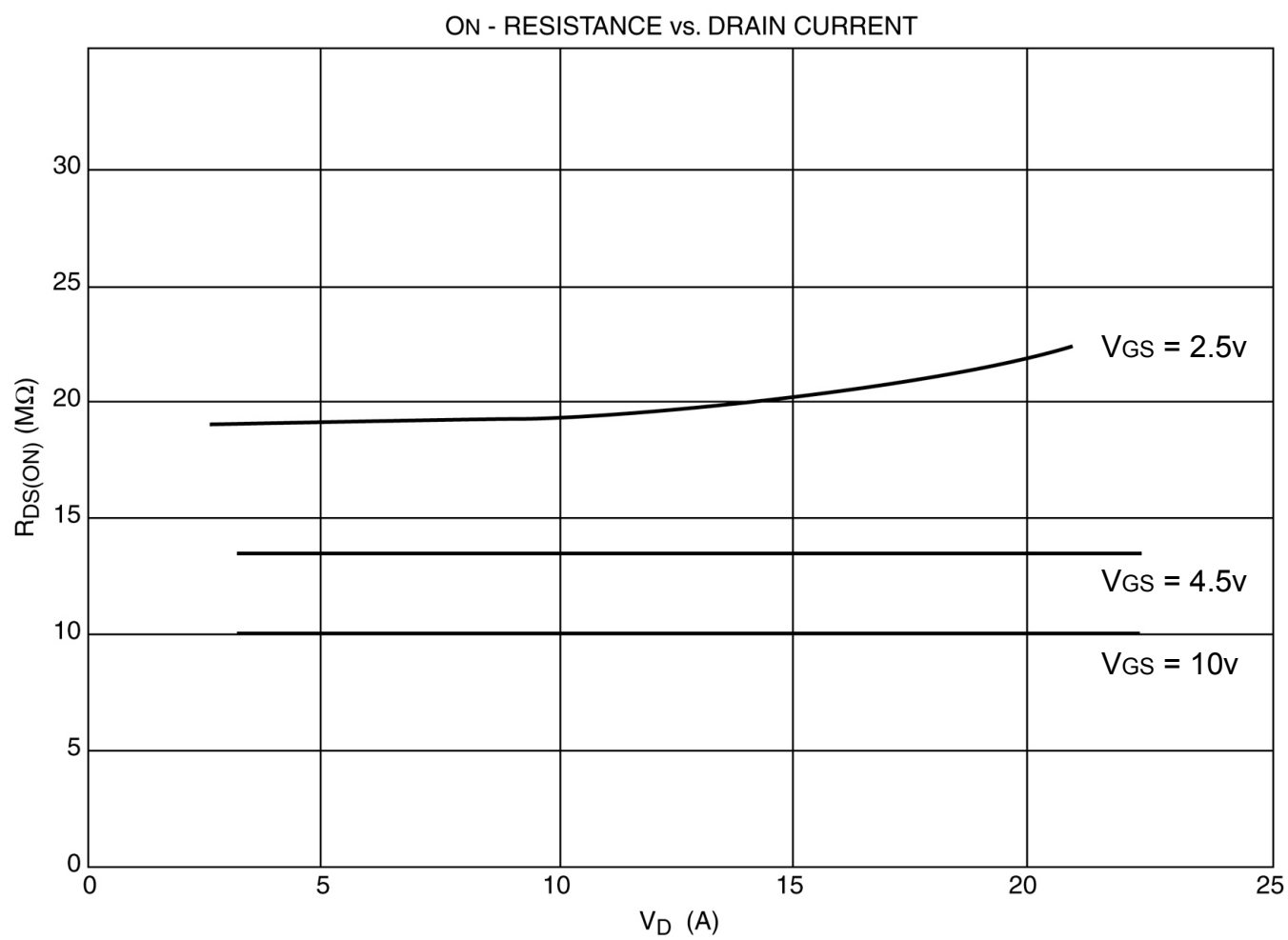
T_A=25°C unless otherwise specified

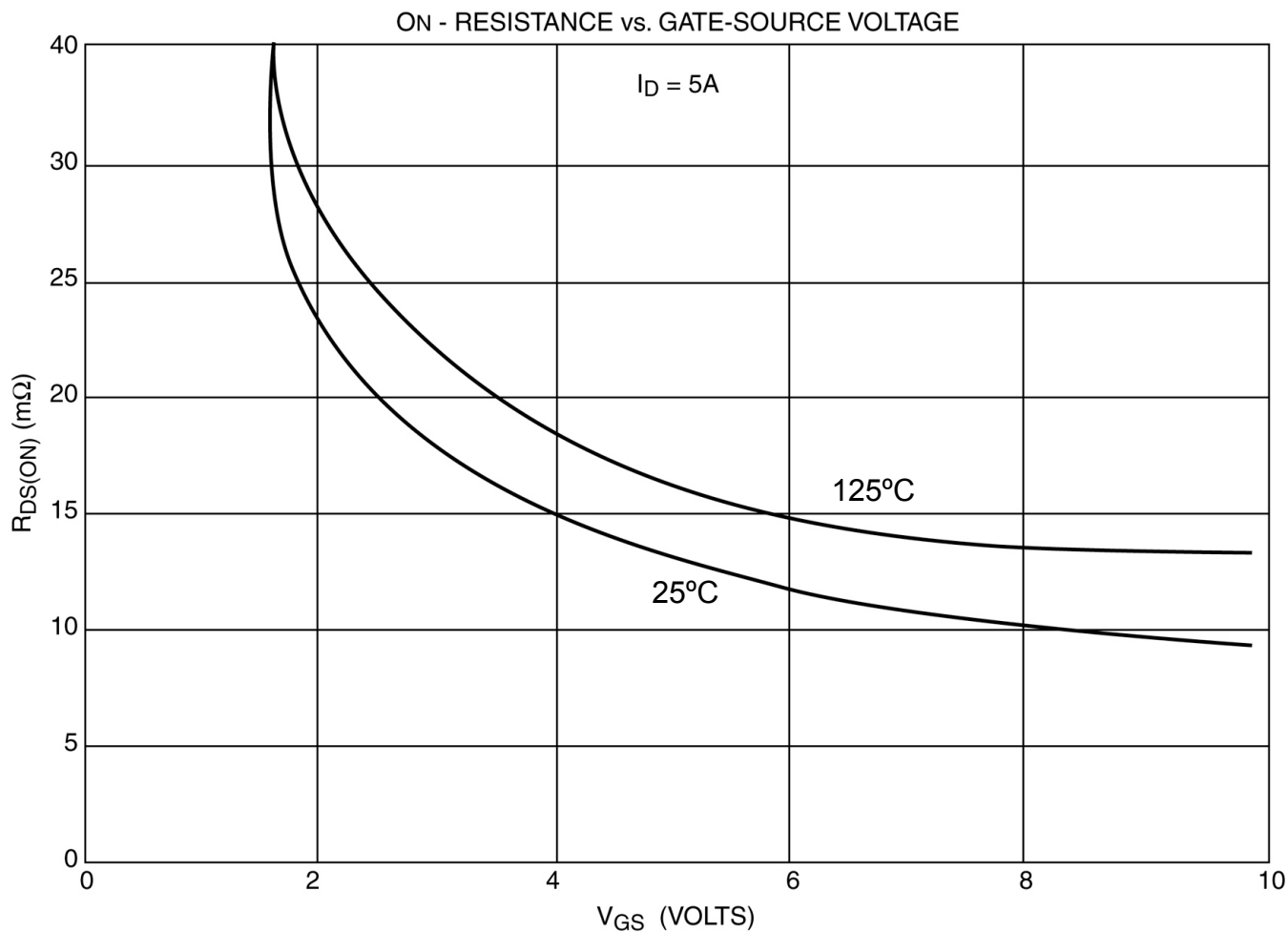
Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V _{(BD)S_{IS2S}}	Source-to-Source Breakdown Voltage	V _{GS} =0V, I _S =250μA	20			V
I _{SIS2S}	Zero Gate Voltage Source Current	V _{SIS2} =20V, V _{GS} =0V, T=150°C			50	μA
I _{GSS}	Gate-Body Leakage	V _{GS} =7V, V _{SIS2} =0V			100	nA
I _{GSS}	Gate-Body Leakage	V _{GS} =12V, V _{SIS2} =0V			10	mA
V _{GS(th)}	Gate Threshold Voltage	V _{SIS2} =V _{GS} , I _S =250μA		0.8	1.2	V
r _{SIS2(on)}	Source-to-Source On-State Resistance	V _{GS} =4.5V, I _S =6.5A		26	30	mΩ
	Source-to-Source On-State Resistance	V _{GS} =2.5V, I _S =5.5A		38	44	mΩ
r _{DS I(on) equivalent}	Source-to-Source On-State Resistance	V _{GS} =4.5V, I _S =6.5A		13	15	mΩ
	Drain-to-Source On-State Resistance	V _{GS} =2.5V, I _S =5.5A		19	22	mΩ
C _{iss}	Input Capacitance	V _{SIS2} =20V, V _G =0V, F=1MHZ		1100		pF
C _{oss}	Output Capacitance	V _{SIS2} =20V, V _G =0V, F=1MHZ		400		pF
C _{rss}	Reverse Transfer Capacitance	V _{SIS2} =20V, V _G =0V, F=1MHZ		300		pF
Q _g	Total Gate Charge	V _{GS} =5V, I _S =8A, V _{SIS2} =10V		15		nC
t _{rr}	Source-Drain Reverse Recovery Time	I _S =1A, V _{GS} =0V, di/dt=100A/μs		40		ns
V _{SS}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.71		V

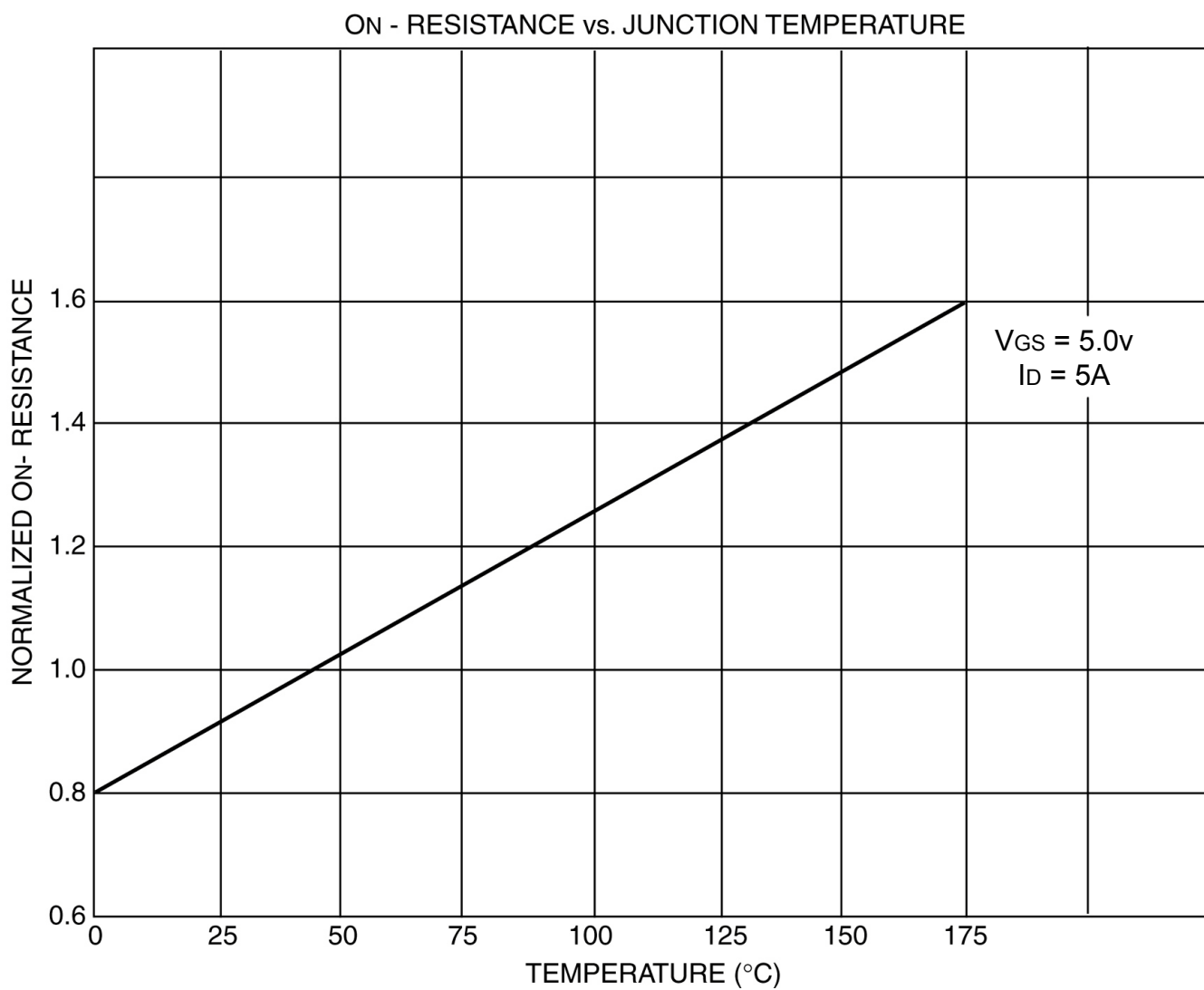


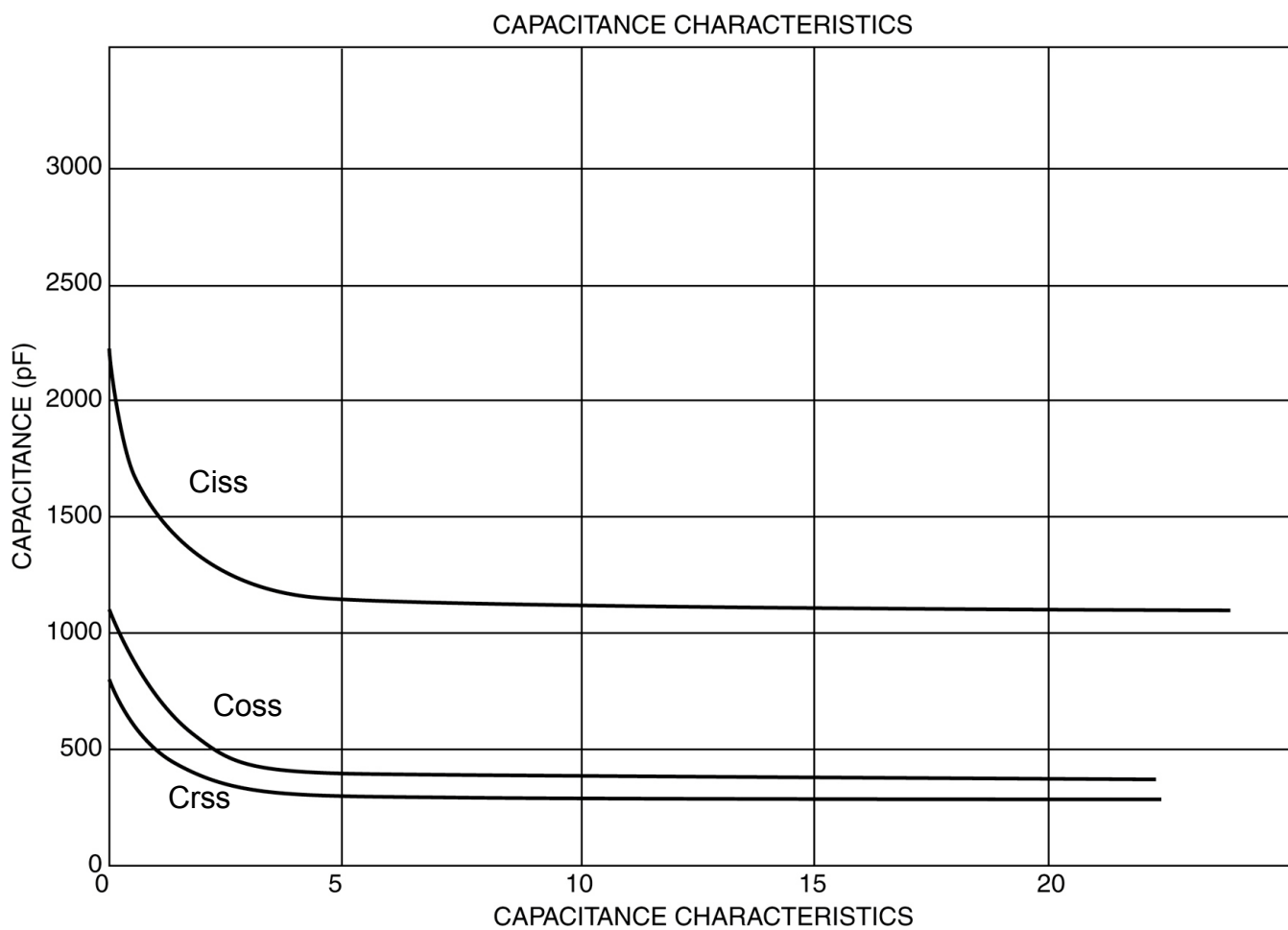
TS8314

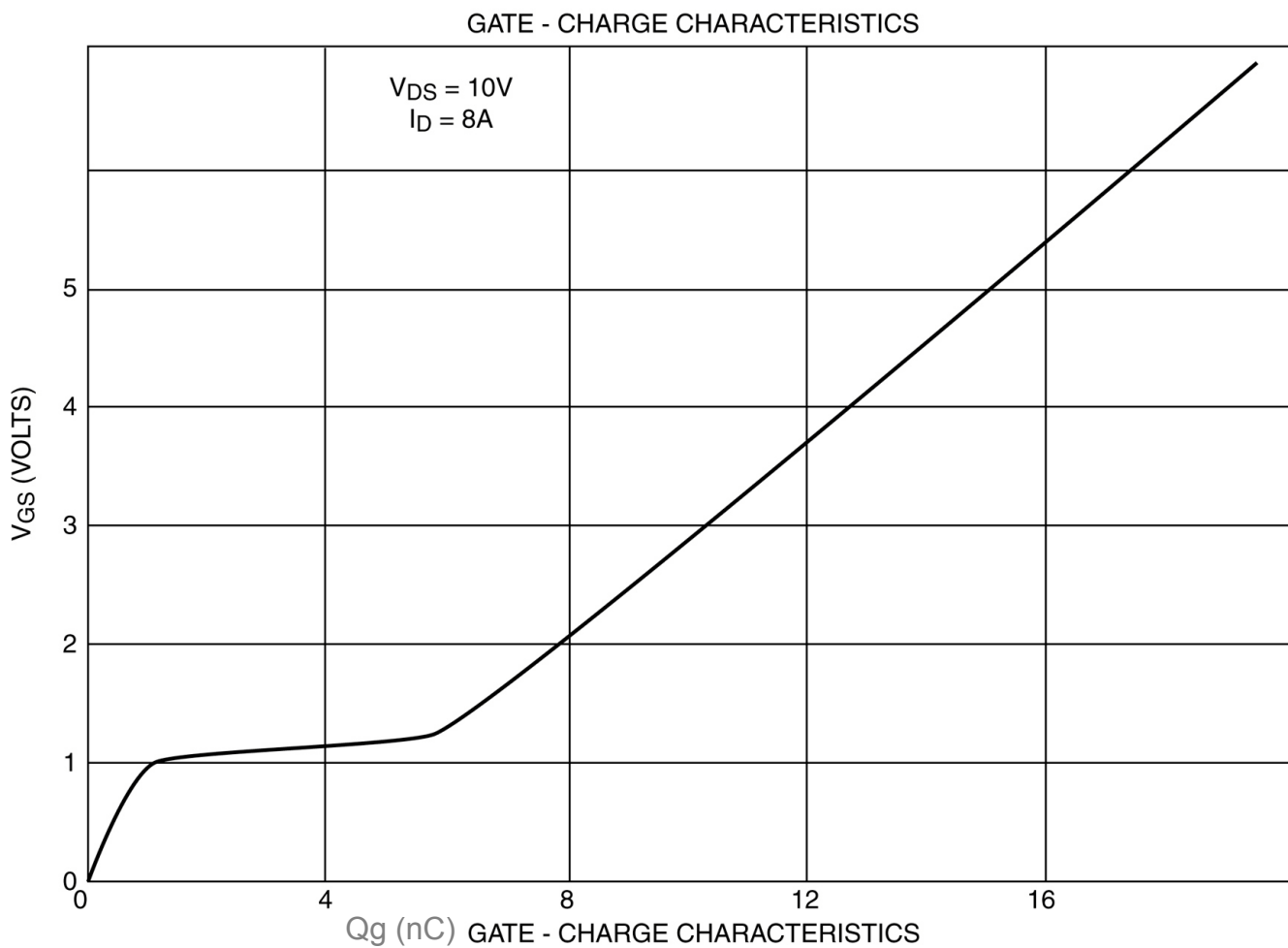


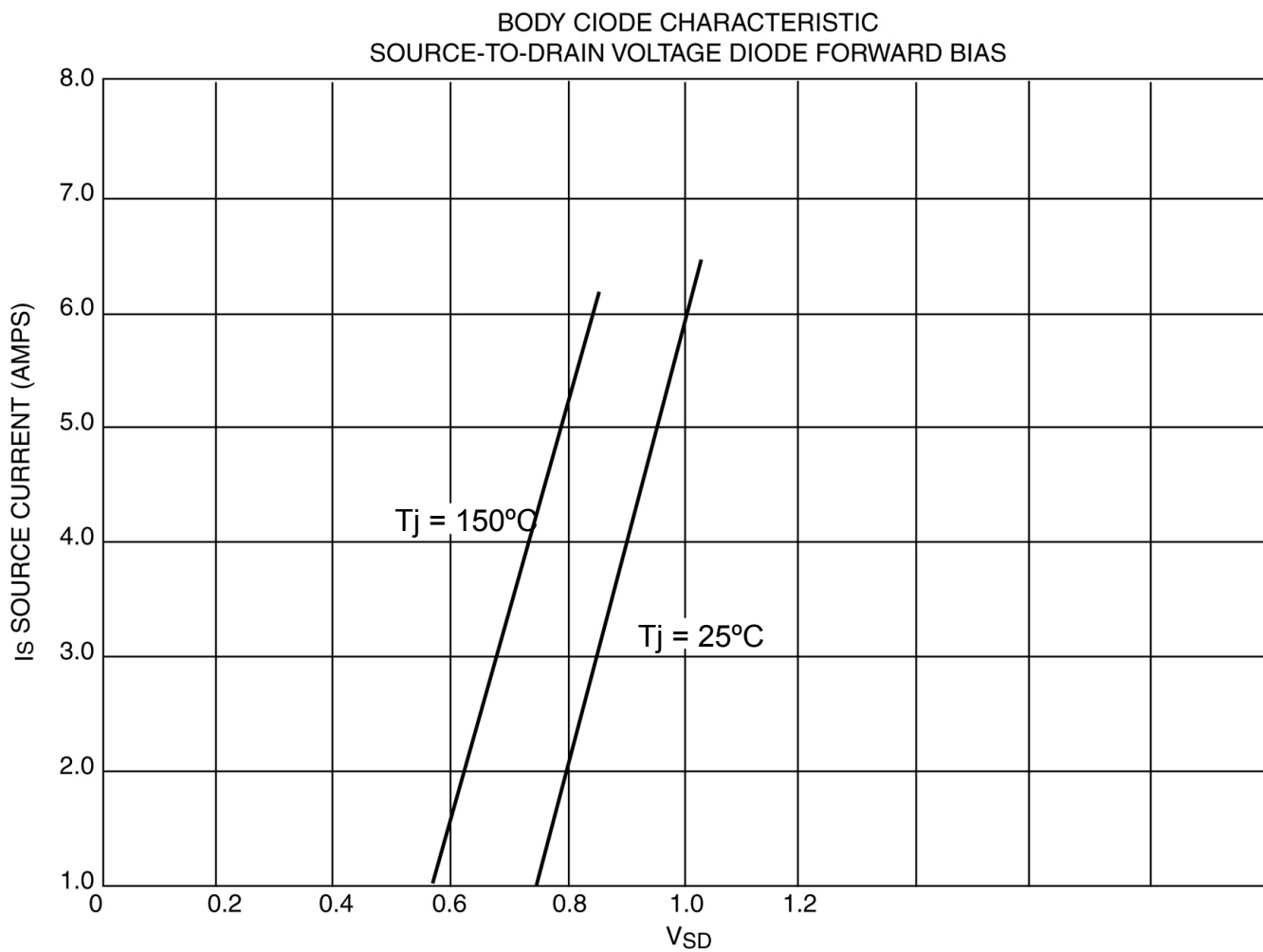








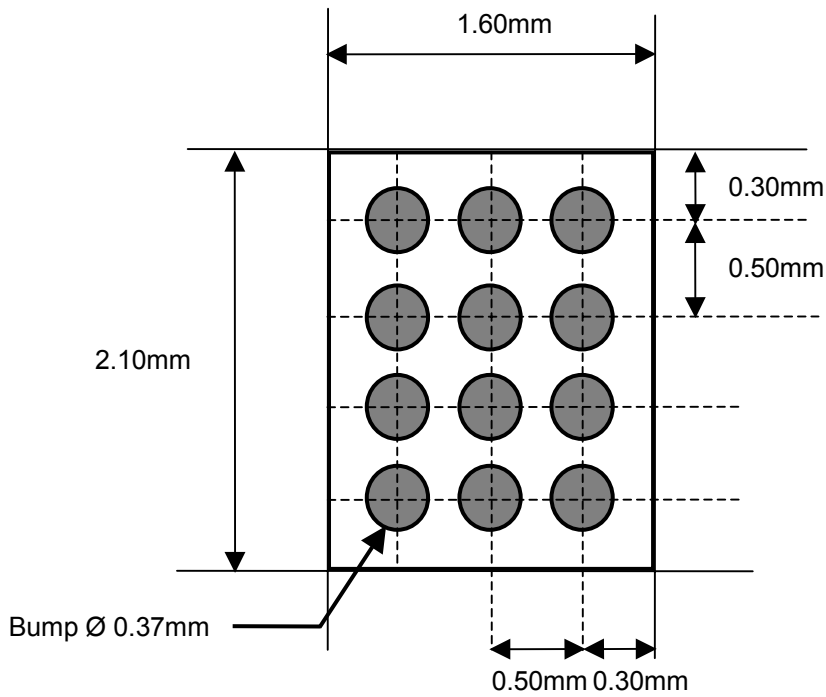
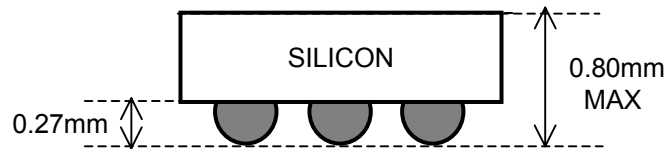






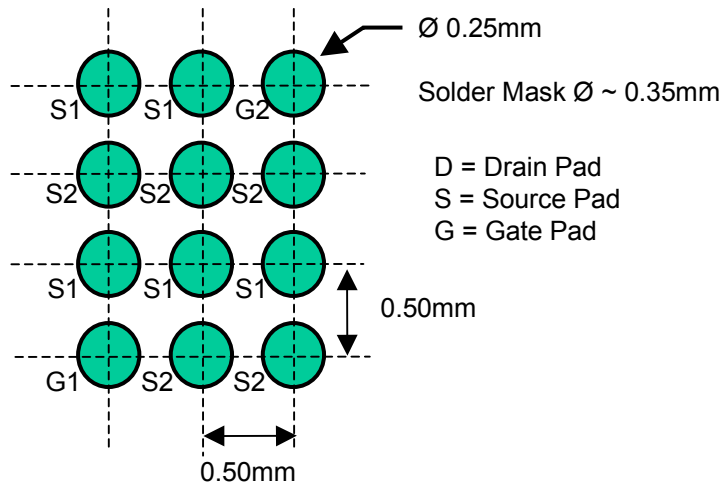
Dimensional Outline and Pad Layout

TS8314

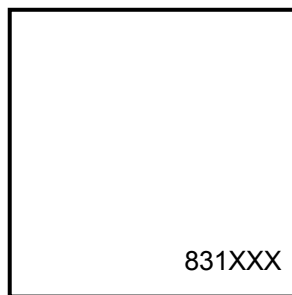


Bumps are Eutectic solder 63/37 Sn/Pb

Dimensional Outline and Pad Layout



LAND PATTERN RECOMMENDATION

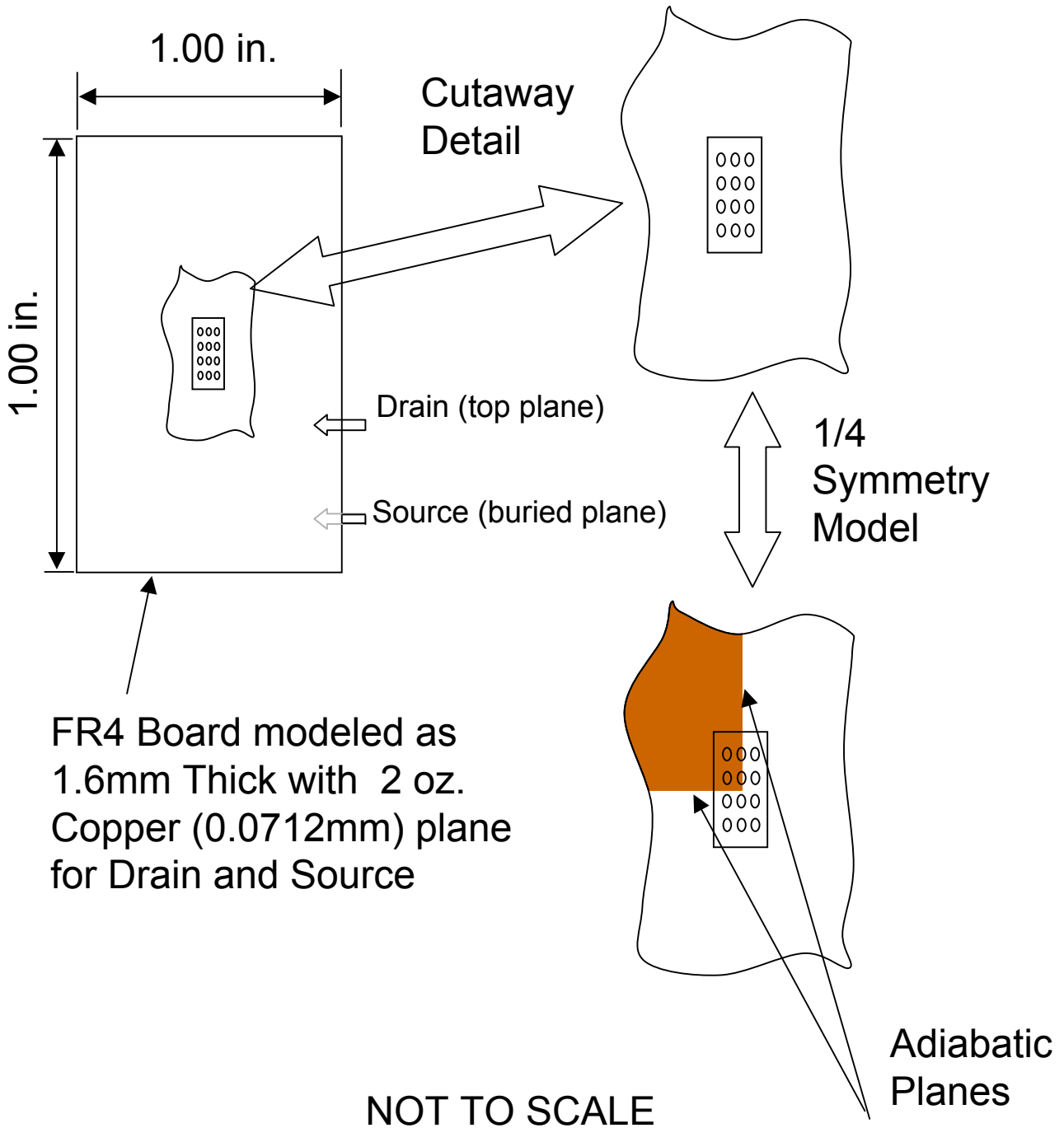


MARK ON BACKSIDE OF DIE

XXX = Date/Lot Traceability Code

TS8314 Thermal Resistance Analysis

TS8314 Die Top View -transparent view for clarity.



Finite Element Model:

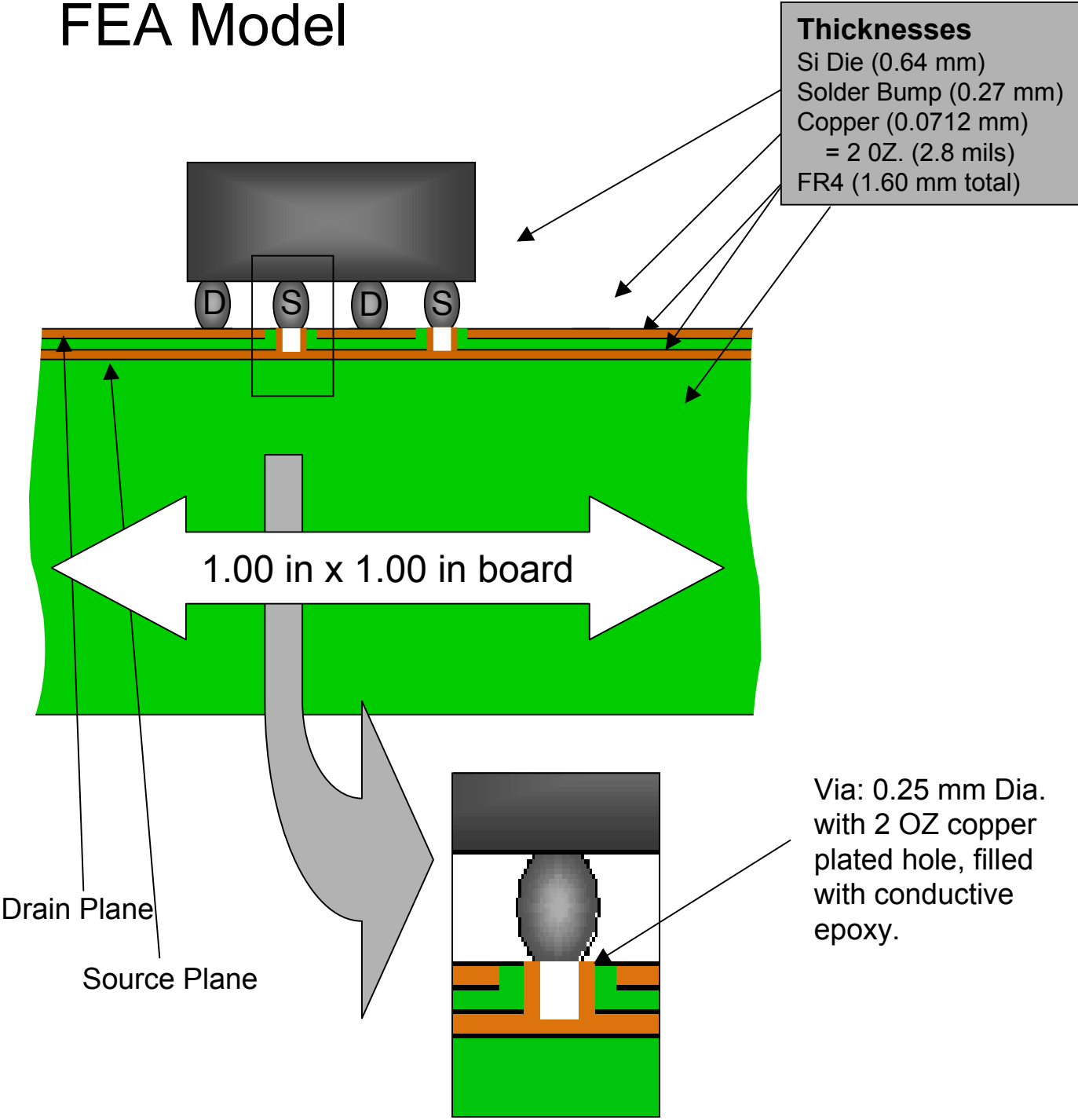
- Linear Thermal elements. Combination of tetrahedrals, 6 noded prisms and 8 noded bricks
- Heat Transfer conditions:
 - Bottom of FR4 board constrained to 25 degrees C
 - Power dissipation = 0.4 W per quarter model, in the form of a uniform heat flux at the die junction surface.
- Linear Thermal conduction analysis. *No convection or radiation* included in model.
- ~9800K elements.

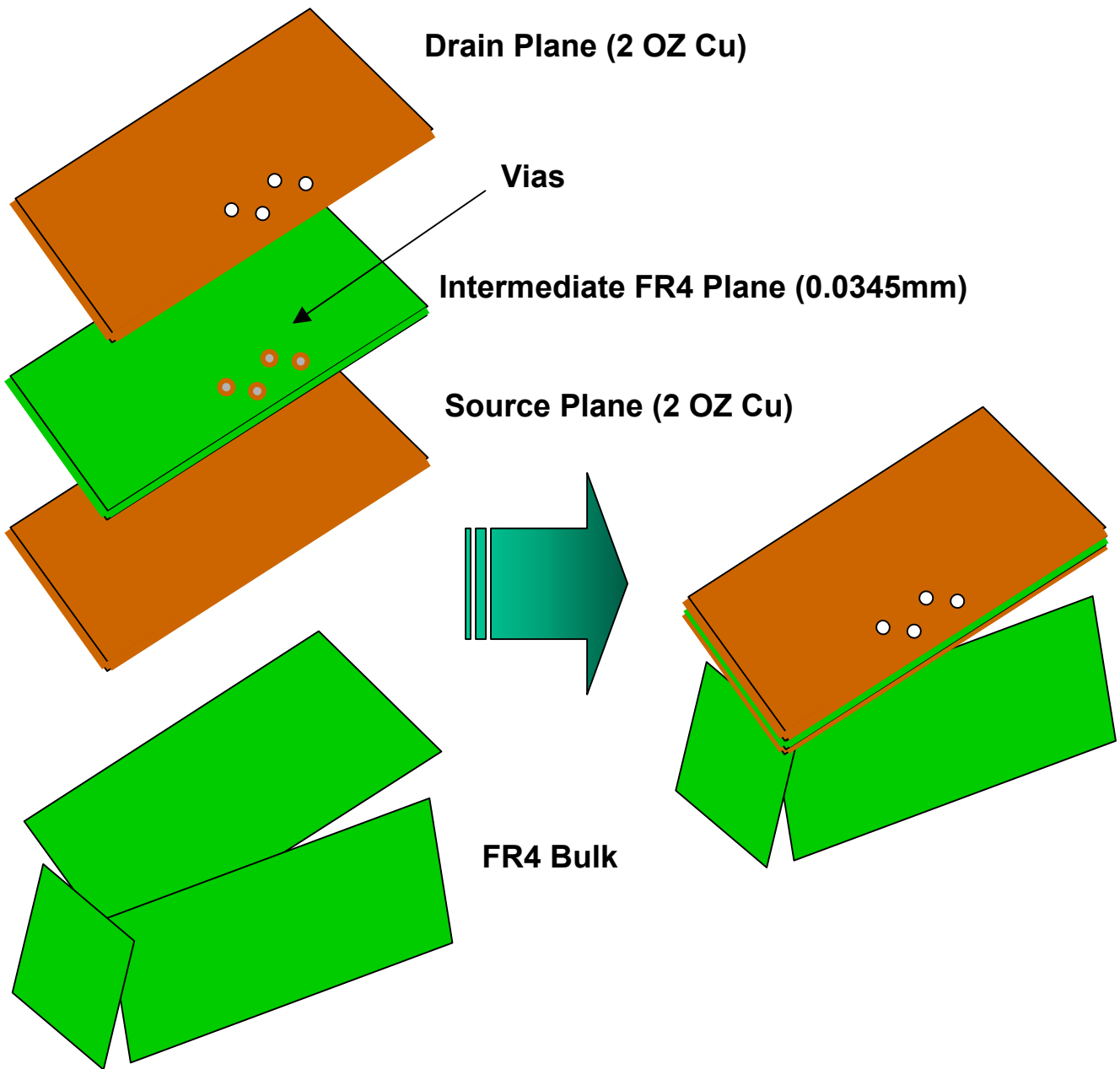
Material Properties Used for Analysis

Material	Thickness (mm)	K (W/m°C)
FR4	1.60000	2.5
Copper Layers (2 oz.)	0.07120	390
Solder (96.8Sn/2.6Ag/.6Cu)	0.27000	50
Silicon	0.64000	150
Via (Composite of Cu and Epoxy)	See model	210
NOTE: 1. Values obtained from http://www.boulder.nist.gov/div853/lead%20free/part2.htm		
2. Solder thermal conductivity is best conservative estimate based on composition		

Model: Taiwan Semiconductor TS8314 Part

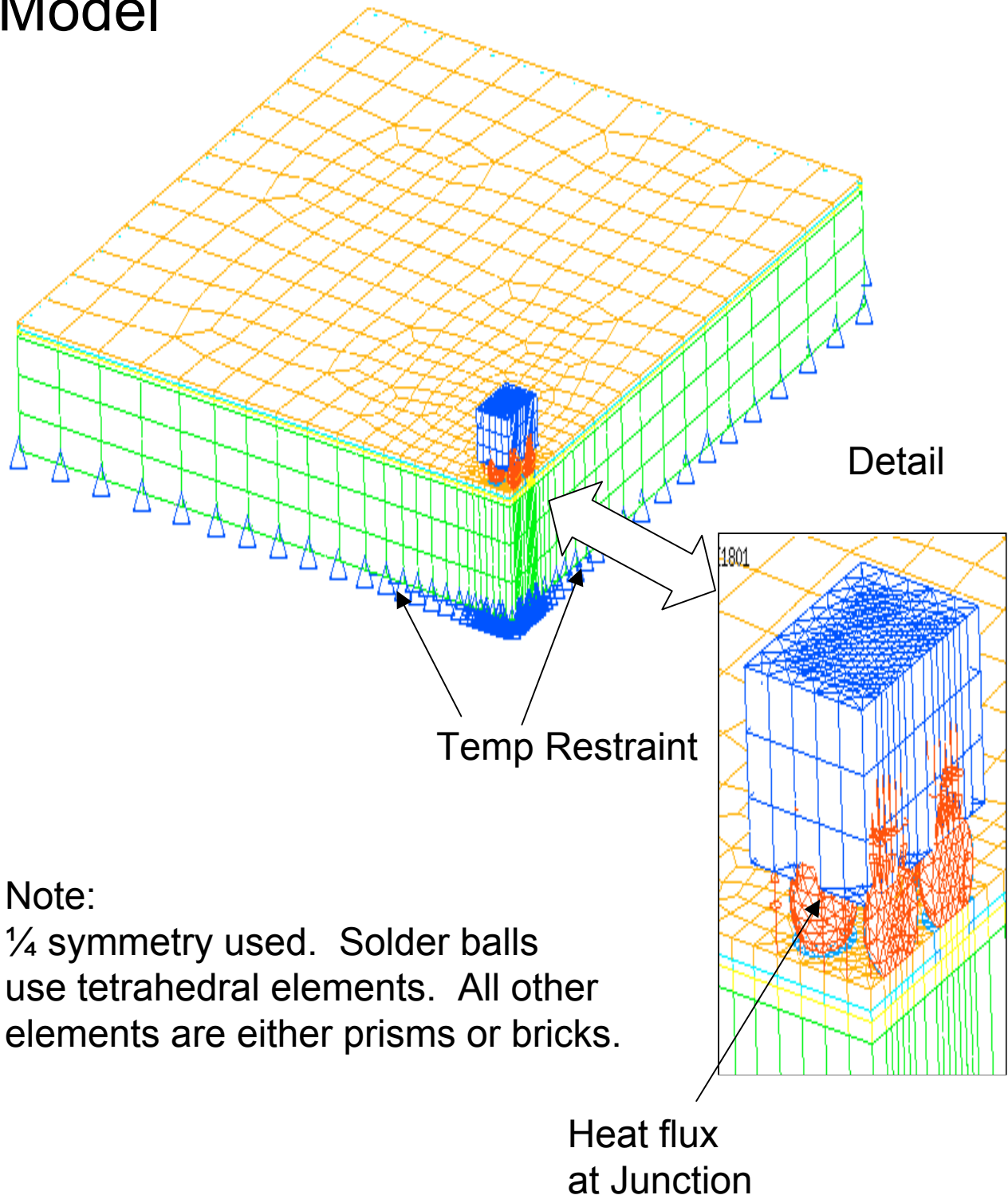
Cross Section of FEA Model





BREAKDOWN OF FR4 LAYERS USED
 IN THE FE MODEL. Total Thickness 1.6 mm)
 This illustration shows the $\frac{1}{2}$ symmetry model.
 The actual FE model uses $\frac{1}{4}$ symmetry for efficiency.

FEA Model

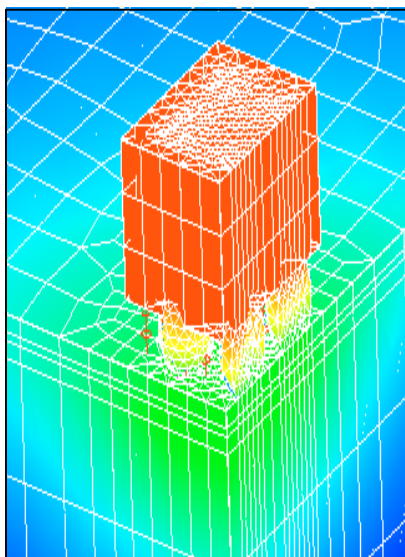
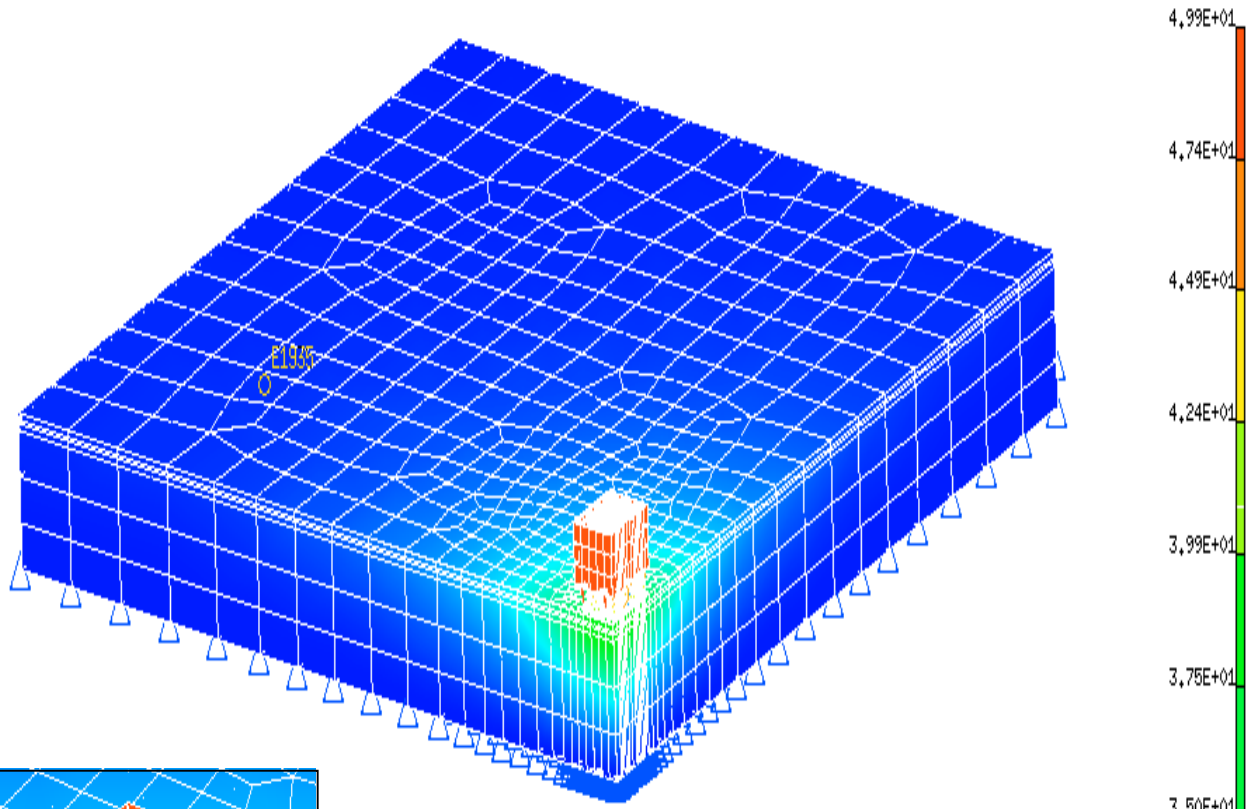


Note:
1/4 symmetry used. Solder balls use tetrahedral elements. All other elements are either prisms or bricks.

General Result:

RESULTS: 1- B,C, 1,TEMPERATURE_1,LOAD SET 1
TEMPERATURE - MAG MIN: 2,50E+01 MAX: 4,99E+01

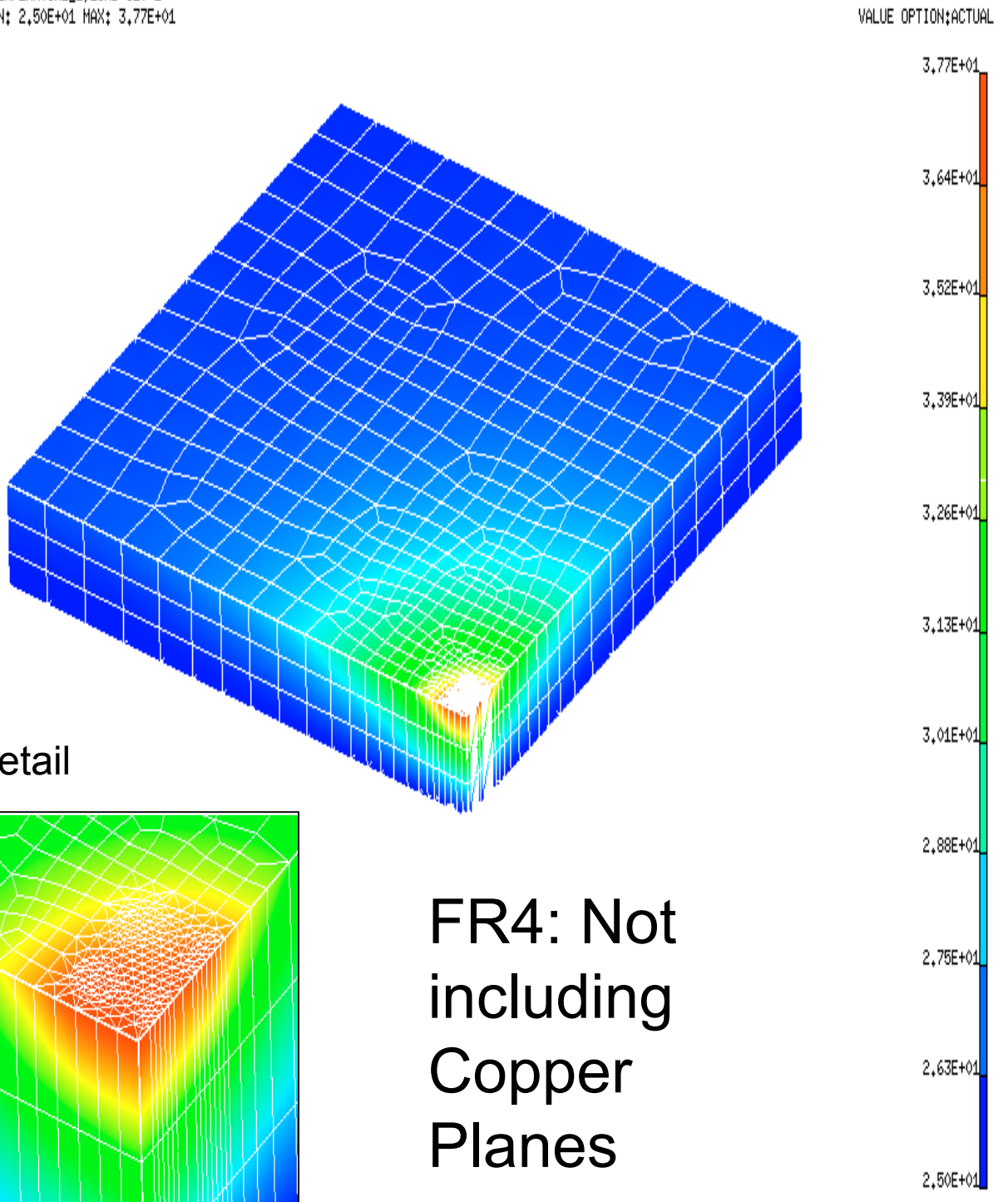
VALUE OPTION:ACTUAL



Detail

About 56% of the temp drop occurs in the FR4 layers, while 44% occurs in the solder ball.

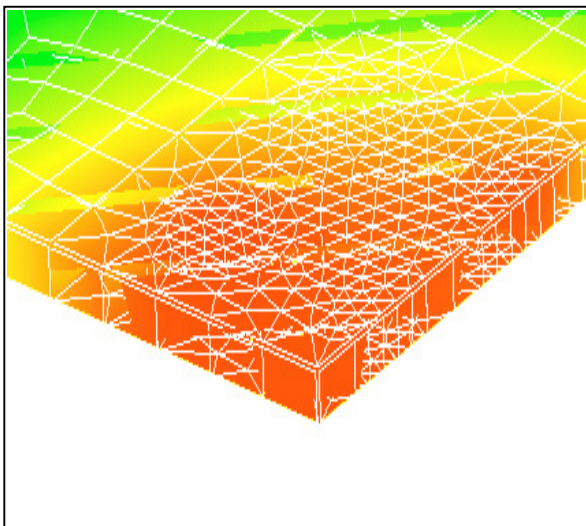
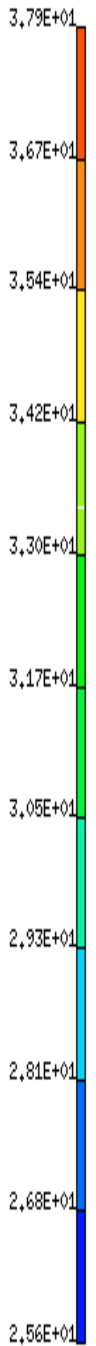
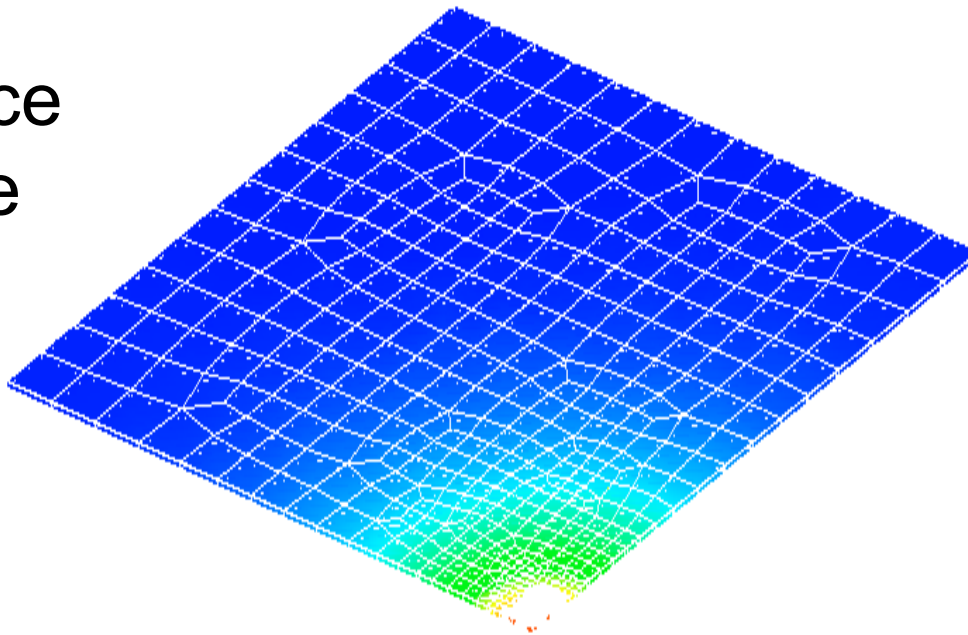
RESULTS: 1- B,C, 1,TEMPERATURE_1,LOAD SET 1
TEMPERATURE - MAG MIN: 2,50E+01 MAX: 3,77E+01



RESULTS: 1- B.C. 1,TEMPERATURE_1,LOAD SET 1
TEMPERATURE - MAG MIN: 2,56E+01 MAX: 3,79E+01

VALUE OPTION:ACTUAL

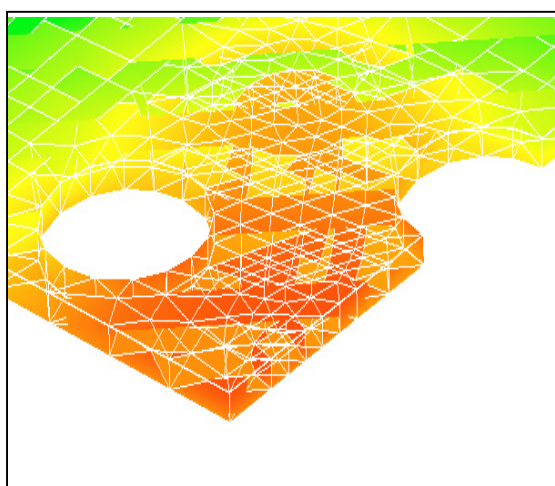
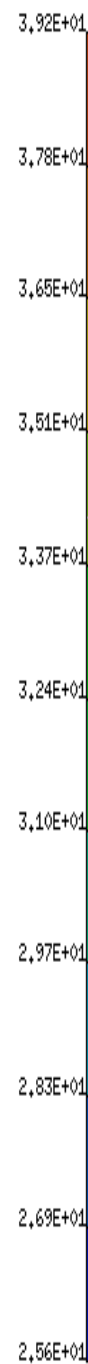
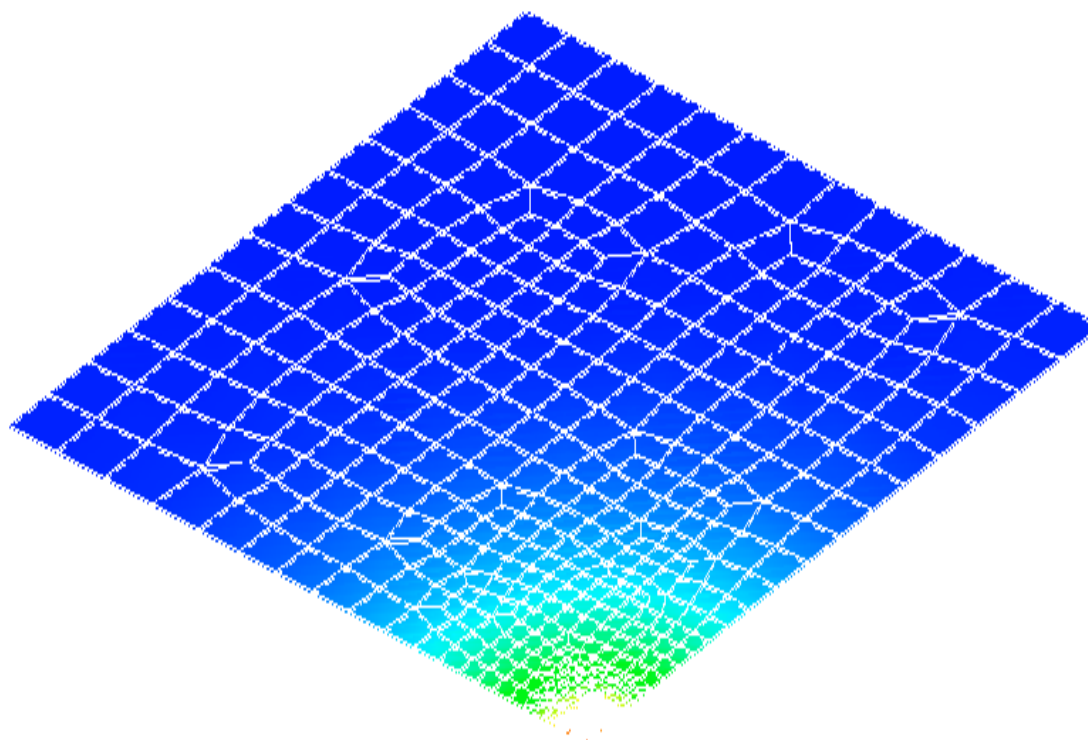
FR4: source plane



Detail

RESULTS: 1- B,C, 1,TEMPERATURE_1,LOAD SET 1
TEMPERATURE - MAG MIN; 2,56E+01 MAX; 3,92E+01

VALUE OPTION;ACTUAL

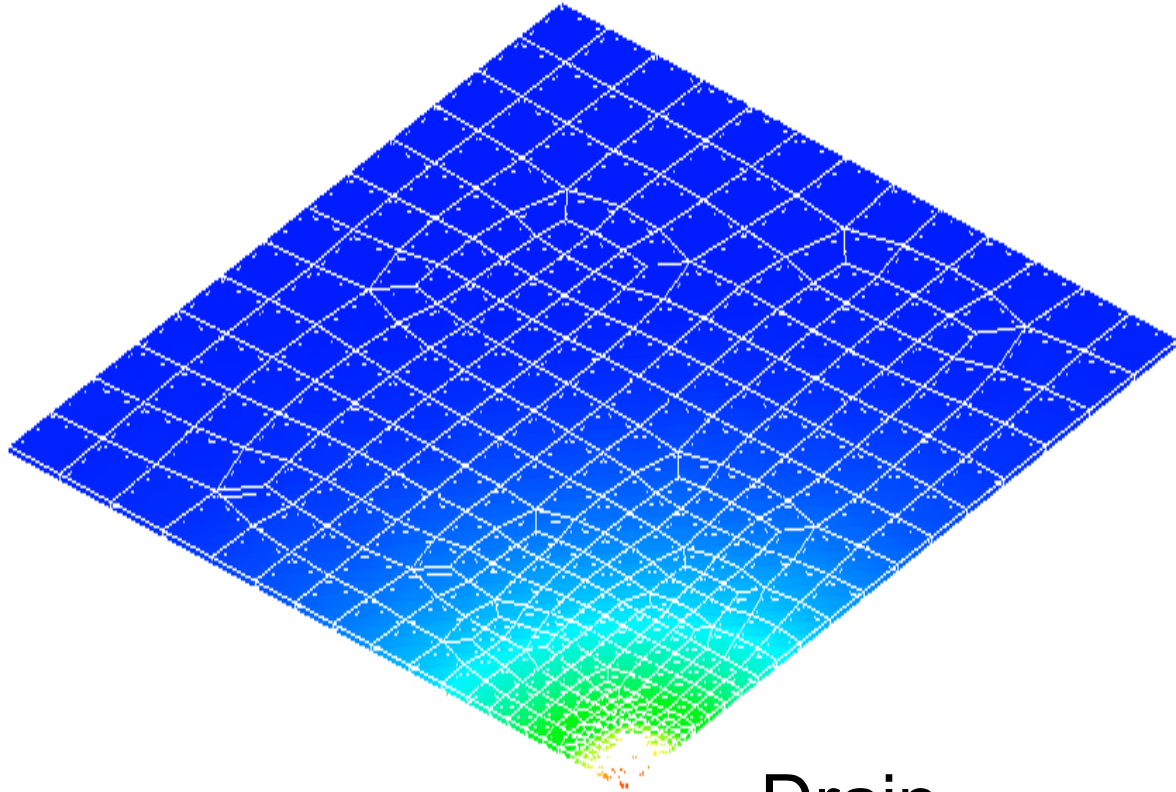


Intermediate
FR4 plane

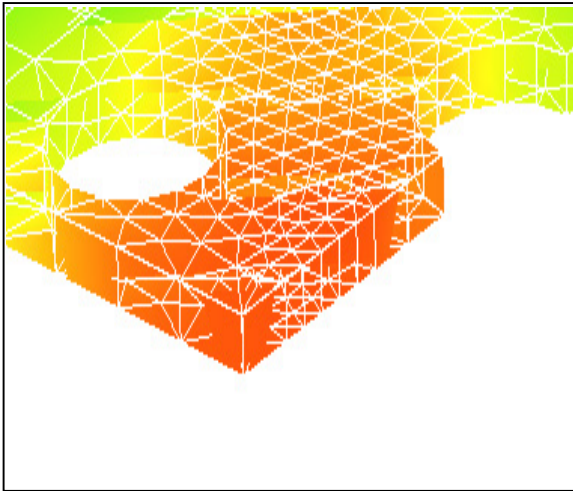
Detail

RESULTS: 1- B,C, 1,TEMPERATURE_1,LOAD SET 1
TEMPERATURE - MAG MIN: 2,56E+01 MAX: 3,93E+01

VALUE OPTION:ACTUAL



Drain
FR4
plane



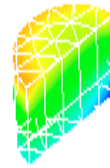
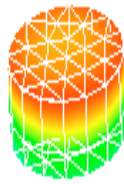
Detail

RESULTS: 1- B,C, 1,TEMPERATURE_1,LOAD SET 1
TEMPERATURE - MAG MIN: 3,66E+01 MAX: 3,94E+01

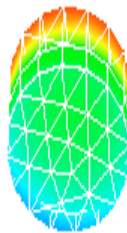
VALUE OPTION:ACTUAL

Vias from
solder balls to
source plane

Top Side



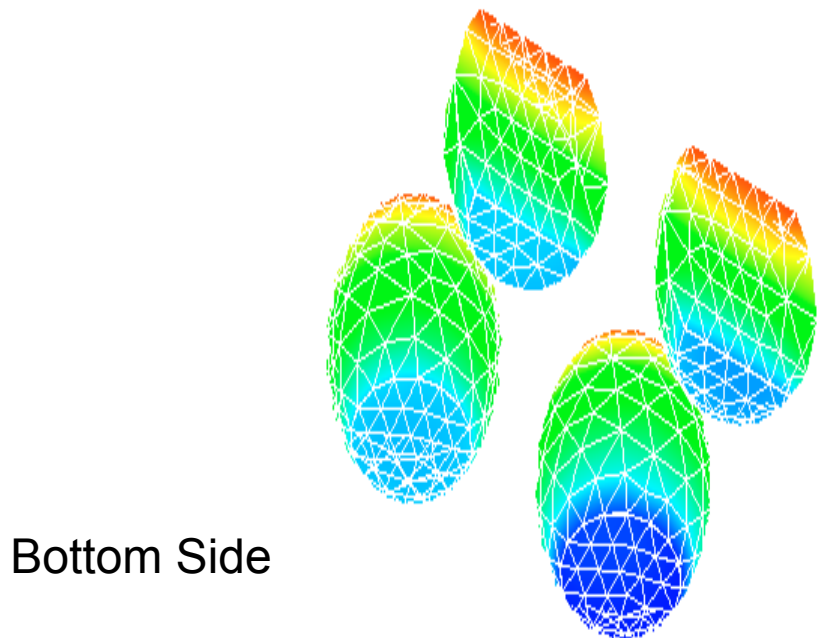
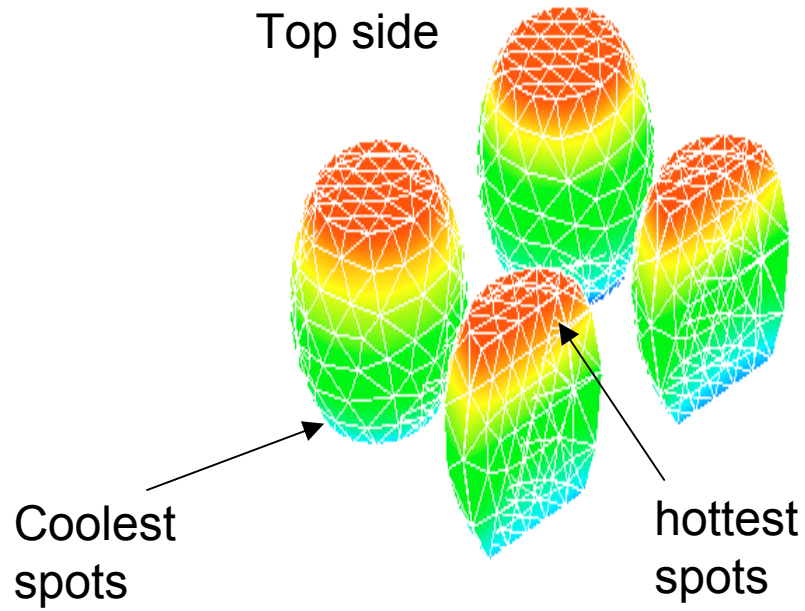
Bottom Side



RESULTS: 1- B.C. 1,TEMPERATURE_1,LOAD SET 1
TEMPERATURE - MAG MIN: 3,65E+01 MAX: 4,92E+01

VALUE OPTION:ACTUAL

Solder Balls:

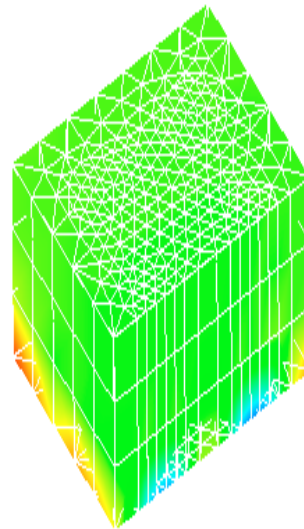


RESULTS: 1- B,C, 1,TEMPERATURE_1,LOAD SET 1
TEMPERATURE - MAG MIN: 4,87E+01 MAX: 5,00E+01

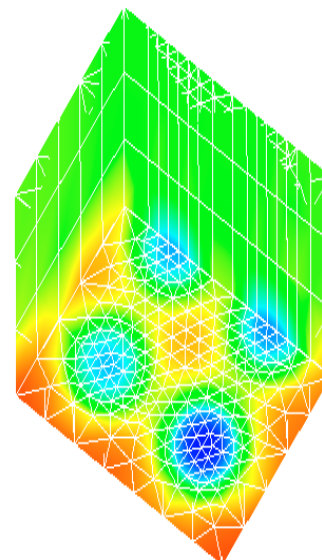
VALUE OPTION:ACTUA

Top Side

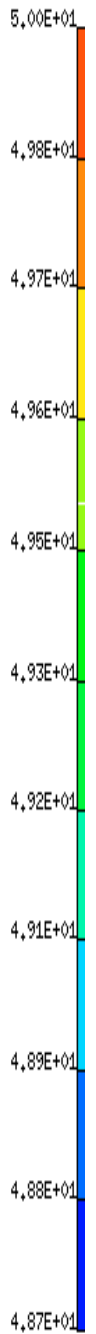
Silicon:



NOTE: The difference between min and max temperatures is only 1.3°C.



Bottom Side



Summary of Results

Thermal Resistance calculations:

$$\theta = \frac{\Delta T}{\text{Power}}$$

Layer *	ΔT (°C)	Resistance (°C/W)
Junction to bottom of Ball (Average)	10.5000	6.56250
Ball to bottom of Drain Plane	0.0037	0.00231
Drain Plane to bottom of Intermediate FR4	1.3800	0.86250
Intermediate FR4 to bottom of Source Plane	0.0120	0.00750
Source Plane to bottom of FR4	12.5500	7.84375
Total Junction to bottom of FR4	24.4457	15.27856

* temperatures are taken on the hottest spot in each layer and the node directly underneath it on the opposite side

