USB20H04

4-Port USB2.0 Hub Controller

Datasheet

Product Features

General Features

- Compliant with USB2.0 Specification
- Hub controller IC with four downstream ports
- Four transaction translators ensure maximum USB throughput
- Enables bus-powered Hi-Speed hub design
- Compatible with On-The-Go (OTG) USB devices
- Integrated Session Request Protocol (SRP) operates with dual-role OTG hosts
- Default configuration with pin selectable options
- Serial interface for configuration from EEPROM or microcontroller when default is not used
- Flexible OEM configuration options
- Available in a 64-pin TQFP package

Hardware Features

- Detects removal of self-power and automatically changes mode to bus-power
- Integrated termination and pull-up/pull-down resistors
- Internal short circuit protection of DP and DM lines
- On-chip oscillator uses low cost 24MHz crystal
- Supports individual or ganged over-current protection and power control
- LED drivers for each downstream port

OEM Selectable Features

- Configure as a bus-powered or self-powered Hi-Speed USB hub
- Configure port power switching and current sensing on an individual or ganged basis
- Enable LED indicator support
- Enable multiple transaction translators
- Enable compound device support on a port by port basis
- Enable downstream facing ports on a port by port basis

Pin Selectable Options for Default Configuration

- Select operation as either a Bus-Powered hub or a Self-Powered hub

ORDERING INFORMATION

Order Number(s):

USB20H04-JD for 64 pin, 10x10x1.4 TQFP package

USB20H04-JT for 64 pin, 10x10x1.4 TQFP package (green, lead-free)

80 Arkay Drive
Hauppauge, NY 11788
(631) 435-6000
FAX (631) 273-3123

USB20H04 Datasheet Revisions

PAGE(S)	SECTION/FIGURE/ENTRY	CORRECTION	REVISION LEVEL AND DATE
Cover	Ordering Information	Added lead-free part number	Revision 1.63 (10-14-04)
26	Table 8.4	Removed 0000 from the over-current timer value, which places it into the reserved category	Revision 1.62 (09-10-04)
15, 16, 18	Table 5.2, 6.1, 6.2, 6.4	Lower limit for the 1.8V regulator specification changed from 1.6 to 1.74V. (Note upper limit restored to previous value of 2.0V)	Revision 1.61 (07-28-04)
15	Table 5.2 – Recommended Operating Conditions	1.8V regulator specification changed to ±5%. (was ±10%)	Revision 1.6 (07-14-04)
13	Table 4.3 - USB I/O Signals	VBUSDET pin description updated	Revision 1.5 (04-01-04)
Cover	Title	Title changed from “Hi-Speed USB Hub Controller IC” to “4-Port USB2.0 Hub Controller”	Revision 1.4 (12-10-03)
24	Figure 8.2 - Internal Default Mode	Updated diagram.	Revision 1.3 11-13-03
20	7.5.2 - I^2C Memory Interface	Removed last sentence.	Revision 1.3 11-11-03
24	Figure 8.2 - Internal Default Mode	Updated figure.	Revision 1.3 11-11-03
27	Table 8.6 - Default Configuration Values	Updated table with note about PID changing with silicon revision.	Revision 1.3 11-11-03
36	Figure 10.1 - High Level Block Diagram of a Self-Powered Hub	Removed (128x8) from figure.	Revision 1.3 11-11-03
	Cover - Ordering Information	Changed from “USB20H04*L*-JD” to “USB20H04-JD”.	Revision 1.3 11-05-03
8	Chapter 1 General Description	Added paragraph 3.	Revision 1.3 10-31-03
9	1.3 Pin Selectable Options to the Default Configuration	Added new section.	Revision 1.3 10-31-03
10	Figure 2.1 - Block Diagram	Added default configuration to diagram.	Revision 1.3 10-31-03
19	7.4 Internal Configuration Select	Section is updated.	Revision 1.3 10-31-03
24	8.1.2 Internal Default Configuration	Section is updated.	Revision 1.3 10-31-03
27	Table 8.6 - Default Configuration Values	Table added.	Revision 1.3 10-31-03
23	Chapter 8 Implementation Notes	Modified first paragraph.	Revision 1.2 08-04-03
28	Table 8.7 - Time Values to Configure from SMBus	Values added to MAX column: T2 – 32 ns T4 – 70 ns	Revision 1.2 08-04-03

PAGE(S)	SECTION/FIGURE/ENTRY	CORRECTION	REVISION LEVEL AND DATE
29	Table 8.8 - Time Values to Configure From EEPROM	Value added to MAX column: T4 – 70 ns	Revision 1.2 08-04-03
28	Figure 8.3 - Timing for Configuration from SMBus	Updated figure	Revision 1.2 08-04-03
29	Figure 8.4 - Timing to Complete Configuration from EEPROM	Updated figure	Revision 1.2 08-04-03
16, 16, 18	Chapter 6 Electrical Characteristics	Updated the following tables: Table 6.1 - Electrical Characteristics: Supply Pins, Table 6.2 - DC Electrical Characteristics: Digital Pins, Table 6.4 - DC Electrical Characteristics: Analog I/O Pins (DP/DM) Removed Table 6.5 – Dynamic Characteristics: Analog I/O Pins (DP/DM)	Revision 1.2 07-31-03
27	8.4.1 External Hardware Reset	Updated section	Revision 1.2 07-31-03
28	Table 8.7 - Time Values to Configure from SMBus	Updated table	Revision 1.2 07-31-03
29	8.4.1.2 EEPROM Configuration Timing	Updated: Table 8.8 - Time Values to Configure From EEPROM	Revision 1.2 07-31-03
	Features	Changed reference to QFP package to TQFP package.	Revision 1.1 07/28/03
11	Figure 3.1– 64 Pin TQFP	Updated figure title	Revision 0.94 1/31/03
13	Table 4.3 - USB I/O Signals	See tracked changes	Revision 0.94 1/31/03
15	Table 5.1 - Absolute Maximum Ratings (In accordance with the Absolute Maximum Rating system (IEC 60134)	Replaced table	Revision 0.94 1/31/03
18	Table 6.4 - DC Electrical Characteristics: Analog I/O Pins (DP/DM)	Removed reference to Figure 6.1	Revision 0.94 1/31/03
18	Dynamic Characteristics: Analog I/O Pins (DP/DM)	Removed references to Figure 6.2	Revision 0.94 1/31/03
19	7.1 Bus-Power Detect	See tracked changes	Revision 0.94 1/31/03
20	7.5.1 SMBus Slave	See tracked changes	Revision 0.94 1/31/03
23	8.1 Configuration Implementations	See tracked changes	Revision 0.94 1/31/03
23	8.1.1 Interfacing a 2-wire Serial EEPROM	See tracked changes	Revision 0.94 1/31/03
24	Table 8.1 - Summary of OEM Value Programming	See tracked changes	Revision 0.94 1/31/03

PAGE(S)	SECTION/FIGURE/ENTRY	CORRECTION	REVISION LEVEL AND DATE
25	Table 8.3 - Address 7; Config_Byte_2	See tracked changes	Revision 0.94 1/31/03
-	Figure 8.3 – RESET_N Timing for EEPROM Mode	This figure has been removed	Revision 0.94 1/31/03
-	Table 8.6 – RESET_N Timing for EEPROM Mode	This table has been removed	Revision 0.94 1/31/03
28	Figure 8.3 - Timing for Configuration from SMBus	Added figure	Revision 0.94 1/31/03
28	Table 8.7 - Time Values to Configure from SMBus	Added table	Revision 0.94 1/31/03
36	Figure 10.1 - High Level Block Diagram of a Self-Powered Hub	Updated figure	Revision 0.94 1/31/03

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Chapter 1 General Description

The USB20H04 four-port hub controller is fully compliant with the USB2.0 Specification and does not require firmware development. When connected to a high-speed host, the four downstream facing ports can operate at low-speed (1.5Mb/s), full-speed (12Mb/s), or high-speed (480Mb/s). As required by the USB2.0 Specification, the USB20H04 is fully backward compatible with legacy full-speed hosts. A dedicated Transaction Translator (TT) is available for each downstream facing port. This architecture ensures maximum USB throughput for each connected device when operating with mixed-speed peripherals.

The USB20H04 supports both bus-powered and self-powered configurations. For self-powered operation, an external supply is used to power the downstream facing ports. In bus-powered mode, all power is derived from the upstream facing port and no external power supply is required. An external USB power distribution switch device is used to control V_{BUS} switching to downstream ports, and to limit current and sense over-current conditions.

A default configuration is available in the USB20H04 following a reset. This configuration may be sufficient for some applications when it is desired to save the expense of an EEPROM. The controller may also be configured from a microcontroller or an external EEPROM. When using the microcontroller interface, the USB20H04 appears as an SMBus slave device. The EEPROM interface supports a 2-wire I^2C device.

All required resistors on the USB ports are integrated into the USB20H04. This includes all series termination resistors on D+ and D– pins and all required pull-down and pull-up resistors on D+ and D– pins. The over-current sense inputs for the downstream facing ports have internal pull-up resistors.

Throughout this document the upstream facing port of the hub will be referred to as the upstream port, and the four downstream facing ports will be called the downstream ports.

1.1 Applications

The Universal Serial Bus (USB) hub may be used in a number of applications:

- Standalone hubs
- Keyboards
- Monitors
- Motherboard hubs
- Docking stations and port replicators
- Printers and scanners
- External storage devices
- Auxiliary battery docks

1.2 OEM Selectable Features

The 4-Port Hub supports several OEM selectable features:

- Operation as a bus-powered, self-powered or dynamic-powered hub. (When configured for dynamic operation, the controller automatically switches to bus-powered mode if a local power source is unavailable).
- Configure downstream facing port power switching on an individual or ganged basis.
- Configure downstream facing port over-current sensing on an individual or ganged basis.
- Enable downstream facing port LED indicators.
- Select multiple or single transaction translator mode.
- Select whether the hub is part of a compound device (when any downstream facing port is permanently hardwired to a USB peripheral device, the hub is part of a compound device).
- Select the presence of a permanently hardwired USB peripheral device on a port by port basis.
- Enable downstream facing ports a port by port basis.
- Enable EOP generation of EOF1 when operating in full-speed mode, as described in Section 11.3.1 of the USB2.0 Specification.
- Enable USB On-The-Go Session Request Protocol (SRP) support.
- Configure the delay time for filtering the over-current sense inputs.
- Configure the delay time until port power is good after the SetPortPower command is received.
- Indicate the maximum current that the 4-port hub consumes from an upstream port.
- Indicate the maximum current required for the hub controller.

1.3 Pin Selectable Options to the Default Configuration

The USB20H04 includes a default configuration for those applications where an external EEPROM or SMBus device is not available to provide the configuration. This configuration may be adequate in some applications. A pin selectable feature supports configuration as either a bus-powered hub or a self-powered hub determined by the logic level of the SELF_PWR pin following reset.

Chapter 2 Functional Block Diagram

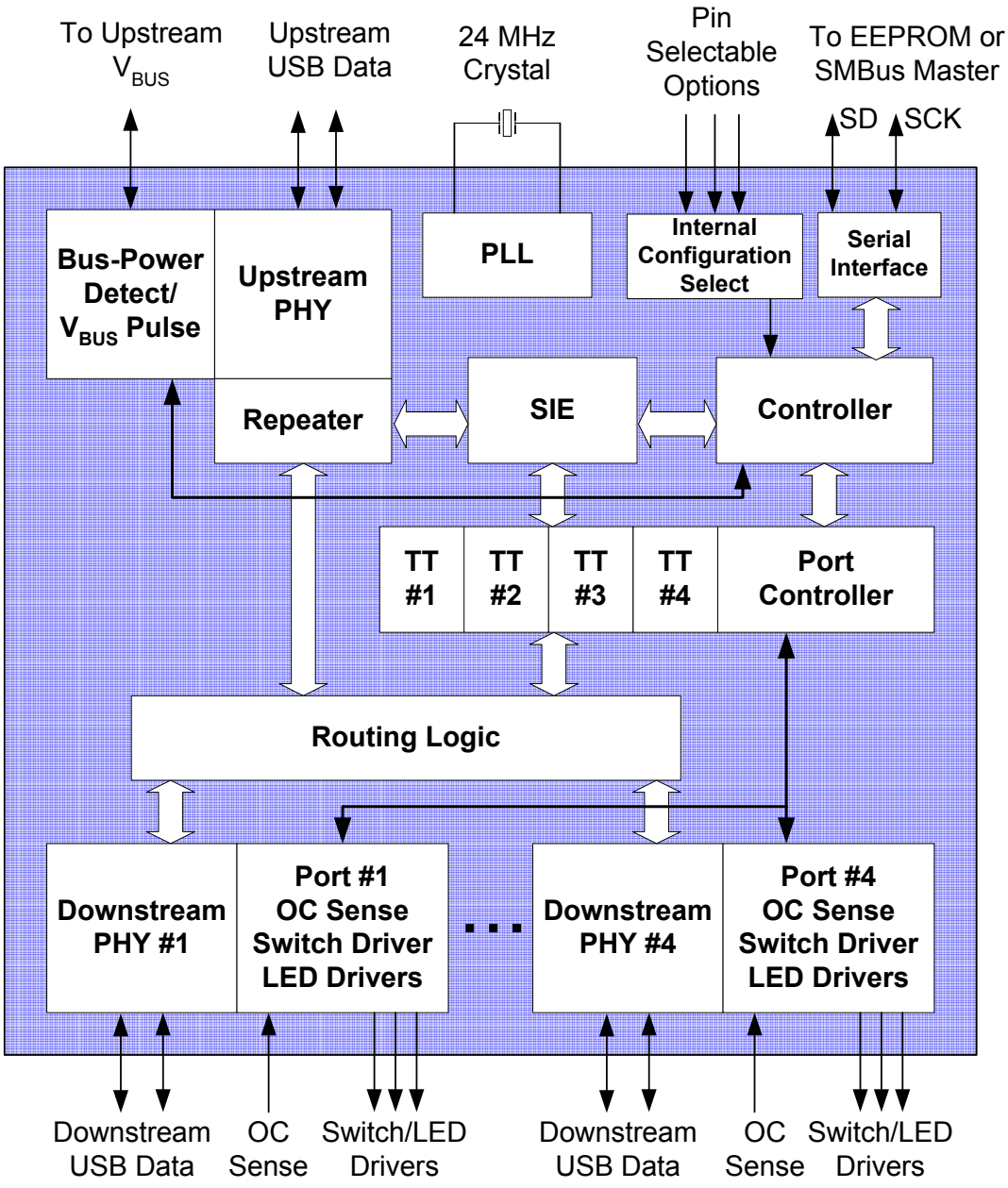

Figure 2.1 - Block Diagram

Chapter 3 Pinout

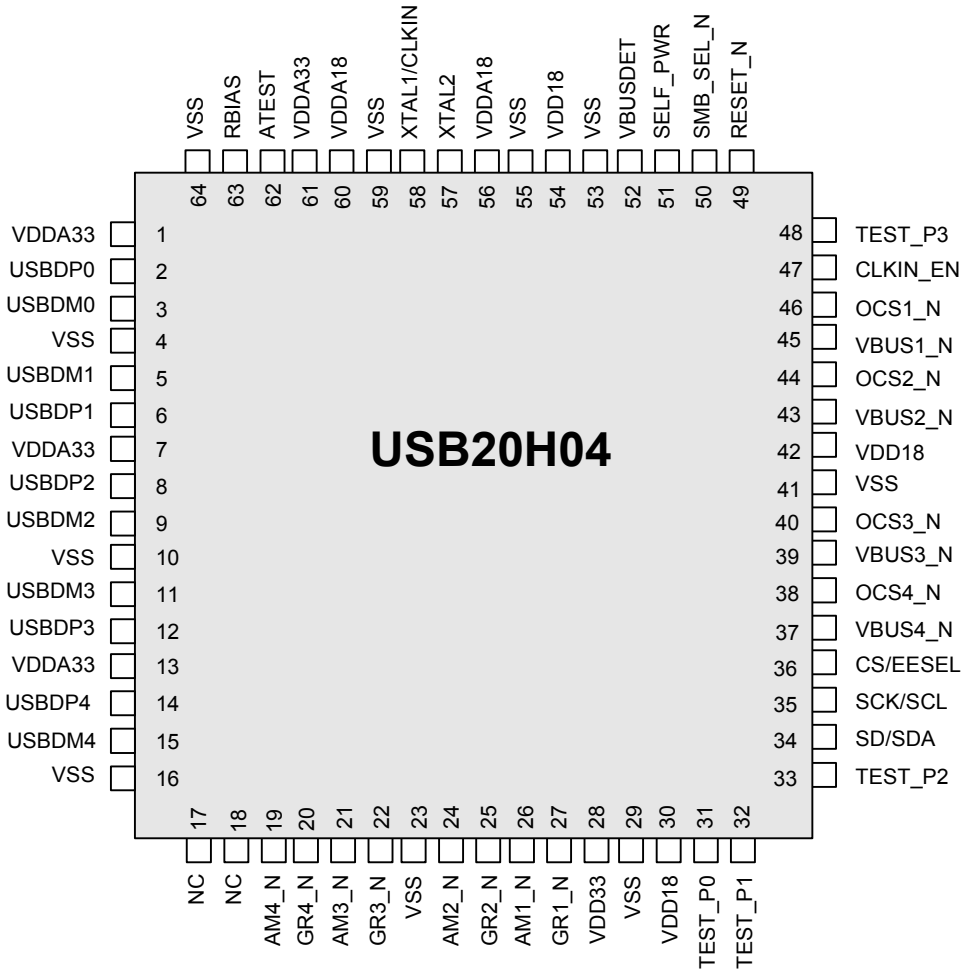

Figure 3.1– 64 Pin TQFP

Chapter 4 Interface Signal Definition

4.1 Pin Descriptions

Table 4.1 - System Interface Signals

NAME	BUFFER TYPE	ACTIVE LEVEL	DESCRIPTION
RESET_N	IS	Low	**Chip Reset**. The minimum active low pulse is 100ns. See section 8.4 for a complete description of operation following a reset.
SELF_PWR	I	High	**Self-power Detect**. Detects availability of local self-power source: 0: Self/local power source is NOT available (i.e., 4- Port Hub gets all power from Upstream USB V_{BUS}). 1: Self/local power source is available.
TEST_P0	IPD	N/A	**Test Pin.** Do Not Connect
TEST_P1	IPD	N/A	**Test Pin.** Do Not Connect
TEST_P2	IPD	N/A	**Test Pin.** Do Not Connect
TEST_P3	IPD	N/A	**Test Pin.** Do Not Connect
ATEST	AO	N/A	**Test Pin.** Do Not Connect

Table 4.2 – Configuration Select and Serial Port Interface

NAME	BUFFER TYPE	ACTIVE LEVEL	DESCRIPTION		
SMB_SEL_N	I	N/A	**SMBus Select**. Selects between configuration via the SMBus interface, or from an external EEPROM or using the internal default, as described in the table below.		
			SMB_SEL_N	CS/EE_SEL	SMBus or EEPROM interface configuration.
			0	0	SMBus slave. Address: 0101100
			0	1	SMBus slave. Address: 0101101
			1	0	Internal default configuration.
			1	1	2-wire EEPROM interface.
CS/EE_SEL	IO8	N/A	**Chip Select**. This multifunction pin is sampled on the rising edge of RESET_N. If SMB_SEL_N = 1, the internal default configuration will be used when this pin is low, or the external I2C EEPROM will supply the configuration when this pin is high. When SMB_SEL_N = 0, this pin selects the SMBus slave address, as described in the table above. Connect a 1k ohm resistor in series with the input when connecting this pin to either VDD or VSS.		
SD/SDA	IOSD12	N/A	**Serial Data**. Data I/O on the 2-Wire interface.		
SCK/SCL	IOSD12	N/A	**Serial Clock**. Clock for the 2-Wire interface.		

Table 4.3 - USB I/O Signals

NAME	BUFFER TYPE	ACTIVE LEVEL	DESCRIPTION
USBDP0	IO-U	N/A	Upstream USB Positive Data Pin.
USBDM0	IO-U	N/A	Upstream USB Negative Data Pin.
VBUSDET	IO8	N/A	Detects state of upstream V_{BUS} power. When designing a detachable hub, this pin must be connected to the V_{BUS} power pin of the USB port that is upstream of the hub. For self-powered applications with a permanently attached upstream host, this pin must be connected to either 3.3V or 5.0V (typically VDD3.3). The USB20H04 monitors VBUSDET to determine when to assert the internal D+ pull-up resistor (signaling a connect event). When using the SRP feature, it is necessary to add a 100k ohm resistor from this pin to VSS in order to properly dissipate the upstream V_{BUS} Pulse (pulsed with an 8mA drive capability).
USBDP1	IO-U	N/A	USB Positive Data Pin to downstream port 1.
USBDM1	IO-U	N/A	USB Negative Data Pin to downstream port 1.
VBUS1_N	O8	Low	Enables power to downstream port 1.
OCS1_N	IPU	Low	Over-Current Sense input. Internal pull-up resistor to 3.3V.
GR1_N	OD8	Low	Enables green indicator to downstream port 1.
AM1_N	OD8	Low	Enables amber indicator to downstream port 1.
USBDP2	IO-U	N/A	USB Positive Data Pin to downstream port 2.
USBDM2	IO-U	N/A	USB Negative Data Pin to downstream port 2.
VBUS2_N	O8	Low	Enables power to downstream port 2.
OCS2_N	IPU	Low	Over-Current Sense input. Internal pull-up resistor to 3.3V.
GR2_N	OD8	Low	Enables green indicator to downstream port 2.
AM2_N	OD8	Low	Enables amber indicator to downstream port 2.
USBDP3	IO-U	N/A	USB Positive Data Pin to downstream port 3.
USBDM3	IO-U	N/A	USB Negative Data Pin to downstream port 3.
VBUS3_N	O8	Low	Enables power to downstream port 3.
OCS3_N	IPU	Low	Over-Current Sense input. Internal pull-up resistor to 3.3V.
GR3_N	OD8	Low	Enables green indicator to downstream port 3.
AM3_N	OD8	Low	Enables amber indicator to downstream port 3.
USBDP4	IO-U	N/A	USB Positive Data Pin to downstream port 4.
USBDM4	IO-U	N/A	USB Negative Data Pin to downstream port 4.
VBUS4_N	O8	Low	Enables power to downstream port 4.
OCS4_N	IPU	Low	Over-Current Sense input. Internal pull-up resistor to 3.3V.
GR4_N	OD8	Low	Enables green indicator to downstream port 4.
AM4_N	OD8	Low	Enables amber indicator to downstream port 4.

Table 4.4 - Biasing and Clock Oscillator Signals

NAME	BUFFER TYPE	ACTIVE LEVEL	DESCRIPTION
RBIAS	I-R	N/A	**External 1% bias resistor.** Requires a 12KΩ resistor to ground. Used for setting HS transmit current level and on-chip termination impedance.
XTAL1/CLKIN	ICLKx	N/A	**External crystal.** 24MHz crystal or external clock input when a crystal is not used. Connect a 5M ohm resistor from this pin to XTAL2 when a crystal is used.
XTAL2	OCLKx	N/A	**External crystal.** 24MHz crystal. Not connected when using an external clock.
CLKIN_EN	I	High	**Clock Input Enable.** When high, an external CMOS clock drives XTAL1.

Table 4.5 - Power and Ground Signals

NAME	BUFFER TYPE	ACTIVE LEVEL	DESCRIPTION
VDD3.3	N/A	N/A	**3.3V Digital Supply**. Powers digital pads.
VDD1.8	N/A	N/A	**1.8V Digital Supply**. Powers digital core.
VSS	N/A	N/A	**Signal Ground**.
VDDA3.3	N/A	N/A	**3.3V Analog Supply**. Powers analog I/O and 3.3V analog circuitry.
VDDA1.8	N/A	N/A	**1.8V Analog Supply.** Powers 1.8V analog circuitry.

4.2 Buffer Type Descriptions

Table 4.6 – USB20H04 Buffer Type Descriptions

BUFFER	DESCRIPTION
I	Input
IPU	Input with weak internal pull-up resistor.
IPD	Input with weak internal pull-down resistor
IS	Input with Schmitt trigger
IO8	Input/Output with 8mA drive
IOSD12	Open drain with 12mA sink with Schmitt trigger. Meets I2C-Bus Spec Version 2.1
O8	Output with 8mA drive
OD8	Open drain with 8mA sink
ICLKx	XTAL clock input
OCLKx	XTAL clock output
IO-U	Defined in USB specification
AO	Analog Output
I-R	3.3V Tolerant Analog Pin

Chapter 5 Limiting Values

Table 5.1 - Absolute Maximum Ratings (In accordance with the Absolute Maximum Rating system (IEC 60134)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
1.8V Supply Voltage (VDD1.8 and VDDA1.8)	VDD1.8		-0.5		2.5	V
3.3V Supply Voltage (VDD3.3 and VDDA3.3)	VDD3.3		-0.5		4.0	V
Voltage on any I/O pin			-0.3		5.5	V
Voltage on XTAL1/CLKIN and XTAL2			-0.3		3.6	V
Storage Temperature	TSTG		-40		+125	oC

Table 5.2 - Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
1.8V Supply Voltage (VDD1.8 and VDDA1.8)	$V_{DD1.8}$		1.74	1.8	2.0	V
3.3V Supply Voltage (VDD3.3 and VDDA3.3)	$V_{DD3.3}$		3.0	3.3	3.6	V
Input Voltage on Digital Pins	V_I		0.0		$V_{DD3.3}$	V
Input Voltage on Analog I/O Pins (DP, DM)	$V_{I(I/O)}$		0.0		$V_{DD3.3}$	V
Ambient Temperature	T_A		0		+70	^oC

Table 5.3 - Recommended Crystal/External Clock Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Crystal Frequency				24 (+/- 100ppm)		MHz
External Clock Frequency		XTAL1/CLKIN driven by the external clock; no connection at XTAL2; and CLKIN_EN is high		24 (+/- 100ppm)		MHz
External Clock Duty Cycle			45	50	55	%
External Clock RMS Jitter					100	ps

Chapter 6 Electrical Characteristics

Table 6.1 - Electrical Characteristics: Supply Pins

($V_{DD1.8}$ =1.74 to 2.0V; $V_{DD3.3}$ =3.0 to 3.6V; V_{SS} = 0V; T_A = 0 °C to +70°C; unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Suspend State	$I_{CC1.8SUS}$	Suspended		100		uA
	$I_{CC3.3SUS}$	Suspended		200		uA
1 Port Low-Speed/Full-Speed	$I_{CC1.8FS1}$	1 downstream port active		100		mA
	$I_{CC3.3FS1}$			55		mA
1 Port High-Speed	$I_{CC1.8HS1}$	1 downstream port active		100		mA
	$I_{CC3.3HS1}$			75		mA
2 Ports Low-Speed/Full-Speed	$I_{CC1.8FS2}$	2 downstream ports active		100		mA
	$I_{CC3.3FS2}$			55		mA
2 Ports High-Speed	$I_{CC1.8HS2}$	2 downstream ports active		100		mA
	$I_{CC3.3HS2}$			95		mA
3 Ports Low-Speed/Full-Speed	$I_{CC1.8FS3}$	3 downstream ports active		100		mA
	$I_{CC3.3FS3}$			55		mA
3 Ports High-Speed	$I_{CC1.8HS3}$	3 downstream ports active		105		mA
	$I_{CC3.3HS3}$			115		mA
4 Ports Low-Speed/Full-Speed	$I_{CC1.8FS4}$	4 downstream ports active		100		mA
	$I_{CC3.3FS4}$			55		mA
4 Ports High-Speed	$I_{CC1.8HS4}$	4 downstream ports active		105		mA
	$I_{CC3.3HS4}$			135		mA
Unconfigured	$I_{CC1.8UNC}$	Prior to enumeration		70		mA
	$I_{CC3.3UNC}$			10		mA
Enumerated State	$I_{CC1.8CON}$	Upstream port active Full-Speed/Hi-Speed		70		mA
	$I_{CC3.3CON}$			10		mA

Table 6.2 - DC Electrical Characteristics: Digital Pins

(VDD1.8 =1.74 to 2.0V; VDD3.3 =3.0 to 3.6V; VSS = 0V; TA = 0 °C to +70°C; unless otherwise specified.)

PARAMETER	SYMBOL	COMMENTS	MIN	TYP	MAX	UNITS
Refer to Section 4.1 for relationship between buffers and pin names.						
IS Input Buffer						
Low Input Level	V_{ILI}	TTL Levels			0.8	V
High Input Level	V_{IHI}	TTL Levels	2.0			V
Hysteresis	V_{HYSI}		250	300	350	mV
Low Input Leakage	I_{IL}	V_{IN} = 0	-10		+10	uA
High Input Leakage	I_{IH}	V_{IN} = $V_{DD3.3}$	-10		+10	uA

PARAMETER	SYMBOL	COMMENTS	MIN	TYP	MAX	UNITS
I, IPD, IPU Input Buffer						
Low Input Level	V_{ILI}	TTL Levels			0.8	V
High Input Level	V_{IHI}	TTL Levels	2.0			V
Low Input Leakage	I_{IL}	V_{IN} = 0	-10		+10	uA
High Input Leakage	I_{IH}	V_{IN} = $V_{DD3.3}$	-10		+10	uA
ICLK Input Buffer						
Low Input Level	V_{ILCK}	TTL Levels			0.8	V
High Input Level	V_{IHCK}	TTL Levels	2.0			V
Hysteresis	V_{HYSC}		50		100	mV
O8 and IO8 Buffer						
Low Output Level	V_{OL}	I_{OL} = 8 mA @ $V_{DD3.3}$ = 3.3V			0.8	V
High Output Level	V_{OH}	I_{OH} = -4mA @ $V_{DD3.3}$ = 3.3V	2.4			V
Output Leakage	I_{OL}	V_{IN} = 0 to $V_{DD3.3}$ (Note 6.1)	-10		+10	uA
OD8 and IOD8 Buffer						
Low Output Level	V_{OL}	I_{OL} = 8 mA @ $V_{DD3.3}$ = 3.3V			0.8	V
Output Leakage	I_{OL}	V_{IN} = 0 to $V_{DD3.3}$ (Note 6.1)	-10		+10	uA
IOSD12 Buffer						
Low Output Level	V_{OL}	I_{OL} = 12 mA @ $V_{DD3.3}$ = 3.3V			0.8	V
Output Leakage	I_{OL}	V_{IN} = 0 to $V_{DD3.3}$ (Note 6.1)	-10		+10	uA
Hysteresis	V_{HYSI}		250	300	350	mV

Note 6.1 - Output Leakage is measured with the current pins in high impedance.

Table 6.3 - Pin Capacitance

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Clock Input Capacitance	C_{CLKIN}				12	pF
Input Capacitance	C_{IN}	All pins – except DPx/DMx pins			8	pF
Output Capacitance	C_{OUT}	All pins – except DPx/DMx pins			12	pF

Table 6.4 - DC Electrical Characteristics: Analog I/O Pins (DP/DM)

(VDD1.8 =1.74 to 2.0V; VDD3.3 =3.0 to 3.6V; VSS = 0V; TA = 0 °C to +70°C; unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FS FUNCTIONALITY						
Input levels						
Differential Receiver Input Sensitivity	V_{DIFS}	| VI(DP) - VI(DM) |	0.2			V
Differential Receiver Common-Mode Voltage	V_{CMFS}		0.8		2.5	V
Single-Ended Receiver Low Level Input Voltage	V_{ILSE}				0.8	V
Single-Ended Receiver High Level Input Voltage	V_{IHSE}		2.0			V
Output Levels						
Low Level Output Voltage	V_{FSOL}	Pull-up resistor on DP; R_L = 1.5kΩ to $V_{DD3.3}$			0.3	V
High Level Output Voltage	V_{FSOH}	Pull-down resistor on DP, DM; R_L = 15kΩ to GND	2.8		3.6	V
Termination						
Driver Output Impedance for HS and FS	Z_{HSDRV}	Steady state drive	40.5	45	49.5	Ω
Pull-up Resistor Impedance	Z_{PU}		1.425		1.575	KΩ
Termination Voltage For Pull-up Resistor On Pin DP	V_{TERM}		3.0		3.6	V
HS FUNCTIONALITY						
Input levels						
HS Differential Input Sensitivity	V_{DIHS}	| VI(DP) - VI(DM) |	100			mV
HS Data Signaling Common Mode Voltage Range	V_{CMHS}		-50		500	mV
HS Squelch Detection Threshold (Differential)	V_{HSSQ}	Squelch Threshold			100	mV
		Unsquelch Threshold	150			mV
Output Levels						
High Speed Low Level Output Voltage (DP/DM referenced to GND)	V_{HSOL}	When driven into a precision 45Ω load	-10		10	mV
High Speed High Level Output Voltage (DP/DM referenced to GND)	V_{HSOH}	When driven into a precision 45Ω load	360		440	mV
High Speed IDLE Level Output Voltage (DP/DM referenced to GND)	V_{OLHS}	When driven into a precision 45Ω load	-10		10	mV
Chirp-J Output Voltage (Differential)	V_{CHIRPJ}	HS termination resistor disabled, pull-up resistor connected.	700		1100	mV
Chirp-K Output Voltage (Differential)	V_{CHIRPK}	HS termination resistor disabled, pull-up resistor connected.	-900		-500	mV
Leakage Current						
OFF-State Leakage Current	I_{LZ}				± 1	uA
Port Capacitance						
Transceiver Input Capacitance	C_{IN}	Pin to GND		5	10	pF

6.1 Dynamic Characteristics: Analog I/O Pins (DP/DM)

- Compliant with USB2.0 Specification. For complete specifications consult the *Universal Serial Bus Specification Revision 2.0.*

Chapter 7 Functional Overview

Figure 2.1 shows the functional block diagram of the USB2.0 Hub Controller. Each of the functions is described in detail below.

7.1 Bus-Power Detect

The VBUSDET pin on the USB20H04 monitors the state of the upstream V_{BUS} signal and will not pull-up the DP0 resistor if V_{BUS} is not active. If V_{BUS} goes from an active to an inactive state (not powered), the USB20H04 will remove power from the DP0 pull-up resistor within 10 seconds.

To support a dual-role OTG host on the upstream port, the USB20H04 has the ability to pulse the inactive V_{BUS} line. This is defined as V_{BUS} pulsing in the OTG specification. For a more detailed discussion of the OTG features of the USB20H04, please see "Application Note 10.4 Using the USB20H04 with an OTG Host".

7.2 Upstream PHY

The upstream PHY includes the transmitter and receiver that operate in high-speed or full-speed mode, depending on the current hub configuration and the host. The required termination resistors are internal to the USB20H04.

To support a dual-role OTG host on the upstream port, the USB20H04 has the ability to attach a 1.5K ohm resistor to the DP0 pin for 5 to 10ms. This is defined as data-line pulsing in the OTG specification.

7.3 Clock/PLL

The USB20H04 requires a 24MHz signal as a reference clock for the internal PLL. An external crystal is used with the internal oscillator, or an external clock signal can be provided.

7.4 Internal Configuration Select

A default configuration for the USB20H04 is present immediately after RESET_N negation. When the default configuration values will not be used, user defined values must be provided from an external source via the serial interface. The user defined values to be configured are described in section 8.2.

See Section 8.1 for typical circuit examples showing how to select either the default configuration or an external EEPROM. The pins used to select the source of configuration values are given in Table 4.2.

The internal default configuration is enabled when SMB_SEL_N is high and CS/EE_SEL is low on the rising edge of RESET_N. When the SELF_PWR pin is low on the rising edge of RESET_N, the bus-powered default configuration is loaded. If the SELF_PWR pin is high, the self-powered default configuration is loaded. This allows the default configuration to be bus-powered or self-powered following a reset.

7.5 Serial Interface

External configuration data is loaded via the serial interface. The serial interface appears as either an SMBus slave, or an I^2C memory interface.

7.5.1 SMBus Slave

The USB20H04 conforms to voltage, power, and timing specifications as set forth in the SMBus 1.0 Specification for Slave-Only devices. The SMBus interface shares the same pins as the EEPROM interface. If the SMB_SEL_N pin is configured to activate the SMBus interface, external EEPROM support is no longer available and the user-defined configuration values must be downloaded via the SMBus. A separate Application Note 9.29, "USB20H04 4-Port USB2.0 Hub Controller - Configuration Programming" provides details for configuring the USB20H04 via the SMBus.

7.5.2 I^2C Memory Interface

A basic I^2C-bus interface is provided for reading configuration data from an external EEPROM following a reset. The USB20H04 acts as the master and generates the serial clock and the START and STOP conditions.

7.6 Repeater

The hub repeater is responsible for managing connectivity between upstream and downstream facing ports which are operating at the same speed. The repeater includes both a high-speed repeater function and a full-/low-speed repeater function. When the upstream port is operating in a high-speed environment, traffic passes through the high-speed repeater to downstream ports that are operating at high-speed. As detailed in the USB specification, the repeater is responsible for managing connectivity on a ‘per packet’ basis. It implements ‘packet signaling’ and ‘resume’ connectivity. If a low-speed device is detected the repeater will not propagate upstream packets to the corresponding port, unless they are preceded by a PREAMBLE PID.

7.7 SIE

Communication with the host is handled by the SIE. The full USB protocol layer is implemented in the SIE, including Endpoint 0 and Endpoint 1. All standard USB requests from the host are handled by the hardware without the need for firmware intervention.

7.8 Controller

The controller implements protocol handling at a higher level. By responding to SETUP packets it coordinates enumeration, and it manages suspend/resume operation.

7.9 Transaction Translator (TT)

The transaction translator supports full-speed and low-speed devices attached to downstream ports in the high-speed environment. To provide the highest level of performance, the USB20H04 Hub provides one Transaction Translator (TT) per port (defined as multiple-TT).

7.10 Port Controller

The port controller provides status and control of individual downstream ports. Any port status change is reported to the host via the hub status change (interrupt) endpoint.

7.11 Downstream PHY

Each of the downstream PHYs include a transmitter and receiver that operate in high-speed, full-speed or low-speed mode, depending on the attached device. The required termination resistors are internal to the USB20H04.

7.12 OC Sense/Switch Driver

One output per port is provided to control an external port power switch and one input per port is provided to sense an external over-current sense. Both ganged and individual (per-port) configurations are supported. See Figure 10.1 - High Level Block Diagram of a Self-Powered Hub for a typical implementation.

7.12.1 Over-Current Sense

An external device monitors the current being provided to attached peripherals, and generates an output during over-current conditions. This output is connected to the OCSx_N input of the USB20H04. This input pin has an internal pull up resistor.

This input is filtered by the USB20H04 for the amount of time configured in the Over-Current Timer field (See Table 8.4 - Address 8; Config_Byte_1) If the input continues to be asserted beyond the configured time, the USB20H04 reports the over-current condition to the host and disables the power switch output associated with that particular port. For use with typical silicon-based power controllers, configure the timer to a value greater than zero to avoid glitches when devices are attached.

7.12.2 Switch Driver

Power to downstream ports is controlled by the VBUSx_N (where x stands for the port number) output connected to an external power switch device. This output may be disabled when an over-current condition has been reported, as described in Section 7.12.1.

7.13 LED Drivers

As per the specification, each downstream port of the hub supports an optional status indicator. The USB20H04 provides one output per port for a green LED and one output per port for an amber LED.

Each port's indicator must be located in a position that obviously associates the indicator with the port. The color and state of the LED is used to provide status information to the user.

Two different modes of operation are supported for the port indicators: automatic mode and manual mode. The USB20H04 defaults to automatic mode upon power-up. In automatic mode, the USB20H04 controls the color of the indicator LED as described in Table 7.1 - Automatic Mode Port Indicators.

Table 7.1 - Automatic Mode Port Indicators

COLOR	DEFINITION
Off	Disconnected, Disabled, Not Configured, Resetting, Testing, Suspending, or Resuming
Amber	Over Current Condition
Green	Enabled, Transmit, or TransmitR

In manual mode, the host controls the color and state of the indicator LED by sending a command to the USB20H04 to put the LED in a particular state. This is described in Table 7.2 - Manual Mode Port Indicators.

Table 7.2 - Manual Mode Port Indicators

COLOR	DEFINITION
Off	Not Operational
Amber	Error Condition
Green	Fully Operational
Blinking Off/Green	Software Attention
Blinking Off/Amber	Hardware Attention

The USB20H04 can be configured to either support or not support port indicators. If port indicators are not included in the hub design, disable this feature in the configuration.

Chapter 8 Implementation Notes

The following sections consist of select functional explanations to aid in implementing the Hub Controller into a system.

8.1 Configuration Implementations

The USB20H04 is normally configured by an external EEPROM connected directly to the serial interface. Typical circuit diagrams are shown below. For a more detailed discussion of the serial interface, including how to configure the USB20H04 using the SMBus mode, please see Application Note 9.29, "USB20H04 4-Port USB2.0 Hub Controller, Configuration Programming". The Application Note also discusses designing a Hub system that supports In Circuit Programming of the EEPROM.

8.1.1 Interfacing a 2-wire Serial EEPROM

The I^2C EEPROM interface is designed to attach to a single “dedicated” I^2C EEPROM. It conforms to the Standard-mode I^2C Specification (100kbit/s transfer rate and 7-bit addressing) for protocol and electrical compatibility. The circuit board designer is required to place external pull-up resistors (10K ohm recommended) on the SDA & SCL lines (per SMBus 1.0 Specification, and EEPROM manufacturer guidelines) to VDD in order to assure proper operation.

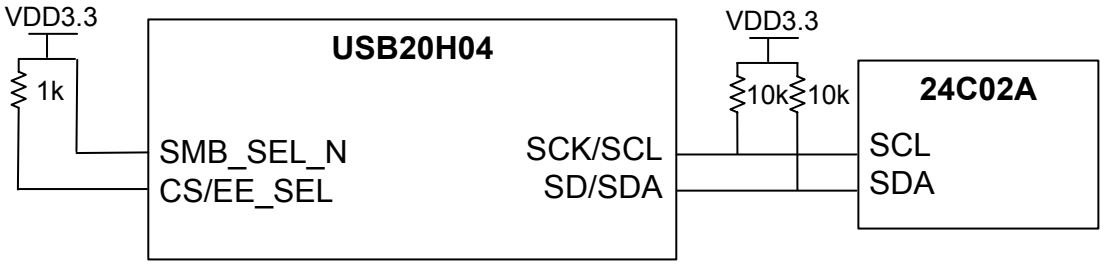

Figure 8.1 - 2-Wire EEPROM Interface

8.1.2 Internal Default Configuration

The internal default configuration is enabled when SMB_SEL_N is high and CS/EE_SEL is low on the rising edge of RESET_N. If SELF_PWR is low, then the bus-powered default settings are loaded.

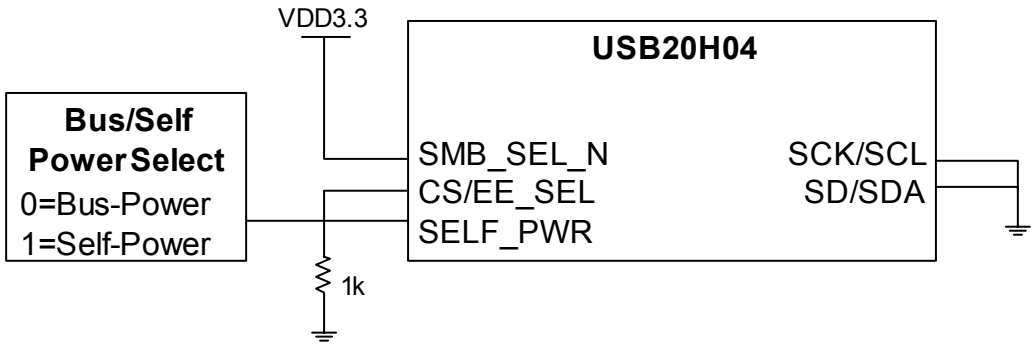

Figure 8.2 - Internal Default Mode

8.2 EEPROM Programming Values

Configuration data is loaded from an external EEPROM following reset. The values to be programmed into the EEPROM are summarized in Table 8.1 - Summary of OEM Value Programming.

Table 8.1 - Summary of OEM Value Programming

ADDRESS	FIELD NAME	DESCRIPTION
0	VID (MSB)	Vendor ID (assigned by USB-IF).
1	VID (LSB)	
2	PID (MSB)	Product ID (assigned by Manufacturer).
3	PID (LSB)	
4	DID (MSB)	Device ID (assigned by Manufacturer).
5	DID (LSB)	
6	Config_Byte_3	Configuration options defined in Table 8.2.
7	Config_Byte_2	Configuration options defined in Table 8.3.
8	Config_Byte_1	Configuration options defined in Table 8.4.
9	Max_Power	Maximum current for this configuration, see Table 8.5.
10	HubContrCurrent	Maximum current for the USB20H04, see Table 8.5.
11	PwrOn2PwrGood	Time until power is stable, see Table 8.5.

Detailed definition of the bits used to program the OEM values are given in Table 8.2 through Table 8.5.

Table 8.2 - Address 6; Config_Byte_3

BIT	FIELD NAME	DESCRIPTION
7	Self-/Bus-Power	Selects either self-powered or bus-powered operation: 0: Self-powered operation. 1: Bus-powered operation.
6	Port Indicators	Selects implementation of port indicators: 0: No port indicators. 1: Port indicators implemented.
5	High-Speed Disable	Selects whether high-speed operation is disabled: 0: High-/Full-Speed operation. 1: Full-Speed only (High-Speed disabled).
4	Multiple TT Support	Selects whether multiple transaction translators are available: 0: Single TT for all ports. 1: Each port has one TT available (multiple TTs supported).
3	EOP Disable	Selects whether EOP generation of EOF1 is disabled when in Full-Speed mode: 0: EOP generation at EOF1. 1: EOP generation at EOF1 disabled.
2	Current Sensing	Selects whether current sensing is ganged on all ports, or on an individual port-by-port basis: 0: Individual port-by-port. 1: Ganged sensing.
1	Power Switching	Selects whether downstream port power switching is ganged on all ports, or on an individual port-by-port basis: 0: Individual port-by-port. 1: Ganged switching.
0	Compound Device	Selects whether the hub is part of a compound device: 0: Not a compound device. 1: Yes, USB20H04 is part of a compound device.

Table 8.3 - Address 7; Config_Byte_2

The ports may be individually configured to be inactive. However, the order in which ports are set to inactive is very specific. Port 4 must be the first port configured to be inactive, followed by port 3.

BIT	FIELD NAME	DESCRIPTION
7:4	Non-Removable Device	Selects which ports include non-removable devices. A one indicates that the port is non-removable: Bit 7: Port 4 is non-removable. Bit 6: Port 3 is non-removable. Bit 5: Port 2 is non-removable. Bit 4: Port 1 is non-removable. All zeroes sets all ports removable.

BIT	FIELD NAME	DESCRIPTION
3:0	Port Non-Active	Selects which ports are active. A one indicates that the port is non-active: Bit 3: Port 4 is non-active. Bit 2: Port 3 is non-active. Bit 1: Port 2 is non-active. Bit 0: Port 1 is non-active. All zeroes sets all ports active. Note: Active ports must be contiguous, and must start with port number 1.

Table 8.4 - Address 8; Config_Byte_1

BIT	FIELD NAME	DESCRIPTION
7	Dynamic Power	Selects the ability to transition to bus-powered operation if the local power source is removed: 0: No dynamic auto-switching. 1: Dynamic auto-switching ability enabled.
6	On-The-Go	Selects the ability to support an OTG host: 0: No OTG support. 1: OTG support enabled.
5:4	Reserved	Set to zero.
3:0	Over-Current Timer	Selects the over-current timer delay in 2 ms increments for the active ports. 0101: delay is 2ms 1010: delay is 4ms 1111: delay is 6ms Note: All other values are reserved

Table 8.5 - Addresses 9 - 11

BIT	FIELD NAME	DESCRIPTION
7:0	Max Power	Current in 2mA increments that the 4-port hub consumes from an upstream port in this configuration. A value of 50, or 32(h), indicates 100 mA.
7:0	HubContrCurrent	Absolute maximum current requirement in 2mA increments of the hub controller electronics. A value of 50, or 32(h), indicates 100 mA.
7:0	PwrOn2PwrGood	Time in 2ms intervals from the time the power on sequence begins on a port until power is good on that port. A value of 50, or 32(h), indicates 100 ms.

8.3 Default Configuration Values

Default values for configuration data are loaded as described in section 8.1.2 and 8.1.3 above. The values programmed are summarized in Table 8.6 - Default Configuration Values.

Table 8.6 - Default Configuration Values

REGISTER ADDRESS	REGISTER NAME	SELF-POWERED DEFAULT (HEX)	BUS-POWERED DEFAULT (HEX)
01h	VID MSB	04	04
02h	VID LSB	24	24
03h	PID MSB	**	**
04h	PID LSB	00	00
05h	DID MSB	00	00
06h	DID LSB	00	00
07h	Config Data Byte 3	58	98
08h	Config Data Byte 2	00	08
09h	Config Data Byte 1	05	05
0Ah	Max Power	00	64
0Bh	Hub Controller Max Current	00	64
0Ch	Power-on Time	80	80

** The default PID value is dependent on the silicon revision.

8.4 Reset

There are two different resets that the USB20H04 will experience. One is a hardware reset (via the RESET_N pin) and the second a USB Reset.

8.4.1 External Hardware Reset

A valid hardware reset is initiated by the assertion of RESET_N for a minimum of 100ns after all power supplies are within operating range.

Assertion of RESET_N (external pin) causes the following:

1. All downstream ports are disabled, and V_{BUS} power to downstream devices is removed.
2. The PHYs are disabled, and the differential pairs will be in a high-impedance state
3. All transactions immediately terminate, and no states are saved.
4. All internal registers return to the default state (in most cases, 00(h)).
5. LED indicators are disabled

After RESET_N is negated, the USB20H04 is ready to be configured as an SMBus slave (if SMB_SEL_N = 0) or it reads OEM specific data from the external EEPROM (if SMB_SEL_N = 1). Default values for configuration data are loaded if the SELF ONLY default strapping option is selected, or if an EEPROM is not present. The timing associated with these options is shown in the tables below.

8.4.1.1 SMBus Configuration Timing

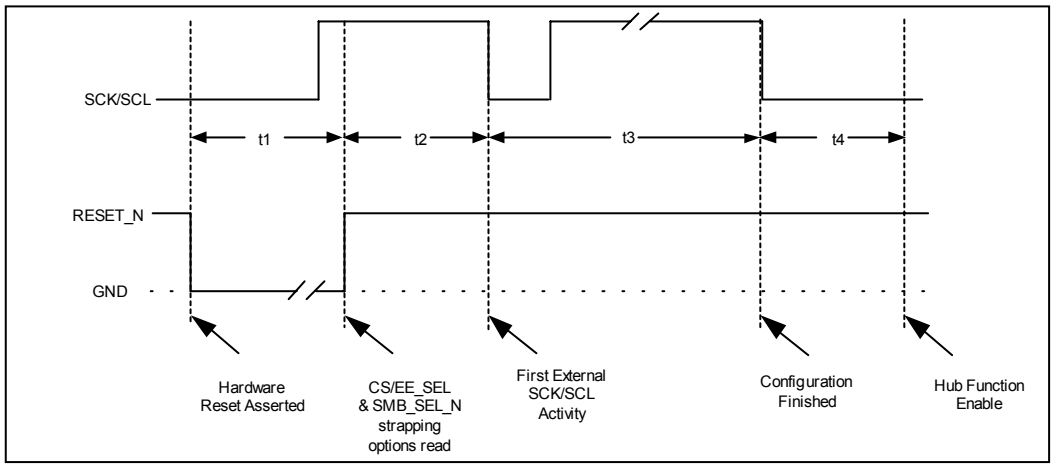

Figure 8.3 - Timing for Configuration from SMBus

Table 8.7 - Time Values to Configure from SMBus

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
T1	RESET_N asserted	100			nsec
T2	USB20H04 recovery/stabilization – until first external SCK/SCL activity	16		32	nsec
T3	Implementation dependent load time				
T4	Configuration finished to Hub enabled		35	70	nsec

8.4.1.2 EEPROM Configuration Timing

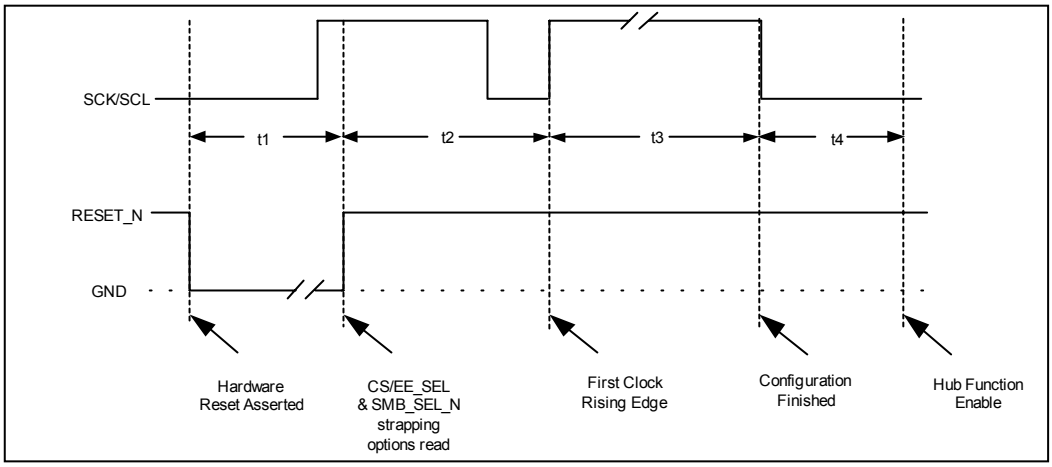

Figure 8.4 - Timing to Complete Configuration from EEPROM

Table 8.8 - Time Values to Configure From EEPROM

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
T1	RESET_N asserted	100			nsec
T2	(I^2C) USB20H04 recovery/stabilization – until first rising edge of SCK/SCL		24	30	µsec
T3	(I^2C) EEPROM configuration to final SCK/SCL activity		8	10	msec
T4	Configuration finished to Hub enabled		35	70	nsec

8.4.2 USB Reset

When the upstream host signals a reset, the USB20H04 does the following:

Note: The USB20H04 does not propagate the upstream USB Reset to downstream devices!

1. Sets default address to 0
2. Sets configuration to: un-configured
3. Negates VBUSx_N (where x stands for the port number) to all downstream ports.
4. Clears all TT buffers.
5. Moves device from suspended to active (if suspended).
6. Complies with Section 11.10 of the USB2.0 specification for behavior after completion of the reset sequence.

The host then configures the hub, and the hub's downstream port devices, in accordance with the USB specification.

Chapter 9 Hub Descriptors

The USB20H04 will not electrically attach to the USB until after it has loaded valid data for all user-defined descriptor fields. A default configuration is present immediately after RESET_N negation. User defined configuration values can be loaded from either an external microcontroller or an external EEPROM.

A hub returns different descriptors based on whether it is operating at high-speed or full-/low-speed. A hub can report three different sets of the descriptors: one descriptor set for full-/low-speed operation and two sets for high-speed operation. The descriptors reported by the USB20H04 are summarized in the following tables. The host retrieves this information by using the GetDescriptor request with the corresponding descriptor type values.

Table 9.1 - Device Descriptor

OFFSET	FULL SPEED	HIGH SPEED	FIELD NAME	DESCRIPTION
0	12h	12h	*bLength*	Size of this descriptor in bytes
1	01h	01h	*bDescriptorType*	DEVICE Descriptor Type
2,3	0200h	0200h	*bcdUSB*	USB Specification Number
4	09h	09h	*bDeviceClass*	Class code assigned by USB-IF for Hubs
5	00h	00h	*bDeviceSubClass*	Class code assigned by USB-IF for Hubs
6	00h	01h*	*bDeviceProtcol*	Protocol code assigned by the USB-IF
7	40h	40h	*bMaxPacketSize0*	64-byte packet size
8,9	user	user	*idVendor*	Vendor ID; OEM value
10,11	user	user	*idProduct*	Product ID; OEM value
12,13	user	user	*bcdDevice*	Device ID; OEM value
14	00h	00h	*iManufacturer*	This optional string is not supported.
15	00h	00h	*iProduct*	This optional string is not supported.
16	00h	00h	*iSerialNumber*	This optional string is not supported.
17	01h	01h	*iNumConfigurations*	Supports 1 configuration

* 02h for multiple-TT

Table 9.2 - Device Qualifier Descriptor

OFFSET	FULL SPEED	HIGH SPEED	FIELD NAME	DESCRIPTION
0	0Ah	0Ah	*bLength*	Size of this descriptor in bytes
1	06h	06h	*bDescriptorType*	DEVICE Qualifier Type
2	00h	00h	*bcdUSB*	USB Specification Version Number (LSB)
3	02h	02h	*bcdUSB*	USB Specification Version Number (MSB)
4	09h	09h	*bDeviceClass*	Class code assigned by USB-IF for Hubs
5	00h	00h	*bDeviceSubClass*	Class code assigned by USB-IF for Hubs
6	00h	01h*	*bDeviceProtcol*	Protocol code.
7	40h	40h	*bMaxPacketSize0*	64-byte packet size for other speed
8	01h	01h	*bNumConfigurations*	Supports 1 other speed configuration
9	00h	00h	*bReserved*	Reserved

* 02h for multiple-TT

Table 9.3 - Standard Configuration Descriptor

OFFSET	FULL SPEED	HIGH SPEED	FIELD NAME	DESCRIPTION
0	09h	09h	*bLength*	Size of this descriptor in bytes
1	02h	02h	*bDescriptorType*	CONFIGURATION Descriptor Type
2,3	yyyyh	yyyyh	*wTotalLength*	Total length of data returned for this configuration yyyyh = 0019h if OTG support is disabled. yyyyh = 001Ch if OTG support is enabled.
4	01h	01h	*bNumInterfaces*	Number of interfaces supported by this configuration
5	01h	01h	*bConfigurationValue*	Value to use as an argument to the SetConfiguration() request to select this configuration.
6	00h	00h	*iConfiguration*	Index of string descriptor describing this configuration (string not supported)
7	*user/ signal (Bitmap)*	*user/ signal (Bitmap)*	*bmAttibutes*	The following values are derived from the OEM value: = A0h for Bus-Powered. = E0h for Self-Powered. All other values are reserved.
8	user (mA)	user (mA)	*bMaxPower*	If Dynamic Power support is disabled, this value is derived from the OEM value for MaxPower consumed from the bus by the hub in this configuration. If Dynamic Power support is enabled, the USB20H04 must be configured for a bus-powered configuration only, and the following values are reported for this field: SELF_PWR = 0, OEM value reported. SELF_PWR = 1, 02h (small upstream load for Self-Powered configuration).

Table 9.4 - Other_Speed_Configuration Descriptor

OFFSET	FULL SPEED	HIGH SPEED	FIELD NAME	DESCRIPTION
0	09h	09h	*bLength*	Size of this descriptor in bytes
1	07h	07h	*bDescriptorType*	Other-Speed Configuration Descriptor Type
2,3	yyyyh*	zzzzh	*wTotalLength*	Total length of data returned for this configuration
				zzzz = 0019h if single TT and OTG disabled.
				zzzz = 001Ch if single TT and OTG enabled.
				zzzz = 0029h if multi-TT and OTG disabled.
				zzzz = 002Fh if multi-TT and OTG enabled.

OFFSET	FULL SPEED	HIGH SPEED	FIELD NAME	DESCRIPTION
4	01h	01h**	*bNumInterfaces*	Number of interfaces supported by this configuration
5	01h	01h	*bConfigurationValue*	Value to use to select configuration.
6	00h	00h	*iConfiguration*	Index of string descriptor describing this configuration (string not supported)
7	*user/ signal (Bitmap)*	*user/ signal (Bitmap)*	*bmAttibutes*	Same as Configuration Descriptor
8	user (mA)	user (mA)	*bMaxPower*	Same as Configuration Descriptor

* Same as Configuration Descriptor

** 02h for multiple-TT

Table 9.5 - Standard Interface Descriptor

OFFSET	FULL SPEED	HIGH SPEED	FIELD NAME	DESCRIPTION
0	09h	09h	*bLength*	Size of this descriptor in bytes
1	04h	04h	*bDescriptorType*	INTERFACE Descriptor Type
2	00h	00h	*bInterfaceNumber*	Number of this interface
3	00h	00h	*bAlternateSetting*	Value used to select this alternate setting for the interface
4	01h	01h	*bNumEndpoints*	Number of endpoints used by this interface (not including endpoint 0)
5	09h	09h	*bInterfaceClass*	Class code assigned by USB for Hubs
6	00h	00h	*bInterfaceSubClass*	Subclass code assigned by USB
7	00h	01h*	*bInterfaceProtcol*	Protocol code assigned by USB
8	00h	00h	*bInterface*	Index of string descriptor describing this configuration (string not supported)

* 02h for multiple-TT

Table 9.6 - Standard Endpoint Descriptor

OFFSET	FULL SPEED	HIGH SPEED	FIELD NAME	DESCRIPTION
0	07h	07h	*bLength*	Size of this descriptor in bytes
1	05h	05h	*bDescriptorType*	ENDPOINT Descriptor Type
2	81h	81h	*bEndpointAddress*	The address of the endpoint on the USB device.
3	03h	03h	*bmAttributes*	Describes the endpoint's attributes (interrupt only, no synchronization, data endpoint).
4,5	0001h	0001h	*wMaxPacketSize*	Maximum packet size for this endpoint
6	FFh	0Ch	*bInterval*	Interval for polling endpoint for data transfers.

Table 9.7 - Interface Descriptor (present if multiple-TT)

OFFSET	HIGH SPEED	FIELD NAME	DESCRIPTION
0	09h	*bLength*	Size of this descriptor in bytes
1	04h	*bDescriptorType*	INTERFACE Descriptor Type
2	00h	*bInterfaceNumber*	Number of this interface
3	01h	*bAlternateSetting*	Value used to select this alternate setting for the interface
4	01h	*bNumEndpoints*	Number of endpoints used by this interface (not including endpoint 0)
5	09h	*bInterfaceClass*	Class code assigned by USB for Hubs
6	00h	*bInterfaceSubClass*	Subclass code assigned by USB
7	02h	*bInterfaceProtcol*	Protocol code assigned by USB
8	00h	*bInterface*	Index of string descriptor describing this configuration (string not supported)

Table 9.8 - On-The-GO (OTG) Descriptor

OFFSET	FULL SPEED	HIGH SPEED	FIELD NAME	DESCRIPTION
0	03h	03h	*bLength*	Size of this descriptor in bytes
1	09h	09h	*bDescriptorType*	OTG Descriptor Type
2	01h	01h	*wMaxPacketSize*	Attribute Fields: D[7:2] = Reserved D1: HNP Support (not supported) D0: SRP Support.

Table 9.9 - Class-Specific Hub Descriptor (Full-Speed and High-Speed)

OFFSET	FIELD NAME	VALUE	DESCRIPTION
0	*Length*	09h	Size of this Descriptor.
1	*Descriptor Type*	29h	Hub Descriptor Type.
2	*NbrPorts*	user	Number of downstream facing ports this Hub supports. Derived from OEM value defined in EEPROM or SMBus load. See Section 11.23.2.1 in the USB Specification. Note: If Dynamic Power is enabled, and the SELF_PWR pin is low (indicating Bus Power Operation), then ports 3 & 4 are not available and either a value of 1 is reported if the OEM value is 1 or a value of 2 is reported if the OEM value is 2, 3 or 4.
3,4	*HubCharacteristics*	user	Defines several characteristics that are derived from OEM values. Also defines TT Think Time (fixed at a value of 00b for 8FS bit times max).
5	*PwrOn2PwrGood*	user	Time (in 2 ms intervals) from the time the power-on sequence begins on a port until power is good on that port. Derived from OEM value.

OFFSET	FIELD NAME	VALUE	DESCRIPTION
6	*HubContrCurrent*	user	Maximum current requirements of the hub controller electronics in mA. Derived from OEM value.
7	*DeviceRemovable*	user	Indicates if port has a removable device attached. Derived from OEM value.
8	*PortPwrCtrlMask*	FFh	Field for backwards USB 1.0 compatibility.

Chapter 10 Application Diagrams

The highly-integrated USB20H04 Hub Controller is complemented with a minimal number of external components to create a complete four-port Hi-Speed USB hub application. Figure 10.1 illustrates one possible hardware configuration, but is not a complete schematic. This block diagram shows a self-powered hub with individual over-current protection and power switching on each downstream port.

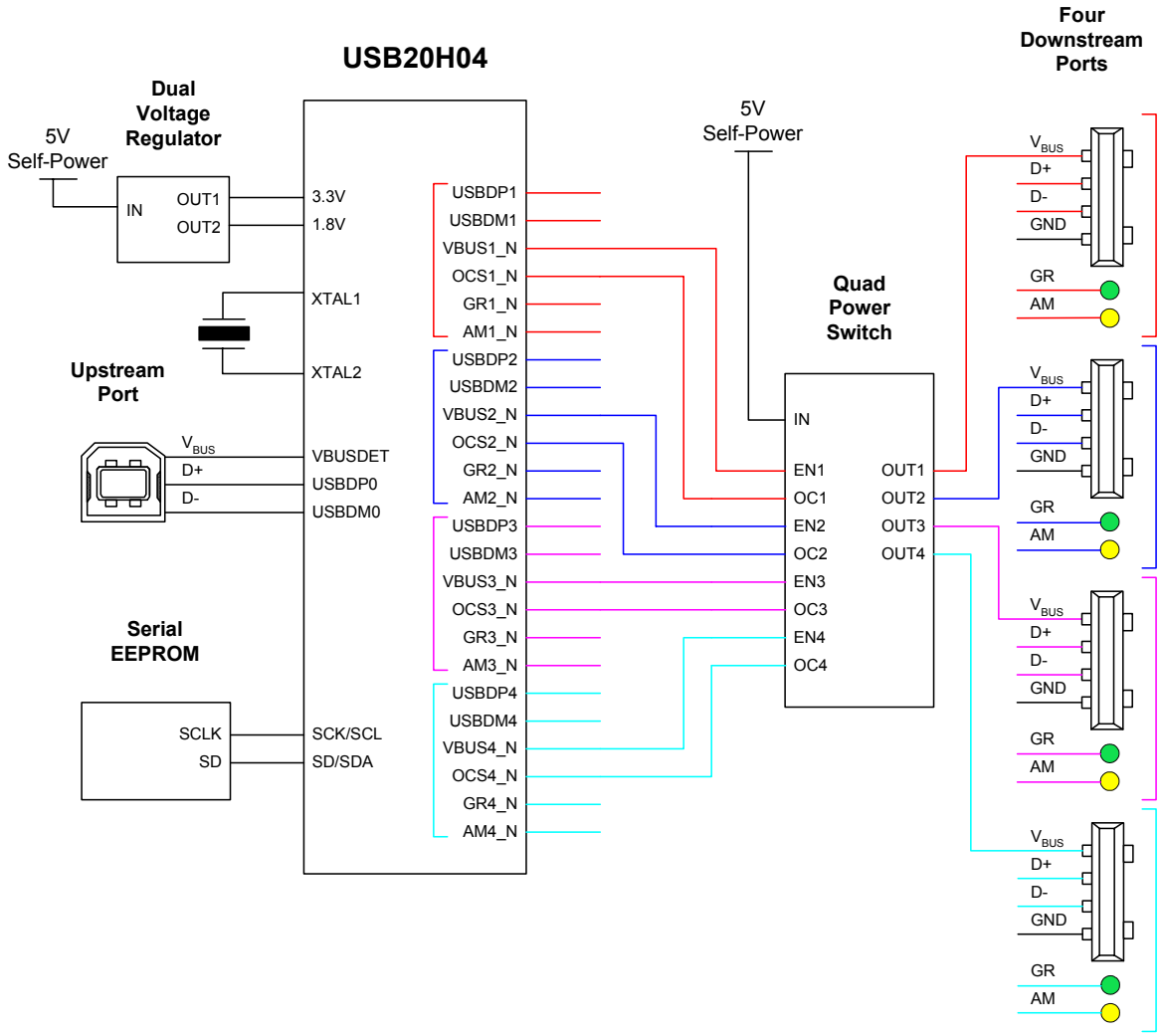

Figure 10.1 - High Level Block Diagram of a Self-Powered Hub

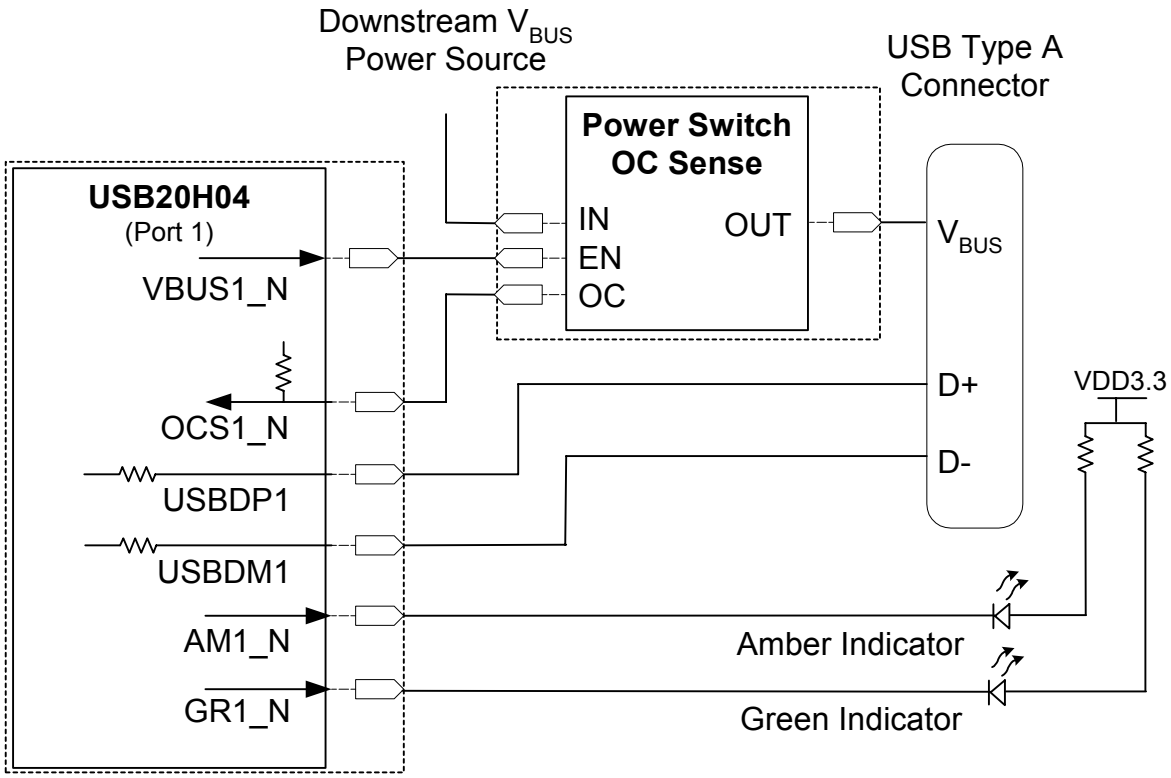

Figure 10.2 - USB Downstream Port Connection

Chapter 11 Package Outline

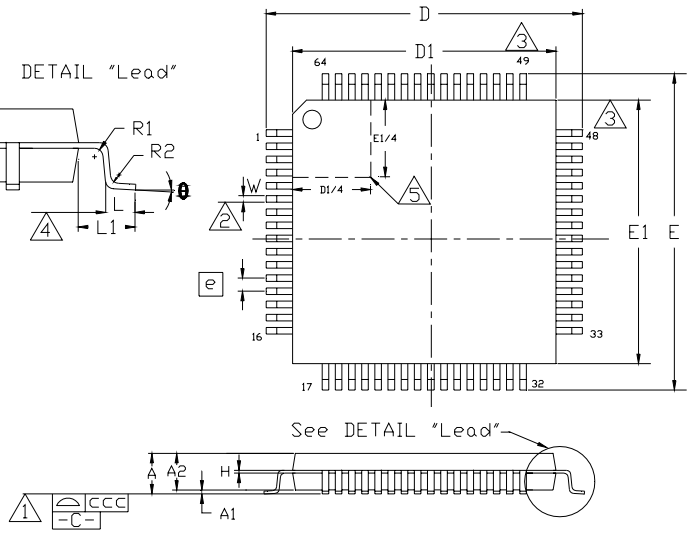

Figure 11.1 - 64 Pin TQFP Package Outline, 10 x 10 x 1.4 Body, 2 MM Footprint

Table 11.1 - 64 Pin TQFP Package Parameters

	MIN	NOMINAL	MAX	REMARKS
A	~	~	1.60	Overall Package Height
A1	0.05	~	0.15	Standoff
A2	1.35	~	1.45	Body Thickness
D	11.80	~	12.20	X Span
D1	9.80	~	10.20	X body Size
E	11.80	~	12.20	Y Span
E1	9.80	~	10.20	Y body Size
H	0.09	~	0.20	Lead Frame Thickness
L	0.45	0.60	0.75	Lead Foot Length
L1	~	1.00	~	Lead Length
e		0.50 Basic		Lead Pitch
θ	0^o	~	7^o	Lead Foot Angle
W	0.17	0.22	0.27	Lead Width
R1	0.08	~	~	Lead Shoulder Radius
R2	0.08	~	0.20	Lead Foot Radius
ccc	~	~	0.08	Coplanarity

Notes:
1. Controlling Unit: millimeter.
2. Tolerance on the true position of the leads is ± 0.04 mm maximum.
3. Package body dimensions D1 and E1 do not include the mold protrusion.
   Maximum mold protrusion is 0.25 mm per side.
4. Dimension for foot length L measured at the gauge plane 0.25 mm above the seating plane.
5. Details of pin 1 identifier are optional but must be located within the zone indicated.