84221

Quad 100BaseTX/10BaseT Physical Layer Device

PRELIMINARY

99191

Features

- **Single Chip 100BaseTX/10BaseT Physical Layer Solution**
- **Four Independent Channels in One IC**
- **3.3V Power Supply with 5V Tolerant I/O**
- **Dual Speed - 10/100 Mbps**
- **Half and Full Duplex**
- **Reduced Pin Count MII (RMII) Interface to Ethernet Controller**
- **MI Interface for Configuration and Status**
- **Optional Repeater Interface**
- **AutoNegotiation for 10/100, Full/Half Duplex Hardware Controlled Advertisement**
- **Meets all Applicable IEEE 802.3, 10BaseT, 100BaseTX Standards**
- **On Chip Wave Shaping - No External Filters Required**
- **Adaptive Equalizer for 100BaseTX**
- **Baseline Wander Correction**
- **LED Outputs**
  - **Link**
  - **Activity**
  - **Collision**
  - **Full Duplex**
  - **10/100**
- **128L PQFP**

Note: Check for latest Data Sheet revision before starting any designs.

SEEQ Data Sheets are now on the Web, at www.lsilogic.com

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Description

The 84221 is a highly integrated Ethernet Transceiver for twisted pair and fiber Ethernet applications. The 84221 can be configured for either 100BaseTX or 10BaseT Ethernet operation.

The 84221 consists of four (4) separate and independent channels. Each channel consists of: 4B5B/Manchester encoder, scrambler, transmitter with wave shaping and on-chip filters, transmit output driver, receiver with adaptive equalizer, filters, baseline wander correction, clock and data recovery, descrambler, 4B5B/Manchester decoder, and controller interface (MII or RMII).

The addition of internal output waveshaping circuitry and on-chip filters eliminates the need for external filters normally required in 100BaseTX and 10BaseT applications.

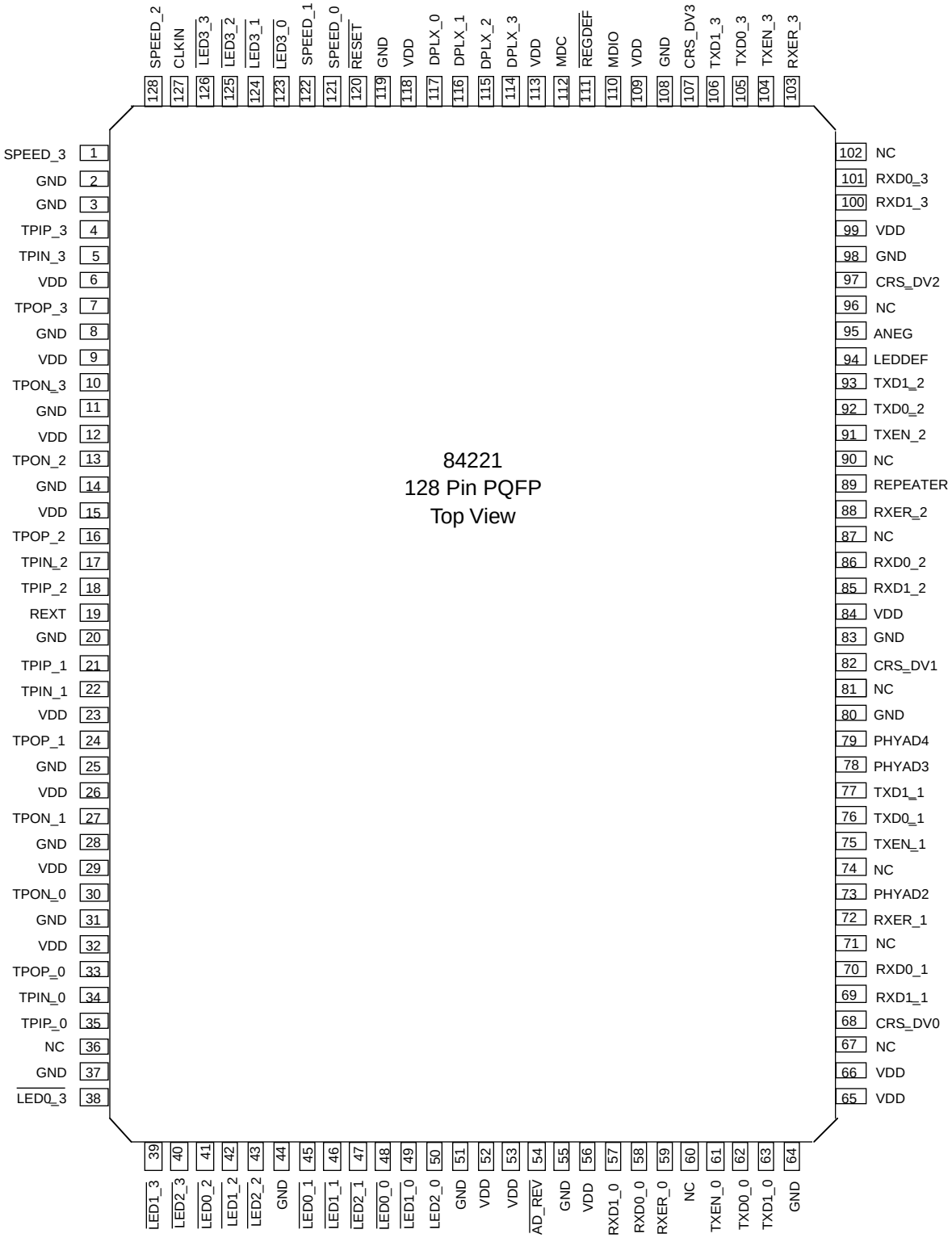
The 84221 can automatically configure itself for 100 or 10 Mbps and Full or Half Duplex operation, for each channel independently, using the on-chip AutoNegotiation algorithm.

The 84221 can access eleven 16-bit registers for each channel through the Management Interface (MI) serial port. These registers comply to Clause 22 of IEEE 802.3u and contain configuration inputs, status outputs, and device capabilities.

The 84221 is ideal as a media interface for 100BaseTX/10BaseT switching hubs, repeaters, routers, bridges, and other multi port applications.

The 84221 is implemented in a low power CMOS technology and operates with a 3.3V power supply.

1.0 Pin Configuration



1.0 PIN DESCRIPTION

Power Supplies			
Pin #	**Pin Name**	**I/O**	**Description**
6 9 12 15 23 26 29 32 52 53 56 65 66 84 99 109 113 118	VDD	—	**Positive Supply.** +3.3 +/-5% Volts.
2 3 8 11 14 20 25 28 31 37 44 51 55 64 80 83 98 108 119	GND	—	**Ground.** 0 Volts.
36 60 67 71 74 81 87 90 96 102	NC	—	**No Connect.** Reserved for future use, must be left floating for proper operation.

1.0 PIN DESCRIPTION (cont'd)

Media Interface			
Pin #	**Pin Name**	**I/O**	**Description**
7 16 24 33	TPOP_[3:0]	O	**Twisted Pair Transmit Output, Positive.**
10 13 27 30	TPON_[3:0]	O	**Twisted Pair Transmit Output, Negative.**
4 18 21 35	TPIP_[3:0]	I	**Twisted Pair Receive Input, Positive.**
5 17 22 34	TPIN_[3:0]	I	**Twisted Pair Receive Input, Negative.**
19	REXT	—	**Transmit Current Set.** An external resistor connected between this pin and GND will set the level for the transmit outputs.

1.0 PIN DESCRIPTION (cont'd)

Controller Interface (RMII)			
Pin #	**Pin Name**	**I/O**	**Description**
127	CLKIN	I	**Clock Input.** This controller interface input latches controller interface data in and out of the device on rising edges for all channels. There must be a 50 Mhz clock tied to this pin.
104 91 75 61	TXEN_[3:0]	I	**Transmit Enable Input.** These interface inputs must be be asserted active high to allow data on TXD and TXER to be clocked in on the rising edges of CLKIN.
[106:105] [93:92] [77:76] [63:62]	TXD[1:0]_3 TXD[1:0]_2 TXD[1:0]_1 TXD[1:0]_0	I	**Transmit Data Input.** These interface inputs contain input di-bit data to be transmitted on the TP outputs and are clocked in on rising edges of CLKIN.
107 97 82 68	CRS_DV[3:0]	O	**Carrier Sense Output.** These interface outputs are asserted active high when valid data is detected on the receive TP inputs and is clocked out on the rising edge of CLKIN.
[100:101] [85:86] [69:70] [57:58]	RXD[1:0]_3 RXD[1:0]_2 RXD[1:0]_1 RXD[1:0]_0	O	**Receive Data Output.** These interface outputs contain recovered di-bit data from the TP inputs and are clocked out on the rising edges of CLKIN.
103 88 72 59	RXER_[3:0]	O	**Receive Error Output.** These interface outputs are asserted active high when coding or other specified errors are detected on the TP inputs and are clocked out on rising edges of CLKIN.

1.0 PIN DESCRIPTION (cont'd)

Management Interface (MI)			
Pin #	**Pin Name**	**I/O**	**Description**
112	MDC	I	**Management Interface (MI) Clock Input.** This MI clock shifts serial data into and out of MDIO on rising edges.
110	MDIO	I/O	**Management Interface (MI) Data Input/Output.** This bidirectional pin contains serial data that is clocked in and out on rising edges of the MDC clock.
111	$\overline{\text{REGDEF}}$	I Pullup	**Invalid Register Read Select** This active low input controls the default values that are read from invalid register locations. If $\overline{\text{REGDEF}}$ = '1' All invalid register locations will return a value of '0000' when read. If $\overline{\text{REGDEF}}$ = '0' All invalid register locations will return a value of 'ffff' when read.
79 78 73	PHYAD[4:2]	I	**MI Physical Device Address Input.** These pins set the three most significant bits of the PHY address. The two least significant bits of the PHY address are set internally to match the channel number, as shown below: Channel 3: PHYAD1 = 1, PHYAD0 = 1 Channel 2: PHYAD1 = 1, PHYAD0 = 0 Channel 1: PHYAD1 = 0, PHYAD0 = 1 Channel 0: PHYAD1 = 0, PHYAD0 = 0

1.0 PIN DESCRIPTION (cont'd)

LED Drivers			
Pin #	**Pin Name**	**I/O**	**Description**
126 125 124 123	$\overline{\text{LED3\_[3:0]}}$	O	**LED Output.** The default functions of these pins are 100 Mbps Link Detect outputs assuming LEDDEF = 0. These pins can drive an LED from both VDD and GND. Please refer to Table 1a. for LED description
40 43 47 50	$\overline{\text{LED2\_[3:0]}}$	O	**LED Output.** The default functions of these pins are Activity Detect outputs assuming LEDDEF = 0. These pins can drive an LED from both VDD and GND. Please refer to Table 1a. for LED description
39 42 46 49	$\overline{\text{LED1\_[3:0]}}$	O	**LED Output.** The default functions of these pins are Full Duplex Detect outputs assuming LEDDEF = 0. These pins can drive an LED from both VDD and GND. Please refer to Table 1a. for LED description
38 41 45 48	$\overline{\text{LED0\_[3:0]}}$	O	**LED Output.** The default functions of these pins are 10 Mbps Link Detect outputs assuming LEDDEF = 0. These pins can drive an LED from both VDD and GND. Please refer to Table 1a. for LED description
94	LEDDEF	I Pulldown	**LED Default Select Input.** This pin changes the default selection for the LED's in the MI Serial Port Global Configuration Register. 1 = LINK + ACT, COL, FDX, 10/100 0 = LINK100, ACT, FDX, LNK10

1.0 PIN DESCRIPTION (cont'd)

Miscellaneous			
Pin #	**Pin Name**	**I/O**	**Description**
95	ANEG	I	**AutoNegotiation Enable Input.** This digital input, ANDed with register bit 0.12, enables AutoNegotiation for all channels. 1 = AutoNegotiation On & Combined with Speed and Duplex pins, control advertisement. Please refer to Table 1 for the different combinations. 0 = Off
1 128 122 121	SPEED_[3:0]	I	**Speed Selection Input.** These digital inputs, ANDed with register bit 0.13, select speed in each corresponding channel. Please refer to Table 1 for the different combinations. 1 = 100 Mbps Mode 0 = 10 Mbps Mode
114 115 116 117	DPLX_[3:0]	I	**Duplex Selection Input.** These digital inputs, ORed with register bit 0.8, select the duplex mode in EACH corresponding channel. They control advertisement when ANEG is enabled. Please refer to Table 1 for the different combinations. 1 = Full Duplex Mode 0 = Half Duplex Mode
89	REPEATER	I	**Repeater Mode Enable Input.** This digital input, ORed with register bit 17.14, enables repeater mode for ALL channels. 1 = Repeater Mode Enabled 0 = Normal Operation
54	$\overline{\text{AD\_REV}}$	I Pullup	**Address Reverse Input.** 1 = Normal In this mode, physical ports 0-3 are mapped to MI addresses 0-3 in the same order. 0 = Reverse Address Mode Select In this mode, physical ports 0-3 are mapped to MI addresses 3-0 respectively. This is the reverse to the normal order.
120	$\overline{\text{RESET}}$	I Pullup	**Hardware Reset Input.** 1 = Normal 0 = Device In Reset State (Reset is complete 50 ms after $\overline{\text{RESET}}$ goes high).

Table 1. AutoNegotiation, Speed & Duplex Mode Combinations

Input Pins				Mode Selected			
Aneg	Speed[3:0]	Duplx [3:0]	Auto-neg	Forced Modes [Note 2]		Advertised Capabilities	
				Speed	DPLX	Speed	DPLX
0	0000	0000	Off	10	Half	na	na
0	0000	1111	Off	10	Full	na	na
0	1111	0000	Off	100	Half	na	na
0	1111	1111	Off	100	Full	na	na
1	0000	0000	On	na	na	10	Half
1	0000	1111	On	na	na	10	Half/Full
1	1111	0000	On	na	na	10/100	Half/Full[3]
1	1111	1111	On	na	na	10/100	Half

Note 1: The single ANEG pin applies to all four channels. The four Speed and DPLX apply to each individual channel. The pins above are shown for all four channels, but each channel can be individually configured for SPEED and DPLX by appropriately setting the pin for that channel.

Note 2: Forced Modes assume that registers 0 and 4 are at default values.

Note 3: the 84221 can be either controlled through the software or through the hardware. If the device needs to be controlled through the software (Registers 0 to 4), then these seven pins (ANEG, Speed[3:0] , Duplx[3:0]) have to be tied to their default values of 1, 1111, and 0000 respectively.

Table 1a. LED Definitions as per the LEDDEF pin

Name	Output State Description	LED tied to GND	LED tied to Vdd	LEDDEF
$\overline{\text{LED0}}$	0 = 100 Mbps Link Detected	Off	On	LEDDEF = 1
(10/100)	1 = 10 Mbps Link Detected	On	Off	
	Trisate = No Link	Off	Off	
$\overline{\text{LED1}}$	0 = Full Duplex Mode Detect with Link Pass	Off	On	
(Fdx/Hdx)	1 = Half Duplex Mode Detect with Link Pass	On	Off	
	Tristate = No Link	Off	Off	
$\overline{\text{LED2}}$ (Col)	0 = Collision Detect	Off	On	
	1 = No Collision	On	Off	
$\overline{\text{LED3}}$	0 = Link Detect	Off	On	
(Link + Act)	Blink = Link Detect + Activity	Blink	Blink	
	1 = No Link Detect or Activity	On	Off	

$\overline{\text{LED0}}$[1]	0 = 10 Mbps Link Detected	Off	On	LEDDEF = 0
(Link10)	1 = No 10 Mbps Link Detected	On	Off	
$\overline{\text{LED1}}$	0 = Full Duplex Mode Detect with Link Pass	Off	On	
(Fdx/Hdx)	1 = Half Duplex Mode Detect with Link Pass	On	Off	
	Tristate = No Link	Off	Off	
$\overline{\text{LED2}}$	Blink = Activity Occurred (Stretch pulse to 100 ms)	Off	On	
(Act)	1 = No Activity	On	Off	
$\overline{\text{LED3}}$	0 = Link100 Detected	Off	On	
	1 = No Link100	On	Off	
(Link100)	Detected			

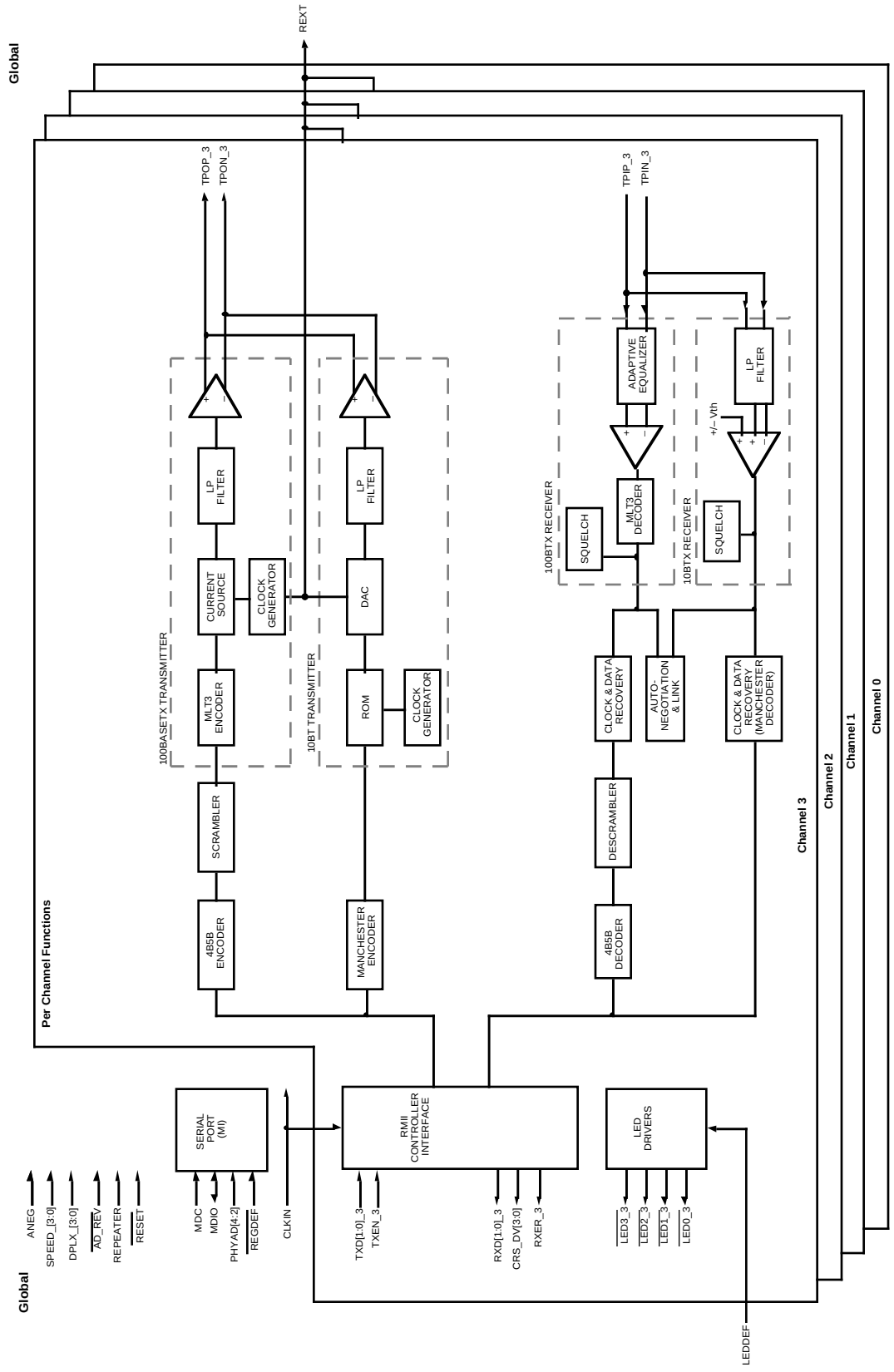


Figure 1. 84221 Block Diagram

2.0 Functional Description

2.1 GENERAL

The 84221 is a complete 10/100 Mbps Ethernet Media Interface IC. The 84221 has four separate and independent channels. Each channel has the following main sections: controller interface, encoder, decoder, scrambler, descrambler, clock and data recovery, twisted pair interface transmitter, twisted pair interface receiver, and auto negotiation. A Management Interface (MI) serial port, which provides access to eleven registers for each channel, is common to all four channels. Figure 1 shows the 84221 block diagram.

The 84221 can operate as a 100BaseTX device (100 Mbps mode) or as a 10BaseT device (10 Mbps mode). The 100 Mbps and 10 Mbps modes differ in data rate, signalling protocol, and allowed wiring as follows:

- *The 100 Mbps TX mode uses two pairs of category 5, or better, UTP or STP twisted pair cable with 4B5B encoded, scrambled, and MLT3 coded (ternary) 125 MHz data to achieve a throughput of 100 Mbps.*
- *The 10 Mbps mode uses two pairs of category 3, or better, UTP or STP twisted pair cable with Manchester encoded 10 MHz binary data to achieve a 10 Mbps thruput.*

The data symbol format on the fiber or twisted pair cable for the 100 and 10 Mbps modes is defined in IEEE 802.3 specifications and shown in Figure 2.

On the transmit side for 100 Mbps operation, data is received on the controller interface from an external Ethernet controller per the format shown in Figure 3. The data is sent to the encoder for formatting. For TX operation, the encoded data is sent to the scrambler. The encoded and scrambled data is then sent to the TX transmitter. The transmitter converts the encoded and scrambled data into MLT3 ternary format. The transmitter then preshapes the output and drives the twisted pair cable.

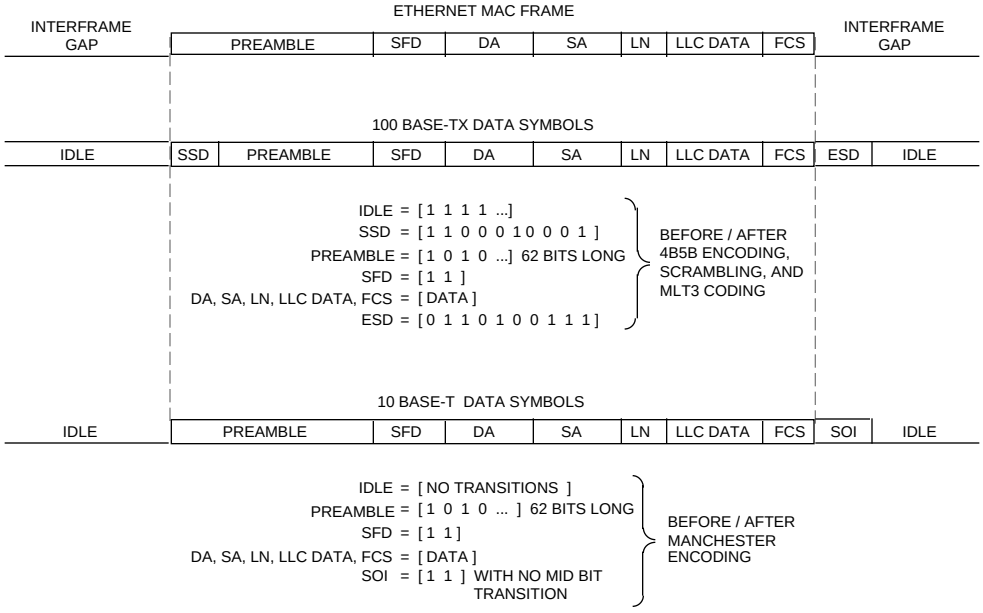


Figure 2. Frame Format

On the receive side for 100BaseTX operation, the TX receiver removes any high frequency noise from the input, equalizes the input signal to compensate for the low pass effects of the cable, and qualifies the data with a squelch algorithm. The TX receiver then converts the data from MLT3 coded twisted pair levels to internal digital levels. The output of the receiver then goes to a clock and data recovery block which recovers a clock from the incoming data, uses the clock to latch in valid data into the device, and converts the data back to NRZ data. The data is then unscrambled and decoded by the 4B5B decoder and descrambler, respectively, and output to an external Ethernet controller by the controller interface.

10 Mbps operation is similar to the 100 Mbps operation, except:

- *There is no scrambler/descrambler.*
- *The encoder/decoder is Manchester instead of 4B5B.*
- *The data rate is 10 Mbps instead of 100 Mbps.*
- *The twisted pair symbol data is two level Manchester instead of ternary MLT3.*

The AutoNegotiation block automatically configures each channel for either 100BaseTX or 10BaseT, and either Full or Half Duplex operation. This configuration is based on the capabilities selected for the channel and capabilities detected from the remote device connected to the channel.

The Management Interface (the MI serial port) is a two pin bidirectional link through which configuration inputs can be set and channel status outputs read.

Each block plus the operating modes are described in more detail in the following sections. Since the 84221 can operate as a 100BaseTX or a 10BaseT device, each of the following sections describes the performance in both 100 and 10 Mbps modes.

2.2 CONTROLLER INTERFACE (RMII)

2.2.1 General

The controller interface is the interface between the device and an external Ethernet Media Access Controller (MAC). The specific controller interface type implemented on the device is the Reduced Pin Count Media Independent Interface, also referred to as RMII. The RMII is a two bit wide packet data interface between an Ethernet PHY and MAC that was defined by an industry group, the RMII Consortium. The RMII is a reduced pin count version of the IEEE 802.3 MII. The 84221 meets all the RMII requirements outlined in the RMII Consortium specifications and can directly connect to any Ethernet controller that also complies with the RMII specifications.

2.2.2 100 Mbps

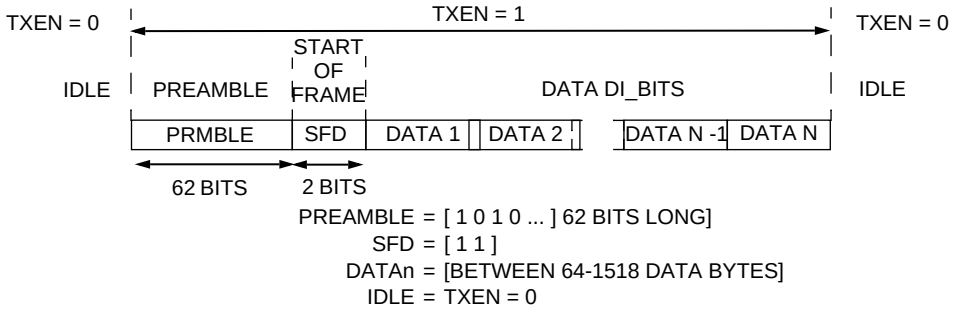
The RMII consists of eight signals: (1) two transmit data inputs (TXD[1:0]), (2) a transmit enable input (TXEN), (3) two receive data outputs (RXD[1:0]), (4) a carrier sense/ data valid input (CRS), (5) a receive data error input (RXER), and (6) global clock input (CLKIN). The global clock, CLKIN, is a common signal for all eight channels. All other signals are replicated for each channel. CLKIN operates at a frequency of 50 MHz.

Data in RMII is transmitted/received in 2-bit wide word, called di-bits, on TXD[1:0]/RXD[1:0], respectively. The RMII frame format and bit order is defined in the RMII Consortium specifications and is also shown in Figure 3.

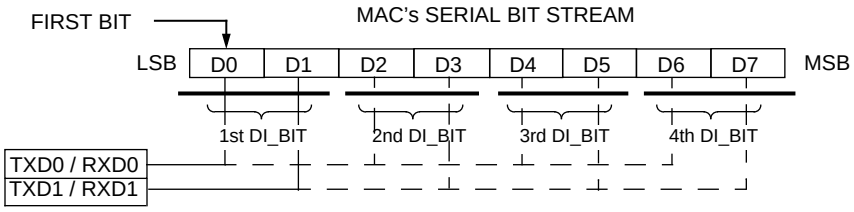
On the transmit side, the CLKIN input runs continuously at 50 MHz. When no data is to be transmitted, TXEN must be deasserted. While TXEN is deasserted, TXD[1:0] are ignored and no data is clocked into the device. When TXEN is asserted, it is clocked in on the rising edge of CLKIN along with the data on TXD[1:0]. TXD[1:0] input data is two bit wide packet data whose format needs to be the same as specified in the RMII Consortium specification and also shown in Figure 3. When all packets have been latched into the device, TXEN must be deasserted.

On the receive side, when no packets are being received, CRS is deasserted and RXD[1:0] is held low. When the start of packet is detected, CRS is asserted active high on the rising edge of CLKIN and RXD[1:0]=00 until the receive packet data is available to be output onto RXD[1:0]. When the packet data is available to be output, it is clocked out onto RXD[1:0] on rising edges of CLKIN while CRS still remains asserted high. When the end of packet is detected on the receive input, CRS toggles high and low at a 25 MHz rate until all of the packet data has been output onto the RXD[1:0] pins. Once all of the packet data has been output on RXD[1:0], then CRS is deasserted on rising edges of CLKIN. If dribble bits occur on the receive input, a non-integer number of data octets will be output on RXD[1:0]. If the device is in the Link Fail state, CRS always stays deasserted. The packet data on RXD[1:0] has the same frame structure and bit order as the TXD[1:0] data and is specified in the RMII Consortium specification and also shown in Figure 3.

An elastic buffer is present in the receive data path because the input receive data is referenced to the recovered clock and the receive data output on RXD0 has to be referenced to CLKIN. The receive buffer is 32 bits in length. Receive input data fills the elastic buffer to a predetermined threshold level before data is passed to the



a.) MAC Frame Format



b.) RMII DI_BIT Order

Signals	Bit Value																			
TXD0	X	X	1[1]	1	.	.	.	.	.	.	.	.	.	1[2]	1	1	1	D0[3]	D2	D4	D6
TXD1	X	X	0	0	.	.	.	.	.	.	.	.	.	0	0	0	1	D1	D3	D5	D7[4]
TXEN	0	0	1	1	.	.	.	.	.	.	.	.	.	1	1	1	1	1	1	1	1

1. 1st preamble di-bit transmitted.
2. 1st sfd di-bit transmitted.
3. 1st data di-bit transmitted.
4. D0 through D7 are the first 8 bits of the data field.

c.) Transmit Preamble and SFD Bits

Signals	Bit Value																			
RXD0	0	0	0	0	.	.	.	0	1[1]	1	.	.	.	.	1[2]	1	1	1	D0[3]	D3	D4	D6
RXD1	0	0	0	0	.	.	.	0	0	0	.	.	.	.	0	0	0	1	D1	D4	D5	D7[4]
CRS_DV	0	0	1	1	.	.	.	1	1	1	.	.	.	.	1	1	1	1	1	1	1	1

1. 1st preamble di-bit received. Device may eliminate either all or some of the preamble di-bit, up to 1st SFD.
2. 1st sfd di-bit received.
3. 1st data di-bit received.
4. D0 through D7 are the first 8 bits of the data field.

d.) Receive Preamble and SFD Bits

Figure 3. RMII Frame Format

RMII receive outputs. This predetermined threshold level can be configured to be either 4 bits or 16 bits by appropriately setting the receive buffer threshold select bit in the MI serial port Global Configuration register. If the elastic buffer underflows or overflows, RXER is asserted and RXD[1:0]=01 for all data bits from the underflow/overflow detect point until the end of the packet.

RXER is a receive error output that is asserted when certain errors are detected on the receive data. RXER is asserted on rising edge of CLKIN for all data bits of the packet starting from the RXER detect point until the end of the packet. In addition, any packet that contains an RXER will substitute RXD[1:0]=01 for all the data bits from the RXER detect point until the end of packet.

There is no collision indication for RMII. Collision can be sensed external to the device when both TXEN and CRS are asserted at the same time. Also, there is no internal TXEN loopback in RMII mode.

2.2.3 10 Mbps

10 Mbps RMII operation is identical to 100 Mbps RMII operation, except: (1) Each transmit data di-bit must be input on TXD[1:0] for ten consecutive CLKIN cycles, and (2) Each receive data di-bit will be output on RXD[1:0] for ten consecutive CLKIN cycles.

2.2.4 RMII Disable

The RMII inputs and outputs can be disabled by setting the MII disable bit in the MI serial port Control register. When the RMII is disabled, the inputs are ignored, the outputs are placed in high impedance state, and the TP output is high impedance.

2.3 ENCODER

2.3.1 4B5B Encoder - 100 Mbps

100BaseTX requires that this data be 4B5B encoded. 4B5B coding converts the 4 bit data nibbles into 5 bit data words. The mapping of the 4B nibbles to the 5B code words is specified in IEEE 802.3 and shown in Table 2. The 4B5B encoder on the 84221 takes 4B nibbles from the controller interface, converts them into 5B words according to, Table 2, and sends the 5B words to the scrambler. The 4B5B encoder also substitutes the first eight bits of the preamble with the SSD delimiters (/J/K/ symbols) and adds an ESD delimiter (/T/R/ symbols) to the end of each packet, as defined in IEEE 802.3 and shown in Figure 2. The 4B5B encoder also fills the period between packets, called the idle period, with a continuous stream of idle symbols, as shown in Figure 2.

Table 2. 4B/5B Symbol Mapping

Symbol Name	Description	5B Code	4B Code
0	Data 0	11110	0000
1	Data 1	01001	0001
2	Data 2	10100	0010
3	Data 3	10101	0011
4	Data 4	01010	0100
5	Data 5	01011	0101
6	Data 6	01110	0110
7	Data 7	01111	0111
8	Data 8	10010	1000
9	Data 9	10011	1001
A	Data A	10110	1010
B	Data B	10111	1011
C	Data C	11010	1100
D	Data D	11011	1101
E	Data E	11100	1110
F	Data F	11101	1111
I	Idle	11111	0000
J	SSD #1	11000	0101
K	SSD #2	10001	0101
T	ESD #1	01101	0000
R	ESD #2	00111	0000
H	Halt	00100	Undefined
---	Invalid codes	All others*	0000*

* These 5B codes are not used. For decoder, these 5B codes are decoded to 4B 0000. For encoder, 4B 0000 is encoded to 5B 11110, as shown in symbol 0.

2.3.2 Manchester Encoder - 10 Mbps

The Manchester encoding process combines clock and NRZ data such that the first half of the data bit contains the complement of the data, and the second half of the data bit contains the true data, as specified in IEEE 802.3. This guarantees that a transition always occurs in the middle of the bit cell. The 84221 Manchester encoder converts the 10 Mbps NRZ data from the controller interface into a single data stream for the TP transmitter and adds a start of idle pulse (SOI) at the end of the packet as specified in IEEE 802.3 and shown in Figure 2.

The Manchester encoding process is only done on actual packet data, and the idle period between packets is not Manchester encoded, but filled with link pulses.

2.4 DECODER

2.4.1 4B5B Decoder - 100 Mbps

Since the TX input data is 4B5B encoded on the transmit side, it must also be decoded by the 4B5B decoder on the receive side. The mapping of the 5B nibbles to the 4B code words is specified in IEEE 802.3 and shown in Table 2. The 84221 4B5B decoder takes the 5B code words from the descrambler, converts them into 4B nibbles per Table 2, and sends the 4B nibbles to the RMII controller interface. The 4B5B decoder also strips off the SSD delimiter (/J/K/ symbols) and replaces them with two 4B Data 5 nibbles (/5/ symbol), and strips off the ESD delimiter (/T/R/ symbols) and replaces it with two 4B Data 0 nibbles (/I/ symbol), per IEEE 802.3 specifications and shown in Figure 2.

The 4B5B decoder detects SSD, ESD and, codeword errors in the incoming data stream as specified in IEEE 802.3. These errors are indicated by asserting RXER output while the errors are being transmitted across RXD[1:0].

2.4.2 Manchester Decoder - 10 Mbps

In Manchester coded data, the first half of the data bit contains the complement of the data, and the second half of the data bit contains the true data. The 84221 Manchester decoder converts the single data stream from the TP receiver into NRZ data for the controller interface by decoding the data and stripping off the SOI pulse. Since the clock and data recovery block has already separated the clock and data from the TP receiver, the Manchester decoding process to NRZ data is inherently performed by that block.

2.5 CLOCK AND DATA RECOVERY

2.5.1 Clock Recovery - 100 Mbps

Clock recovery is done with a PLL. If there is no valid data present on the receive inputs, the PLL is locked to the CLKIN clock. When valid data is detected on the receive inputs with the squelch circuit and when the adaptive equalizer has settled, the PLL input is switched to the incoming data stream. The PLL then recovers a clock by locking onto the transitions of the incoming signal. The recovered clock is output to the Controller Interface block.

2.5.2 Data Recovery - 100 Mbps

Data recovery is performed by latching in data from the receive inputs with the recovered clock extracted by the PLL.

2.5.3 Clock Recovery - 10 Mbps

The clock recovery process for 10 Mbps mode is identical to the 100 Mbps mode, except:

- *The PLL is switched from CLKIN to the TP input when the squelch indicates valid data.*
- *The PLL locks onto the preamble signal in less than 12 transitions (bit times).*
- *Some of the preamble data symbols are lost while the PLL is locking onto the preamble, however, the data receiver block recovers enough preamble symbols to pass at least 3 bytes of preamble to the controller interface as shown in Figure 3.*

2.5.4 Data Recovery

The data recovery process for 10 Mbps mode is identical to the 100 Mbps mode.

2.6 SCRAMBLER

2.6.1 100 Mbps

100BaseTX requires scrambling to reduce the radiated emmisions on the twisted pair. The 84221 scrambler takes the encoded data from the 4B5B encoder, scrambles it per the IEEE 802.3 specifications, and sends it to the TP transmitter. The scrambler circuitry of the 84221 is designed so that none of the individual scrambler sections on-chip will be synchronous with the others to minimize EMI issues.

2.6.2 10 Mbps

A scrambler is not used in 10 Mbps mode.

2.7 DESCRAMBLER

2.7.1 100 Mbps

The 84221 descrambler takes the scrambled data from the data recovery block, descrambles it per the IEEE 802.3 specifications, aligns the data on the correct 5B word boundaries, and sends it to the 4B5B decoder.

The algorithm for synchronization of the descrambler is the same as the algorithm outlined in the IEEE 802.3 specification. Once the descrambler is synchronized, it will maintain synchronization as long as enough descrambled idle pattern 1's are detected within a given interval. To stay in synchronization, the descrambler needs to detect at least 25 consecutive descrambled idle pattern 1's in a 1 mS interval. If 25 consecutive descrambled idle pattern 1's are not detected within the 1 mS interval, the descrambler goes out of synchronization and restarts the synchronization process.

2.7.2 10 Mbps

A descrambler is not used in 10 Mbps mode.

2.8 TWISTED PAIR TRANSMITTER

2.8.1 100 Mbps

The TP transmitter consists of an MLT3 encoder, waveform generator and line driver.

The MLT3 encoder converts the NRZI data from the scrambler into a three level code required by IEEE 802.3. MLT3 coding uses three levels and converts 1's to transitions between the three levels, and converts 0's to no transitions or changes in level.

The purpose of the waveform generator is to shape the transmit output pulse. The waveform generator takes the MLT3 three level encoded waveform and uses an array of switched current sources to control the shape of the twisted pair output signal in order to meet IEEE 802.3 requirements. The output of the switched current sources then goes through a low pass filter in order to "smooth" the output and remove any high frequency components. In this way, the waveform generator preshapes the output waveform transmitted onto the twisted pair cable to meet the pulse template requirements outlined in IEEE 802.3. The waveform generator eliminates the need for any external filters on the TP transmit output. The line driver converts the shaped and smoothed waveform to a current output that can drive 100 meters of category 5 unshielded twisted pair cable or 150 ohm shielded twisted pair cable.

2.8.2 10 Mbps

The TP transmitter operation in 10 Mbps mode is much different than the 100 Mbps transmitter. Even so, the transmitter still consists of a waveform generator and line driver.

The purpose of the waveform generator is to shape the output transmit pulse. The waveform generator consists of a ROM, DAC, clock generator, and filter. The DAC generates a stair-stepped representation of the desired output waveform. The stairstepped DAC output then goes through a low pass filter in order to "smooth" the DAC output and remove any high frequency components. The DAC values are determined from the ROM output; the ROM outputs are chosen to shape the pulse to the desired template and are clocked into the DAC at high speed by the clock generator. In this way, the waveform generator preshapes the output waveform to be transmitted onto the twisted pair cable to meet the pulse template requirements outlined in IEEE 802.3 Clause 14 and also shown in Figure 4. The waveshaper replaces and eliminates external filters on the TP transmit output.

The line driver converts the shaped and smoothed waveform to a current output that can drive 100 meters of category 3/4/5 100 Ohm unshielded twisted pair cable or 150 Ohm shielded twisted pair cable, without any external filters. During the idle period, no output signal is transmitted on the TP outputs (except link pulse).

2.9 TWISTED PAIR RECEIVER

2.9.1 Receiver - 100 Mbps

The TP receiver detects input signals from the twisted pair input and converts it to a digital data bit stream ready for clock and data recovery. The receiver can reliably detect data from a 100Base-TX compliant transmitter that has been passed through 0-100 meters of 100 Ohm category 5 UTP.

The 100 Mbps receiver consists of an adaptive equalizer, baseline wander correction circuit, comparators, and MLT-3 decoder. The TP inputs first go to an adaptive equalizer. The adaptive equalizer compensates for the low pass characteristic of the cable, and it has the ability to adapt and compensate for 0-100 meters of category 5, 100 Ohm UTP. The baseline wander correction circuit restores the DC component of the input waveform that was removed by external transformers. The comparators convert the equalized signal back to digital levels and are used to qualify the data with the squelch circuit. The MLT-3 decoder takes the three level MLT-3 digital data from the comparators and converts it back to normal digital data to be used for clock and data recovery.

2.9.2 Receiver - 10 Mbps

The 10 Mbps mode receiver is much simpler than the 100 Mbps mode receiver and is identical to the 100 Mbps receiver except:

- *The adaptive equalizer is disabled and bypassed.*
- *The baseline wander correction circuit is disabled.*
- *The 10 Mbps receiver is able to detect input signals from the twisted pair cable that are within the template specified in IEEE 802.3 Clause 14 and shown in Figure 5.*
- *The output of the squelch comparator is used for squelch, link pulse detect, SOI detect, reverse polarity detect.*
- *The data comparator is a zero crossing comparator whose output is used for clock and data recovery.*

2.9.3 Squelch - 100 Mbps

The squelch block determines whether the input contains valid data. The 100 Mbps TX squelch is one of the criteria used to determine link intergrity. The squelch comparators compare the TX inputs against fixed positive and negative thresholds, called squelch levels.

The output from the squelch comparator goes to a digital squelch circuit, which determines whether the receive input data on that channel is valid. If the data is invalid, the receiver is in the squelched state. If the input voltage exceeds the squelch levels at least four times with alternating polarity within a 10 uS interval, the data is considered to be valid by the squelch circuit and the receiver now enters into the unsquelch state.

In the unsquelch state, the receive threshold level is reduced by approximately 30% for noise immunity reasons and is called the unsquelch level. When the receiver is in the unsquelch state the input signal is considered valid.

The device stays in the unsquelch state until loss of data is detected. Loss of data is detected if no alternating polarity unsquelch transitions are detected during any 10 uS interval. When the loss of data is detected, the receive squelch level is re-established.

2.9.4 Squelch - 10 Mbps

The TP squelch algorithm for 10 Mbps mode is identical to the 100 Mbps mode, except:

- *The 10 Mbps squelch algorithm is not used for link integrity, but to sense the beginning of a packet.*
- *The receiver goes into the unsquelch state if the input voltage exceeds the squelch levels for three bit times with alternating polarity within a 50-250 nS interval.*
- *The receiver goes into the squelch state when SOI is detected.*
- *Unsquelch detection has no affect on link integrity, link pulses are used for that in 10 Mbps mode.*
- *Start of packet is determined when the receiver goes into the unsquelch state and CRS is asserted.*
- *The receiver meets the squelch requirements defined in IEEE 802.3 Clause 14.*

2.9.5 Receive Level Adjust

The receiver squelch and unsquelch levels can be lowered by 4.5 dB by setting the receive level adjust bit in the MI serial port Channel Configuration register. By setting this bit, the device can support cable lengths exceeding 100 meters.

2.10 COLLISION

The collision function is not present in the 84221. The MAC should be able to reliably detect collision based on the TXEN and CRS_DV signals.

2.11 START OF PACKET

2.11.1 100 Mbps

Start of packet for 100 Mbps mode is indicated by a unique Start of Stream Delimiter (SSD). The SSD pattern consists of the two /J/K/ 5B symbols inserted at the beginning of the packet in place of the first two preamble symbols, as defined in IEEE 802.3 Clause 24 and shown in Table 2 and Figure 2.

The transmit SSD is generated by the 4B5B encoder and the /J/K/ symbols are inserted by the 4B5B encoder at the beginning of the transmit data packet in place of the first two 5B symbols of the preamble, as shown in Figure 2.

The receive pattern is detected by the 4B5B decoder by examining groups of 10 consecutive code bits (two 5B words) from the descrambler. Between packets, the receiver will be detecting the idle pattern, which is 5B /I/ symbols. While in the idle state, CRS_DV is deasserted.

If the receiver is in the idle state and 10 consecutive code bits from the receiver consist of the /J/K/ symbols, the start of packet is detected, data reception is begun, CRS_DV is asserted, and /5/5/ symbols are substituted in place of the /J/K/ symbols.

If the receiver is in the idle state and 10 consecutive code bits from the receiver consist of a pattern that is neither /I/ I/ nor /J/K/ symbols but contains at least 2 non-contiguous 0's, then activity is detected but the start of packet is considered to be faulty and a False Carrier Indication (also referred to as bad SSD) is signalled to the controller interface. When False Carrier is detected while CRS_DV is asserted, RXD[1:0]=11, 10 for two di-bits while RXER is asserted. Once a False Carrier Event is detected, the idle pattern (two /I/I/ symbols) must be detected before any new SSD's can be sensed.

If the receiver is in the idle state and 10 consecutive code bits from the receiver consist of a pattern that is neither /I/ I/ nor /J/K/ symbols but does not contain at least 2 non contiguous 0's, the data is ignored and the receiver stays in the idle state.

2.11.2 10 Mbps

Since the idle period in 10 Mbps mode is defined to be no data on the TP inputs, then the start of packet for 10 Mbps mode is detected when valid data is detected by the TP squelch circuit. When start of packet is detected, CRS is asserted as described in the Controller Interface Section. Refer to the TP Squelch - 10 Mbps Section for the algorithm for valid data detection.

2.12 END OF PACKET

2.12.1 100 Mbps

End of packet for 100 Mbps mode is indicated by an End of Stream Delimiter (referred to as ESD). The ESD pattern consists of the two /T/R/ 4B5B symbols inserted after the end of the packet, as defined in IEEE 802.3 Clause 24 and shown in Table 2 and Figure 2.

The transmit ESD is generated by the 4B5B encoder and the /T/R/ symbols are inserted by the 4B5B encoder after the end of the transmit data packet, as shown in Figure 2.

The receive ESD pattern is detected by the 4B5B decoder by examining groups of 10 consecutive code bits (two 5B words) from the descrambler during valid packet reception to determine whether there is an ESD.

If the 10 consecutive code bits from the receiver during valid packet reception consist of the /T/R/ symbols, the end of packet is detected, data reception is terminated, CRS_DV is deasserted, and /I/I/ symbols are substituted in place of the /T/R/ symbols.

If 10 consecutive code bits from the receiver during valid packet reception do not consist of /T/R/ symbols, but consist of /I/I/ symbols instead, the packet is considered to have been terminated prematurely and abnormally. When this premature end of packet condition is detected, RXER remains asserted for the nibble associated with the first /I/ symbol detected and then RXER and CRS_DV are all deasserted.

2.12.2 10 Mbps

The end of packet for 10 Mbps mode is indicated with the SOI (Start of Idle) pulse. The SOI pulse is a positive double wide pulse containing a Manchester code violation inserted at the end of every packet.

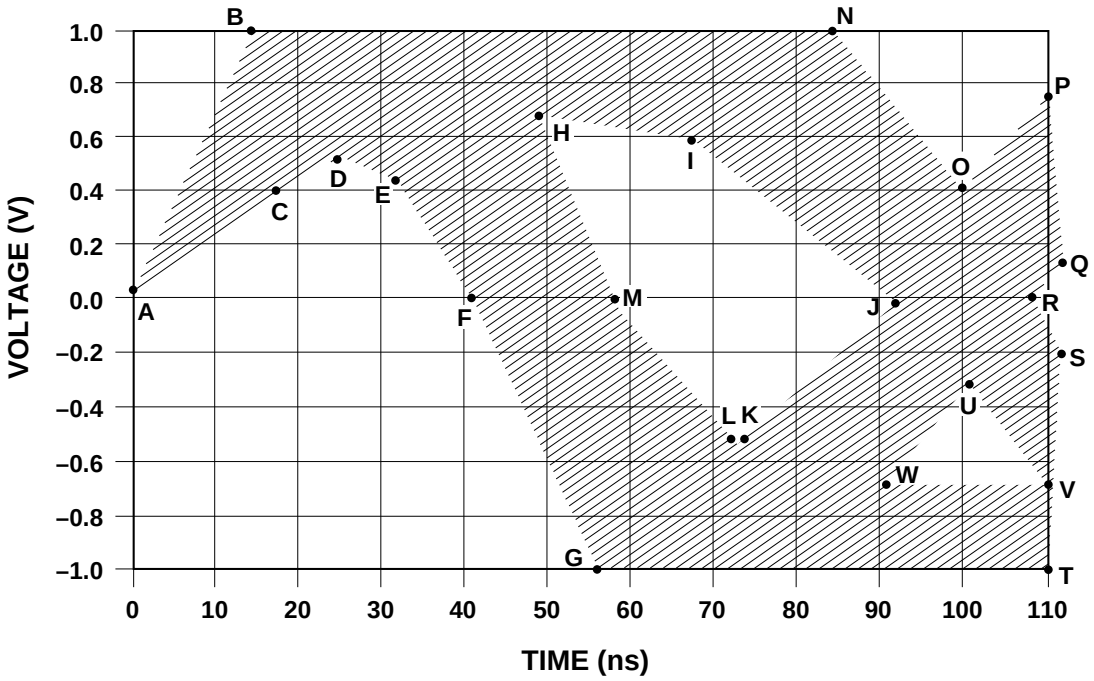
The transmit SOI pulse is generated by the TP transmitter and inserted at the end of the data packet after TXEN is deasserted. The transmitted SOI output pulse at the TP output is shaped by the transmit waveshaper to meet the pulse template requirements specified in IEEE 802.3 Clause 14 and shown in Figure 6.

The receive SOI pulse is detected by the TP receiver by sensing missing data transitions. Once the SOI pulse is detected, data reception is ended and CRS and RXDV are deasserted.

2.13 LINK INTEGRITY & AUTONEGOTIATION

2.13.1 General

The 84221 can be configured to implement either the standard link integrity algorithms or the AutoNegotiation algorithm.



Reference	Time (ns) Internal MAU	Voltage (V)
A	0	0
B	15	1.0
C	15	0.4
D	25	0.55
E	32	0.45
F	39	0
G	57	-1.0
H	48	0.7
I	67	0.6
J	89	0
K	74	-0.55
L	73	-0.55
M	61	0
N	85	1.0
O	100	0.4
P	110	0.75
Q	111	0.15
R	111	0
S	111	-0.15
T	110	-1.0
U	100	-0.3
V	110	-0.7
W	90	-0.7

Figure 4. TP Output Voltage Template - 10 Mbps

The standard link integrity algorithms are used solely to establish an active link to and from a remote device. There are different standard link integrity algorithms for 10 and 100 Mbps modes. The AutoNegotiation algorithm is used for two purposes:

- *To automatically configure the device for either 10/100 Mbps and Half/Full Duplex modes*
- *Establish an active link to and from a remote device*

The standard link integrity and AutoNegotiation algorithms are described below.

2.13.2 10Base-T Link Integrity Algorithm

The 84221 uses the same 10Base-T link integrity algorithm that is defined in IEEE 802.3 clause 14. This algorithm uses normal link pulses, referred to as NLP's and transmitted during idle periods, to determine if a device has successfully established a link with a remote device (called Link Pass state). The transmit link pulse meets the template defined in IEEE 802.3 Clause 14 and shown in Figure 7. Refer to IEEE 802.3 Clause 14 for more details if needed.

2.13.3 100Base-TX Link Integrity Algorithm

Since 100Base-TX is defined to have an active idle signal, then there is no need to have separate link pulses like those defined for 10Base-T. The 84221 uses the squelch criteria and descrambler synchronization algorithm on the input data to determine if the device has successfully established a link with a remote device (called Link Pass state). Refer to IEEE 802.3 for details on both algorithms.

2.13.4 AutoNegotiation Algorithm

As stated previously, the AutoNegotiation algorithm is used for two purposes:

- *To automatically configure the device for either 10/100 Mbps and Half/Full Duplex modes*
- *To establish an active link to and from a remote device*

The AutoNegotiation algorithm is the same algorithm that is defined in IEEE 802.3 Clause 28. AutoNegotiation uses a burst of link pulses, called fast link pulses and referred to as FLP's, to pass up to 16 bits of signaling back and forth between the 84221 and a remote device. The transmit

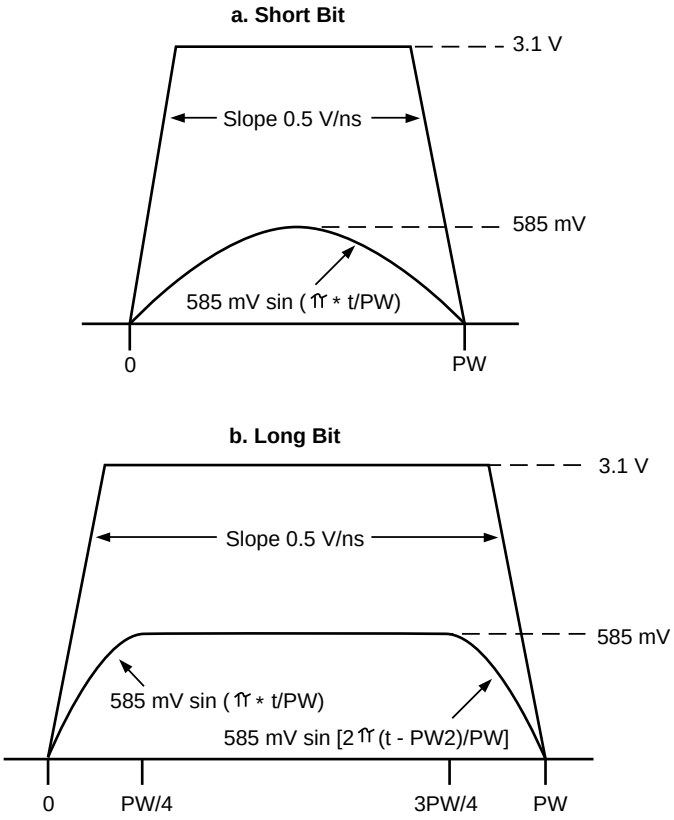


Figure 5. TP Input Voltage Template - 10 Mbps

FLP pulses meet the template specified in IEEE 802.3 and shown in Figure 7. A timing diagram contrasting NLP's and FLP's is shown in Figure 8.

The AutoNegotiation algorithm is initiated by any of the following events:

- *Powerup*
- *Device Reset*
- *AutoNegotiation Reset*
- *Entering the Link Fail state*

Once a negotiation has been initiated, the 84221 first determines if the remote device has AutoNegotiation capability. If the device is not AutoNegotiation capable and is just transmitting either a 10Base-T or 100Base-TX signal, the 84221 will sense that and place itself in the correct mode. If the 84221 detects FLP's from the remote device, then the remote device is determined to have AutoNegotiation capability and the device then uses the contents of the MI serial port AutoNegotiation Advertisement register and FLP's to advertise it's capabilities to a remote device. The remote device does the same, and the capabilities read back from the remote device are stored in the MI serial port AutoNegotiation Remote End Capability register. The 84221 negotiation algorithm then matches it's capabilities to the remote devices capabilities and determines to what mode the device should be configured according to the priority resolution algorithm defined in IEEE 802.3 Clause 28. Once the negotiation process is completed, the 84221 then configures itself for either 10 or 100 Mbps mode and either Full or Half Duplex modes (depending on the outcome of the negotiation process), and it switches to either the 100Base-TX or 10Base-T link integrity algorithms (depending on which mode was enabled by AutoNegotiation). Refer to IEEE 802.3 Clause 28 for more details.

2.13.5 AutoNegotiation Outcome Indication

The outcome or result of the AutoNegotiation process is stored in the speed detect and duplex detect bits in the MI serial port Status Output register.

2.13.6 AutoNegotiation Status

The status of the AutoNegotiation process can be monitored by reading the AutoNegotiation Acknowledgement Bit in the MI serial port Status register.

2.13.7 AutoNegotiation Enable

The AutoNegotiation algorithm can be enabled (or restarted) by setting the AutoNegotiation enable bit in the MI serial port Control register or by asserting the ANEG pin. The AutoNegotiatiopn enable bit and ANEG pin both have to be high to enable AutoNegotiation. When the AutoNegotiation algorithm is enabled, the device halts all transmissions including link pulses for 1200-1500 mS, enters the Link Fail state, and restarts the negotiation process. When the AutoNegotiation algorithm is disabled, the selection of 100 Mbps or 10 Mbps mode is determined by the speed select bit in the MI serial port Control register, and the selection of Half or Full Duplex is determined by the duplex select bit in the MI serial port Control register.

2.13.8 AutoNegotiation Reset

The AutoNegotiation algorithm can be initiated at any time by setting the AutoNegotiation reset bit in the MI serial port Control register.

2.13.9 Link Indication

Receive link detect activity can be monitored through the link detect bit in the MI serial port Status and Status Output registers or it can also be programmed to appear on LED status pins by appropriately setting the programmable LED select bits in the MI serial port Configuration 2 register as shown in Table 3. Whenever the LED Status pins are programmed to be a link detect output, these pins are asserted low whenever the device is in the Link Pass state.

2.13.10 Link Disable

The link integrity function can be disabled by setting the link disable bit in the MI serial port Configuration 1 register. When the link integrity function is disabled, the device is forced into the Link Pass state, configures itself for Half/Full Duplex based on the value of the duplex bit in the MI serial port Control register, configures itself for 100/10 Mbps operation based on the values of the speed bit in the MI serial port Control register, and continues to transmit NLP's or TX idle patterns, depending on whether the device is in 10 or 100 Mbps mode.

2.14 JABBER

2.14.1 100 Mbps

The jabber function is disabled in the 100 Mbps mode.

2.14.2 10 Mbps

A jabber condition occurs when the transmit packet exceeds a predetermined length. When jabber is detected, the TP transmit outputs are forced to the idle state, collision is asserted, and jabber register bits in the MI serial port Status and Channel Status Output registers are set.

2.15 RECEIVE POLARITY CORRECTION

2.15.1 100 Mbps

No polarity detection or correction is needed in 100 Mbps mode.

2.15.2 10 Mbps

The polarity of the signal on the TP receive input is continuously monitored. If one SOI pulse indicates incorrect polarity on the TP receive input, the polarity is internally determined to be incorrect, and the reverse polarity bit is set in the MI serial port Channel Status Output register.

The 84221 will automatically correct for the reverse polarity condition provided that the autopolarity feature is not disabled.

2.16 FULL DUPLEX MODE

2.16.1 100 Mbps

Full Duplex mode allows transmission and reception to occur simultaneously.

The device can be either forced into Half or Full Duplex mode, or the device can detect either Half or Full Duplex capability from a remote device and automatically place itself in the correct mode.

Each channel can be forced into the Full or Half Duplex modes by either setting the duplex bit in the MI serial port Control register or asserting the DPLX pin for the corresponding channel with AutoNegotiation disabled.

The device can automatically configure itself for Full or Half Duplex modes by using the AutoNegotiation algorithm to advertise and detect Full and Half Duplex capabilities to and from a remote terminal. For detailed information, refer to the LINK INTEGRITY & AUTONEGOTIATION Section.

2.16.2 10 Mbps

Full Duplex in 10 Mbps mode is identical to the 100 Mbps mode.

2.16.3 Full Duplex Indication

Full Duplex detect activity can be monitored through the duplex detect bit in the MI serial port Channel Status Output register.

Full Duplex detect activity also appears on the $\overline{LED1}$ pin by default.

2.17 10/100 MBPS SELECTION

2.17.1 General

The device can be forced into either the 100 or 10 Mbps mode, or the device can detect 100 or 10 Mbps capability from a remote device and automatically place itself in the correct mode.

The device can be forced into either the 100 or 10 Mbps mode by either setting the speed select bit in the MI serial port Control register or by setting the SPEED pin with AutoNegotiation disabled. Both the speed select bit and SPEED pin need to be set to the same speed (10 or 100) for the device to be properly configured. The speed select bit and SPEED pin are ignored if AutoNegotiation is enabled.

The device can automatically configure itself for 100 or 10 Mbps mode by using the AutoNegotiation algorithm to advertise and detect 100 and 10 Mbps capabilities to and from a remote device. Refer to the LINK INTEGRITY & AUTONEGOTIATION Section for more details on AutoNegotiation.

2.17.2 10/100 MBPS Indication

The device speed (100/10 Mbps) can be monitored through the speed bit in the MI serial port Channel Status Output register.

2.18 RESET

The 84221 is reset when either:

(1) VDD is applied to the device,

(2) the reset bit is set in the MI serial port Control register, or

(3) the $\overline{RESET}$ pin is asserted active low.

When the reset is initiated by either (1) or (2), an internal power-on reset pulse is generated which resets all internal circuits, forces the MI serial port bits to their default values, and latches in new values for the MI address. After the power-on reset pulse has finished, the reset bit in the MI serial port Control register is cleared and the device is ready for normal operation. The device is guaranteed to be ready for normal operation 50 mS after the reset was initiated.

When the reset is initiated by (3), the identical procedure takes place as in (1) and (2), except the device stays in reset until the $\overline{RESET}$ pin is deasserted high.

2.19 POWERDOWN

The 84221 can be powered down by setting the powerdown bit in the MI serial port Control register. In powerdown mode, the TP outputs are in high impedance state, all functions are disabled except the MI serial port, and the power consumption is reduced to a minimum. The device will be ready for normal operation 50 mS after powerdown is deasserted.

2.20 CLOCK

The 84221 requires a 50 MHz reference frequency for internal signal generation in RMII mode. This reference frequency must be applied to the CLKIN pin.

2.21 LED DRIVERS

The $\overline{LED[3:0]}$ outputs can drive LED's tied to either VDD or GND. The LED definitions assume that the LED outputs are active low. If the LED Anodes are tied to the positive power supply (through limiting resistors), the LED will indicate the event as shown in Table 3. If the LED Cathodes are tied to ground and the Anodes to the 84221 Driver output, they will indicate the respective complementary events.

The LED[3:0] outputs can also drive other digital inputs.

Table 3. LED Function Definition

LEDDEF	LED3	LED2	LED1	LED0
1	LINK + ACT	COL	FDX	10/100
0	LINK 100	ACT	FDX	LINK10

Notes:
Default = 000 When pin LEDDEF = 0

Table 4. LED Event Definition

Symbol	Definition
ACT	Activity Occurred, Stretch Pulse to 100 mS
COL	Collision Occurred, Stretch Pulse to 100 mS
LINK100	100 Mb Link Detected
LINK10	10 Mb Link Detected
LINK	100 Mb or 10 Mb Link Detected
LINK+ACT	LED on if Link Detected (10 or 100). LED Blinks if Activity Determined, Stretch Pulse to 100 mS
FDX	Full Duplex Mode Detected with Link Pass
10/100	10 Mb Mode Enabled (High) or 100 Mb Mode Enabled (Low) with Link Pass

2.22 REPEATER MODE

The 84221 has one predefined repeater mode which can be enabled by asserting the REPEATER pin.

2.23 MI SERIAL PORT

2.23.1 Signal Description

The MI serial port has five pins, MDC, MDIO, and PHYAD[4:2]. MDC is the serial shift clock input. MDIO is a bidirectional data I/O pin. PHYAD[4:2] are physical address pins.

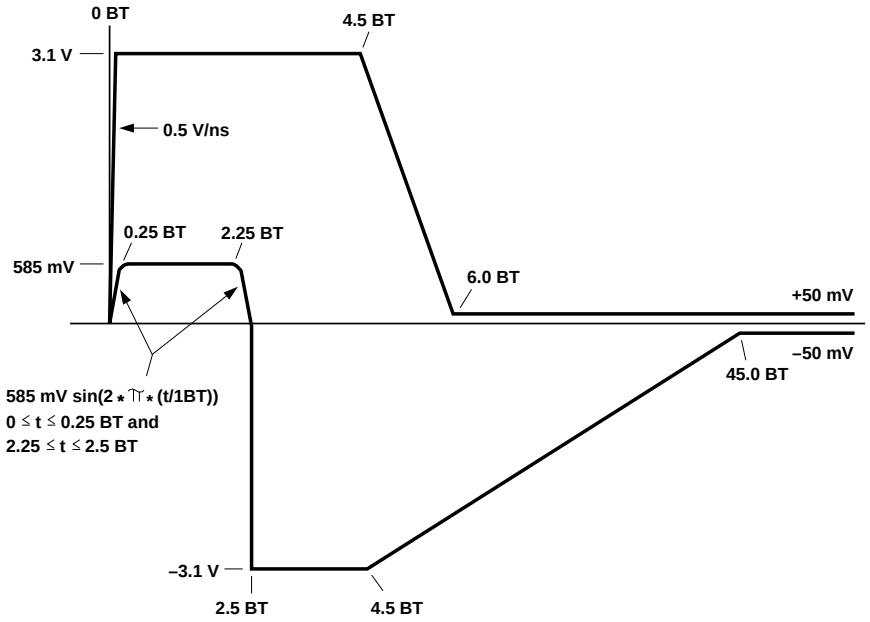


Figure 6. SOI Output Voltage Template - 10 Mbps

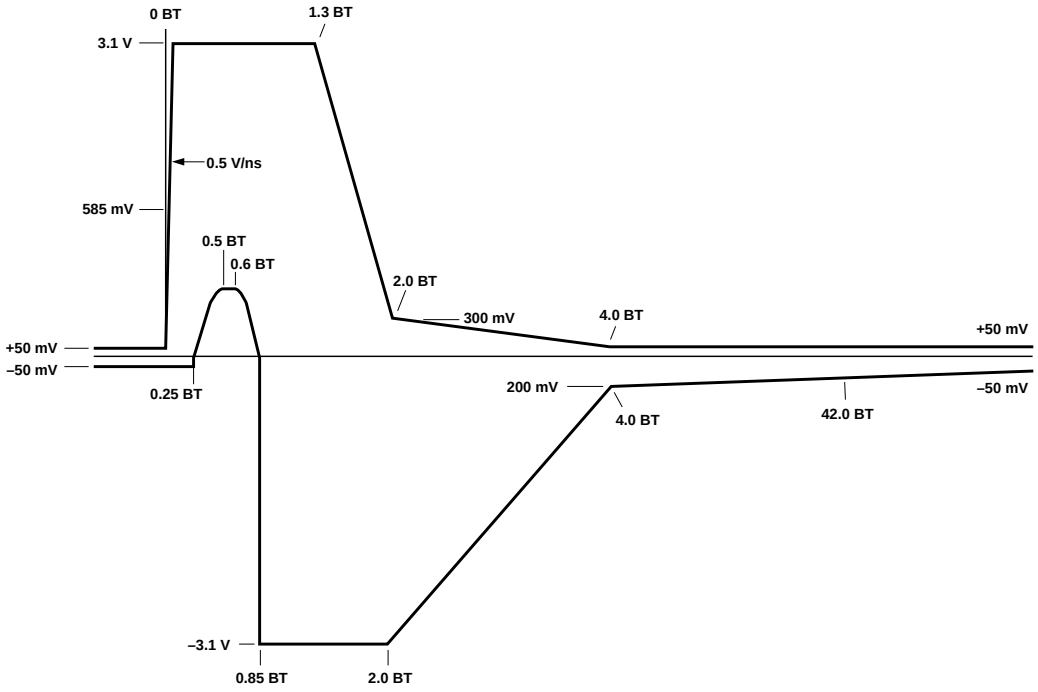


Figure 7. Link Pulse Output Voltage Template - 10 Mbps

Pins PHYAD[4:2] set the three most significant bits of the PHY address. The two least significant bits of the PHY address are set internally to match the channel number, as shown in Table 5.

Table 5. PHYAD[1:0] Settings

	PHYAD1	PHYAD0
Channel 3	1	1
Channel 2	1	0
Channel 1	0	1
Channel 0	0	0

2.23.2 Timing

Figure 10 shows a timing diagram for a MI serial port cycle.

The MI serial port is idle when at least 32 continuous 1's are detected on MDIO and remains idle as long as continuous 1's are detected. During idle, MDIO is in the high impedance state. When the MI serial port is in the idle state, a 01 pattern on the MDIO pin initiates a serial shift cycle. Data on MDIO is then shifted in on the next 14 rising edges of MDC (MDIO is high impedance). If the register access mode is not enabled, on the next 16 rising edges of MDC, data is either shifted in or out on MDIO, depending on whether a write or read cycle was selected with the bits READ and WRITE. After the 32 MDC cycles have been completed, one complete register has been read/written, the serial shift process is halted, data is latched into the device, and MDIO goes into high impedance state. Another serial shift cycle cannot be initiated until the idle condition (at least 32 continuous 1's) is detected.

2.23.3 Bit Types

Since the serial port is bidirectional, there are many types of bits. The bit type definitions are summarized in Table 6.

Write bits (W) are inputs during a write cycle and are high impedance during a read cycle. Read bits (R) are outputs during a read cycle and high impedance during a write cycle. Read/Write bits (R/W) are actually write bits that

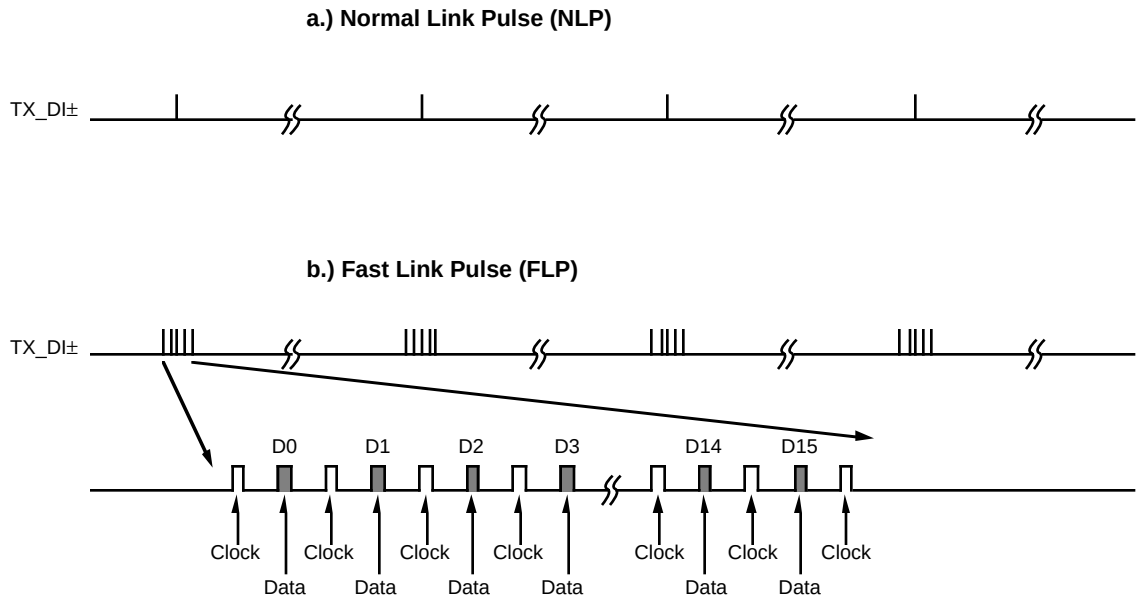


Figure 8. NLP vs. FLP Link Pulse

can be read out during a read cycle. R/WSC bits are R/W bits that are self clearing after a set period of time or after a specific event has completed. R/LL bits are read bits that latch themselves when they go low, and they stay latched low until read. After they are read, they are reset high. R/LH bits are the same as R/LL bits, except that they latch high. R/LT are read bits that latch themselves whenever they make a transition or change value, and they stay latched until they are read. After R/LT bits are read, they are updated to their current value. The R/LT bits can also be programmed to assert the interrupt function as described in the Interrupt section.

Table 6. MI Register Bit Type Definition

Symbol	Name	Definition	
		Write Cycle	Read Cycle
W	Write	Input	No Operation, Hi Z
R	Read	No Operation, Hi Z	Output
R/W	Read/Write	Input	Output
R/WSC	Read/Write Self Clearing	Input Clears Itself After Operation Completed	Output
R/LL	Read/Latching Low	No Operation, Hi Z	Output When Bit Goes Low, Bit Latched. When Bit Is Read, Bit Updated.
R/LH	Read/Latching High	No Operation, Hi Z	Output When Bit Goes High, Bit Latched. When Bit Is Read, Bit Updated.
R/LT	Read/Latching on Transition	No Operation, Hi Z	Output When Bit Transitions, Bit Latched And Interrupt Set When Bit Is Read, Interrupt Cleared And Bit Updated.

2.23.4 Frame Structure

The structure of the serial port frame is shown in Table 7 and a timing diagram is shown in Figure 10. Each serial port access cycle consists of 32 bits (or 720 bits if multiple register access is enabled and REGAD[4:0]=11111), exclusive of idle. The first 16 bits of the serial port cycle are always write bits and are used for addressing. The last 16/704 bits are from one/all of the 4 x 11 data registers.

The first 2 bits in Table 7 and Figure 10 are start bits and need to be written as a 01 for the serial port cycle to continue. The next 2 bits are read and write bits which determine whether the accessed data register bits will be read or write. The next 5 bits are device addresses. The 3 most significant bits must match the values on pins PHYAD[4:2] and the 2 least significant bits select one of four channels for access. The next 5 bits are register address select bits which select one of the eleven registers for access. The next 2 bits are turnaround bits which are not an actual register bits but extra time to switch MDIO from write to read if necessary. The final 16 bits of the MI serial port cycle (or 704 bits if multiple register access is enabled and REGAD[4:0]=11111) come from the specific data register designated by the register address bits REGAD[4:0].

2.23.5 Register Structure

The 84221 has eleven 16 bit registers for each channel. All eleven registers are available for setting configuration inputs and reading status outputs. A map of the registers is shown in Table 8. The eleven registers consist of six registers that are defined by IEEE 802.3 specifications (Registers 0-5) and five registers that are unique to the 84221 (Registers 16-20).

The structure and bit definition of the Control Register is shown in Table 9. This register stores various configuration inputs and its bit definition complies with the IEEE 802.3 specifications.

The structure and bit definition of the Status Register is shown in Table 10. This register contains device capabilities and status output information and its bit definition complies with the IEEE 802.3 specifications.

The structure and bit definition of the PHY ID Register 1 and PHY ID Register 2 is shown in Table 11 and Table 12, respectively. These registers contain an identification code unique to the 84221 and their bit definition complies with the IEEE 802.3 specifications.

The structure and bit definition of the Auto Negotiation Advertisement and Auto Negotiation Remote End Capability registers is shown in Table 13 and Table 14, respectively. These registers are used by the Auto Negotiation algorithm and their bit definition complies with the IEEE 802.3 specifications.

The structure and bit definition of the Global Configuration Register is shown in Table 15. This register is common for all four channels. It stores various configuration inputs.

The structure and bit definition of the Channel Configuration Register is shown in Table 16. This register stores various configuration inputs unique to each channel.

The structure and bit definition of the Channel Status Output Register is shown in Table 17. This register contains output status information from each channel.

The structure and bit definition of the Global Interrupt Mask Register is shown in Table 18. This register is common for all four channels. Bit 7 is the interrupt indication. The 7 least significant bits are the Mask bits for the R/LT status bits in the Channel Status Output Register.

Register 20 in Table 19 is reserved for factory use only. All bits must be set to the pre-set default states shown for normal operation.

2.23.6 Invalid Registers

The registers in locations 6-15 and 21-31 are not implemented on the device, hence unused. When an unused register is read, the value returned can be configured to be either all 0s or all 1s by appropriately pinstrapping the REGDEF pin.

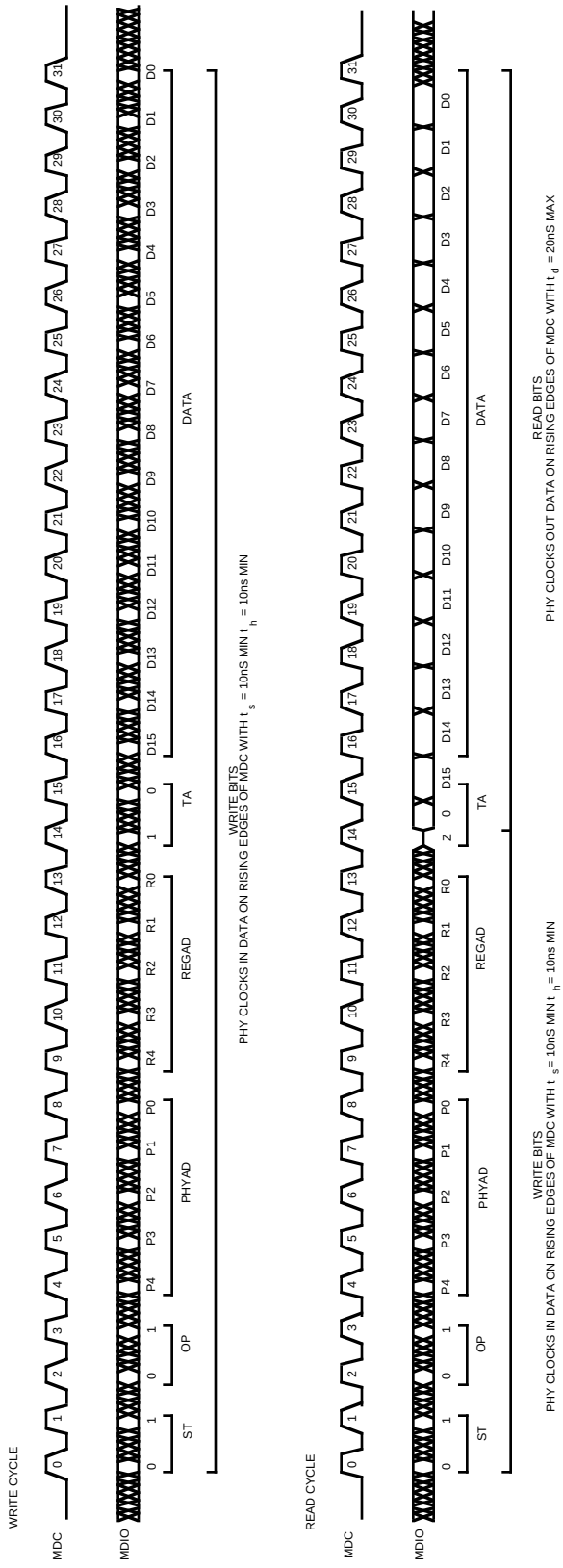


Figure 10. MI Serial Port Frame Timing Diagram

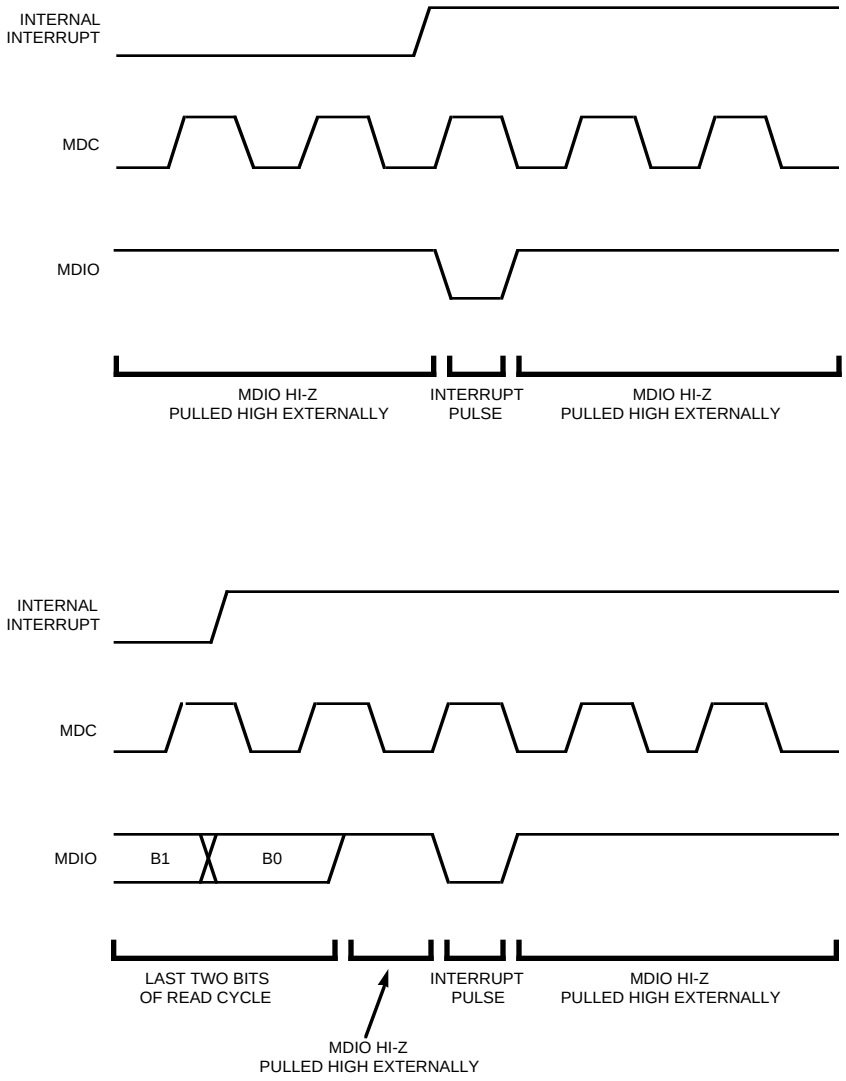


Figure 11. MDIO Interrupt Pulse

3.0 REGISTER DESCRIPTION

Table 7. MI Serial Port Structure

<Idle>	<Start>	<Read>	<Write>	<PHY Addr.>	<Reg. Addr.>	<Turnaround>	<Data>
IDLE	ST[1:0]	READ	WRITE	PHYAD[4:0]	REGAD[4:0]	TA[1:0]	D[15:0]

MI Registers - Address and Default Value

REGAD	Name	Default (Hex Code)
00000	Control Register	3000
00001	Status Register	7809
00010	PHY ID 1 Register	0016
00011	PHY ID 2 Register	F840
00100	Auto Negotiation Advertisement Register	01E1
00101	Auto Negotiation Remote Capability Register	0000
10000	Reserved	0008
10001	Reserved	0002
10010	Channel Status Output Register	0340/0240/ 0140/0040
10011	Reserved	007F
10100	Reserved	0000

Symbol	Name	Definition	R/W
IDLE	Idle Pattern	These bits are an idle pattern. Device will not initiate an MI cycle until it detects at least 32 1's.	W
ST[1:0]	Start Bits	When ST[1:0]=01, a MI serial port access cycle starts.	W
READ	Read Select	1 = Read Cycle	W
WRITE	Write Select	1 = Write Cycle	W
PHYAD[4:0]	Physical Device Address	When PHYAD[4:2] bits match the PHYAD[4:2] pins, the MI serial port is selected for operation. PHYAD[1:0] is used for channel selection: PHYAD [1:0]=11 For Channel 3 PHYAD [1:0]=10 For Channel 2 PHYAD [1:0]=01 For Channel 1 PHYAD [1:0]=00 For Channel 0	W
REGAD4[4:0]	Register Address	If REGAD[4:0]=00000-11100, these bits determine the specific register from which D[15:0] is read/written. If multiple register access is enabled and REGAD[4:0]=11111, all registers are read/written in a single cycle.	W
TA[1:0]	Turnaround Time	These bits provide some turnaround time for MDIO When READ=1, TA[1:0]=Z0 When WRITE=1, TA[1:0]=ZZ	R/W
D[15:0]+	Data	These 16 bits contain data to/from one of the eleven registers selected by register address bits REGAD[4:0].	R or W

		x.15	x.14	x.13	x.12	x.11	x.10	x.9	x.8	x.7	x.6	x.5	x.4	x.3	x.2	x.1	x.0
0	Control	RST	LPBK	SPEED	ANEG_EN	PDN	RMII_DIS	ANEG_RST	DPLX	COLTST	0	0	0	0	0	0	0
		R/WSC	R/W	R/W	R/W	R/W	R/W	R/WSC	R/W	R/WSC	R	R	R	R	R	R	R
		0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
1	Status	CAP_T4	CAP_TXF	CAP_TXH	CAP_TF	CAP_TH	0	0	0	0	CAP_SUPR	ANEG_ACK	REM_FLT	CAP_ANEG	LINK	JAB	EXREG
		R	R	R	R	R	R	R	R	R	R	R	R/LH	R	R/LL	R/LH	R
		0	1	1	1	1	0	0	0	0	0	0	0	1	0	0	1
2	PHY ID #1	OUI3	OUI4	OUI5	OUI6	OUI7	OUI8	OUI9	OUI10	OUI11	OUI12	OUI13	OUI14	OUI15	OUI16	OUI17	OUI18
		R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
		0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0
3	PHY ID #2	OUI19	OUI20	OUI21	OUI22	OUI23	OUI24	PART5	PART4	PART3	PART2	PART1	PART0	REV3	REV2	REV1	REV0
		R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
		1	1	1	1	1	0	0	0	0	1	0	0	—	—	—	—
4	AutoNegot. Advertisement	NP	ACK	RF	0	0	PAUSE	T4	TX_FDX	TX_HDX	10_FDX	0	0	0	0	0	CSMA
		R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	1
5	AutoNegot. Remote Capability	NP	ACK	RF	0	0	PAUSE	T4	TX_FDX	TX_HDX	10_FDX	0	0	0	0	0	CSMA
		R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
16	Reserved	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0
17	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
18	Channel Status Output	RPOL	0	0	0	0	0	—	—	0	LINK_FAIL	SPD_DET	DPLX_DET	0	0	0	0
		R	R	R	R	R	R	R	R	R	R/LT	R/LT	R/LT	R/LT	R/LT	R/LT	R/LT
		0	0	0	0	0	0	11/10/01/00	11/10/01/00	0	1	0	0	0	0	0	0
19	Reserved	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
20	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 8. MI Serial Port Register Map

Table 9. Register 0 – Control Register Definition

0.15	0.14	0.13	0.12	0.11	0.10	0.9	0.8
RST	LPBK	SPEED	ANEG_EN	PDN	RMII_DIS	ANEG_RST	DPLX
R/WSC	R/W	R/W	R/W	R/W	R/W	R/WSC	R/W
0.7	0.6	0.5	0.4	0.3	0.2	0.1	0.0
COLTST	0	0	0	0	0	0	0
R/WSC	R	R	R	R	R	R	R

Bit	Symbol	Name	Definition	R/W	Default
0.15	RST	Reset	1 = Reset, Bit Self Clearing After Reset Completed 0 = Normal	R/WSC	0
0.14	LPBK	Loopback Enable	1 = Loopback Mode enabled 0 = Normal	R/W	0
0.13	SPEED	Speed Select	1 = 100 Mbps Selected (100BaseTX) 0 = 10 Mbps Selected (10BaseT) Note: This Bit can be Overridden with SPEED pin.	R/W	1
0.12	ANEG_EN	Auto Negotiation Enable	1 = Auto Negotiation Enabled 0 = Auto Negotiation Disabled Note: This Bit can be Overridden with ANEG pin.	R/W	1
0.11	PDN	Power Down Enable	1 = Power Down 0 = Normal	R/W	0
0.10	RMII_DIS	RMII Interface Disable	1 = RMII Interface Disable 0 = Normal	R/W	0
0.9	ANEG_RST	Auto Negotiation Reset	1 = Restart Auto Negotiation Process, Bit Self Clearing After Reset Completed 0 = Normal	R/WSC	0
0.8	DPLX	Duplex Mode Select	1 = Full Duplex 0 = Half Duplex Note: This Bit can be Overridden with DPLX pin.	R/W	0
0.7	COLTST	Collision Test Enable	1 = Collision Test Enabled 0 = Normal	R/W	0
0.6 through 0.0			Reserved	R	0

Note: 0.15 Bit Is Shifted First

Table 10. Register 1- Status Register Definition

1.15	1.14	1.13	1.12	1.11	1.10	1.9	1.8
CAP_T4	CAP_TXF	CAP_TXH	CAP_TF	CAP_TH	0	0	0
R	R	R	R	R	R	R	R

1.7	1.6	1.5	1.4	1.3	1.2	1.1	1.0
0	CAP_SUPR	ANEG_ACK	REM_FLT	CAP_ANEG	LINK	JAB	EXREG
R	R	R	R/LH	R	R/LL	R/LH	R

Bit	Symbol	Name	Definition	R/W	Default
1.15	CAP_T4	100BaseT4 Capable	0 = Not Capable of 100BaseT4 Operation	R	0
1.14	CAP_TXF	100BaseTX Full Duplex Capable	1 = Capable of 100BaseTX Full Duplex	R	1
1.13	CAP_TXH	100BaseTX Half Duplex Capable	1 = Capable of 100BaseTX Half Duplex	R	1
1.12	CAP_TF	10BaseT Full Duplex Capable	1 = Capable of 10BaseT Full Duplex	R	1
1.11	CAP_TH	10BaseT Half Duplex Capable	1 = Capable of 10BaseT Half Duplex	R	1
1.10 through 1.7			Reserved	R	0
1.6	CAP_SUPR	MI Preamble Suppression Capable	0 = Not Capable of Accepting MI Frames with Preamble Suppression	R	0
1.5	ANEG_ACK	Auto Negotiation Acknowledgment	1 = Auto Negotiation Acknowledgment Process Complete 0 = Auto Negotiation Not Complete	R	0
1.4	REM_FLT	Remote Fault Detect	1 = Remote Fault detect. This bit is set when Remote Fault Bit 5.13 is set. 0 = No Remote Fault	R/LH	0
1.3	CAP_ANEG	Auto Negotiation Capable	1 = Capable of Auto Negotiation	R	1
1.2	LINK	Link Status	1 = Link Detect (Same As Bit 18.6 Inverted) 0 = Link Not Detect	R/LL	0
1.1	JAB	Jabber Detect	1 = Jabber Detect 0 = Normal	R/LH	0
1.0	EXREG	Extended Register Capable	1 = Extended Registers Exist	R	1

Note: 1.15 Bit Is Shifted First

Tabel 11. Register 2 - PHY ID Register 1 Definition

2.15	2.14	2.13	2.12	2.11	2.10	2.9	2.8
OUI3	OUI4	OUI5	OUI6	OUI7	OUI8	OUI9	OUI10
R	R	R	R	R	R	R	R

2.7	2.6	2.5	2.4	2.3	2.2	2.1	2.0
OUI11	OUI12	OUI13	OUI14	OUI15	OUI16	OUI17	OUI18
R	R	R	R	R	R	R	R

Bit	Symbol	Name	Definition	R/W	Default
2.15	OUI3	Company ID,	SEEQ OUI = 00-A0-7D	R	0
2.14	OUI4	Bits 3-18			0
2.13	OUI5				0
2.12	OUI6				0
2.11	OUI7				0
2.10	OUI8				0
2.9	OUI9				0
2.8	OUI10				0
2.7	OUI11				0
2.6	OUI12				0
2.5	OUI13				0
2.4	OUI14				1
2.3	OUI15				0
2.2	OUI16				1
2.1	OUI17				1
2.0	OUI18				0

Note: 2.15 Bit Is Shifted First

Table 12. Register 3 - PHY ID Register 2 Definition

3.15	3.14	3.13	3.12	3.11	3.10	3.9	3.8
OUI19	OUI20	OUI21	OUI22	OUI23	OUI24	PART5	PART4
R	R	R	R	R	R	R	R

3.7	3.6	3.5	3.4	3.3	3.2	3.1	3.0
PART3	PART2	PART1	PART0	REV3	REV2	REV1	REV0
R	R	R	R	R	R	R	R

Bit	Symbol	Name	Definition	R/W	Default
3.15 3.14 3.13 3.12 3.11 3.10	OUI19 OUI20 OUI21 OUI22 OUI23 OUI24	Company ID, Bits 3-18	SEEQ OUI = 00-A0-7D	R	1 1 1 1 1 0
3.9 3.8 3.7 3.6 3.5 3.4	PART5 PART4 PART3 PART2 PART1 PART0	Manufacturer's Part Number	04	R	0 0 0 1 0 0
3.3 3.2 3.1 3.0	REV3 REV2 REV1 REV0	Manufacturer's Revision Number		R	– – – –

Note: 3.15 Bit Is Shifted First

Table 13. Register 4 - AutoNegotiation Advertisement Register Definition

4.15	4.14	4.13	4.12	4.11	4.10	4.9	4.8
NP	ACK	RF	0	0	PAUSE	T4	TX_FDX
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W

4.7	4.6	4.5	4.4	4.3	4.2	4.1	4.0
TX_HDX	10_FDX	0	0	0	0	0	CSMA
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Symbol	Name	Definition	R/W	Default
4.15	NP	Next Page Enable	0 = No Next Page	R/W	0
4.14	ACK	Acknowledge	1 = Auto Negotiation Word Recognized 0 = Not Recognized	R	0
4.13	RF	Remote Fault	1 = Auto Negotiation Remote Fault Detect 0 = No Remote Fault	R/W	0
4.12 through 4.11			Reserved	R/W	0
4.10	PAUSE	PAUSE Frame Capable	1 = Capable of Transmitting and Receiving Pause Frames 0 = Not Capable	R/W	0
4.9	T4	100BaseT4 Capable	1 = Capable of 100BaseT4 0 = Not Capable	R/W	0
4.8	TX_FDX	100BaseTX Full Duplex Capable	1 = Capable of 100BaseTX Full Duplex 0 = Not Capable	R/W	1
4.7	TX_HDX	100BaseTX Half Duplex Capable	1 = Capable of 100BaseTX Half Duplex 0 = Not Capable	R/W	1
4.6	10_FDX	10BaseTX Full Duplex Capable	1 = Capable of 10BaseTX Full Duplex 0 = Not Capable	R/W	1
4.5	10_HDX	10BaseTX Half Duplex Capable	1 = Capable of 10BaseTX Half Duplex 0 = Not Capable	R/W	1
4.4 through 4.1			Reserved	R/W	0
4.0	CSMA	CSMA 802.3 Capable	1 = Capable of 802.3 CSMA Operation 0 = Not Capable	R/W	1

Note: 4.15 Bit Is Shifted First

Table 14. Register 5 - AutoNegotiation Remote Capability Definition

5.15	5.14	5.13	5.12	5.11	5.10	5.9	5.8
NP	ACK	RF	0	0	PAUSE	T4	TX_FDX
R	R	R	R	R	R	R	R

5.7	5.6	5.5	5.4	5.3	5.2	5.1	5.0
TX_HDX	10_FDX	0	0	0	0	0	CSMA
R	R	R	R	R	R	R	R

Bit	Symbol	Name	Definition	R/W	Default
5.15	NP	Next Page Enable	1 = Next Page Exists 0 = No Next Page	R	0
5.14	ACK	Acknowledge	1 = Received Auto Negotiation Word Recognized 0 = Not Recognized	R	0
5.13	RF	Remote Fault	1 = Auto Negotiation Remote Fault Detect 0 = No Remote Fault	R	0
5.12 through 5.11			Reserved	R	0
5.10	PAUSE	PAUSE Frame Capable	1 = Capable of Transmitting and Receiving Pause Frames 0 = Not Capable	R	0
5.9	T4	100BaseT4 Capable	1 = Capable of 100BaseT4 0 = Not Capable	R	0
5.8	TX_FDX	100BaseTX Full Duplex Capable	1 = Capable of 100BaseTx Full Duplex 0 = Not Capable	R	0
5.7	TX_HDX	100BaseTX Half Duplex Capable	1 = Capable of 100BaseTx Half Duplex 0 = Not Capable	R	0
5.6	10_FDX	10BaseTX Full Duplex Capable	1 = Capable of 10BaseTx Full Duplex 0 = Not Capable	R	0
5.5	10_HDX	10BaseTX Half Duplex Capable	1 = Capable of 10BaseTx Half Duplex 0 = Not Capable	R	0
5.4 through 5.1			Reserved	R	0
5.0	CSMA	CSMA 802.3 Capable	1 = Capable of 802.3 CSMA Operation 0 = Not Capable	R	0

Note: 5.15 Bit Is Shifted First

Table 15. Register 16 - Reserved

16.15	16.14	16.13	16.12	16.11	16.10	16.9	16.8
0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

16.7	16.6	16.5	16.4	16.3	16.2	16.1	16.0
0	1	0	0	1	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Symbol	Name	Definition	R/W	Default
16.15 thru 16.0	—	—	Reserved for factory use. Must be written with default values specified above for normal operation	—	—

Table 16. Register 17 - Reserved

17.15	17.14	17.13	17.12	17.11	17.10	17.9	17.8
0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

17.7	17.6	17.5	17.4	17.3	17.2	17.1	17.0
0	0	0	0	0	0	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Symbol	Name	Definition	R/W	Default
17.15 thru 17.0	—	—	Reserved for factory use. Must be written with default values specified above for normal operation	—	—

Table 17. Register 18 - Channel Status Output Register Definition

18.15	18.14	18.13	18.12	18.11	18.10	18.9	18.8
RPOL							
R	R	R	R	R	R	R	R

18.7	18.6	18.5	18.4	18.3	18.2	18.1	18.0
	LINK_FAIL	SPD_DET	DPLX_DET				JAB
R	R/LT	R/LT	R/LT	R/LT	R/LT	R/LT	R/LT

Bit	Symbol	Name	Definition	R/W	Default
18.15	RPOL	Reversed Polarity Detect	1 = Reversed Polarity Detect 0 = Normal	R	0
18.14			Reserved		0
18.13 through 18.10			Reserved	R	0 0 0 0
18.9 18.8			Reserved	R	11/10/ 01/00
18.7			Reserved	R	0
18.6	LINK_FAIL	Link Fail Detect	1 = Link Not Detected 0 = Normal	R/LT	1
18.5	SPD_DET	100/10 Speed Detect	1 = Device in 100BaseTx Mode 0 = Device in 10 BaseT Mode	R/LT	0
18.4	DPLX_DET	Duplex Detect	1 = Device in Full Duplex Mode 0 = Device in Half Duplex Mode	R/LT	0
18.3			Reserved	R/LT	0
18.2			Reserved	R/LT	0
18.1			Reserved	R/LT	0
18.0	JAB	Jabber Detect	1 = Jabber Detected 0 = Normal	R/LT	0

Note: 18.15 Bit Is Shifted First

Table 18. Register 19 - Reserved

19.15	19.14	19.13	19.12	19.11	19.10	19.9	19.8
0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

19.7	19.6	19.5	19.4	19.3	19.2	19.1	19.0
0	1	1	1	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Symbol	Name	Definition	R/W	Default
19.15 thru 19.	—	—	Reserved for factory use. Must be written with default values specified above for normal operation	—	—

Table 19. Register 20 - Reserved Register

20.15	20.14	20.13	20.12	20.11	20.10	20.9	20.8
0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

20.7	20.6	20.5	20.4	20.3	20.2	20.1	20.0
0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Symbol	Name	Definition	R/W	Default
20.15 Thru 20.0			Reserved for Factory Use. Must be written to 0 for Normal Operation	R/W	0

Note: 20.15 Bit Is Shifted First

4.0 APPLICATION INFORMATION

4.1 EXAMPLE SCHEMATICS

A typical example of the 84221 used for a switching hub application in twisted pair mode is shown in Figure 12; an example of the 84221 used in fiber mode is shown in Figure 13.

4.2 TP INTERFACE

4.2.1 Transmit Interface

The interface between the TP outputs on TPOP/N and the twisted pair cable is typically transformer coupled and terminated with the two resistors as shown in Figure 12.

The transformer for the transmitter is recommended to have a winding ratio of 1:1 with the center tap of the primary winding tied to VDD, as shown in Figure 12. The specifications for such a transformer are shown in Table 20. Sources for quad transformers compatible with the 84221 are listed in Table 21. Note that both "Stacked" and "Non-Stacked pin out types are listed. The Stacked and Non-Stacked designation refers to the type of RJ-45 connector used on the secondary side (line side) of the transformer. The pinout of these types differ slightly so that traces to the magnetics may be kept as short and direct as possible.

The "non-stacked" RJ-45 (also referred to as harmonica) is a traditional horizontally oriented connector consisting of four RJ-45 jacks in a single in-line assembly.

The newer "stacked" connector consists of a two-over-two configuration so that four RJ-45 jacks are located in the footprint area of two side by side connectors. This is a significant improvement for higher density multi-port applications and smaller system form-factors.

The SEEQ 84221 pin-out has been optimized for connection to transformers and connectors designed for the higher density stacked configuration. The SEEQ Quad Transceiver will also operate with non-stacked connectors using either transformers that map the pin-out to the non-stacked configuration, or by using trace "crossovers" on the pc board layout.

The transformers listed with "non-stacked" pin-outs use crossover connections inside the part to map the stacked pin-out of the 84221 to non-stacked RJ-45 connectors. Crossovers internal to the transformer are not made in a controlled impedance environment, so this can impact, somewhat, the cross-talk performance of the system.

For best cross-talk and system performance, it is suggested that stacked connector and transformer configurations be used. Alternately, non-stacked connectors may be used with stacked transformer types and the crossover wiring can be put on the pc board using a ground plane to reduce impedance mismatch.

The transmit output needs to be terminated with two external termination resistors in order to meet the output impedance and return loss requirements of IEEE 802.3. It is recommended that these two external resistors be connected from VDD to each of the TPOP/N outputs, and their value should be chosen to provide the correct termination impedance when looking back through the transformer from the twisted pair cable, as shown in Figure 12. The value of these two external termination resistors depends on the type of cable driven by the device. Refer to the Cable Selection Section for more details on choosing the value of these resistors.

To minimize common mode output noise and to aid in meeting radiated emissions requirements, it may be necessary to add a common mode choke on the transmit outputs as well as add common mode bundle termination. The transformers listed in Table 21 all contain common mode chokes on both the transmit and receive sides, as shown in Figure 12. Common mode bundle termination is achieved by tying the unused pairs in the RJ45 to chassis ground through 75 ohm resistors and a 0.01 uF capacitor, as shown in Figure 12.

To minimize noise pickup into the transmit path in a system or on a PCB, the loading on TPOP/N_ should be minimized and both outputs should always be loaded equally.

Table 20. TP Transformer Specification

Parameter	Specification	
	Transmit	Receive
Turns Ratio	1:1 CT	1:1
Inductance, (uH Min)	350	350
Leakage Inductance, (uH)	0.2	0.2
Capacitance (pF Max)	15	15
DC Resistance (Ohms Max)	0.4	0.4

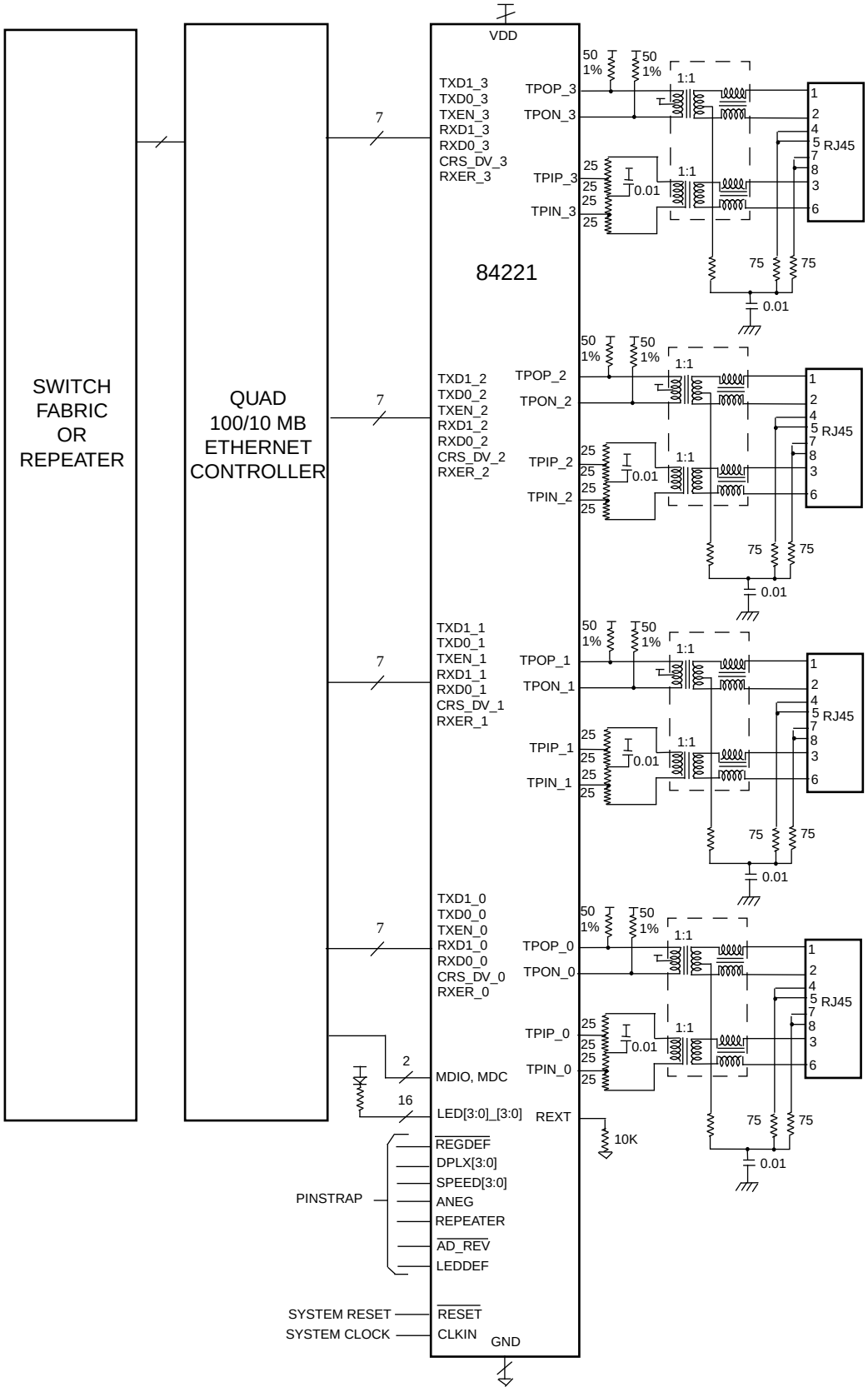


Figure 12. Typical Switching Hub Port Schematic Using the 84221 in Twisted Pair Mode

Table 21. TP Transformer Sources

Vendor	Part Number	Pin Out Type
Pulse	H1062	Stacked
bel	S558-5999B47	Stacked
nano pulse	6931-30	Stacked
Valor	ST6179	Stacked
Halo	TG110-S453NX	Stacked
Pulse	H1053	Non-Stacked
bel	S558-5999-J5	Non-Stacked
nano pulse	6949-30	Non - Stacked
Valor	ST6403P	Non-Stacked
Halo	TG110-S456NX	Non-Stacked

4.2.2 Receive Interface

Receive data is typically transformer coupled into the receive inputs on TPIP/N and terminated with an external resistor as shown in Figure 12.

The transformer for the receiver is recommended to have a winding ration of 1:1, as shown in Figure 12. The specifications for such a transformer are shown in Table 20. Sources for the transformer are listed in Table 21.

The receive input needs to be terminated with the correct termination impedance to meet the input impedance and return loss requirements of IEEE 802.3. In addition, the receive TP inputs need to be attenuated. It is recommended that both the termination and attenuation be accomplished by placing four external resistors in series across the TPIP/N inputs as shown in Figure 12. The resistors should be 25%/25%/25%/25% of the total series resistance, and the total series resistance should be equal to the characteristic impedance of the cable (100 ohms for UTP, 150 Ohms for STP). For 100 Ohm twisted pair the resistor string values should be 25 Ohms each (1%). It is also recommended that a 0.1uF capacitor be placed between the center of the series resistor string and Vcc in order to provide an AC ground for attenuating common mode signal at the input. This capacitor is also shown in Figure 12.

To minimize common mode input noise and to aid in meeting susceptibility requirements, it may be necessary to add a common mode choke on the receive input as well as add common mode bundle termination. The transformers listed in Table 24 contain common mode chokes on both the transmit and receive sides, as shown in Figure 12. Common mode bundle termination is achieved by tying the receive secondary center tap and the unused pairs in the RJ45 to chassis ground through 75 ohm resistors and a 0.01 uF capacitor, as shown in Figure 12.

In order to minimize noise pickup into the receive path in a system or on a PCB, the loading on TPIP/N should be minimized and both inputs should be loaded equally.

4.3 TP TRANSMIT OUTPUT CURRENT SET

The TPOP/N output current level is set by an external resistor tied between REXT and GND. This output current is determined by the following equation where R is the value of REXT:

$I_{out} = (10K/R) * I_{ref}$

Where I_{ref} *= 40 mA (100 Mbps, UTP)*

= 32.6 mA (100 Mbps, STP)

= 100 mA (10 Mbps, UTP)

= 81.6 mA (10 Mbps, STP)

For 100 Ohm UTP, REXT should be typically set to 10K ohms and REXT should be a 1% resistor in order to meet IEEE 802.3 specified levels. Once REXT is set for the 100 Mbps and UTP modes as shown by the equation above, I_{ref} *is then automatically changed inside the device when the 10 Mbps mode or UTP120/STP150 modes are selected as described in the Twisted Pair Characteristics Transmit Section.*

Keep resistor REXT as close to pins REXT and GND as possible in order to reduce noise pickup into the transmitter.

Since the TP output is a current source, capacitive and inductive loading can reduce the output voltage level from the ideal. Thus, in an actual application, it might be necessary to adjust the value of the output current to compensate for external loading. The TP output level can be adjusted by changing the value of the external resistor tied to RXT.

4.4 TRANSMITTER DROOP

The IEEE 802.3 specification has a transmitter output droop requirement for 100BaseTX. Since the 84221 TP output is a current source, it has no perceptible droop by itself. However, the open circuit inductance of the transformer added to the device transmitter output as shown in Figure 12 will cause droop to appear at the transmit interface to the TP wire. If the transformer connected to the 84221 outputs meets the requirements in Table 20, the transmit interface to the TP cable will meet the IEEE 802.3 droop requirements.

4.5 CONTROLLER INTERFACE

4.5.1 General

The 84221 interfaces seemlessly to any standard controller that has a RMII interface that fully complies with the specification created by the RMII consortium.

4.5.2 Clocks

The 84221 requires a 50 MHz clock that must be applied to the CLKIN input. Data is clocked in on the rising edge of CLKIN.

4.5.3 RMII Disable

The RMII outputs can be placed in the high impedance state and inputs disabled by setting the RMII disable bit in the MI serial port Control register. When this bit is set to the disable state, the TP outputs are both disabled and transmission is inhibited. The default value of this bit when the device powers up or is reset is dependent on the device address. If the device address latched into PHYAD[4:0] at reset is 11111, it is assumed that the device is being used in applications where there maybe more than one device sharing the RMII bus, like external PHY's or adapter cards, so the device powers up with the RMII interface disabled. If the device address latched into PHYAD[4:0] at reset is not 11111, it is assumed that the device is being used in an application where it is the only device on the RMII bus, like hubs, so the device powers up with the RMII interface enabled.

4.6 REPEATER APPLICATIONS

4.6.1 RMII Based Repeaters

The 84221's RMII interface can interface to any repeater controller with a RMII interface. The 84221 does add additional latency since the internal data path goes through the unexposed MII interface. So any repeater implementation has to carefully consider the repeater bit budget impact due to the additional latency.

4.7 SERIAL PORT

4.7.1 General

The 84221 has a MI serial port to set all of the devices's configuration inputs and read out the status outputs. Any external device that has an IEEE 802.3 compliant MI interface can connect directly to the 84221 without any glue logic, as shown in Figure 12 and Figure 13.

As described earlier, the MI serial port consists of five lines: MDC, MDIO, and PHYAD[4:2]. However, only 2 lines, MDC and MDIO, are needed to shift data in and out.

PHYAD[4:2] define the three most significant bits of the PHY address, as described in the Section 4.7.2, Serial Port Addressing Section.

4.7.2 Serial Port Addressing

The device address for the MI serial port is selected by connecting the PHYAD[4:2] pins to the desired value. The PHYAD[1:0] addresses are internally hardwired for each channel as shown in both Tables 5 and 7.

4.8 UNMANAGED PORT CONFIGURATION

The 84221 has configuration inputs which can "over-ride" the default configuration state obtained on POWER-UP or RESET of the device. Use of these pins ANEG, SPEED_[3:0], and DPLX_[3:0] allow selection of Global Autonegotiation, Individual Port Speed (10/100), and Individual Port Duplex (Full/Half), by properly strapping

these pins to VDD or VSS as shown in Table 23. Note that these pins SHOULD NOT FLOAT, but must be connected either High or Low for proper operation.

In order to obtain the "Default Mode of Operation", ie: Auto-negotiation enabled, 100MBs, and Half Duplex; the ANEG, SPEED_[3:0], and DPLX_[3:0] pins should be set to 1,1,0 respectively.

Table 23. Hardware Configuration

Configuration State	Auto-Negotiate	Speed	Duplex
Normal (POC/RESET)	Enabled	Advertise 10/100	Advertise Full/Half
Config Pins	ANEG=1	SPEED_ [3:0]=1	DPLX_ [3:0]=0
Complement State	Disabled	10MBs	Full
Config Pins	ANEG=0	SPEED_ [3:0]=0	DPLX_ [3:0]=1

4.9 LONG CABLE

IEEE 802.3 specifies that 10BaseT and 100BaseTX operate over twisted pair cable lengths from 0 to 100 meters. The squelch levels can be reduced by 4.5 dB if the receive level adjust bit is appropriately set in the MI serial port Channel Configuration register, which will allow the 84221 to operate with up to 150 meters of twisted pair cable. The equalizer is already designed to accomodate between 0 to 150 meters of cable.

4.10 CLOCK

The 84221 requires a 25 MHz reference frequency for internal signal generation in MII mode, and 50 MHz in RMII mode. The appropriate reference frequency must be applied to the CLKIN pin.

4.11 LED DRIVERS

The $\overline{LED[3:0]}$ outputs can all drive LED's tied to VDD as shown in Figure 12 and Figure 13. In addition, the $\overline{LED[3:0]}$ outputs can drive LED's tied to GND as well. The LED definitions assume that the LED outputs are tied to VDD, active low signals (otherwise the LED outputs will indicate their respective opposite events.)

The LEDDEF pin determines the default settings for LED[3:0]. If LEDDEF = 0, the default functions for $\overline{LED[3:0]}$ are Link 100, Activity, Full Duplex, and Link 10, respectively. If LEDDEF = 1, the LED functions for LED[3:0] are forced to LINK + ACTIVITY, Collision, Full Duplex and 10/100 Mbps operation, respectively. Table 5 defines the LED functions. Table 4 defines the LED events.

The LED[3:0] outputs can also drive other digital inputs. Thus, LED[3:0] can also be used as digital outputs whose function can be user defined and controlled through the MI serial port.5V Compatible I/O Operation.

4.12 5V COMPATIBLE I/O OPERATION

The input and output pins of the 84221 are tolerant of signal levels up to a maximum of 5.5V (including overshoot etc.). This allows the transceiver to be operated with 5V controllers that have TTL I/O characteristics (0.8 to 2.0V Input levels) without the use of levelshifters or other interfaces.

Controllers and other system components may be operate with 5V supplies and all inter-chip signals may be connected directly to the 84221. All required external logic levels must retain TTL compatability since the 84221 outputs are not guaranteed to achieve higher than 2.3V with a load of 10ma. However, the inputs of the 84221 will tolearte TTL or CMOS logic levels being driven into the device.

This should make replacement of the Physical Layer transceivers in existing designs quite simple since any 5V devices do not need to be changed.

4.13 POWER SUPPLY DECOUPLING

All VDD's on each individual side should be connected together (grouped) and tied to a power plane, as close as possible to the 84221 supply pins. If the VDD's vary in potential by even a small amount, noise and latchup can result. The 84221 VDD pins should be kept to within 50 mV of each other.

All GND's should be connected as close as possible to the device with a large ground plane. If the GND's vary in potential by even a small amount, noise and latchup can result. The GND pins should be kept to within 50 mV of each other.

A 0.01-0.1uF decoupling capacitor should be connected between the VDD group and GND on each of the 4 sides of the 84221 as close as possible to the device pins, preferably within 0.5 in. The value should be chosen depending on whether the noise from VDD-GND is high or low frequency. A conservative approach would be to use two decoupling capacitors on each side, one 0.1uf for low frequencys, and one 0.001 uf for high frequency noise on the power supply.

The VDD connection to the transmit transformer center tap shown in Figures 12 and 13 must be well decoupled in order to minimize common mode noise injection from the supply into the twisted pair cable. It is recommended that a 0.01 uF decoupling capacitor be placed between the transformer center tap VDD connection and the 84221 GND plane. This decoupling capacitor should be physically placed as close as possible to the transformer center tap, preferably within 0.5 in.

The PCB layout and power supply decoupling discussed above should provide sufficient decoupling to achieve the following when measured at the device:

(1) the resultant AC noise voltage measured across each VDD/GND set should be less than 100 mVpp,

(2) all VDD's should be within 50 mVpp of each other, and

(3) all GND's should be within 50 mVpp of each other.

5.0 SPECIFICATIONS

5.1 ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are limits beyond which may cause permanent damage to the device or affect device reliability. All voltages are specified with respect to GND, unless otherwise specified.

V_{DD} Supply Voltage ..... -0.3V to +4.0V
All Inputs and Outputs ..... -0.3V to 5.5V
Package Power Dissipation ..... 3.0 Watt @ 70 ^{o}C
Storage Temperature ..... -65 to +150 ^{o}C
Temperature Under Bias..... -10 to +80 ^{o}C
Lead Temperature (Soldering, 10 Sec)..... 260 ^{o}C
Body Temperature (Soldering, 30 Sec) ..... 220 ^{o}C

Note that all inputs and outputs are 5V tolerant

5.2 DC ELECTRICAL CHARACTERISTICS

Unless otherwise noted, all test conditions are as follows:

1. T_A= 0 to +70 ^{o}C
2. V_{DD} = 3.3V $\pm$5%
3. 25 MHz $\pm$0.01%
4. REXT = 10K $\pm$1%, no load

SYM	PARAMETER	LIMIT MIN	LIMIT TYP	LIMIT MAX	UNIT	CONDITIONS
V_{IL}	Input Low Voltage			0.8	Volt	
V_{IH}	Input High Voltage	2			Volt	
I_{IL}	Input Low Current			±1	uA	VIN = GND All Except $\overline{\text{RESET}}$
		10		50	uA	VIN = GND $\overline{\text{RESET}}$
I_{IH}	Input High Current			±1	uA	VIN = 5V for all except $\overline{\text{REGDEF}}$ VIN = VDD for $\overline{\text{REGDEF}}$
V_{OL}	Output Low Voltage			0.4	Volt	IOL = -4 mA, Except $\overline{\text{LED[3:0]}}$
				1	Volt	IOL = -20 mA, $\overline{\text{LED[3:0]}}$
V_{OH}	Output High Voltage	VDD -1.0			Volt	IOH = 4 mA All Except $\overline{\text{LED[3:0]}}$
		VDD -1.0			Volt	IOH = 10 mA, $\overline{\text{LED[3:0]}}$
		2.4			Volt	IOH = 10 uA
C_{IN}	Input Capacitance		5		pF	
I_{DD}	VDD Supply Current			450	mA	Transmitting 100%, 100 Mbps
				450	mA	Transmitting 100%, 10 Mbps
I_{GND}	GND Supply Current			700	mA	Transmitting 100%, 100 Mbps, Note 1
				700	mA	Transmitting 100%, 10 Mbps, Note 1
				200	uA	Powerdown

Note 1. IGND includes current flowing into GND from the external resistors and transformer on TPOP/ TPON as shown in Figure 12.

Twisted Pair Characteristics, Transmit

Unless otherwise noted, all test conditions are as follows:

1. T_A= 0 to +70 ^oC
2. V_{DD} = 3.3 V ±5%
3. 25 MHz ±0.01%
4. REXT=10K ±1%, no load
5. TPOP/N Loading Shown in Figure 12 or Equivalent

SYM	PARAMETER	LIMIT MIN	LIMIT TYP	LIMIT MAX	UNIT	CONDITIONS
T_{OV}	TP Differential Output Voltage	0.950	1.000	1.050	V pk	100 Mbps, UTP Mode, 100 Ohm Load
		1.165	1.225	1.285	V pk	100 Mbps, STP Mode, 150 Ohm Load
		2.2	2.5	2.8	V pk	10 Mbps, UTP Mode, 100 Ohm Load
		2.694	3.062	3.429	V pk	10 Mbps, STP Mode, 150 Ohm Load
T_{OVS}	TP Differential Output Voltage Symmetry	98		102	%	100 Mbps, Ratio of Positive And Negative Amplitude Peaks on TPOP/N
T_{ORF}	TP Differential Output Rise And Fall Time	3.0		5.0	nS	100 Mbps
T_{ORFS}	TP Differential Output Rise And Fall Time Symmetry			±0.5	nS	100 Mbps, Difference Between Rise And Fall Times on TPOP/N
T_{ODC}	TP Differential Output Duty Cycle Distortion			±0.25	ns	100 Mbps, Output Data=0101... NRZI Pattern Unscrambled, Measure At 50% Points
T_{OJ}	TP Differential Output Jitter			±0.7	ns	100 Mbps, Output Data=Scrambled /H/
T_{OO}	TP Differential Output Overshoot			5.0	%	100 Mbps
T_{OVT}	TP Differential Output Voltage Template	See Figure 4				10 Mbps
T_{SOI}	TP Differential Output SOI Voltage Template	See Figure 6				10 Mbps
T_{LPT}	TP Differential Output Link Pulse Voltage Template	See Figure 7				10 Mbps, NLP and FLP
T_{OIV}	TP Differential Output Idle Voltage			50	mV	10 Mbps, Measured on Secondary Side of Xfmr in Figure 12
T_{OIA}	TP Output Current	38	40	42	mA pk	100 Mbps, UTP with TLVL[3:0]=1000
		31.06	32.66	34.26	mA pk	100 Mbps, STP with TLVL[3:0]=1000
		88	100	112	mA pk	10 Mbps, UTP with TLVL[3:0]=1000
		71.86	81.64	91.44	mA pk	10 Mbps, STP with TLVL[3:0]=1000
T_{OIR}	TP Output Current Adjustment Range	0.80		1.2		Adjustable with REXT, Relative to T_{OIA} with REXT=10K
		0.86		1.16		Adjustable with TLVL[3:0]. See Section 4.3. Relative to Value at TLVL[3:0]=1000.
T_{ORA}	TP Output Current TLVL Step Accuracy			±50	%	Relative to Ideal Values in Table 2. Values Relative to Output with TLVL[3:0]=1000.
T_{OR}	TP Output Resistance		10K		Ohm	
T_{OC}	TP Output Capacitance		15		pF	

Twisted Pair Characteristics, Receive

Unless otherwise noted, all test conditions are as follows:

1. TA= 0 to +70°C
2. VDD = 3.3V +5%
3. 25 MHz +0.01%
4. REXT = 10K +1%, no load
5. 62.5/10 MHz Square Wave on TP inputs in 100/10 Mbps

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
R_{ST}	TP Input Squelch Threshold	166		500	mV pk	100 Mbps, RLVL=0
		310		540	mV pk	10 Mbps, RLVL=0
		60		200	mV pk	100 Mbps, RLVL=1
		217		378	mV pk	10 Mbps, RLVL=1
R_{UT}	TP Input Unsquelch Threshold	100		300	mV pk	100 Mbps, RLVL=0
		186		324	mV pk	10 Mbps, RLVL=0
		60		180	mV pk	100 Mbps, RLVL=1
		130		227	mV pk	10 Mbps, RLVL=1
R_{OCV}	TP Input Open Circuit Voltage		V_{DD}- 2.4 ± 0.2		Volt	Voltage on Either TPIP or TPIN with Respect to GND
R_{CMR}	TP Input Common Mode Voltage Range		R_{OCV} ±0.25		Volt	Voltage on Either TPIP or TPIP with Respect to GND
R_{DR}	TP Input Differential Voltage Range			V_{DD}	Volt	
R_{IR}	TP Input Resistance	5K			ohm	
R_{IC}	TP Input Capacitance		10		pF	

AC Test Timing Conditions

Unless otherwise noted, all test conditions are as follows:

1. T_A= 0 to +70 ^{O}C
2. V_{DD} = 3.3 V ±5%
3. 25 MHz ±0.01%
4. REXT = 10K ±1%, no load
5. Input conditions:
   - All Inputs: tr,tf <= 5 nS, 20-80%
6. Output Loading
   - TPOP/N: Same as Figure 12 or Equivalent, 10 pF
   - REGDEF: 1K Pullup, 50 pF
   - All Other Digital Outputs: 25 pF
7. Measurement Points:
   - TPOP/N, TPIP/N: 0 V During Data, ±0.3 V at start/end of packet
   - All other inputs and outputs: 1.4 V

5.7 Clock Timing Characteristics

Refer To Figure 16 For Timing Diagram

SYM	PARAMETER	LIMIT MIN	LIMIT TYP	LIMIT MAX	UNIT	CONDITIONS
t_1	CLKIN Period	19.996	20	20.002	nS	
t_2	CLKIN High Time	7			nS	
t_3	CLKIN Low Time	7			nS	

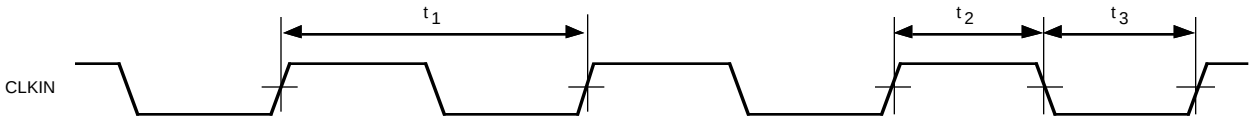


Figure 16. Output Timing

Transmit Timing Characteristics

Refer To Figures 17-18 For Timing Diagram

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
t_{15}	TXEN Setup Time	4			nS	
t_{16}	TXEN Hold Time	2			nS	
t_{19}	TXD Setup Time	4			nS	
t_{20}	TXD Hold Time	2			nS	
t_{23}	Transmit Propagation Delay	60		140	nS	100 Mbps
				600	nS	10 Mbps
t_{24}	Transmit Output Jitter			±0.7	nS pk-pk	100 Mbps
				± 5.5	nS pk-pk	10 Mbps
t_{25}	Transmit SOI Pulse Width To 0.3V	250			nS	10 Mbps
t_{26}	Transmit SOI Pulse Width to 40 mV			4500	nS	10 Mbps
t_{27}	$\overline{\text{LEDn}}$ Delay Time			25	mS	Activity
t_{28}	$\overline{\text{LEDn}}$ Pulse Width	80		105	mS	Activity

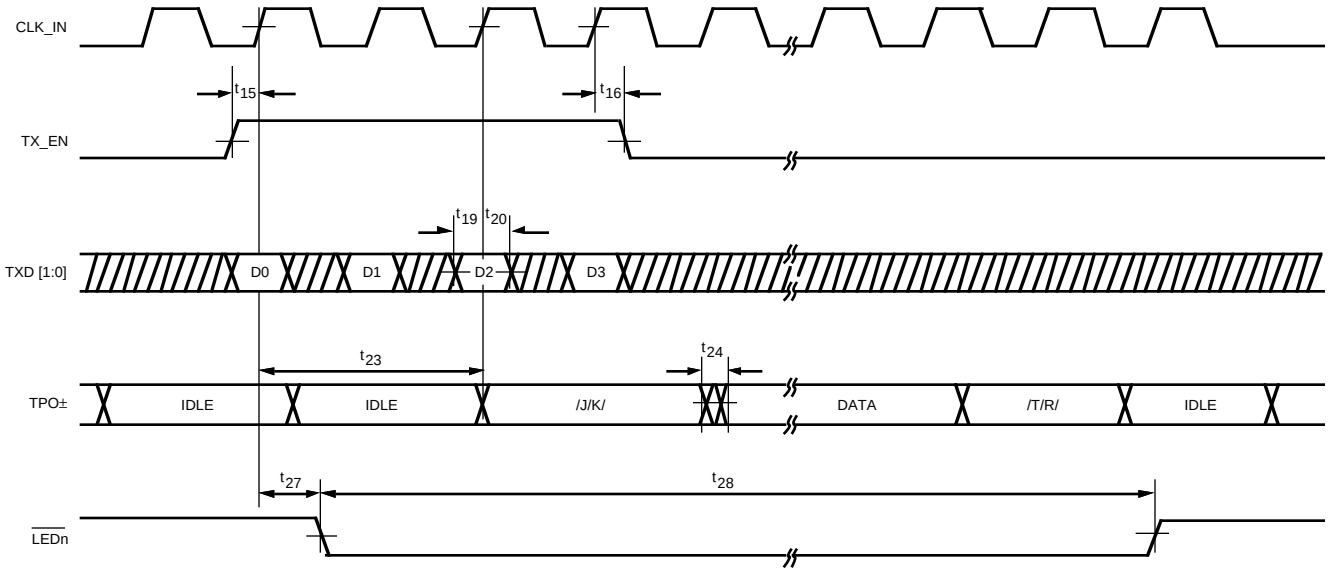
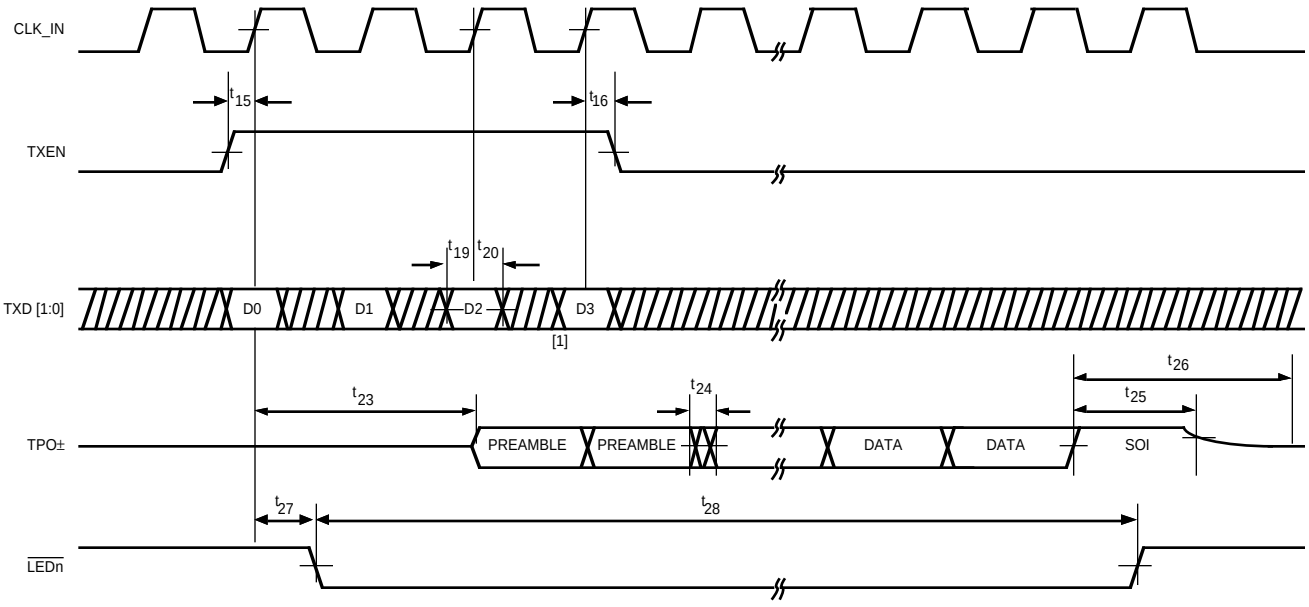


Figure 17. Transmit Timing - 100 Mbps



[1] = Each Di-Bit is present on RXD[1:0] for ten consecutive CLKIN cycles.

Figure 18. Transmit Timing - 10 Mbps

Receive Timing Characteristics

Refer To Figures 19-22 For Timing Diagram

SYM	PARAMETER	LIMIT MIN	LIMIT TYP	LIMIT MAX	UNIT	CONDITIONS
t_{31}	Start of Packet to CRS_DV Assert Delay			200	nS	100 Mbps
				400	nS	10 Mbps
t_{32}	End of Packet to CRS_DV Deassert Delay	130		240	nS	100 Mbps
				1000	nS	10 Mbps
t_{33}	Start of Packet to Valid RXD[1:0] Delay			240	nS	100 Mbps
				3600	ns	10 Mbps
t_{34}	End of Packet to Valid RXD[1:0] Delay			360	ns	100 Mbps
				2800	ns	10 Mbps
t_{37}	CLKIN to RXD[1:0], RXER Delay	2		6	nS	100 Mbps and 10 Mbps
t_{40}	SOI Pulse Minimum Width Required for Idle Detection	125		200	nS	10 Mbps Measured TPIP/N from last zero cross to 0.3 V point.
t_{41}	Receive Input Jitter			±2.0	nS pk-pk	100 Mbps
				±13.5	nS pk-pk	10 Mbps
t_{43}	$\overline{\text{LEDn}}$ Delay Time			25	mS	Activity
t_{44}	$\overline{\text{LEDn}}$ Pulse Width	60		105	mS	Activity
t_{45}	RXD, CRS_DV RXER Output Rise and Fall Times			5	nS	

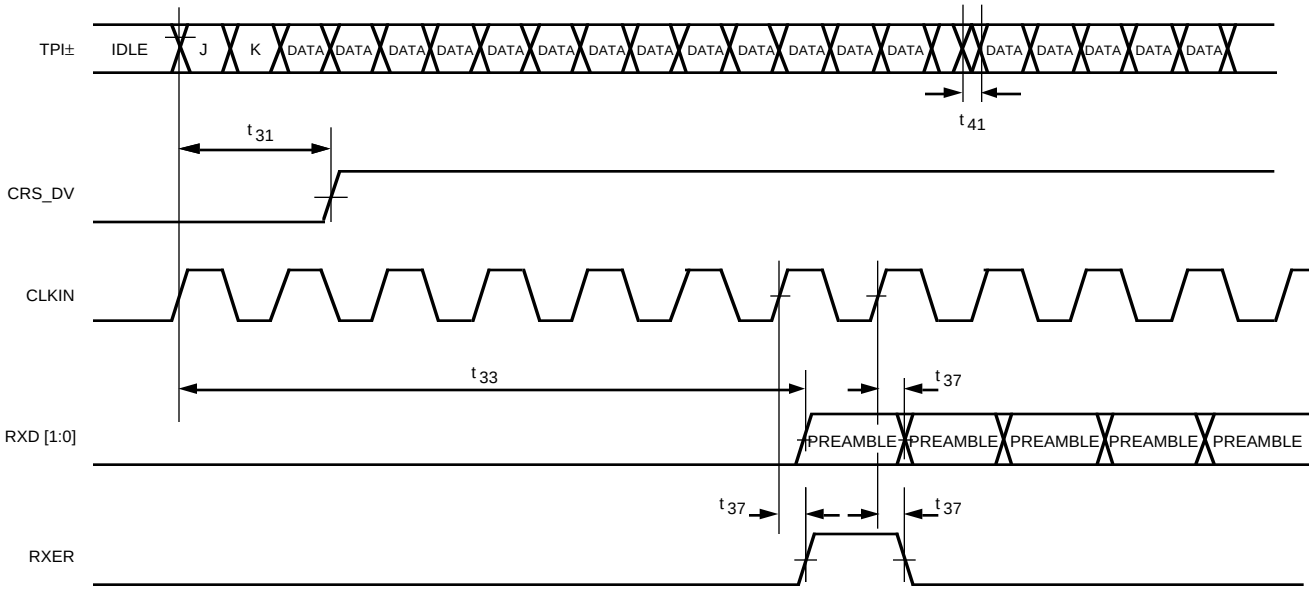


Figure 19. Receive Timing, Start of Packet - 100 Mbps

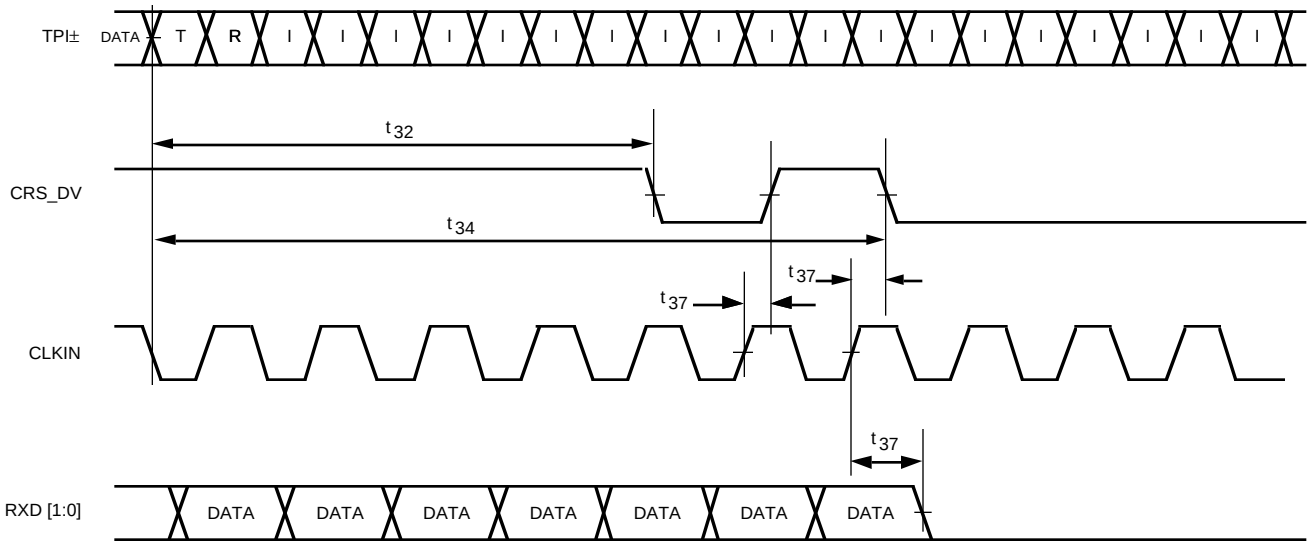
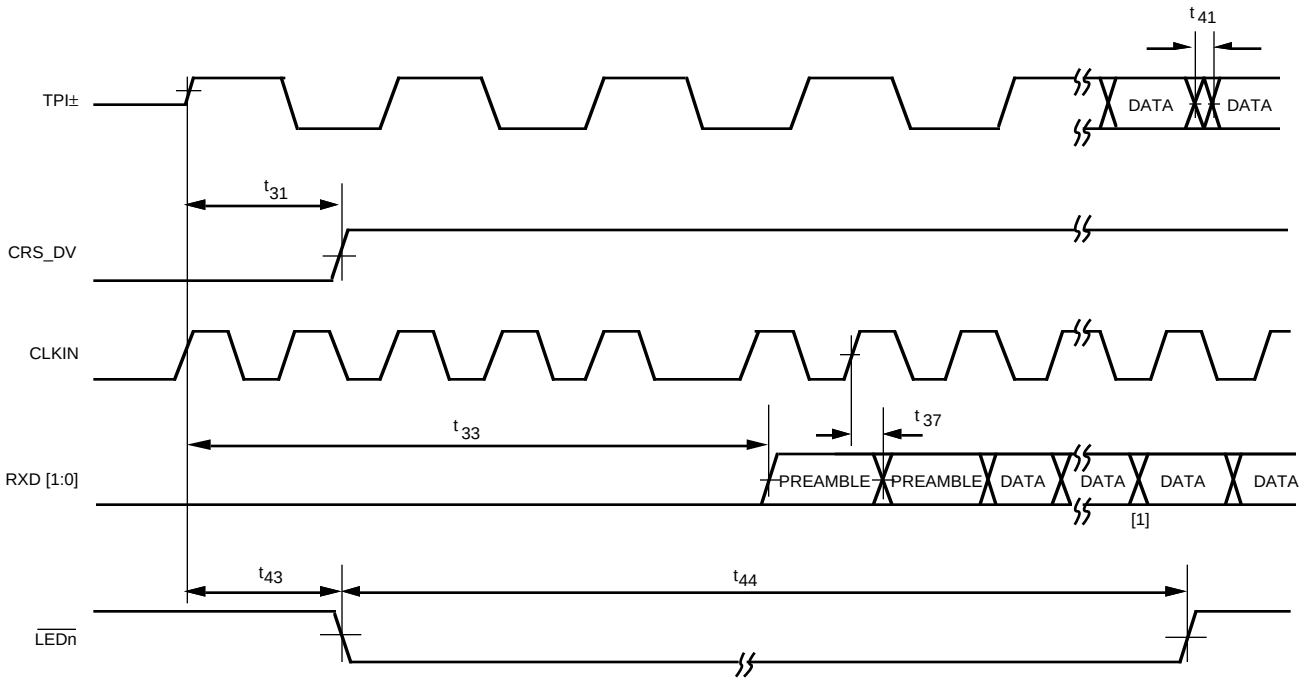
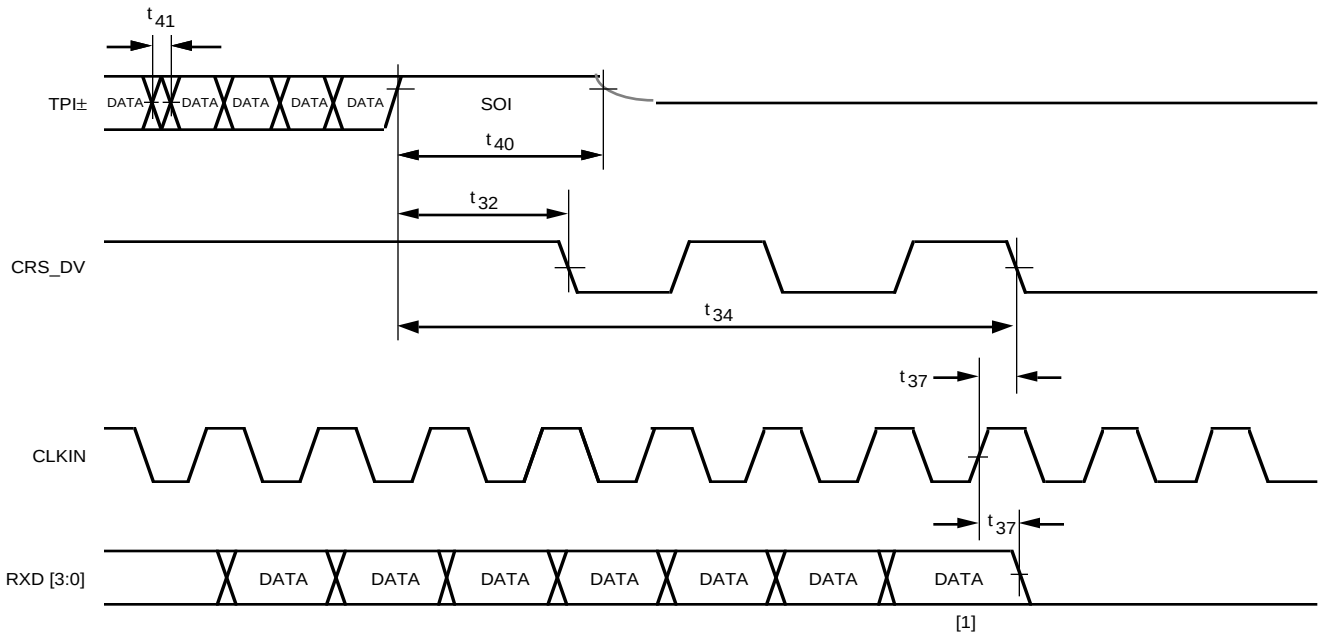


Figure 20. Receive Timing, End of Packet - 100 Mbps



[1]: Each Di-Bit is present on RXD[1:0] for 10 consecutive CLKIN cycles.

Figure 21. Receive Timing, Start of Packet - 10 Mbps



[1]: Each Di-Bit is present on RXD[1:0] for 10 consecutive CLKIN cycles.

Figure 22. Receive Timing, End of Packet - 10 Mbps

Link Pulse Timing Characteristics

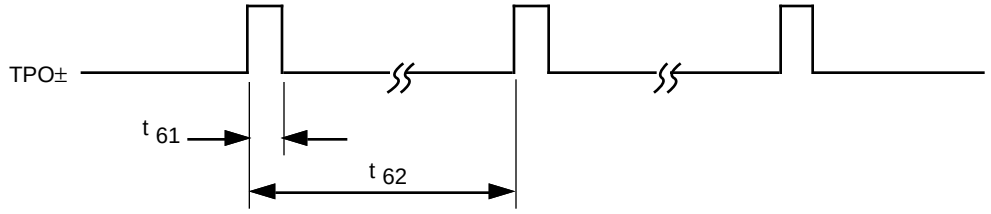
Refer To Figures 23-24 For Timing Diagram

SYM	PARAMETER	LIMIT			UNIT	CONDITION
		MIN	TYP	MAX		
t_{61}	NLP Transmit Link Pulse Width	See Figure 8			ns	
t_{62}	NLP Transmit Link Pulse Period	8		24	mS	
t_{63}	NLP Receive Link Pulse Width Required For Detection	50			nS	
t_{64}	NLP Receive Link Pulse Minimum Period Required For Detection	6		7	mS	link_test_min
t_{65}	NLP Receive Link Pulse Maximum Period Required For Detection	50		150	mS	link_test_max link_loss
t_{66}	NLP Receive Link Pulses Required To Exit Link Fail State	3	3	3	Link Pulses	lc_max
t_{67}	FLP Transmit Link Pulse Width	100		150	nS	
t_{68}	FLP Transmit Clock Pulse To Data Pulse Period	55.5	62.5	69.5	uS	interval_timer
t_{69}	FLP Transmit Clock Pulse To Clock Pulse Period	111	125	139	uS	
t_{70}	FLP Transmit Link Pulse Burst Period	8		22	mS	transmit_link_burst_timer
t_{71}	FLP Receive Link Pulse Width Required For Detection	50			nS	
t_{72}	FLP Receive Link Pulse Minimum Period Required For Clock Pulse Detection	5		25	uS	flp_test_min_timer
t_{73}	FLP Receive Link Pulse Maximum Period Required For Clock Pulse Detection	165		185	uS	flp_test_max_timer
t_{74}	FLP Receive Link Pulse Minimum Period Required For Data Pulse Detection	15		47	uS	data_detect_min_timer

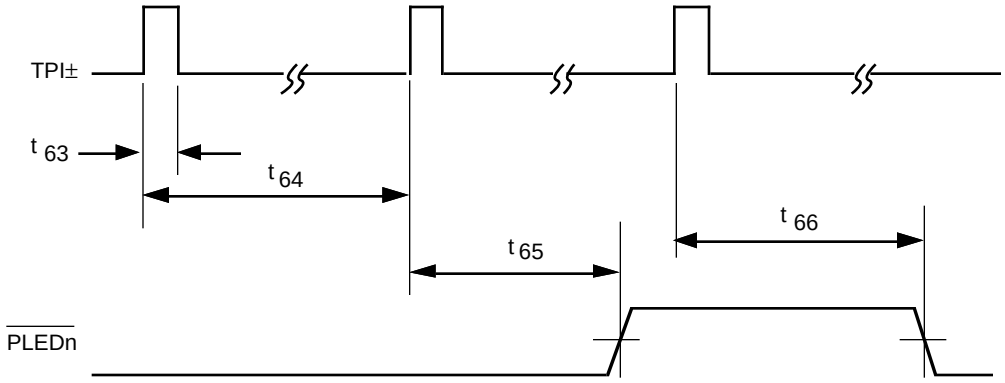
LINK PULSE TIMING CHARACTERISTICS (Continued)

Refer To Figures 23-24 For Timing Diagram

SYM	PARAMETER	LIMIT			UNIT	CONDITION
		MIN	TYP	MAX		
t_{75}	FLP Receive Link Pulse Maximum Period Required For Data Pulse Detection	78		100	uS	data_detect_max_timer
t_{76}	FLP Receive Link Pulses Required To Detect Valid FLP Burst	17		17	Link Pulses	
t_{77}	FLP Receive Link Pulse Burst Minimum Period Required For Detection	5		7	mS	nlp_test_min_timer
t_{78}	FLP Receive Link Pulse Burst Maximum Period Required For Detection	50		150	mS	nlp_test_max_timer
t_{79}	FLP Receive Link Pulses Bursts Required To Detect AutoNegotiation Capability	3	3	3	Link Pulse Bursts	
t_{80}	FLP Receive Acknowledge Fail Period	1200		1500	mS	
t_{81}	FLP Transmit Renegotiate Link Fail Period	1200		1500	mS	break_link_timer
t_{82}	NLP Receive Link Pulse Maximum Period Required For Detection After FLP Negotation Has Completed	750		1000	mS	link_fail_inhibit_timer

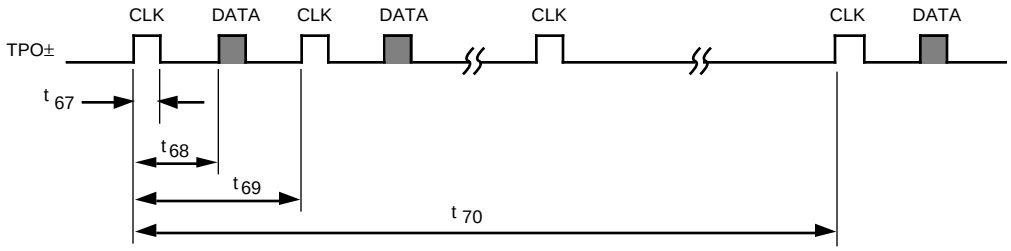


a.) Transmit NLP

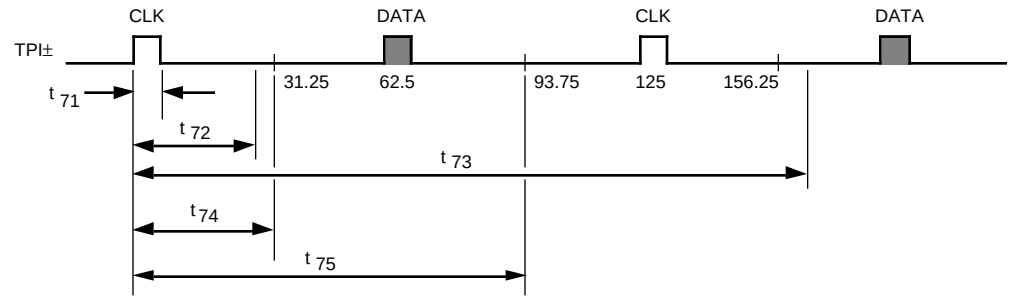


b.) Receive NLP

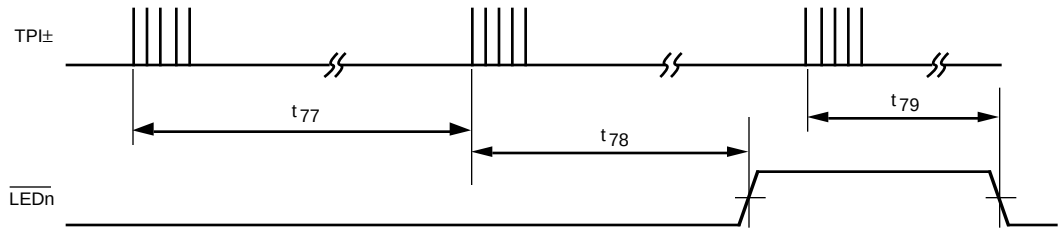
Figure 23. NLP Link Pulse Timing



a.) Transmit FLP and Transmit FLP Burst



b.) Receive FLP



c.) Receive FLP Burst

Figure 24. FLP Link Pulse Timing

Jabber Timing Characteristics

Refer To Figure 25 For Timing Diagram

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
t_{91}	Jabber Activation Delay Time	50		100	mS	10 Mbps
t_{92}	Jabber Deactivation Delay Time	250		750	mS	10 Mbps

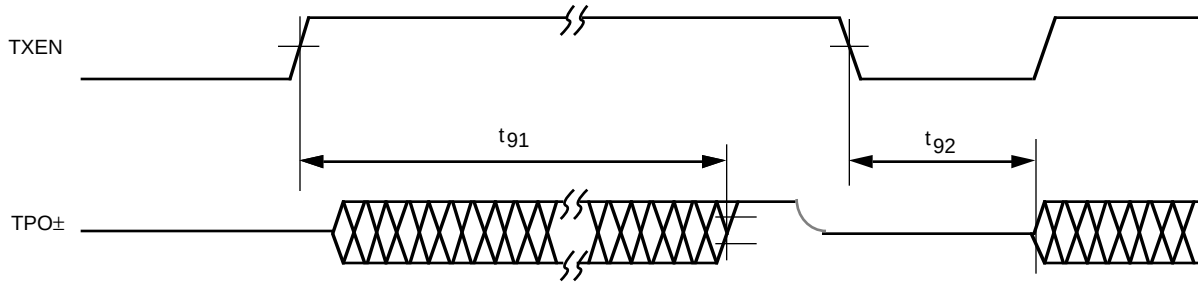


Figure 25 Jabber Timing

LED Driver Timing Characteristics

Refer To Figure 26 For Timing Diagram

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
t_{96}	$\overline{\text{LED[3:0]}}$ On Time	80		105	mS	$\overline{\text{LED[3:0]}}$ Programmed to Blink
t_{97}	$\overline{\text{LED[3:0]}}$ Off Time	80		105	mS	$\overline{\text{LED[3:0]}}$ Programmed to Blink

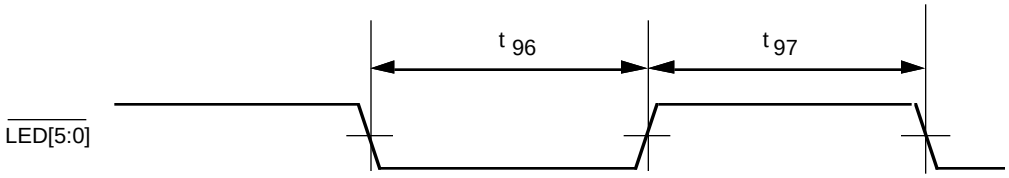


Figure 26. LED Driver Timing

MI Serial Port Timing Characteristics

Refer To Figure 27 For Timing Diagram

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
t_{101}	MDC High Time	20			nS	
t_{102}	MDC Low Time	20			nS	
t_{103}	MDIO Setup Time	10			nS	Write Bits
t_{104}	MDIO Hold Time	10			nS	Write Bits
t_{105}	MDC To MDIO Delay			20	nS	Read Bits
t_{106}	MDIO Hi-Z To Active Delay			20	nS	Write-Read Bit Transition
t_{107}	MDIO Active To HI-Z Delay			20	nS	Read-Write Bit Transition
t_{108}	Frame Delimiter (Idle)	32			Clocks	# of Consecutive MDC Clocks With MDIO = 1
t_{110}	MDC To MDIO Interrupt Pulse Assert Delay			100	nS	
t_{111}	MDC To MDIO Interrupt Pulse Deassert Delay			100	nS	

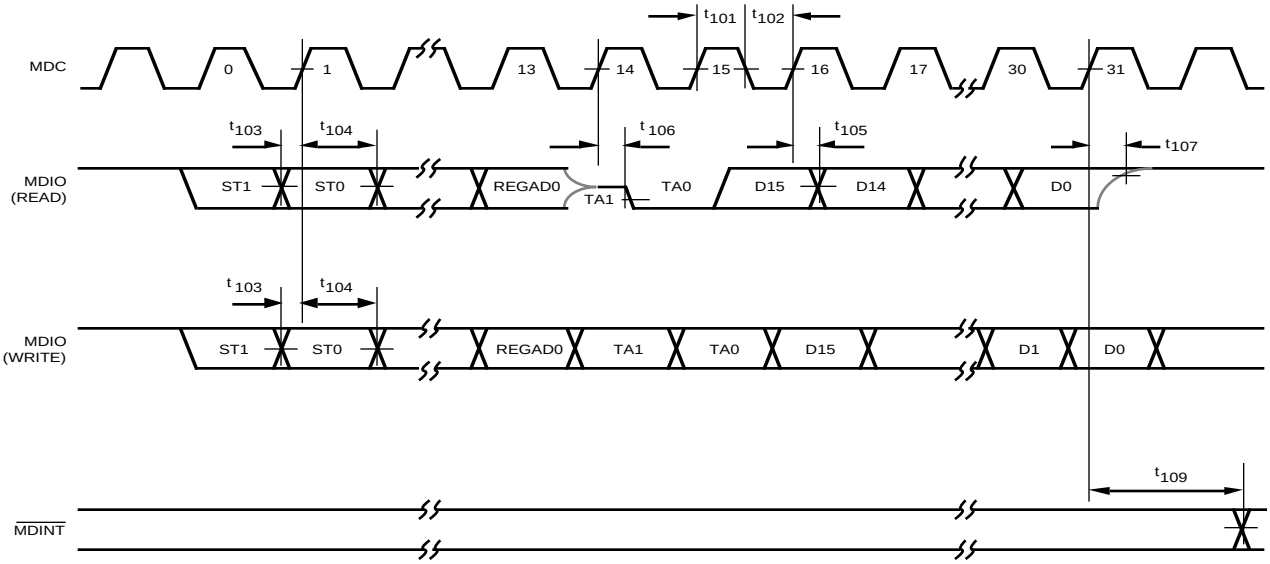
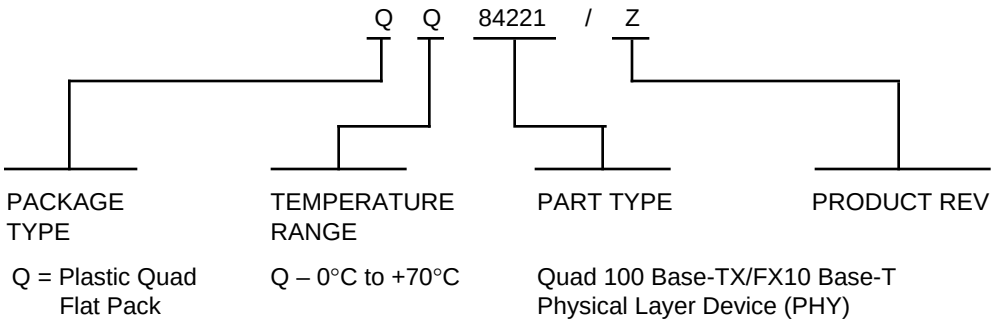


Figure 27. MI Serial Port Timing

Ordering Information



Revision History

99191

Document Revision changed to MD400184/A

Global: All references to FX or 100BaseFX have been deleted.

Page 16: Section 2.4.1 4B5B Decoder - 100 Mbps
- Paragraph #2 has had a copy change.
- Section 2.6.3 Scambler Bypass, has been deleted.

Page 17: Section 2.7.1 100 Mbps
- Paragraph #3 has been deleted.
- Section 2.7.3 has been deleted.

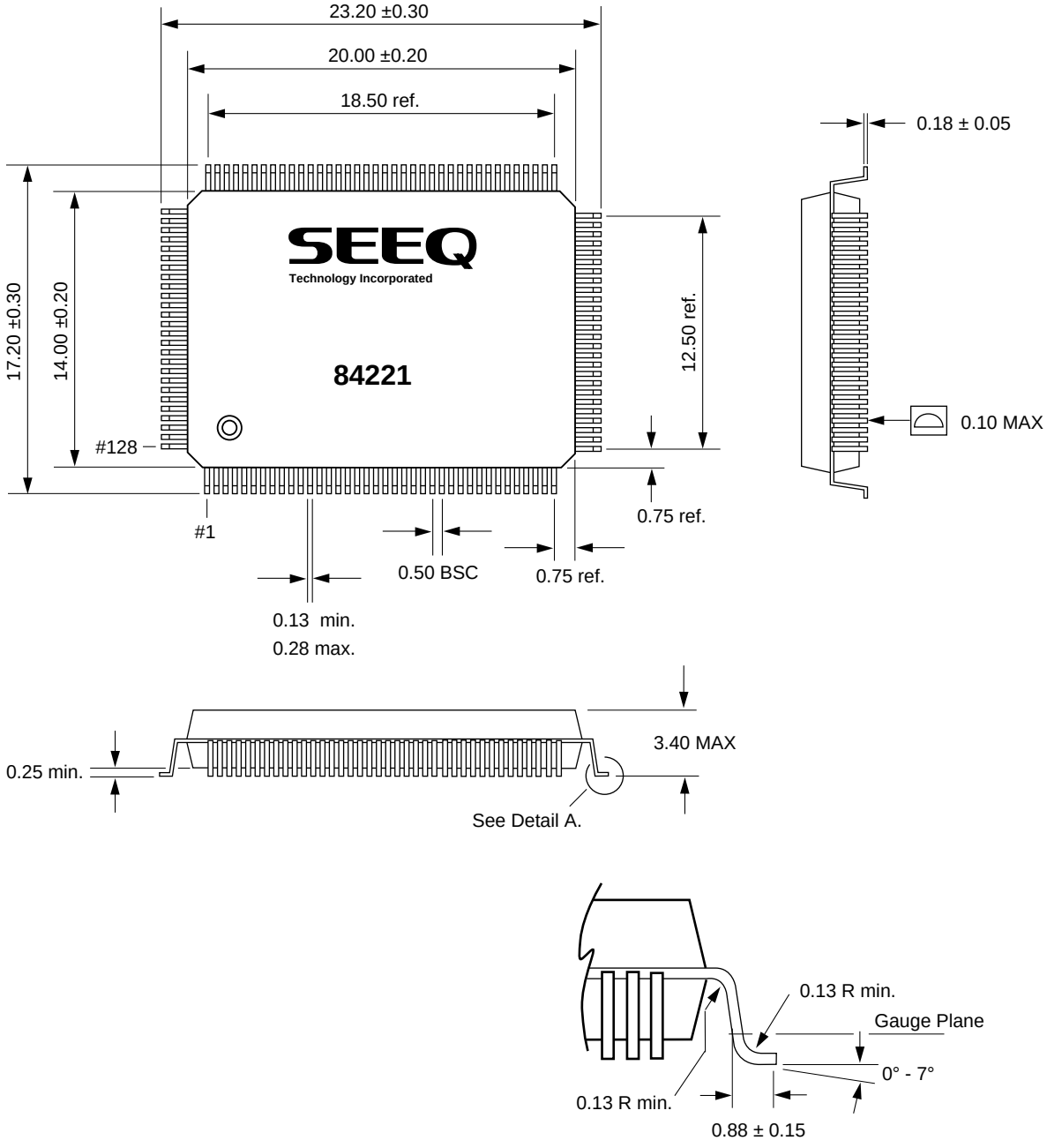
Page 19: Section 2.11.1 100 Mbps
- Paragraph #5 has had a copy change.
- Section 2.12.1 100 Mbps has had a copy change.

Page 32: Table 8. MI Serial Port Register Map
- 18 Channel Status Output , Bit X.14 is now 0, Bit X.9 and X.8 are now —, Bits X.3, X.2, X.1, X.0 are now 0.

Page 67: Figure 25. Jabber Timing
- Timing COL,and CRS have been deleted.

Page 41: Table 17. Register 18 - Channel Status Output Register Definition
- Bits 18.14, 18.9, 18.8, 18.3, 18.2, 18.1 are now blank.
- Definitions 18.14, 18.9, 18.8, 18.3, 18.2, 18.1, have been changed to Reserved.
- Symbol and name for 18.14, 18.9, 18.8, 18.3, 18.2, 18.1 are now blank.

128 Pin PQFP



Detail A.

1. All dimensions are in (millimeters).