Features

- Fast Read Access Time - 80 ns
- Low Power CMOS Operation
  - 100 µA max. Standby
  - 25 mA max. Active at 5 MHz
- Wide Selection of JEDEC Standard Packages
  - 32-Lead 600-mil PDIP and Cerdip
  - 32-Pad PLCC and LCC
  - 32-Lead 450-mil SOIC (SOP)
  - 32-Lead TSOP
- 5 V ± 10% Supply
- High Reliability CMOS Technology
  - 2000 V ESD Protection
  - 200 mA Latchup Immunity
- Rapid Programming - 100 µs/byte (typical)
- Two-line Control
- CMOS and TTL Compatible Inputs and Outputs
- Integrated Product Identification Code
- Full Military, Industrial and Commercial Temperature Ranges

4 Megabit (512K x 8) UV Erasable CMOS EPROM

Description

The AT27C040 chip is a low-power, high-performance 4,194,304 bit ultraviolet erasable and electrically programmable read only memory (EPROM) organized as 512K x 8 bits. The AT27C040 requires only one 5-V power supply in normal read mode operation. Any byte can be accessed in less than 80 ns, eliminating the need for speed reducing WAIT states on high-performance microprocessor systems.

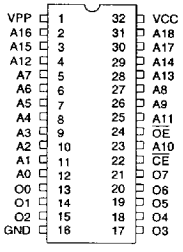
Atmel's 0.7-micron scaled CMOS technology provides for significantly lower active power consumption than competing designs. Power consumption is typically 8 mA in active mode and less than 10 µA in standby mode.

(continued)

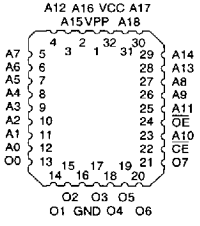
Pin Configurations

Pin Name	Function
A0-A18	Addresses
O0-O7	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable

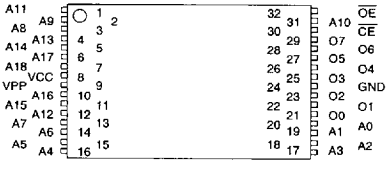
CDIP, PDIP, SOIC, Top View



LCC, PLCC Top View



TSOP Top View
Type 1



Description (Continued)

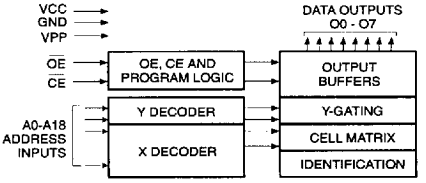
The AT27C040 comes in a choice of industry standard JEDEC-approved packages including: one-time programmable (OTP) plastic PDIP, PLCC, SOIC and TSOP, as well as windowed ceramic Cerdip and LCC. All devices feature two line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to avoid bus contention.

Atmel's AT27C040 has additional features to ensure high quality and efficient production use. The Rapid Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100 µs/byte. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

Erasure Characteristics

The entire memory array of the AT27C040 is erased (all outputs read as V_{OH}) after exposure to ultraviolet light at a wavelength of 2537Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 µW/cm^2 intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15 W•sec/cm^2. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPROM which will be subjected to continuous fluorescent indoor lighting or sunlight.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0 V to +7.0 V(1)
Voltage on A9 with Respect to Ground	-2.0 V to +14.0 V(1)
V_{PP} Supply Voltage with Respect to Ground	-2.0 V to +14.0 V(1)
Integrated UV Erase Dose	7258 W•sec/cm^2

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:
1. Minimum voltage is -0.6 V dc which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75 V dc which may overshoot to +7.0 V for pulses of less than 20 ns.

Operating Modes

Mode \ Pin	$\overline{CE}$	$\overline{OE}$	Ai	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	Ai	X(1)	V_{CC}	D_{OUT}
Output Disable	X	V_{IH}	X	X	V_{CC}	High Z
Standby	V_{IH}	X	X	X	V_{CC}	High Z
Rapid Program(2)	V_{IL}	V_{IH}	Ai	V_{PP}	V_{CC}	D_{IN}
PGM Verify	X	V_{IL}	Ai	V_{PP}	V_{CC}	D_{OUT}
PGM Inhibit	V_{IH}	V_{IH}	X	V_{PP}	V_{CC}	High Z
Product Identification(4)	V_{IL}	V_{IL}	A9=V_H (3) A0=V_{IH} or V_{IL} A1-A18=V_{IL}	X	V_{CC}	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to Programming characteristics.
3. V_H = 12.0 ± 0.5 V.
4. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.

D.C. and A.C. Operating Conditions for Read Operation

		AT27C040				
		-80	-10	-12	-15	-20
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.			-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5 V ± 10%	5 V ± 10%	5 V ± 10%	5 V ± 10%	5 V ± 10%

= Advance Information

3

D.C. and Operating Characteristics for Read Operation

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0 V to V_{CC}	Com.,Ind.		±1	µA
			Mil.		±5	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to V_{CC}	Com.,Ind.		±5	µA
			Mil.		±10	µA
I_{PP1} (2)	V_{PP} (1) Read/Standby Current	V_{PP} = V_{CC}			10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS), $\overline{CE}$ = V_{CC} ± 0.3 V			100	µA
		I_{SB2} (TTL), $\overline{CE}$ = 2.0 to V_{CC}+0.5 V			1	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz, I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}	Com.		25	mA
			Ind.,Mil.		30	mA
V_{IL}	Input Low Voltage			-0.6	0.8	V
V_{IH}	Input High Voltage			2.0	V_{CC}+0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			.45	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA		V_{CC}-0.3		V
		I_{OH} = -2.5 mA		3.5		V
		I_{OH} = -400 µA		2.4		V

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.

2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.

A.C. Characteristics for Read Operation

				AT27C040								
				-80		-10		-12		-15		-20	
Symbol	Parameter	Condition		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Units
t_{ACC} (3)	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	Com., Ind.		80		100		120		150		200	ns
			Mil.						120		150		200	ns
t_{CE} (2)	$\overline{CE}$ to Output Delay	$\overline{OE}$ = V_{IL}			80		100		120		150		200	ns
t_{OE} (2,3)	$\overline{OE}$ to Output Delay	$\overline{CE}$ = V_{IL}			35		35		35		40		60	ns
t_{DF} (4,5)	$\overline{OE}$ or $\overline{CE}$ High to Output Float				30		30		30		30		40	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first			0		0		0		0		0		ns

Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.

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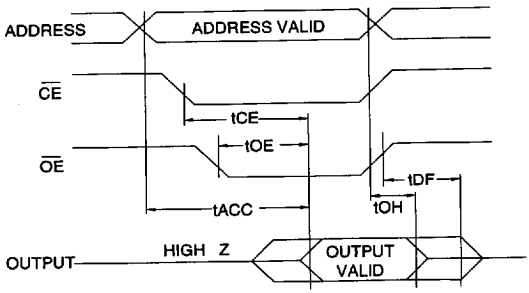
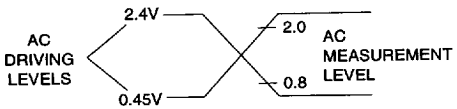
A.C. Waveforms for Read Operation [1]



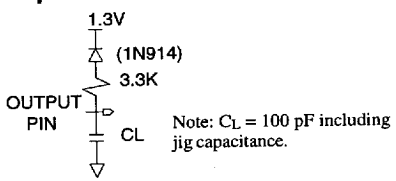
Notes:
1. Timing measurement references are 0.8 V and 2.0 V. Input AC driving levels are 0.45 V and 2.4 V, unless otherwise specified.
2. $\overline{OE}$ may be delayed up to t_{CE}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after the address is valid without impact on t_{ACC}.
4. This parameter is only sampled and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.

Input Test Waveforms and Measurement Levels



t_R, t_F < 20 ns (10% to 90%)

Output Test Load



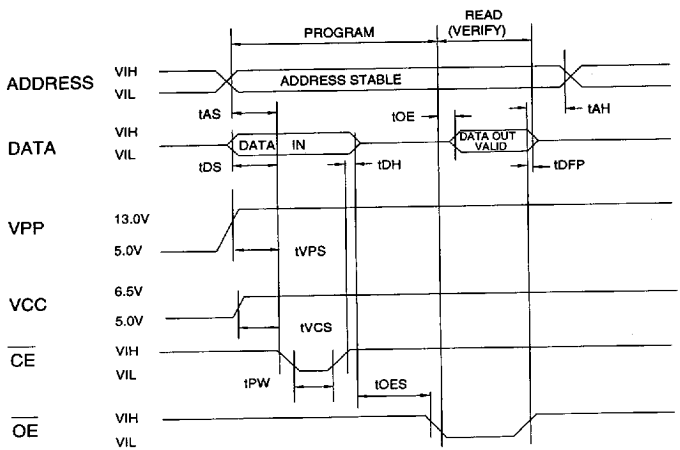
Note: C_L = 100 pF including jig capacitance.

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	8	pF	V_{IN} = 0 V
C_{OUT}	8	12	pF	V_{OUT} = 0 V

Notes: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms [1]



Notes:
1. The Input Timing Reference is 0.8 V for V_{IL} and 2.0 V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the AT27C040 a 0.1-µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

D.C. Programming Characteristics

$T_A = 25 \pm 5^oC$, $V_{CC} = 6.5 \pm 0.25$ V, $V_{PP} = 13.0 \pm 0.25$ V

Symbol	Parameter	Test Conditions	Limits Min	Limits Max	Units
I_{LI}	Input Load Current	$V_{IN}=V_{IL},V_{IH}$		10	µA
V_{IL}	Input Low Level	(All Inputs)	-0.6	0.8	V
V_{IH}	Input High Level		2.0	$V_{CC}+.7$	V
V_{OL}	Output Low Volt.	$I_{OL}=2.1$ mA		.45	V
V_{OH}	Output High Volt.	$I_{OH}=-400$ µA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			40	mA
I_{PP2}	V_{PP} Supply Current	$\overline{CE}=V_{IL}$		20	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

A.C. Programming Characteristics

$T_A = 25 \pm 5^oC$, $V_{CC} = 6.5 \pm 0.25$ V, $V_{PP} = 13.0 \pm 0.25$ V

Symbol	Parameter	Test Conditions* (see Note 1)	Limits Min	Limits Max	Units
t_{AS}	Address Setup Time		2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{OE}$ High to Output Float Delay	(Note 2)	0	130	ns
t_{VPS}	V_{PP} Setup Time		2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{CE}$ Program Pulse Width	(Note 3)	95	105	µs
t_{OE}	Data Valid from $\overline{OE}$	(Note 2)		150	ns

*A.C. Conditions of Test:

Input Rise and Fall Times (10% to 90%) ..... 20 ns
Input Pulse Levels ..... 0.45 V to 2.4 V
Input Timing Reference Level ..... 0.8 V to 2.0 V
Output Timing Reference Level ..... 0.8 V to 2.0 V

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
3. Program Pulse width tolerance is 100 µsec ± 5%.

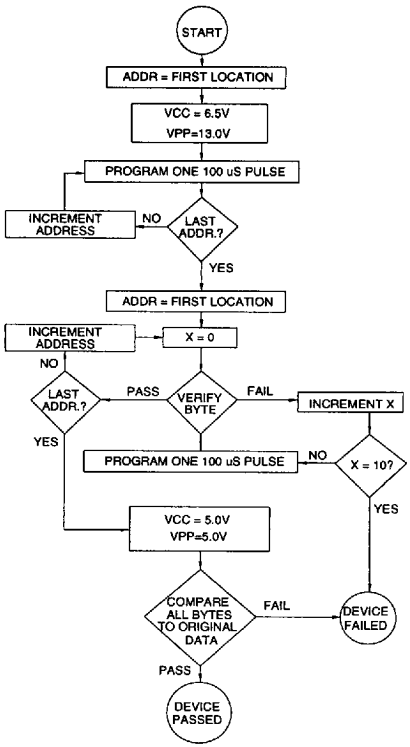
Atmel's 27C040 Integrated Product Identification Code

Codes	Pins A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	0	0	0	0	1	0	1	1	0B

3

Rapid Programming Algorithm

A 100 µs $\overline{CE}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5 V and V_{PP} is raised to 13.0 V. Each address is first programmed with one 100 µs $\overline{CE}$ pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100 µs pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. V_{PP} is then lowered to 5.0 V and V_{CC} to 5.0 V. All bytes are read again and compared with the original data to determine if the device passes or fails.



Ordering Information

= Advance Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
80	25	0.1	AT27C040-80DC AT27C040-80JC AT27C040-80LC AT27C040-80PC AT27C040-80RC AT27C040-80TC	32DW6 32J 32LW 32P6 32R 32T	Commercial (0°C to 70°C)
80	30	0.1	AT27C040-80DI AT27C040-80JI AT27C040-80LI AT27C040-80PI AT27C040-80RI AT27C040-80TI	32DW6 32J 32LW 32P6 32R 32T	Industrial (-40°C to 85°C)
100	25	0.1	AT27C040-10DC AT27C040-10JC AT27C040-10LC AT27C040-10PC AT27C040-10RC AT27C040-10TC	32DW6 32J 32LW 32P6 32R 32T	Commercial (0°C to 70°C)
100	30	0.1	AT27C040-10DI AT27C040-10JI AT27C040-10LI AT27C040-10PI AT27C040-10RI AT27C040-10TI	32DW6 32J 32LW 32P6 32R 32T	Industrial (-40°C to 85°C)
120	25	0.1	AT27C040-12DC AT27C040-12JC AT27C040-12LC AT27C040-12PC AT27C040-12RC AT27C040-12TC	32DW6 32J 32LW 32P6 32R 32T	Commercial (0°C to 70°C)
120	30	0.1	AT27C040-12DI AT27C040-12JI AT27C040-12LI AT27C040-12PI AT27C040-12RI AT27C040-12TI	32DW6 32J 32LW 32P6 32R 32T	Industrial (-40°C to 85°C)
120	30	0.1	AT27C040-12DM AT27C040-12LM	32DW6 32LW	Military (-55°C to 125°C)
150	25	0.1	AT27C040-15DC AT27C040-15JC AT27C040-15LC AT27C040-15PC AT27C040-15RC AT27C040-15TC	32DW6 32J 32LW 32P6 32R 32T	Commercial (0°C to 70°C)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	30	0.1	AT27C040-15DI AT27C040-15JI AT27C040-15LI AT27C040-15PI AT27C040-15RI AT27C040-15TI	32DW6 32J 32LW 32P6 32R 32T	Industrial (-40°C to 85°C)
			AT27C040-15DM AT27C040-15LM	32DW6 32LW	Military (-55°C to 125°C)
			AT27C040-15DM/883 AT27C040-15LM/883	32DW6 32LW	Military/883D Class B, Fully Compliant (-55°C to 125°C)
200	25	0.1	AT27C040-20DC AT27C040-20JC AT27C040-20LC AT27C040-20PC AT27C040-20RC AT27C040-20TC	32DW6 32J 32LW 32P6 32R 32T	Commercial (0°C to 70°C)
200	30	0.1	AT27C040-20DI AT27C040-20JI AT27C040-20LI AT27C040-20PI AT27C040-20RI AT27C040-20TI	32DW6 32J 32LW 32P6 32R 32T	Industrial (-40°C to 85°C)
200	30	0.1	AT27C040-20DM AT27C040-20LM	32DW6 32LW	Military (-55°C to 125°C)
			AT27C040-20DM/883 AT27C040-20LM/883	32DW6 32LW	Military/883D Class B, Fully Compliant (-55°C to 125°C)

Package Type	
32DW6	32 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
32LW	32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
32P6	32 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
32R	32 Lead, 0.450" Wide, Plastic Gull Wing Small Outline OTP (SOIC)
32T	32 Lead, Plastic Thin Small Outline Package OTP (TSOP)