

Description

The GL3917 has been designed to recover data from composite video type signals in KBPS VCR. As well as receiving data, the GL3917 will resynchronize a clock output to the data stream and also provide a composite sync output.

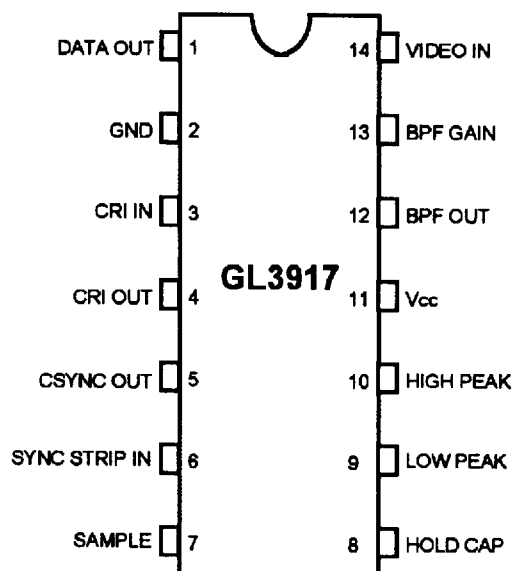
Features

- No Adjustments Required
- Open Collector Output for Up to 12V (TTL Compatible Output)
- Signal Level Insensitivity (Edge Detection)

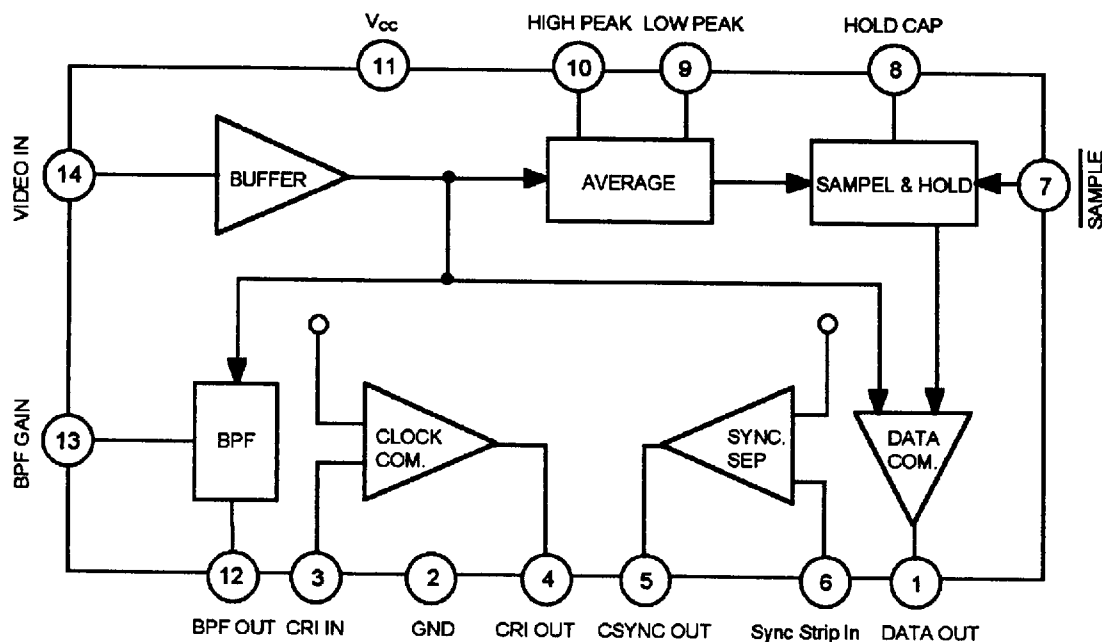
Absolute Maximum Ratings ($T_A=25^\circ\text{C}$)

Supply Voltage	V_{CC}	15	V
Power Dissipation	P_D	660	mW
Operating Temperature	T_{OPR}	-20 to 70	$^\circ\text{C}$
Storage Temperature	T_{STG}	-35 to 135	$^\circ\text{C}$

Pin Configuration



Block Diagram



Electrical Characteristics ($T_A=25^{\circ}\text{C}$, $V_{CC}=12\text{V}$)

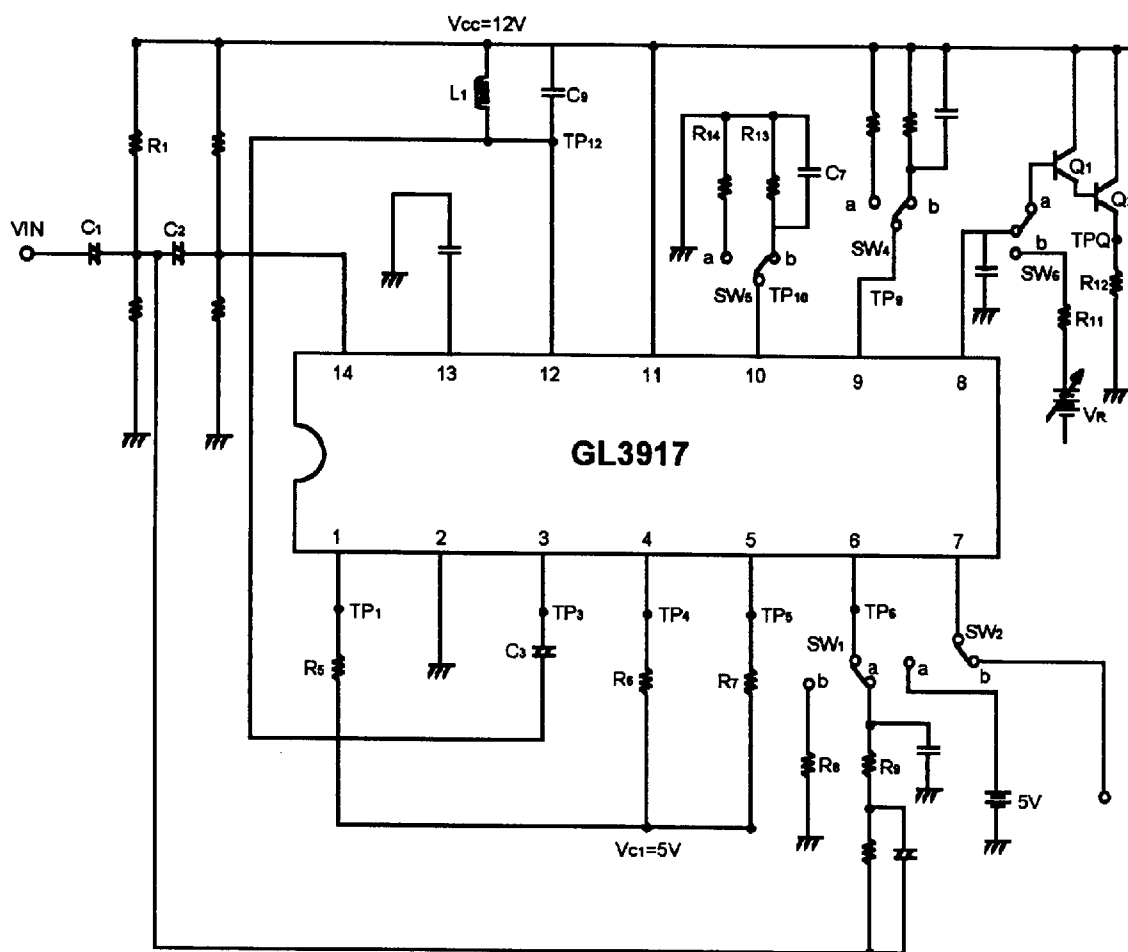
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	No Signal	10.8	12	13.2	V
Quiescent Current	I_{CC}	No Signal	13	19	25	mA
Pin 3 DC Voltage	V_{P3}	$V_{CC} = 12\text{V}$ No Signal	2.6	2.8	3.0	V
Pin 6 DC Voltage	V_{P6}	$V_{CC} = 12\text{V}$ No Signal	8.2	8.8	9.4	V
Pin 8 DC Voltage	V_{P8}	$V_{CC} = 12\text{V}$ No Signal	5.6	6.3	6.9	V
Pin 9 DC Voltage	V_{P9}	$V_{CC} = 12\text{V}$ No Signal	6.6	7.3	7.9	V
Pin 10 DC Voltage	V_{P10}	$V_{CC} = 12\text{V}$ No Signal	4.0	4.6	5.2	V
Pin 13 DC Voltage	V_{P13}	$V_{CC} = 12\text{V}$ No Signal	4.2	4.6	5.0	V
Pin 14 DC Voltage	V_{P14}	$V_{CC} = 12\text{V}$ $1V_{P-P}$, $f_{IN}=503\text{KHz}$, Sinewave	5.7	6	6.3	V
CRI Output Low Level	$V_{L, CRI}$	$V_{CC} = 12\text{V}$ $40mV_{rms}$, $f_{IN}=503\text{KHz}$, Sinewave	—	0.2	0.6	V
CRI Output High Level	$V_{H, CRI}$	$V_{CC} = 12\text{V}$ $40mV_{rms}$, $f_{IN}=503\text{KHz}$, Sinewave	4	5	—	V
CRI Output Rising Time	t_r, CRI	$V_{CC} = 12\text{V}$ $40mV_{rms}$, $f_{IN}=503\text{KHz}$, Sinewave	—	200	500	ns
CRI Output Falling Time	t_f, CRI	$V_{CC} = 12\text{V}$ $40mV_{rms}$, $f_{IN}=503\text{KHz}$, Sinewave	—	250	500	ns
High Peak Attack Time	HPat	$V_{CC} = 12\text{V}$ $1V_{P-P}$, $f_{IN}=20\text{KHz}$, Squarewave	—	200	700	ns
High peak Decay Time	HPdt	$V_{CC} = 12\text{V}$ $1V_{P-P}$, $f_{IN}=20\text{KHz}$, Squarewave	3.5	10.5	—	μs
Low peak Attack Time	LPat	$V_{CC} = 12\text{V}$ $1V_{P-P}$, $f_{IN}=20\text{KHz}$, Squarewave	3.5	10.5	—	μs
Low peak Decay Time	LPdt	$V_{CC} = 12\text{V}$ $1V_{P-P}$, $f_{IN}=20\text{KHz}$, Squarewave	—	200	700	ns
S/H Slew rate	$S_{R, SH}$	$V_{CC} = 12\text{V}$ $1V_{P-P}$, $f_{IN}=20\text{KHz}$, Squarewave	1.6	2.3	—	V/ μs
Data Output Low Level	$V_{L, data}$	$V_{CC} = 12\text{V}$ $354mV_{rms}$, $f_{IN}=503\text{KHz}$, Sinewave	—	0.2	0.6	V
Data Output High Level	$V_{H, data}$	$V_{CC} = 12\text{V}$ $354mV_{rms}$, $f_{IN}=503\text{KHz}$, Sinewave	4.0	5.0	—	V
Data Output Pulse Width	$P_W, data$	$V_{CC} = 12\text{V}$ $88mV_{rms}$, $f_{IN}=503\text{KHz}$, Sinewave	0.9	0.994	1.1	μs
Data Output Rising Time	$t_r, data$	$V_{CC} = 12\text{V}$ $354mV_{rms}$, $f_{IN}=503\text{KHz}$, Sinewave	—	50	100	ns
Data Output Falling Time	$t_f, data$	$V_{CC} = 12\text{V}$ $354mV_{rms}$, $f_{IN}=503\text{KHz}$, Sinewave	—	50	100	ns
Data Output Duty Time	$P_d, data$	$V_{CC} = 12\text{V}$ $354mV_{rms}$, $f_{IN}=503\text{KHz}$, Sinewave	0.9	0.994	1.1	μs



Pin Description

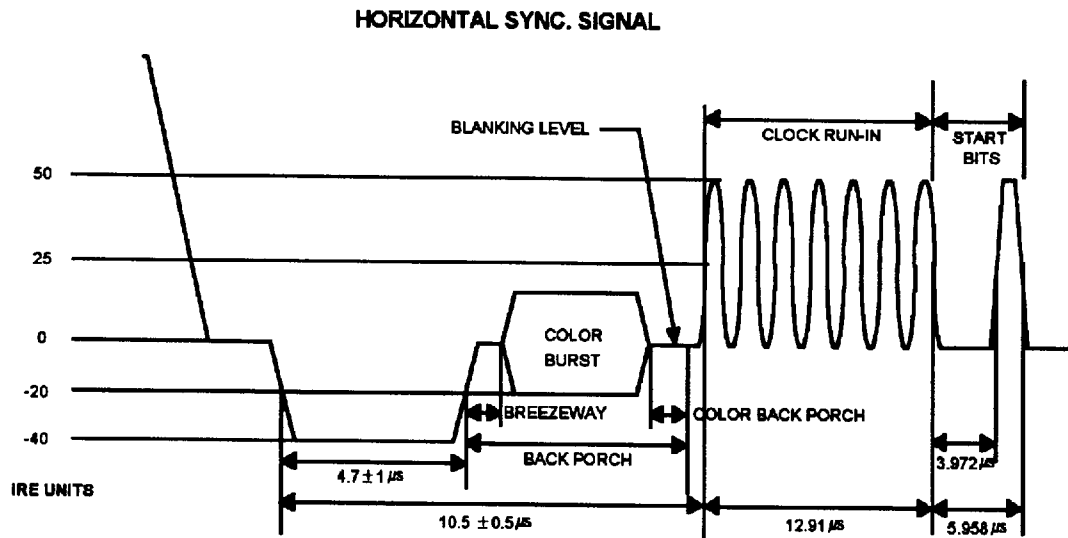
No.	Item	Explanation	No.	Item	Explanation
1	Data Out	Data slice output	8	Hold Cap.	Data Slice Level Molding
2	GND	Ground	9	Low Peak	Low Peak Detection
3	CRI In	Clock Run In Input	10	High Peak	High Peak Detection
4	CRI Out	Clock Run In Slice Output	11	Vcc	Power Supply
5	Csync. Out	Composite Sync Slice Output (Composite Video Signal)	12	BPF Out	Extraction of CRI from Composite Video
6	Sync. Strip In	Composite Sync Slice Input (Composite Video Signal)	13	BPF Gain	Adjust Gain of BPF
7	SAMPLE	Sample and Hold Control Pulse Input	14	Video In	Composite Video Signal Input

AC Test Circuit

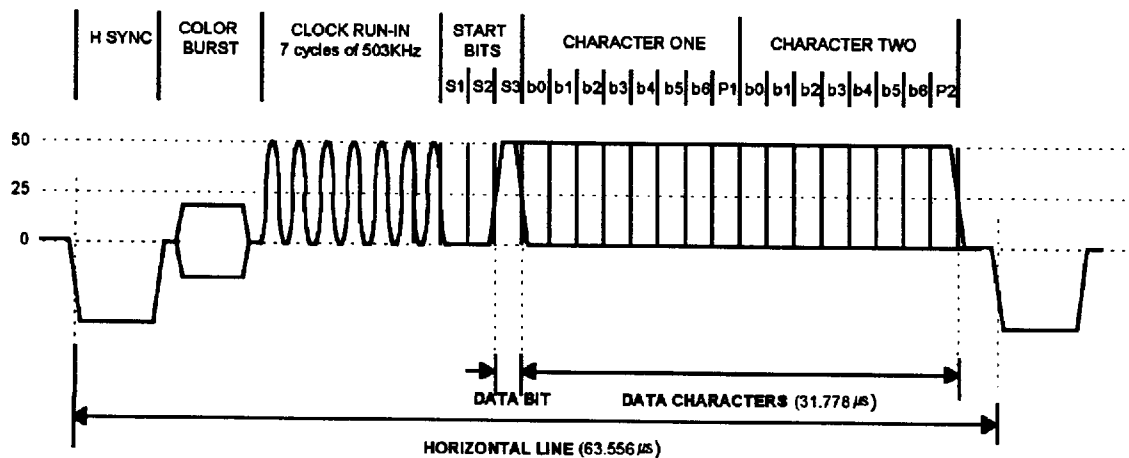




Data Timing



Data Signal format

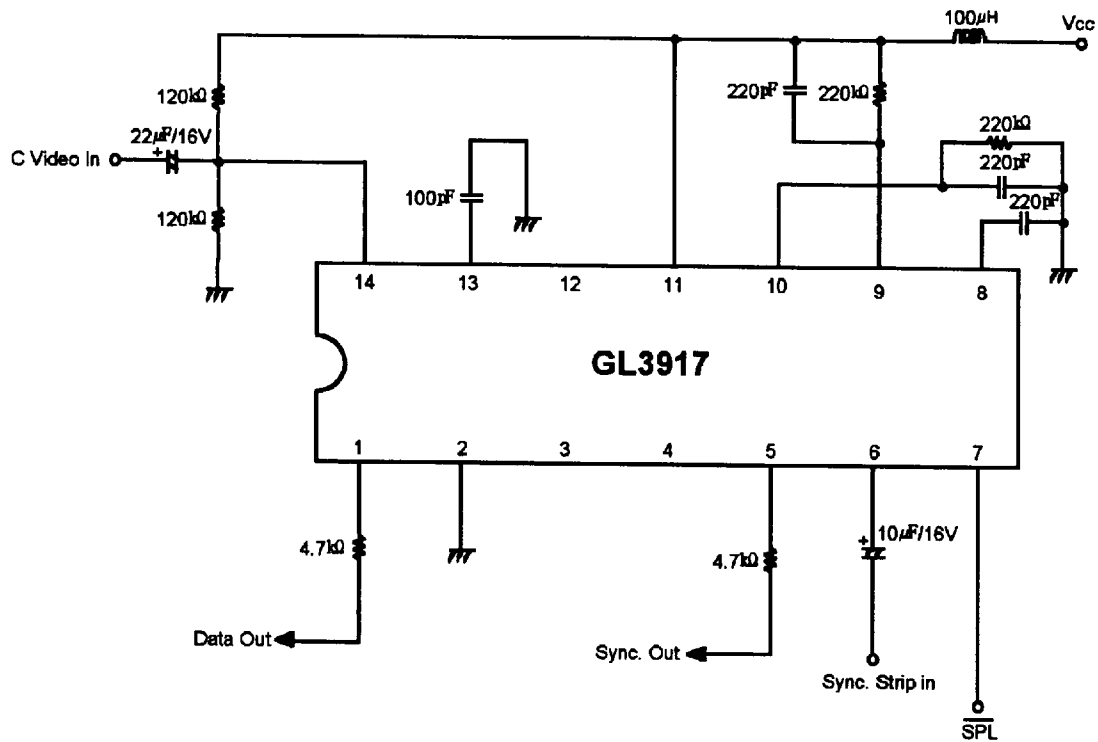


NOTES :

- 1) The Horizontal line frequency f_H is nominally 15734.26 Hz $\pm$ 0.05 Hz. Interval D shall be adjusted to $D=1/(f_H \times 32)$ for the instantaneous f_H at line 21.
- 2) The Clock Run In signal consist of 7.0 cycles of a 0.5034965 MHz (1/D) sinewave when measured from the leading to trailing 0 IRE point. The sinewave is to be symmetrical about the 25 IRE level.
- 3) The negative going midpoints (half amplitude) of the Clock Run In shall be coherent with the midpoints (half amplitude) of the Start and Data bit transitions.
- 4) These values have been chosen to accomodate signals generated by some existing encoders.
- 5) Two characters, each consisting of 7 Data bits and 1 Odd Parity bit.



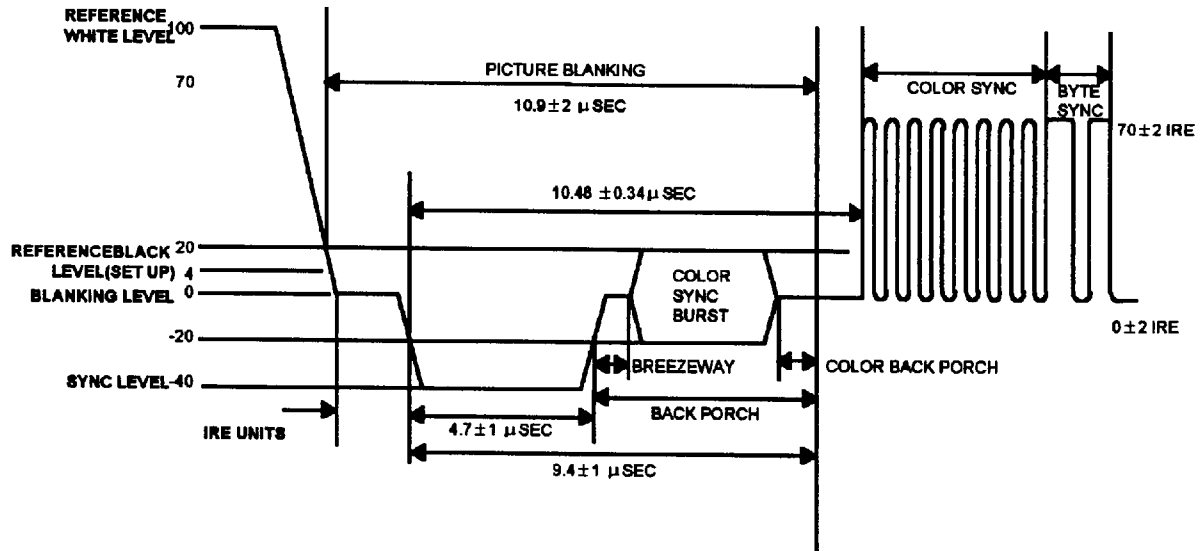
Application Circuit





Data Timing

HORIZONTAL SYNC & BLANKING



Data Line Structure

