Semicustom

Bi-CMOS

ASTRO MASTER IV Specification
(for PLL frequency synthesizers)

MB1570 Series

■ DESCRIPTION

The ASTRO MASTER IV is a master-slice type semi-custom LSI ideal for use in high-frequency front-end circuits in VCO, amplifier, mixer and I/Q modulator devices.

The MB1570 series features an analog circuit unit that is a more highly integrated version of the ASTRO MASTER I series.

The PLL, prescaler and high-frequency analog circuits can be designed to users' specifications using FUJITSU's standard macro cells as well as customized macro cells.

This LSI series uses FUJITSU's latest process technology for power-saving operation and master-slice semi-custom design to reduce lead times and lower costs. In addition, the ultra-compact flat package helps maintain circuit confidentiality, and contributes to lighter, more compact design by reducing the number of components.

The ASTRO MASTER IV is ideal for high-frequency applications, particularly mobile communication devices operating on digital specifications such as PCN, DECT, PHS and so on.

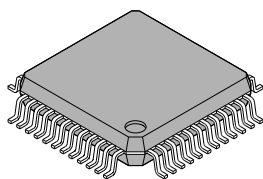ASTRO: Advanced Semi-Custom Technology of Super PLL with RF System on LSI.

■ FEATURES

- PLL circuits can be customized for operating frequency, logical circuits, etc.
- High frequency analog circuits with adjustable resistance levels
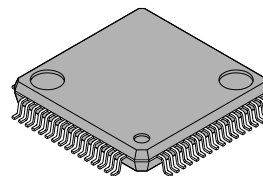
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■ PACKAGES

48-pin Plastic LQFP

64-pin Plastic LQFP

(FPT-48P-M05)

(FPT-64P-M03)

(Continued)
- High speed operating capacity to 3.0 GHz
- On-chip low-current consumption and power-saving circuits
- On-chip high-speed lockup function
- Supply voltage: 2.7 V to 3.3 V (minimum operating voltage to 2.0 V min.)
- Development time (standard): approx. 10 weeks

■ LINEUP

Series	Prescaler	PLL	Analog circuits	Operating frequency	Package	Remarks
					LQFP	
MB1570	2 circuits	2 circuits	6 circuits	3.0 GHz	48 64	For dual frequency synthesizers

■ CHIP LAYOUT

• MB1570 Series
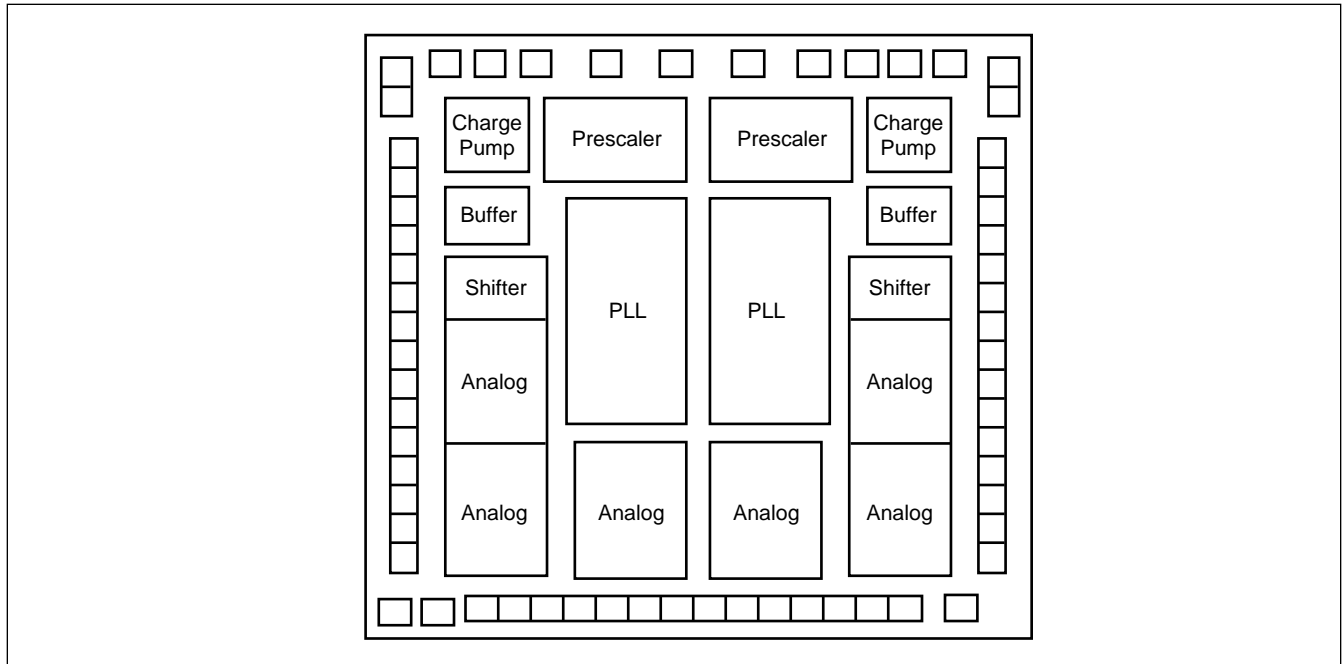
• Analog Cell
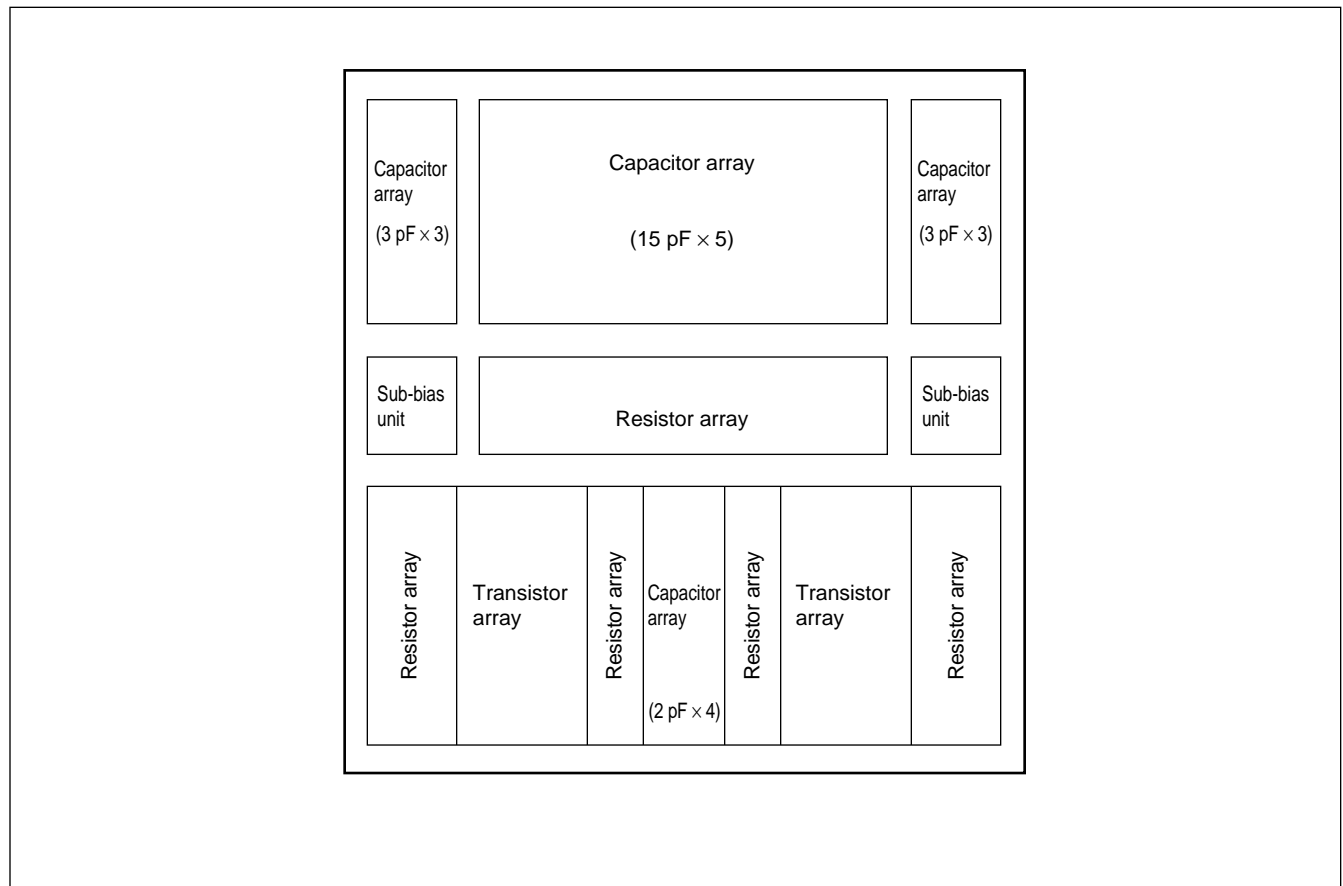
MB1570 Series

■ MACRO CELL DESCRIPTIONS

1. Prescaler

Divides the reference frequency by any given value and outputs the resulting frequency. Choice of two-modulus or fixed output mode.

2. PLL

- **Phase comparator**
The phase comparator has a phase detection range of -2π to $+2\pi$, and is designed to eliminate blind spots in phase comparison by output of a margin-of-error signal to the charge pump even when the phase difference is zero. Phase comparator characteristics can also be tuned to the polarity of VCO.

- **Counters**
The divide ratios of the comparator-side counter and reference-side counter can be either programmable or fixed.

- **Charge pump**
The "H" level output voltage from the charge pump is determined by power supply voltage. Charge pump characteristics for the sending and receiving systems can be optimized for each specific application.
For example, when FM modulation is applied directly to the VCO signal, charge pump characteristics can be adjusted for lower speeds in order to reduce the sensitivity of the synthesizer loop so that output does not track the modulation.

- **Analog switch**
When switching frequencies, the analog switch can be used to switch the capacitance of the low pass filter, to reduce the time constant in the filter and the load on the charge pump. This enables higher lock-up speed. Switch control is synchronous with the LE signal, to that the analog switch is on when the LE signal is "high".

- **High speed lock-up circuit**
This circuit is specially designed for faster lock-up speeds.

- **Intermittent operation control circuit**
This on-chip power-saving function reduces circuit current flow in standby status, enabling devices to operate with less power demand. A special circuit is built in to prevent excessive error signal from increasing lock-up delay during the transition from power-saving mode to operating mode.

- **List of standard macro cells**

Type	Vcc	Icc	Operating frequency	Prescaler divide ratio	Comparator counter divide ratio (M)	Swallow counter divide ratio (A)	Reference counter divide ratio (R)
PLL1	3V	4 mA	1.1 GHz	64/65	16 to 2047	0 to 127	8 to 16383
PLL2		6 mA	2.0 GHz				

Crystal oscillator input frequency: Up to 32 MHz
Standby mode current demand: 100 μA

4

3. High Frequency Analog Cells

- **Mixer**
  Active type double-balanced mixer

- **IF amplifier**
  The IF amplifier is configured from a differential amplifier plus an NPN transistor using emitter-follower output from the differential amplifier.

- **RF amplifier**
  Provides emitter-follower output of the output signal from the emitter-ground circuit. The RF input side can be connected to an internal bias circuit.

- **VCO**
  Configured from an oscillator transistor in a base-ground Colpitts type oscillator circuit, plus a transistor acting as output buffer. Can be connected to external devices such as varicap or resonator.

- **Orthogonal modulator**
  An orthogonal modulator is used for IF frequency modulation. In addition, a flip-flop type 90° phase shift circuit can be included in the configuration.

Note: Circuit format and other details can be adjusted to meet customer requirements.

■ CIRCUIT OPERATING DESCRIPTIONS

1. Intermittent Operation Control Circuit

The intermittent operation control circuit operates the LSI circuits during communication operations and at all other times places the chip in standby status to reduce power demand.

(1) Circuit operation in operating mode

All circuits are in operating status, and the chip performs normal PLL operations.

(2) Circuit operation in standby mode

All circuits that can be stopped without interfering with operation are shut down, and the chip goes into low-power operating mode.

Latch data:	Saves immediately preceding data
Shift register:	Data input enabled
Charge pump output:	High impedance
VCO input voltage:	Saves voltage level stored in low-pass filter during the last operating mode

<Caution> The digital system power supply must still be applied in standby mode.

2. Phase Lock Detection Circuit

To detect phase lock condition from the LD signal pin output, the T-bit should be selected. When the phase difference is greater than tw, the LD pin will output an L level signal, and when the difference is less than tw for 3 or more cycles, the output will change to H level. The length of the tw time interval can be set in the range of 625 ns to 1250 ns by connection to the crystal oscillator.

• **LD Signal operating status**

Operating status	PLL circuit	LD output
Standby mode	Standby	H
Operating mode	Un-lock	L
	Lock	H

3. High Speed Tuning Circuit

The following high speed tuning circuits are available for use according to specific applications.

• **High speed tuning circuits for ASTRO MASTER IV**

| Function	Operation	Optimum applications
Analog switch	Circuit temporarily reduces LPF time constant at lock-up.	Analog portable phone devices (receiving system)
Turbo circuits	For broad-band steps, circuit forcibly switches charge pump on/off	PHS devices
Supercharger circuit	Circuit increases charge pump drive capacity	PHS devices
Hypercharger circuit	Circuit further enhances the drive capacity of the supercharger circuit	PDC, GSM etc.

■ SERIAL DATA

1. Data Bit Configuration

PLL operating settings are made through serial data input. The standard serial format is shown in the table below. Serial data is entered MSB-first, and the data length is in the range of 22 to 37 bits.

• Standard format for serial data

Bit name (abbreviation)		Functional description	Standard bit count
Control bit (CNT bit)		Selects transfer destination (sending or receiving system)	1 to 2
LD select bit (T-bit)		Selects LD output	1 to 2
FC bit (F-bit)		Switches the phase of phase comparator	1
Programmable counter bit (N-bit)		Sets the programmable counter's divide ratio	11
Swallow counter bit (A-bit)		Sets the swallow counter's divide ratio	7
Reference counter bit (R-bit)	Fixed	Sets the reference counter's divide ratio	1 to 2
	Programmable		14

2. Serial Data Input Timing

After the serail data is stored in the shift register, it can be transferred to the latch circuit by means of the LE signal.
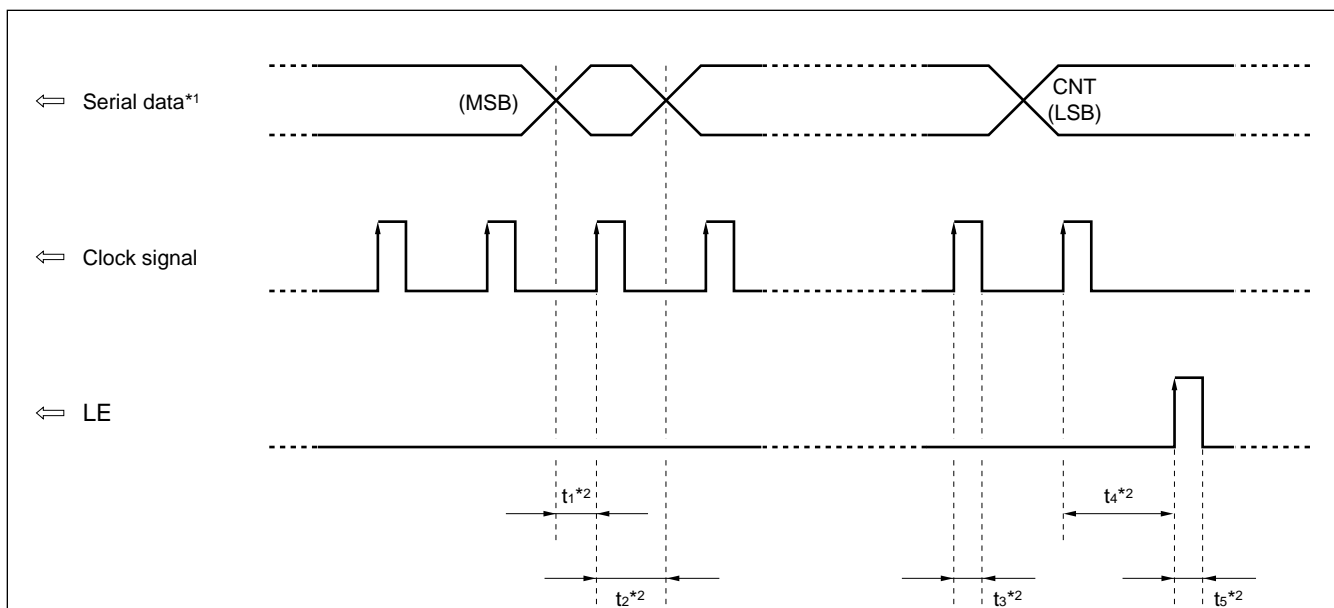
*1: Serial data is input, MSB-first.
*2: $100 \text{ ns} \leq t_1, t_4$ $300 \text{ ns} \leq t_3$ $800 \text{ ns} \leq t_5$ $1000 \text{ ns} \leq t_2$

Notes: • Data input utilizes the serial data, clock and LE signals at supply voltage or lower levels
  • Shift register data is updated sequentially each time the clock signal is input. Data is synchronized with the rising edge of the clock signal, and is read sequentially into the shift register, MSB-first.
  • After LSB input, the LE signal is changed from L level to H level.
  • Shift register data is transferred to the latch circuit while the LE signal is at H level.
  • Each input signal pin has a Schmitt trigger circuit to protect against abnormal operation due to noise.

MB1570 Series

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min.	**Max.**	
Supply voltage*	V_{CC}	−0.5	+4.0	V
Input voltage*	V_{IN}	−0.5	V_{CC} +0.5	V
Output current	I_{OUT}	−10	10	mA
Storage temperature	Tstg	−55	+125	°C

* : Voltage values are based on GND = 0 V.

Note: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min.	**Typ.**	**Max.**	
Supply voltage*1	V_{CC}	2.7*	—	3.3	V
	GND	—	0	—	V
Operating temperature	Ta	−40	—	+85	°C

*1: Voltage values are based on GND = 0 V
*2: Operation is assured to the minimum operating voltage level of 2.0 V min.

■ **ANALOG CIRCUIT CHARACTERISTICS**

Circuit	Parameter		Conditions	Value (typ.)	Unit
VCO	Supply voltage		—	3.0	V
	Current demand		—	11	mA
	Operating frequency		—	900	MHz
	C/N ratio		Offset frequency = 25 kHz, Band width = 16 kHz	77	dB
	S/N ratio		BW = 0.3 to 3 kHz, 3 kHz/Dev	44	dB
	Output power		—	−2	dBm
	Conversion gain		—	6	MHz/V
Mixer	Supply voltage		—	3.0	V
	Current demand		—	12	mA
	Operating frequency	IF	—	800	MHz
		LO	P_{LO} = −10 dBm	110	MHz
		RF	$f_{RF} = f_{LO} + f_{IF}$	910	MHz
	Conversion gain		—	6	dB
	Maximum output power		—	−11	dBm
	1 dB compression point		Output level	−15	dBm
	Intercept point		Input level	−8	dBm
	NF		DSB measurement	12	dB
Amplifier	Supply voltage		—	3.0	V
	Current demand		—	6	mA
	Operating frequency		—	900	MHz
	Gain		f = 900 MHz (−30 dBm in)	14	dB
	Maximum output power		f = 900 MHz	−3	dBm
	1 dB compression point		f = 900 MHz, output level	−8	dBm
	Intercept point		f = 900 MHz, 900.1 MHz, input level	−12	dBm
	NF		f = 900 MHz	2.2	dB

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Circuit	Parameter		Conditions	Value (typ.)	Unit
Orthogonal modulator	Supply voltage		—	3.0	V
	Current demand		—	25	mA
	Operating frequency	LO1	$P_{LO1} = -5$ dBm	500	MHz
		LO2	$P_{LO2} = -5$ dBm	1650	MHz
		RF	$f_{RF} = f_{LO2} + f_{LO1/2}$	1900	MHz
	Output level		—	−14	dBm
	Modulator precision	Amplitude deviation	RMS Magnitude Error	1.9	%
		Phase deviation	RMS Phase Error	0.9	deg.
		Vector error	RMS Vector Error	2.4	%
	Carrier leak		—	−31	dBc

■ ANALOG SYSTEM: BASIC EQUIVALENT CIRCUITS

1. Mixer, IF Amplifier

The MB1570 series features an active-type double-balanced mixer. The LO and RF output can be connected to an internal bias circuit. The mixer output is connected through on-chip load resistor to the chip's power supply, and then to the next-stage IF amplifier. The IF amplifier is configured from a differential amplifier and NPN transistor, and provides emitter-follower differential amplifier output.
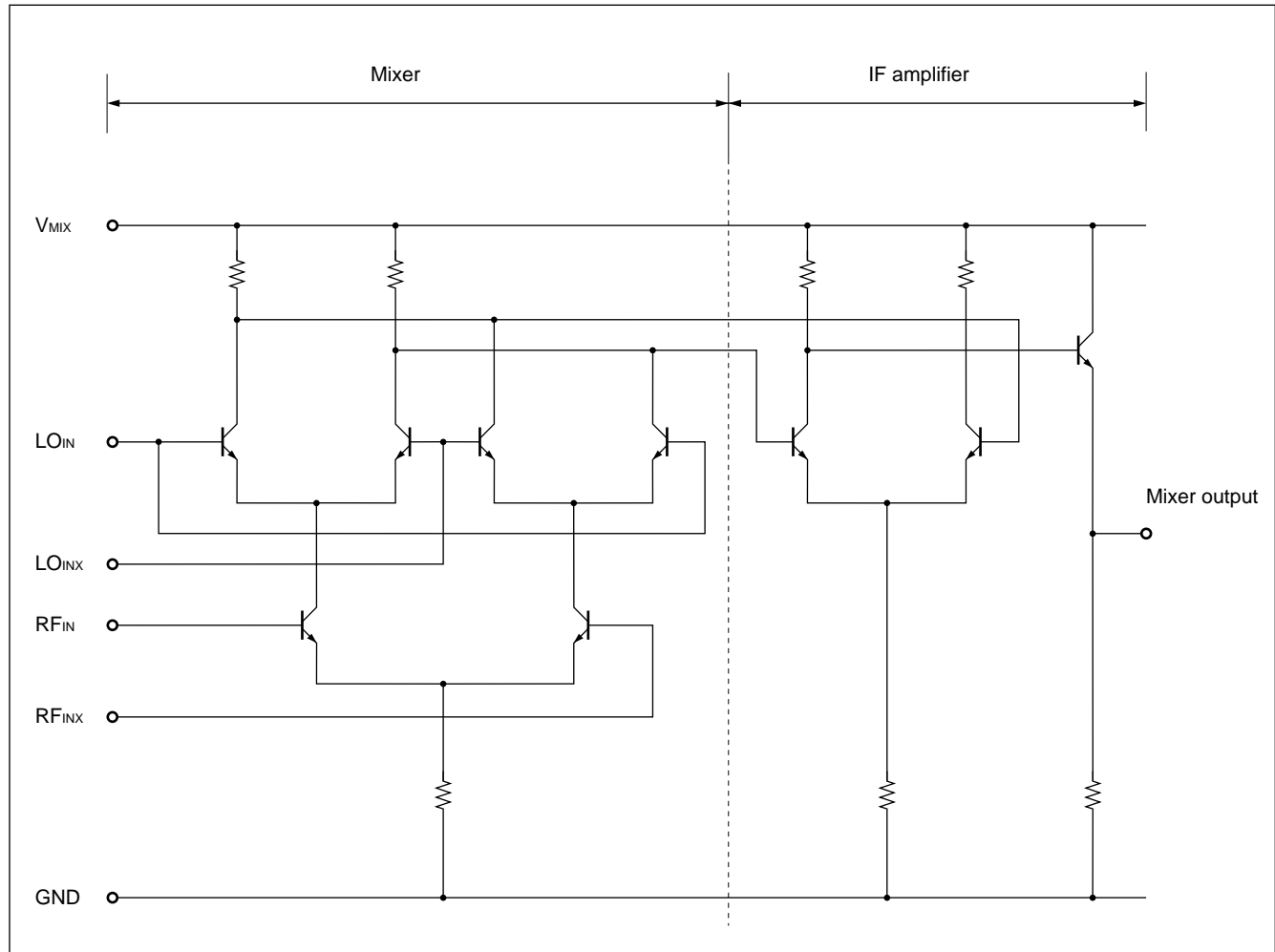
MB1570 Series

2. RF Amplifier

The emitter-ground circuit output signal is output as an emitter-follower signal. The RF input can be grounded to an internal bias circuit.
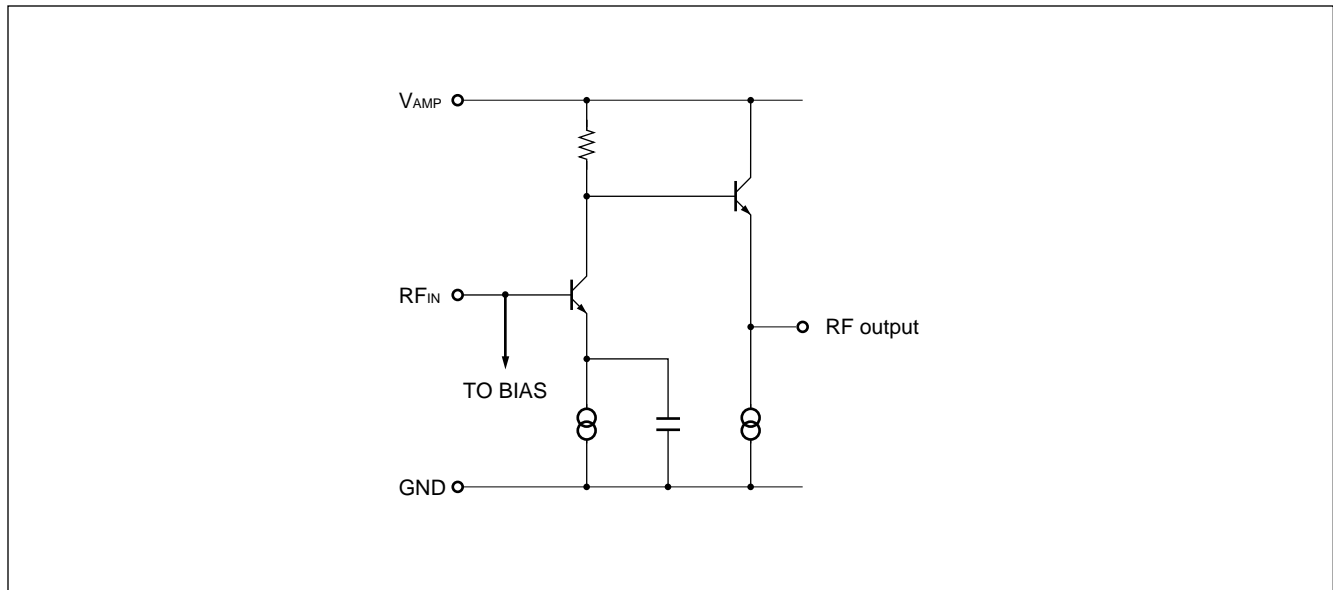
3. VCO Amplifier

The VCO amplifier is configured from an oscillator transistor in a base-ground Colpitts type oscillator circuit, plus a transistor acting as output buffer. The VCO amplifier can be connected to external devices such as varicap or resonator.
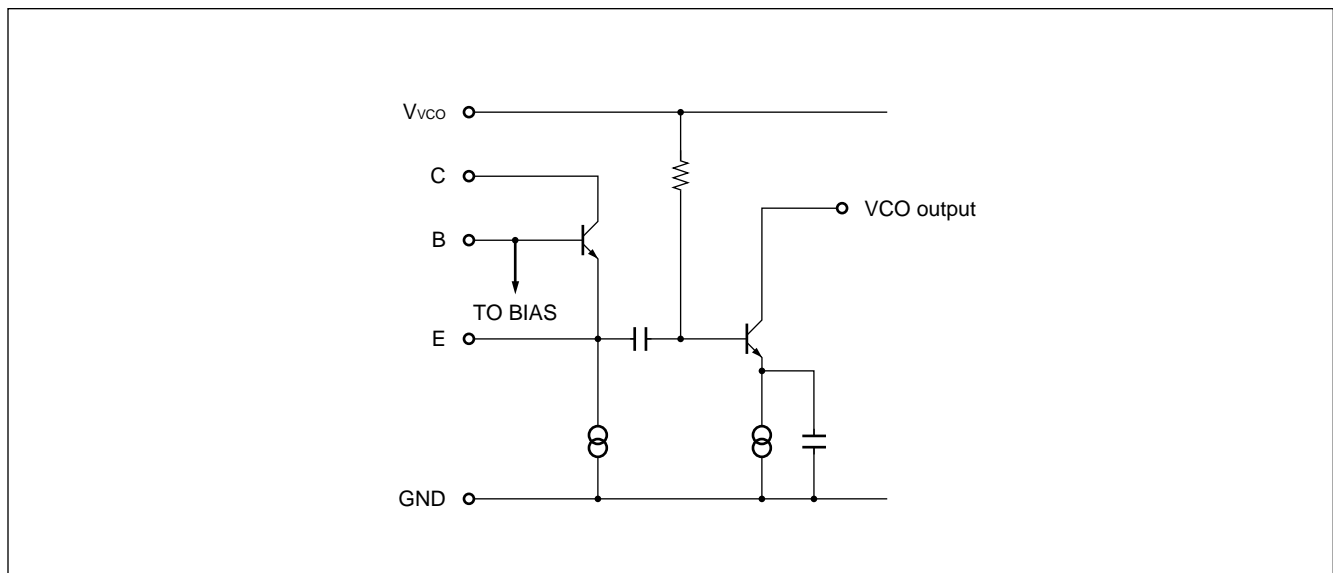
■ DEVELOPMENT PROCESSES

Each product in the ASTRO MASTER IV series is developed through the following processes, based on requirements and specifications supplied by the customer.

1. Feasibility Study

(1) Product specifications and development process study

FUJITSU conducts simulations based on documentation provided by the customer, in order to evaluate the technical and economic feasibility of each proposed design.

Product Documentation

Technical documentation: Functional descriptions, I/O signal descriptions, block diagrams.

Characteristics documentation: For prescalers, PLL, VCO, mixers, amplifiers, etc.

Development Documentation

Delivery schedule documentation: Development schedule, division of responsibilities, etc.

Cost estimates: Volume requirements, development costs, target prices

(2) Product feasibility evaluation

Based on the foregoing studies, FUJITSU and the customer meet to evaluate feasibility.

(3) Development of planned specifications

Circuit functions and characteristics are studied in detail, and circuit specifications and testing specifications are developed. After specifications have been determined, final estimates of the development schedule, timing and cost, and the product price can be produced.

(4) Approval of provisional delivery specifications

After FUJITSU and the customer have determined the feasibility of product development, a provisional delivery schedule is agreed upon.

MB1570 Series

Customer   FUJITSU

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┌─────────────────────────┐      (1)      ┌─────────────────────────┐
( Product specifications,  )───────────────│ Functional study, cost  │
(  conditions for estimation)              │ estimation              │
└─────────────────────────┘               └─────────────────────────┘
            ▲                                          │
            │                                          ▼
            │                                    (2)  ╱◇╲
    No good │                                 ╱         ╲
            └────────────────────────────────  Approval  
                                              ╲         ╱
                                                ╲◇╱
                                                  │ Good
            ┌─────────────────────────┐           (3)   ┌─────────────────────────┐
            │ Detailed product        │─────────────────│ Preparation of          │
            │ documentation           │                 │ documentation for       │
            └─────────────────────────┘                 │ development study       │
                        ▲                                └─────────────────────────┘
                        │                                           │
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                        │                                ┌─────────────────────────┐
                        │                                │ Development schedule,   │
                        │                                │ timing, and price       │
                        │                                │ estimate                │
                        │                                └─────────────────────────┘
                        │                           (4)   │
            No good     │                            ╱◇╲  ▼
                        └────────────────────────  ╱      ╲
                                                   Approval 
                                                  ╲      ╱
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                                                      │ Good
                                            ( Provisional delivery )
                                            (  schedule           )
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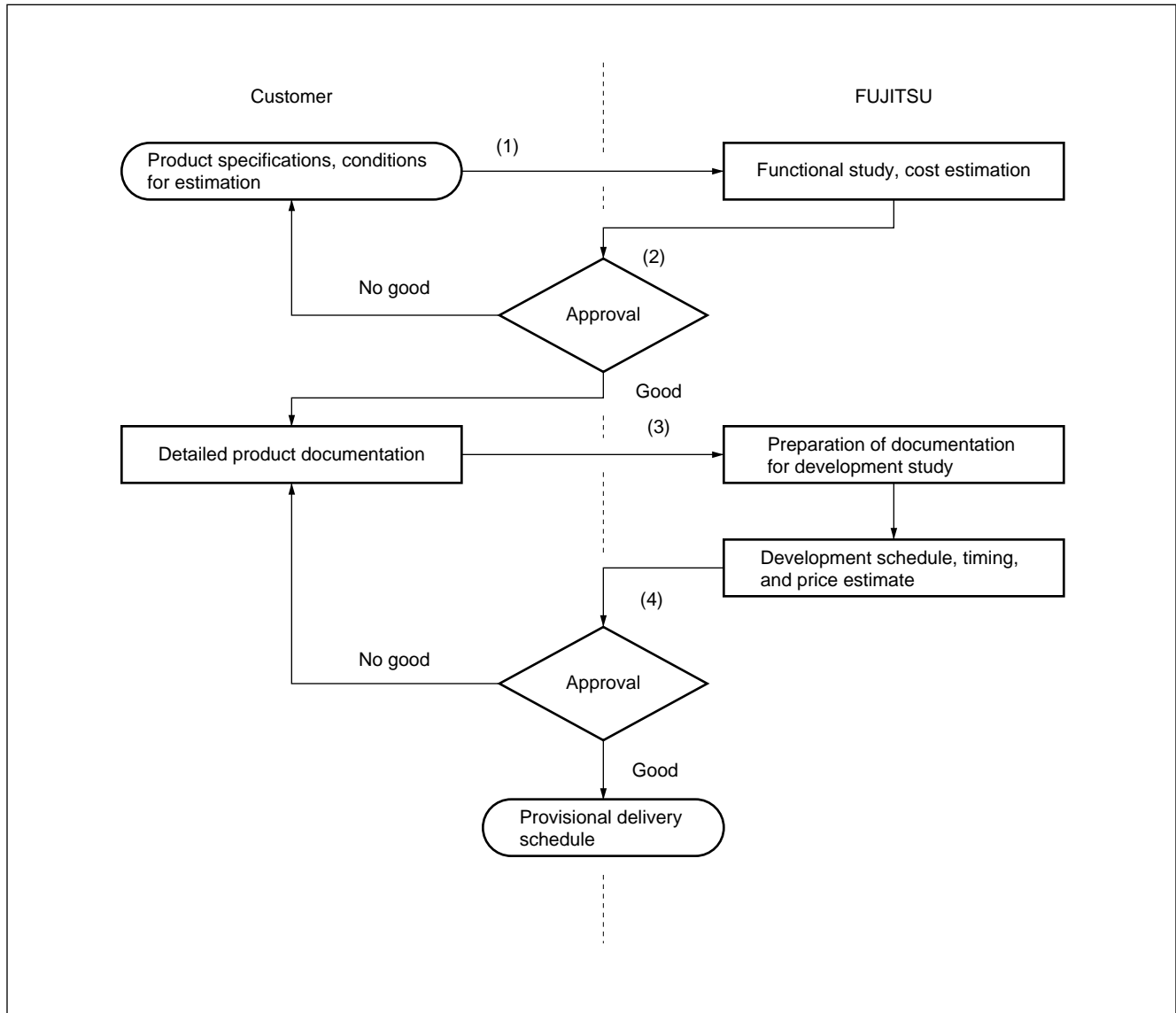
2. LSI Development

(1) LSI design, prototype development

Based on the provisional delivery specifications agreed by the customer and FUJITSU, chip design and prototype work begins. The standard time required for an ES prototype is approximately 10 weeks from the approval of provisional delivery specifications.

(2) ES (engineering sample) evaluation

Both the customer and FUJITSU evaluate the ES prototype based on the provisional delivery specifications.

(3) Final approval

If there are no problems with the evaluation, FUJITSU and the customer agree on final delivery specifications and end development, moving to the mass production stage. The standard lead time for delivery of mass production products is approximately three months.
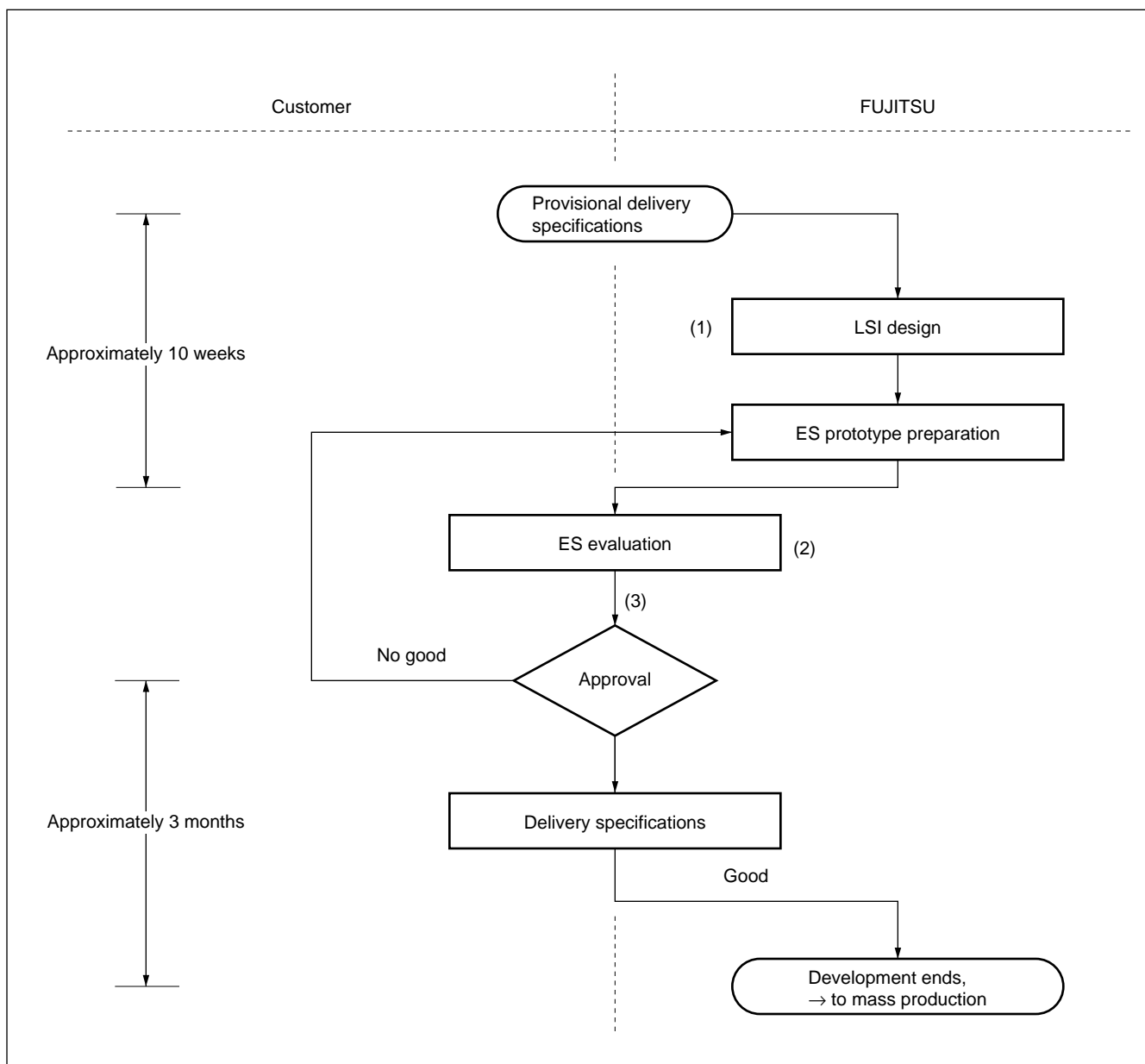
MB1570 Series

■ PACKAGE DIMENSIONS

48-pin Plastic LQFP
(FPT-48P-M05)

*: This dimension does not include resin protraction.

9.00±0.20(.354±.008)SQ

7.00±0.10(.276±.004)SQ

INDEX

LEAD No. 1

0.50±0.08
(.0197±.0031)

0.18$^{+0.08}_{-0.03}$
$\left(.007^{+.003}_{-.001}\right)$

1.50$^{+0.20}_{-0.10}$ (Mounting height)
$\left(.059^{+.008}_{-.004}\right)$

5.50
(.217)
REF

8.00
(.315)
NOM

"A"

0.127$^{+0.05}_{-0.02}$
$\left(.005^{+.002}_{-.001}\right)$

Details of "A" part

0.10±0.10 (STAND OFF)
(.004±.004)

0.50±0.20
(.020±.008)

0 ~10°

□ 0.10(.004)
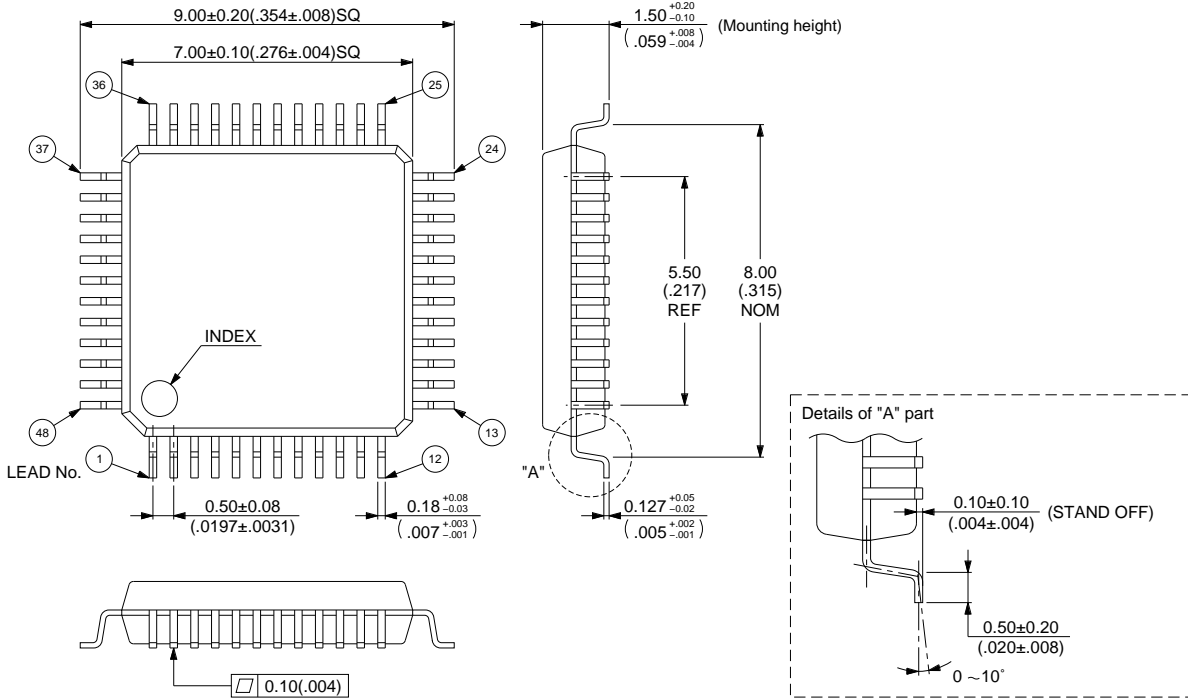
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Dimensions in mm (inches).

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64-pin Plastic LQFP
(FPT-64P-M03)

*: This dimension does not include resin protraction.

12.00±0.20(.472±.008)SQ

10.00±0.10(.394±.004)SQ

48

49

64

LEAD No.

1

INDEX

16

17

32

33

0.50±0.08
(.0197±.0031)

0.18 $^{+0.08}_{-0.03}$
$\left(.007 ^{+.003}_{-.001}\right)$

0.10(.004)

1.50 $_{-0.10}$
$\left(.059 ^{+.008}_{-.004}\right)$ (Mounting height)

7.50
(.295)
REF

11.00
(.433)
NOM

"A"

0.127 $^{+0.05}_{-0.02}$
$\left(.005 ^{+.002}_{-.001}\right)$

Details of "A" part

0.10±0.10
(.004±.004) (STAND OFF)

0.50±0.20
(.020±.008)

0 ~ 10°
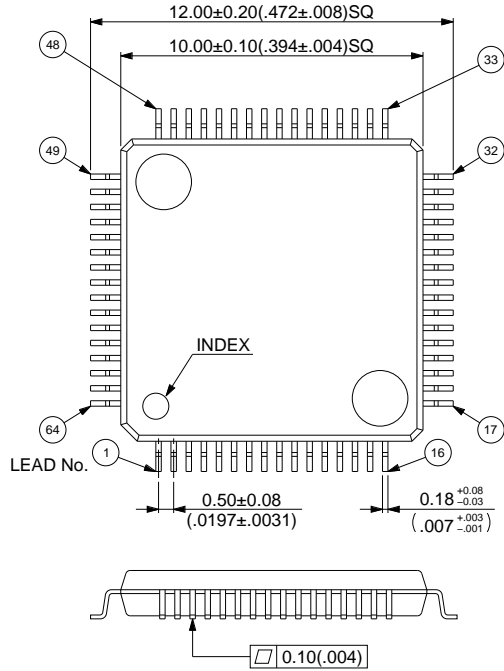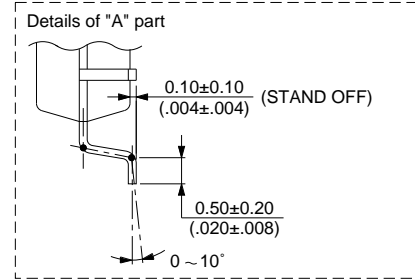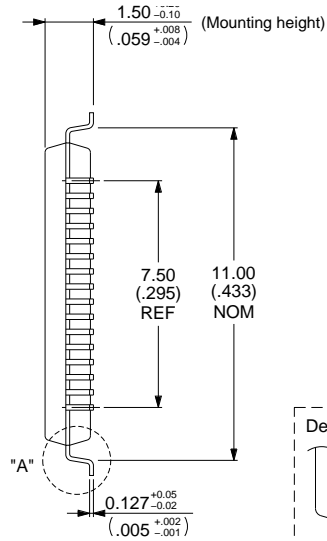
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Dimensions in mm (inches).