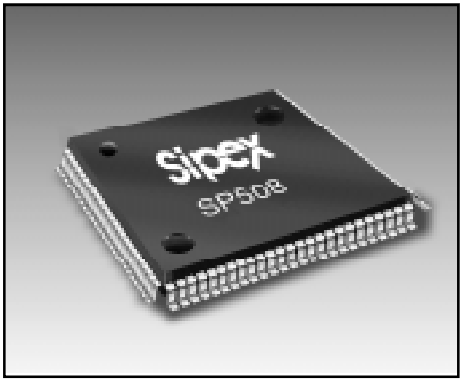
PRELIMINARY INFORMATION

SP508

Rugged 40Mbps, 8 Channel Multiprotocol Transceiver with Programmable DCE/DTE and Termination Resistors



- Fast 40Mbps Differential Transmission Rates
- Improved ESD Tolerance for Analog I/Os
- Internal Transceiver Termination Resistors for V.11 and V.35
- Interface Modes:
  - ✓ RS-232 **(V.28)**
  - ✓ **X.21 (V.11)**
  - ✓ RS-449/V.36 **(V.10 & V.11)**
  - ✓ EIA-530 **(V.10 & V.11)**
  - ✓ EIA-530A **(V.10 & V.11)**
  - ✓ V.35
- Protocols are Software Selectable with 3-Bit Word
- Eight (8) Drivers and Eight (8) Receivers
- Termination Network Disable Option
- Internal Line or Digital Loopback for Diagnostic Testing
- Adheres to NET1/NET2 and TBR-2 Compliancy Requirements
- Easy Flow-Through Pinout
- +5V Only Operation
- Individual Driver and Receiver Enable/Disable Controls
- Operates in either DTE or DCE Mode

DESCRIPTION

The **SP508** is a monolithic device that supports eight (8) popular serial interface standards for Wide Area Network (WAN) connectivity. The **SP508** is fabricated using a low power BiCMOS process technology, and incorporates a Sipex regulated charge pump allowing +5V only operation. Sipex's patented charge pump provides a regulated output of ±5.8V, which will provide enough voltage for compliant operation in all modes. Eight (8) drivers and eight (8) receivers can be configured via software for any of the above interface modes at any time. The **SP508** requires no additional external components for compliant operation for all of the eight (8) modes of operation other than four capacitors used for the internal charge pump. All necessary termination is integrated within the **SP508** and is switchable when V.35 drivers and V.35 receivers, or when V.11 receivers are used. The **SP508** provides the controls and transceiver availability for operating as either a DTE or DCE.

Additional features with the **SP508** include internal loopback that can be initiated in any of the operating modes by use of the $\overline{\text{LOOPBACK}}$ pin. While in loopback mode, receiver outputs are internally connected to driver inputs creating an internal signal path bypassing the serial communications controller for diagnostic testing. The **SP508** also includes a latch enable pin with the driver and receiver address decoder. The internal V.11 or V.35 termination can be switched off using a control pin (TERM_OFF) for monitoring applications. All eight (8) drivers and receivers in the **SP508** include separate enable pins for added convenience. The **SP508** is ideal for WAN serial ports in networking equipment such as routers, access concentrators, network muxes, DSU/CSU's, networking test equipment, and other access devices.

Applicable U.S. Patents-5,306,954; and others patents pending

PRELIMINARY INFORMATION

ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V_{CC} ..... +7V
Input Voltages:
- Logic ..... -0.3V to (V_{CC}+0.5V)
- Drivers ..... -0.3V to (V_{CC}+0.5V)
- Receivers ..... ±15.5V

Output Voltages:
- Logic ..... -0.3V to (V_{CC}+0.5V)
- Drivers ..... ±15V
- Receivers ..... -0.3V to (V_{CC}+0.5V)

Storage Temperature ..... -65°C to +150°C
Power Dissipation 1520mW
(derate 19.0mW/°C above +70°C)
Package Derating:
- $ø_{JA}$ ..... 52.7 °C/W
- $ø_{JC}$ ..... 6.5 °C/W

STORAGE CONSIDERATIONS

Due to the relatively large package size of the 100-pin quad flat-pack, storage in a low humidity environment is preferred. Large high density plastic packages are moisture sensitive and should be stored in Dry Vapor Barrier Bags. Prior to usage, the parts should remain bagged and stored below 40°C and 60%RH. If the parts are removed from the bag, they should be used within 48 hours or stored in an environment at or below 20%RH. If the above conditions cannot be followed, the parts should be baked for four hours at 125°C in order to remove moisture prior to soldering. Sipex ships the 100-pin LQFP in Dry Vapor Barrier Bags with a humidity indicator card and desiccant pack. The humidity indicator should be below 30%RH.

SPECIFICATIONS

T_A = +25°C and V_{CC} = +4.75V to +5.25V unless otherwise noted.

	MIN.	TYP.	MAX.	UNITS	CONDITIONS
LOGIC INPUTS					
V_{IL}			0.8	Volts	
V_{IH}	2.0			Volts	
LOGIC OUTPUTS					
V_{OL}			0.4	Volts	I_{OUT}= –3.2mA
V_{OH}	2.4			Volts	I_{OUT}= 1.0mA
V.28 DRIVER					
DC Parameters					
Outputs					
Open Circuit Voltage			±15	Volts	per ***Figure 1***
Loaded Voltage	±5.0		±15	Volts	per ***Figure 2***
Short-Circuit Current			±100	mA	per ***Figure 4***
Power-Off Impedance	300			Ω	per ***Figure 5***
AC Parameters					**V_{CC} = +5V for AC parameters**
Outputs					
Transition Time			1.5	µs	per ***Figure 6***; +3V to -3V
Instantaneous Slew Rate			30	V/µs	per ***Figure 3***
Propagation Delay					
t_{PHL}	0.5	1	5	µs	
t_{PLH}	0.5	1	5	µs	
Max.Transmission Rate	120	230		kbps	
V.28 RECEIVER					
DC Parameters					
Inputs					
Input Impedance	3		7	kΩ	per ***Figure 7***
Open-Circuit Bias			+2.0	Volts	per ***Figure 8***
HIGH Threshold		1.7	3.0	Volts	
LOW Threshold	0.8	1.2		Volts	
AC Parameters					**V_{CC} = +5V for AC parameters**
Propagation Delay					
t_{PHL}	50	100	500	ns	
t_{PLH}	50	100	500	ns	

SPECIFICATIONS

T_A = +25°C and V_{CC} = +4.75V to +5.25V unless otherwise noted.

	MIN.	TYP.	MAX.	UNITS	CONDITIONS
V.28 RECEIVER (continued)					
AC Parameters (cont.)					
Max.Transmission Rate	120	230		kbps	
V.10 DRIVER					
DC Parameters					
Outputs					
Open Circuit Voltage	±4.0		±6.0	Volts	per ***Figure 9***
Test-Terminated Voltage	$0.9V_{OC}$			Volts	per ***Figure 10***
Short-Circuit Current			±150	mA	per ***Figure 11***
Power-Off Current			±100	µA	per ***Figure 12***
AC Parameters					**V_{CC} = +5V for AC parameters**
Outputs					
Transition Time			200	ns	per ***Figure 13***; 10% to 90%
Propagation Delay					
t_{PHL}	30	100	500	ns	
t_{PLH}	30	100	500	ns	
Max.Transmission Rate	120			kbps	
V.10 RECEIVER					
DC Parameters					
Inputs					
Input Current	–3.25		+3.25	mA	per ***Figures 14*** and ***15***
Input Impedance	4			kΩ	
Sensitivity			±0.3	Volts	
AC Parameters					**V_{CC} = +5V for AC parameters**
Propagation Delay					
t_{PHL}			50	ns	
t_{PLH}			50	ns	
Max.Transmission Rate	120			kbps	
V.11 DRIVER					
DC Parameters					
Outputs					
Open Circuit Voltage			±6.0	Volts	per ***Figure 16***
Test Terminated Voltage	±2.0			Volts	per ***Figure 17***
	$0.5V_{OC}$		$0.67V_{OC}$	Volts	
Balance			±0.4	Volts	per ***Figure 17***
Offset			+3.0	Volts	per ***Figure 17***
Short-Circuit Current			±150	mA	per ***Figure 18***
Power-Off Current			±100	µA	per ***Figure 19***
AC Parameters					**V_{CC} = +5V for AC parameters**
Outputs					
Transition Time			10	ns	per ***Figures 21*** and ***36***; 10% to 90%
Propagation Delay					Using C_L = 50pF;
t_{PHL}		30	50	ns	per ***Figures 33*** and ***36***
t_{PLH}		30	50	ns	per ***Figures 33*** and ***36***
Differential Skew			10	ns	per ***Figures 33*** and ***36***
Max.Transmission Rate	40			Mbps	
V.11 RECEIVER					
DC Parameters					
Inputs					
Common Mode Range	–7		+7	Volts	
Sensitivity			±0.2	Volts	

SPECIFICATIONS

T_A = +25°C and V_{CC} = +4.75V to +5.25V unless otherwise noted.

	MIN.	TYP.	MAX.	UNITS	CONDITIONS
V.11 RECEIVER (continued)					
DC Parameters (cont.)					
Input Current	–3.25		±3.25	mA	per ***Figure 20*** and ***22***; power on or off
Current w/ 100Ω Termination			±60.75	mA	per ***Figure 23*** and ***24***
Input Impedance	4			kΩ	
AC Parameters					**V_{CC} = +5V for AC parameters**
Propagation Delay					Using C_L = 50pF;
t_{PHL}		30	50	ns	per ***Figures 33*** and **38**
t_{PLH}		30	50	ns	per ***Figures 33*** and ***38***
Skew		5		ns	per ***Figure 33***
Max.Transmission Rate	40			Mbps	
V.35 DRIVER					
DC Parameters					
Outputs					
Test Terminated Voltage	±0.44		±0.66	Volts	per ***Figure 25***
Offset			±0.6	Volts	per ***Figure 25***
Output Overshoot	-0.2V_{ST}		+0.2V_{ST}	Volts	per ***Figure 25***; V_{ST} = Steady state value
Source Impedance	50		150	Ω	per ***Figure 27***; $Z_S = V_2/V_1$ x 50
Short-Circuit Impedance	135		165	Ω	per ***Figure 28***
AC Parameters					**V_{CC} = +5V for AC parameters**
Outputs					
Transition Time		7	20	ns	per ***Figure 29***; 10% to 90%
Propagation Delay					
t_{PHL}		30	50	ns	per ***Figures 33*** and ***36***; C_L = 20pF
t_{PLH}		30	50	ns	per ***Figures 33*** and ***36***; C_L = 20pF
Differential Skew			5	ns	per ***Figures 33*** and ***36***; C_L = 20pF
Max.Transmission Rate	40			Mbps	
V.35 RECEIVER					
DC Parameters					
Inputs					
Sensitivity		±50	+100	mV	
Source Impedance	90		110	Ω	per ***Figure 30***; $Z_S = V_2/V_1$ x 50Ω
Short-Circuit Impedance	135		165	Ω	per ***Figure 31***
AC Parameters					**V_{CC} = +5V for AC parameters**
Propagation Delay					
t_{PHL}		30	50	ns	per ***Figures 33*** and ***38***; C_L = 20pF
t_{PLH}		30	50	ns	per ***Figures 33*** and ***38***; C_L = 20pF
Skew		3		ns	per ***Figure 33***; C_L = 20pF
Max.Transmission Rate	40			Mbps	
TRANSCEIVER LEAKAGE CURRENTS					
Driver Output 3-State Current		100	500	µA	per **Figure 32**; Drivers disabled
Rcvr Output 3-State Current		1	10	µA	T_X & R_X disabled, 0.4V - V_O - 2.4V
POWER REQUIREMENTS					
V_{CC}	4.75	5.00	5.25	Volts	
I_{CC} (Shutdown Mode)		1		µA	All I_{CC} values are with V_{CC} = +5V
(V.28/RS-232)		95		mA	f_{IN} = 120kbps; Drivers active & loaded
(V.11/RS-422)		230		mA	f_{IN} = 10Mbps; Drivers active & loaded
(EIA-530 & RS-449)		270		mA	f_{IN} = 10Mbps; Drivers active & loaded
(V.35)		170		mA	V.35 @ f_{IN} = 10Mbps, V.28 @ 20kbps
(EIA-530A)		200		mA	f_{IN} = 10Mbps; Drivers active & loaded

OTHER AC CHARACTERISTICS

T_A = +25°C and V_{CC} = +5.0V unless otherwise noted.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
DRIVER DELAY TIME BETWEEN ACTIVE MODE AND TRI-STATE MODE					
RS-232/V.28					
t_{PZL}; Tri-state to Output LOW		0.11	5.0	µs	C_L = 100pF, **Fig. 34** & **40**; S_2 closed
t_{PZH}; Tri-state to Output HIGH		0.11	2.0	µs	C_L = 100pF, **Fig. 34** & **40**; S_2 closed
t_{PLZ}; Output LOW to Tri-state		0.05	2.0	µs	C_L = 100pF, **Fig. 34** & **40**; S_2 closed
t_{PHZ}; Output HIGH to Tri-state		0.05	2.0	µs	C_L = 100pF, **Fig. 34** & **40**; S_2 closed
RS-423/V.10					
t_{PZL}; Tri-state to Output LOW		0.07	2.0	µs	C_L = 100pF, **Fig. 34** & **40**; S_2 closed
t_{PZH}; Tri-state to Output HIGH		0.05	2.0	µs	C_L = 100pF, **Fig. 34** & **40**; S_2 closed
t_{PLZ}; Output LOW to Tri-state		0.55	2.0	µs	C_L = 100pF, **Fig. 34** & **40**; S_2 closed
t_{PHZ}; Output HIGH to Tri-state		0.12	2.0	µs	C_L = 100pF, **Fig. 34** & **40**; S_2 closed
RS-422/V.11					
t_{PZL}; Tri-state to Output LOW		0.04	10.0	µs	C_L = 100pF, **Fig. 34** & **37**; S_1 closed
t_{PZH}; Tri-state to Output HIGH		0.05	2.0	µs	C_L = 100pF, **Fig. 34** & **37**; S_2 closed
t_{PLZ}; Output LOW to Tri-state		0.03	2.0	µs	C_L = 15pF, **Fig. 34** & **37**; S_1 closed
t_{PHZ}; Output HIGH to Tri-state		0.11	2.0	µs	C_L = 15pF, **Fig. 34** & **37**; S_2 closed
V.35					
t_{PZL}; Tri-state to Output LOW		0.85	10.0	µs	C_L = 100pF, **Fig. 34** & **37**; S_1 closed
t_{PZH}; Tri-state to Output HIGH		0.36	2.0	µs	C_L = 100pF, **Fig. 34** & **37**; S_2 closed
t_{PLZ}; Output LOW to Tri-state		0.06	2.0	µs	C_L = 15pF, **Fig. 34** & **37**; S_1 closed
t_{PHZ}; Output HIGH to Tri-state		0.05	2.0	µs	C_L = 15pF, **Fig. 34** & **37**; S_2 closed
RECEIVER DELAY TIME BETWEEN ACTIVE MODE AND TRI-STATE MODE					
RS-232/V.28					
t_{PZL}; Tri-state to Output LOW		0.05	2.0	µs	C_L = 100pF, **Fig. 35** & **40**; S_1 closed
t_{PZH}; Tri-state to Output HIGH		0.05	2.0	µs	C_L = 100pF, **Fig. 35** & **40**; S_2 closed
t_{PLZ}; Output LOW to Tri-state		0.65	2.0	µs	C_L = 100pF, **Fig. 35** & **40**; S_1 closed
t_{PHZ}; Output HIGH to Tri-state		0.65	2.0	µs	C_L = 100pF, **Fig. 35** & **40**; S_2 closed
RS-423/V.10					
t_{PZL}; Tri-state to Output LOW		0.04	2.0	µs	C_L = 100pF, **Fig. 35** & **40**; S_1 closed
t_{PZH}; Tri-state to Output HIGH		0.03	2.0	µs	C_L = 100pF, **Fig. 35** & **40**; S_2 closed
t_{PLZ}; Output LOW to Tri-state		0.03	2.0	µs	C_L = 100pF, **Fig. 35** & **40**; S_1 closed
t_{PHZ}; Output HIGH to Tri-state		0.03	2.0	µs	C_L = 100pF, **Fig. 35** & **40**; S_2 closed

OTHER AC CHARACTERISTICS (Continued)

T_A = +25°C and V_{CC} = +5.0V unless otherwise noted.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
RS-422/V.11					
t_{PZL}; Tri-state to Output LOW		0.04	2.0	µs	C_L = 100pF, **Fig. 35** & **39**; S_1 closed
t_{PZH}; Tri-state to Output HIGH		0.03	2.0	µs	C_L = 100pF, **Fig. 35** & **39**; S_2 closed
t_{PLZ}; Output LOW to Tri-state		0.03	2.0	µs	C_L = 15pF, **Fig. 35** & **39**; S_1 closed
t_{PHZ}; Output HIGH to Tri-state		0.03	2.0	µs	C_L = 15pF, **Fig. 35** & **39**; S_2 closed
V.35					
t_{PZL}; Tri-state to Output LOW		0.04	2.0	µs	C_L = 100pF, **Fig. 35** & **39**; S_1 closed
t_{PZH}; Tri-state to Output HIGH		0.03	2.0	µs	C_L = 100pF, **Fig. 35** & **39**; S_2 closed
t_{PLZ}; Output LOW to Tri-state		0.03	2.0	µs	C_L = 15pF, **Fig. 35** & **39**; S_1 closed
t_{PHZ}; Output HIGH to Tri-state		0.03	2.0	µs	C_L = 15pF, **Fig. 35** & **39**; S_2 closed
TRANSCEIVER TO TRANSCEIVER SKEW				(per Figures 32, 33, 36, 38)	
RS-232 Driver		100		ns	$[(t_{phl})_{Tx1} - (t_{phl})_{Txn}]$
		100		ns	$[(t_{plh})_{Tx1} - (t_{plh})_{Txn}]$
RS-232 Receiver		20		ns	$[(t_{phl})_{Rx1} - (t_{phl})_{Rxn}]$
		20		ns	$[(t_{phl})_{Rx1} - (t_{phl})_{Rxn}]$
RS-422 Driver		2		ns	$[(t_{phl})_{Tx1} - (t_{phl})_{Txn}]$
		2		ns	$[(t_{plh})_{Tx1} - (t_{plh})_{Txn}]$
RS-422 Receiver		2		ns	$[(t_{phl})_{Rx1} - (t_{phl})_{Rxn}]$
		3		ns	$[(t_{phl})_{Rx1} - (t_{phl})_{Rxn}]$
RS-423 Driver		5		ns	$[(t_{phl})_{Tx2} - (t_{phl})_{Txn}]$
		5		ns	$[(t_{plh})_{Tx2} - (t_{plh})_{Txn}]$
RS-423 Receiver		5		ns	$[(t_{phl})_{Rx2} - (t_{phl})_{Rxn}]$
		5		ns	$[(t_{phl})_{Rx2} - (t_{phl})_{Rxn}]$
V.35 Driver		2		ns	$[(t_{phl})_{Tx1} - (t_{phl})_{Txn}]$
		2		ns	$[(t_{plh})_{Tx1} - (t_{plh})_{Txn}]$
V.35 Receiver		2		ns	$[(t_{phl})_{Rx1} - (t_{phl})_{Rxn}]$
		2		ns	$[(t_{phl})_{Rx1} - (t_{phl})_{Rxn}]$

TEST CIRCUITS

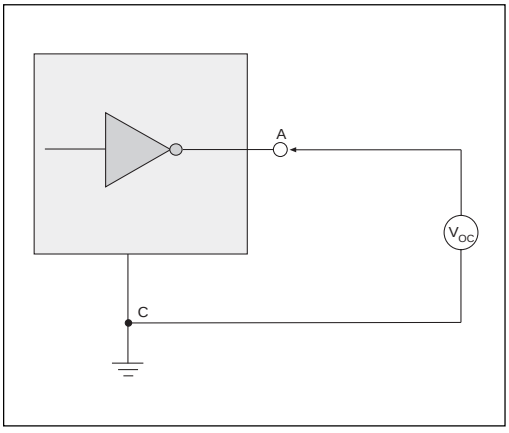


Figure 1. V.28 Driver Output Open Circuit Voltage

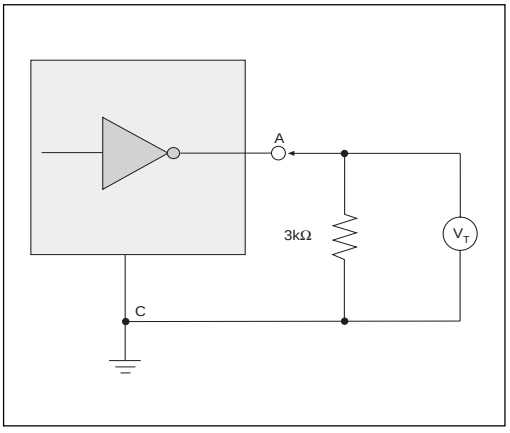


Figure 2. V.28 Driver Output Loaded Voltage

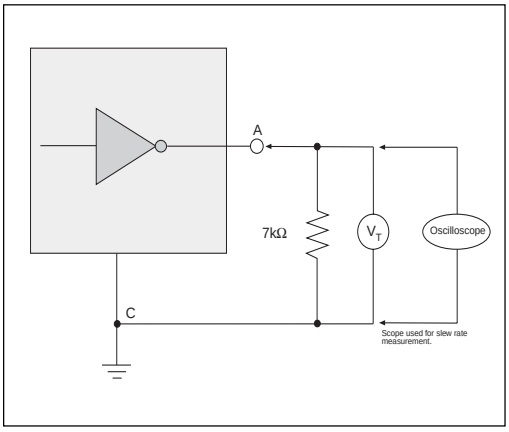


Figure 3. V.28 Driver Output Slew Rate

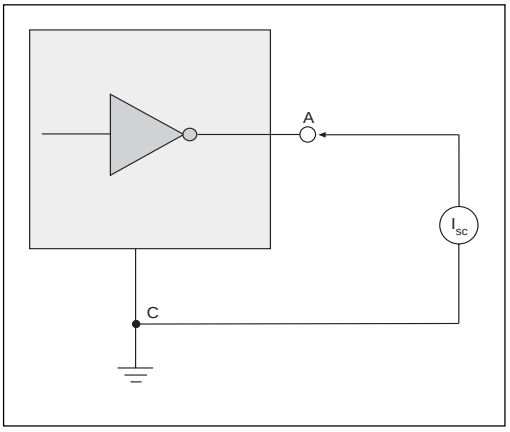


Figure 4. V.28 Driver Output Short-Circuit Current

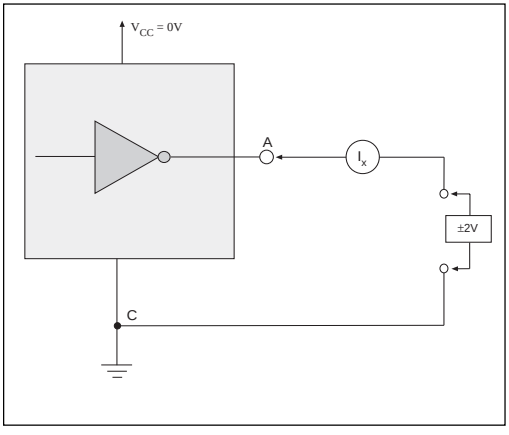


Figure 5. V.28 Driver Output Power-Off Impedance

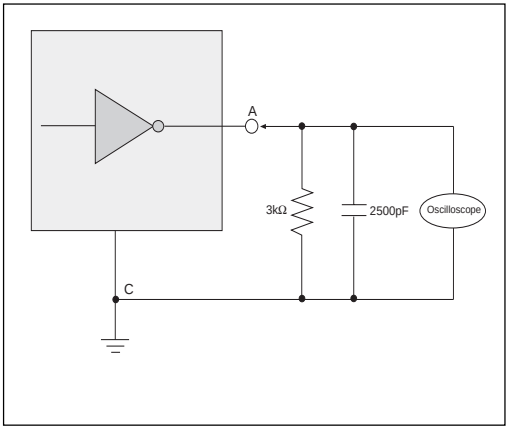


Figure 6. V.28 Driver Output Rise/Fall Times

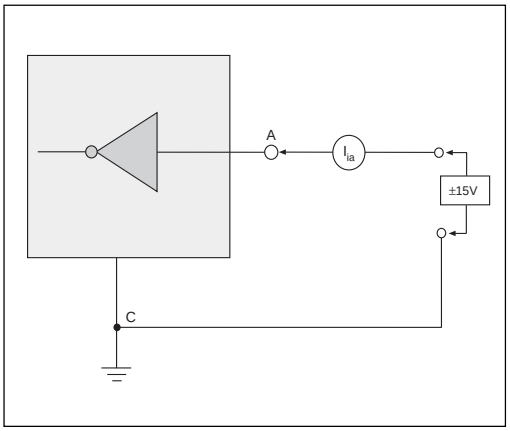


Figure 7. V.28 Receiver Input Impedance

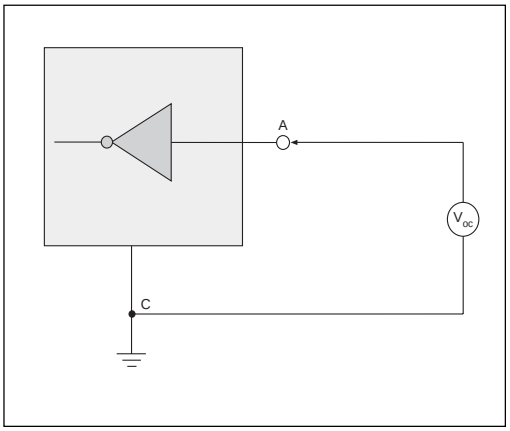


Figure 8. V.28 Receiver Input Open Circuit Bias

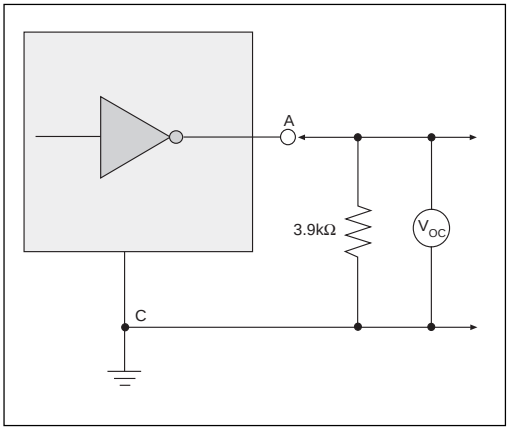


Figure 9. V.10 Driver Output Open-Circuit Voltage

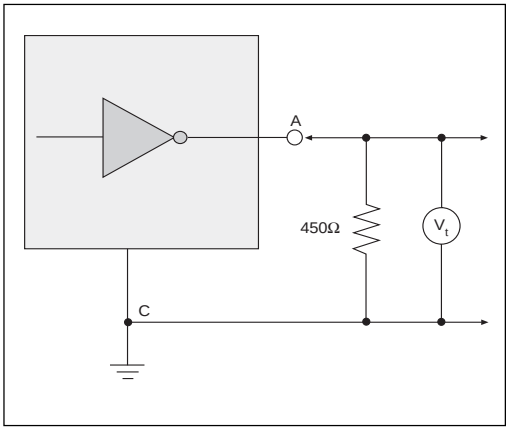


Figure 10. V.10 Driver Output Test Terminated Voltage

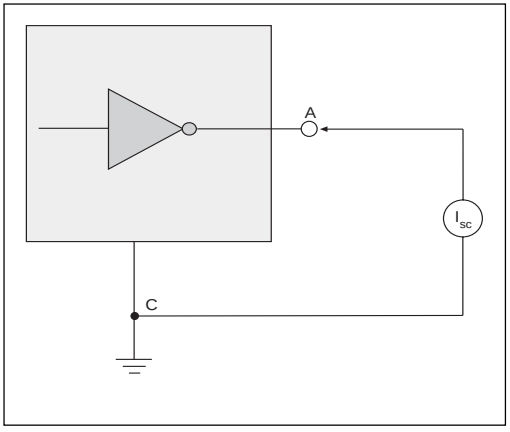


Figure 11. V.10 Driver Output Short-Circuit Current

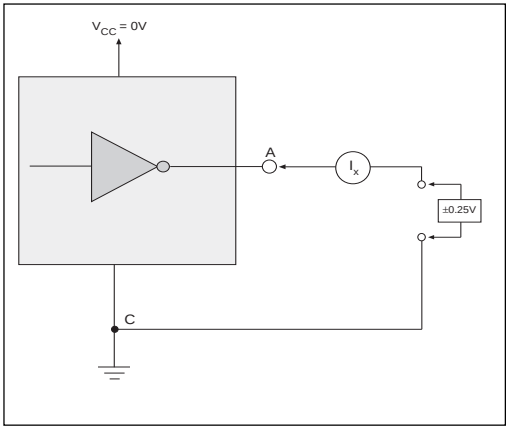


Figure 12. V.10 Driver Output Power-Off Current

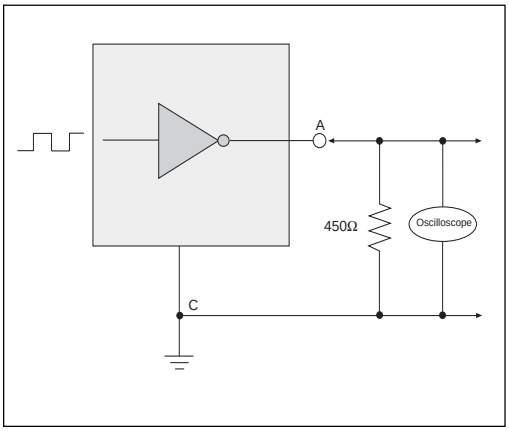


Figure 13. V.10 Driver Output Transition Time

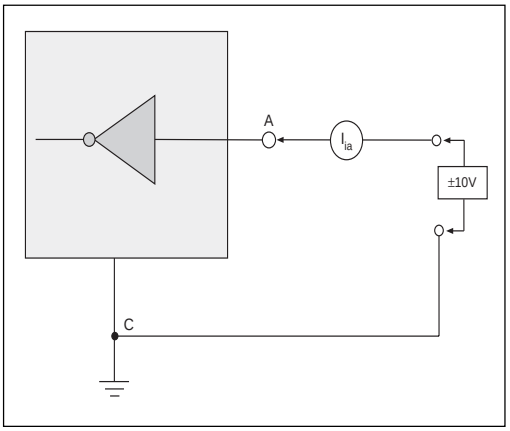


Figure 14. V.10 Receiver Input Current

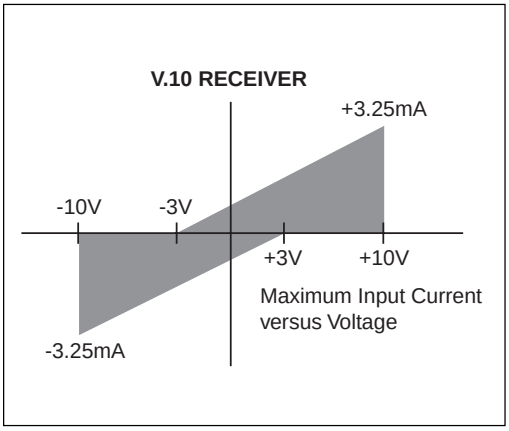


Figure 15. V.10 Receiver Input IV Graph

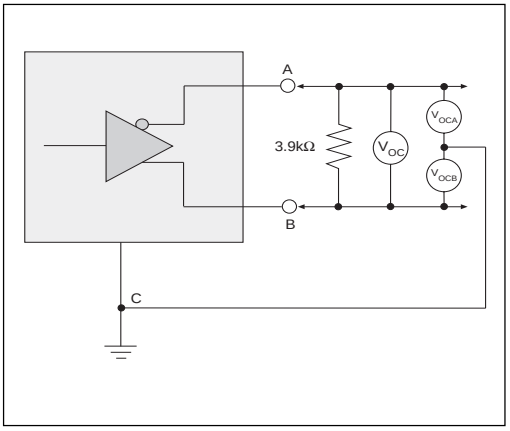


Figure 16. V.11 Driver Output Open-Circuit Voltage

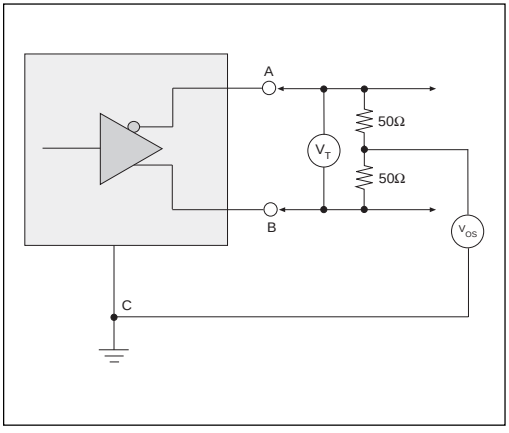


Figure 17. V.11 Driver Output Test Terminated Voltage

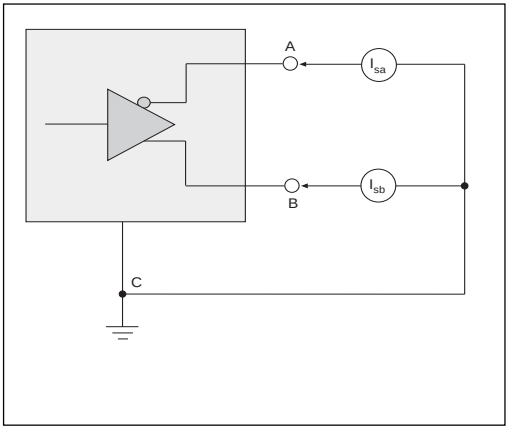


Figure 18. V.11 Driver Output Short-Circuit Current

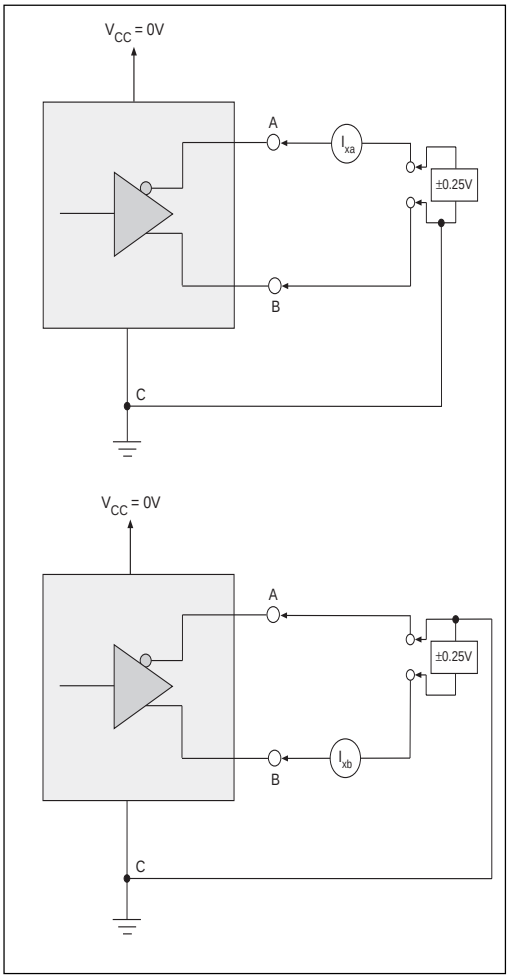


Figure 19. V.11 Driver Output Power-Off Current

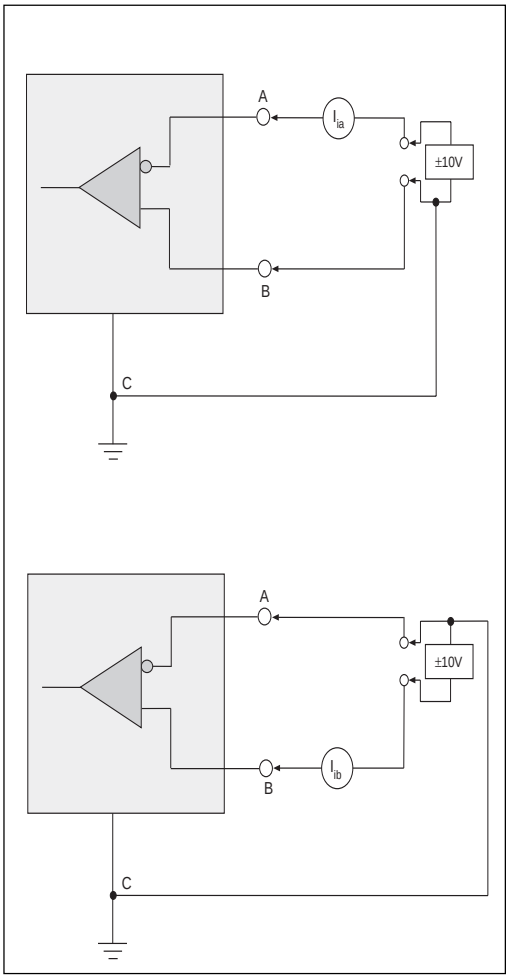


Figure 20. V.11 Receiver Input Current

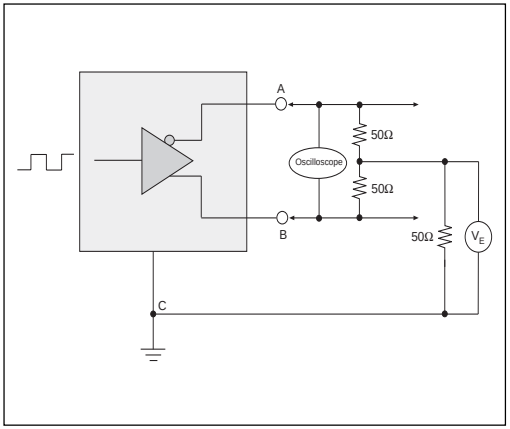


Figure 21. V.11 Driver Output Rise/Fall Time

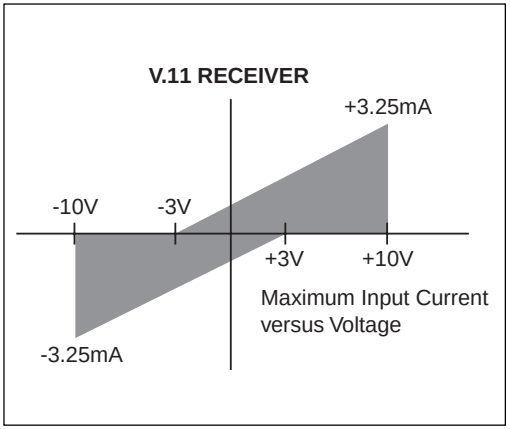


Figure 22. V.11 Receiver Input IV Graph

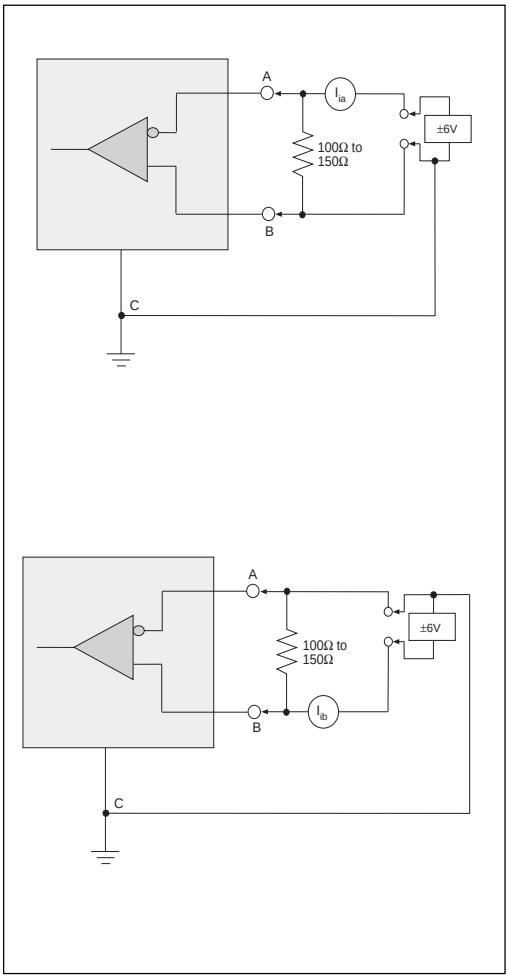


Figure 23. V.11 Receiver Input Current w/ Termination

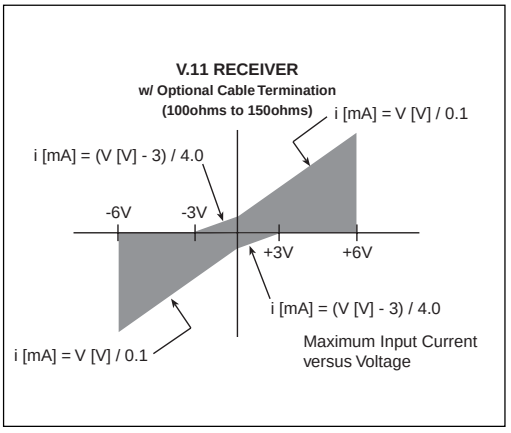


Figure 24. V.11 Receiver Input Graph w/ Termination

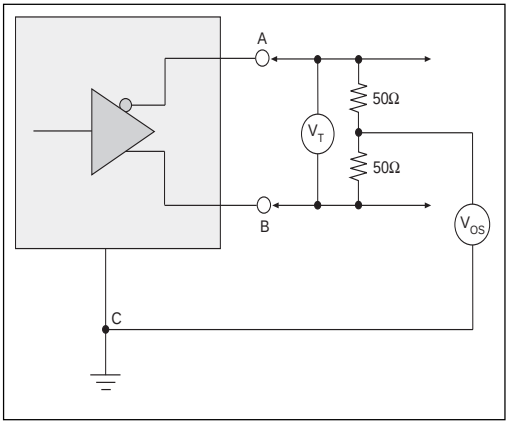


Figure 25. V.35 Driver Output Test Terminated Voltage

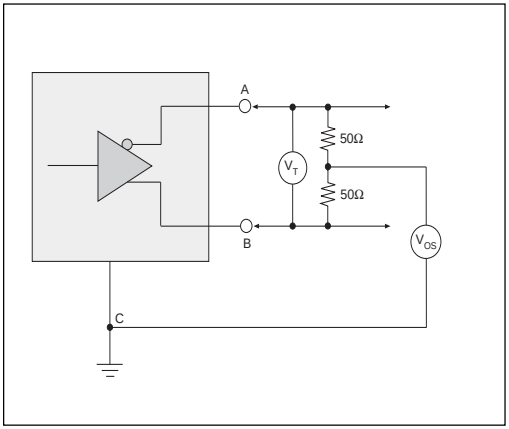


Figure 26. V.35 Driver Output Offset Voltage

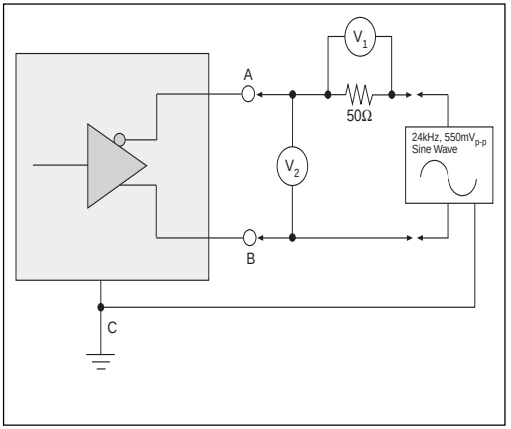


Figure 27. V.35 Driver Output Source Impedance

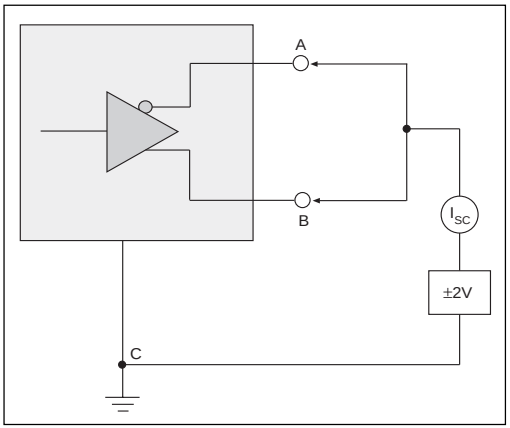


Figure 28. V.35 Driver Output Short-Circuit Impedance

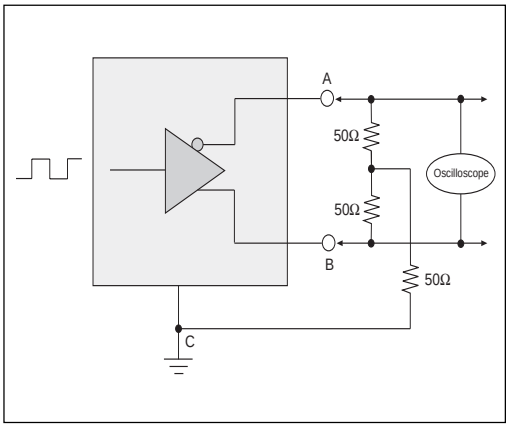


Figure 29. V.35 Driver Output Rise/Fall Time

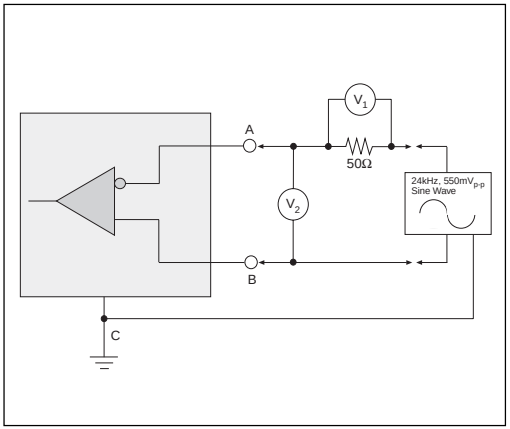


Figure 30. V.35 Receiver Input Source Impedance

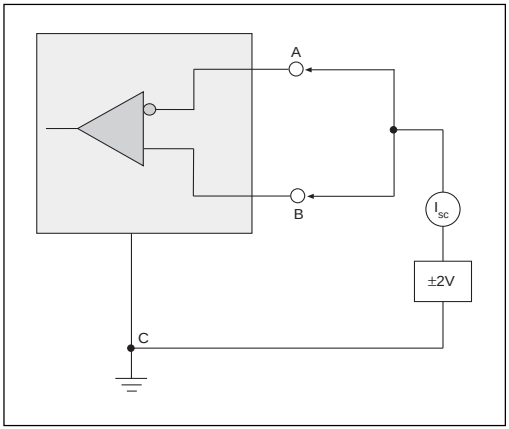


Figure 31. V.35 Receiver Input Short-Circuit Impedance

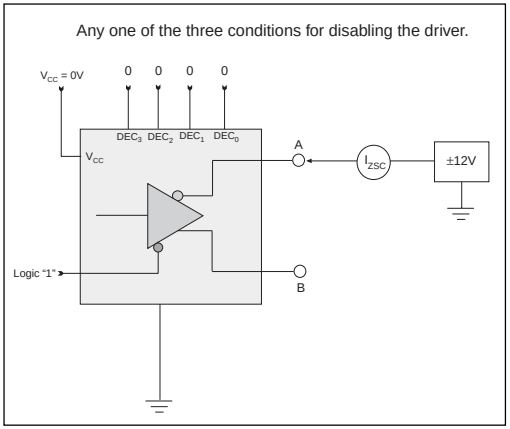


Figure 32. Driver Output Leakage Current Test

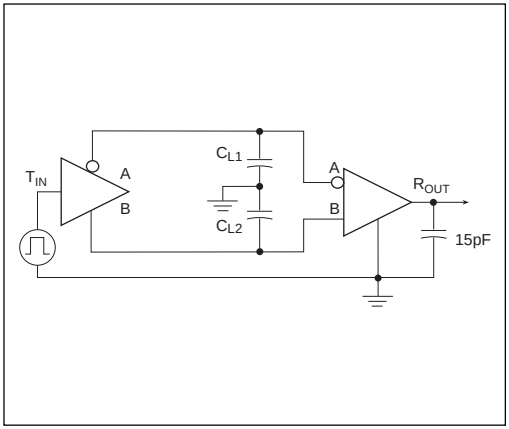


Figure 33. Driver/Receiver Timing Test Circuit

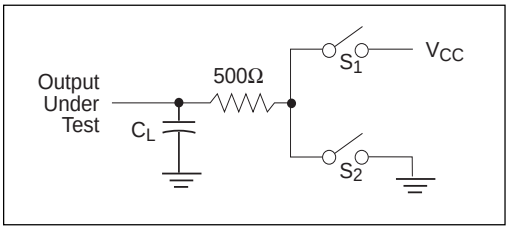


Figure 34. Driver Timing Test Load Circuit

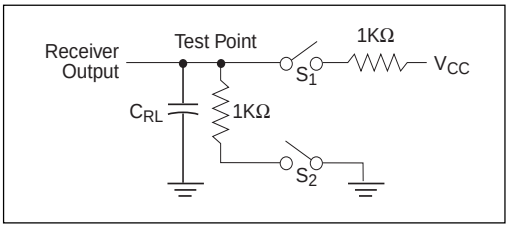


Figure 35. Receiver Timing Test Load Circuit

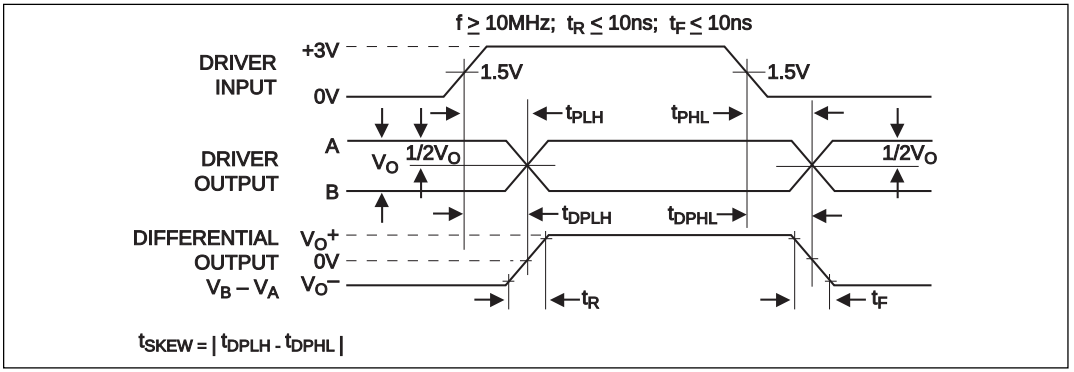


Figure 36. Driver Propagation Delays

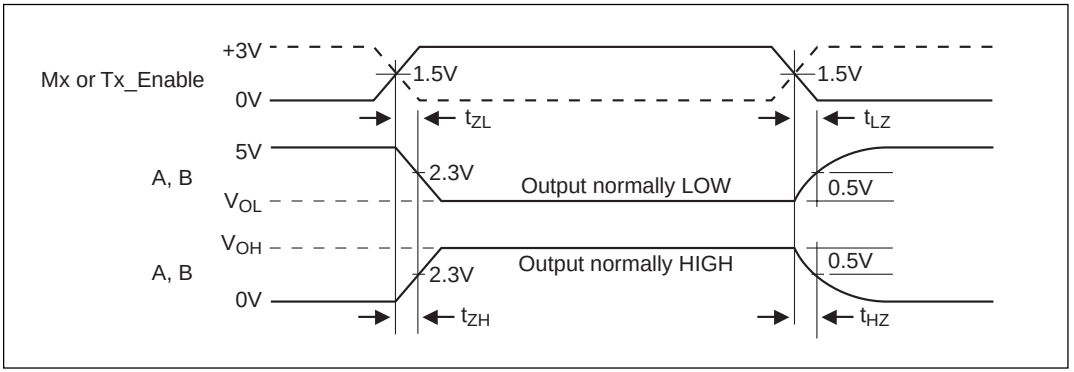


Figure 37. Driver Enable and Disable Times

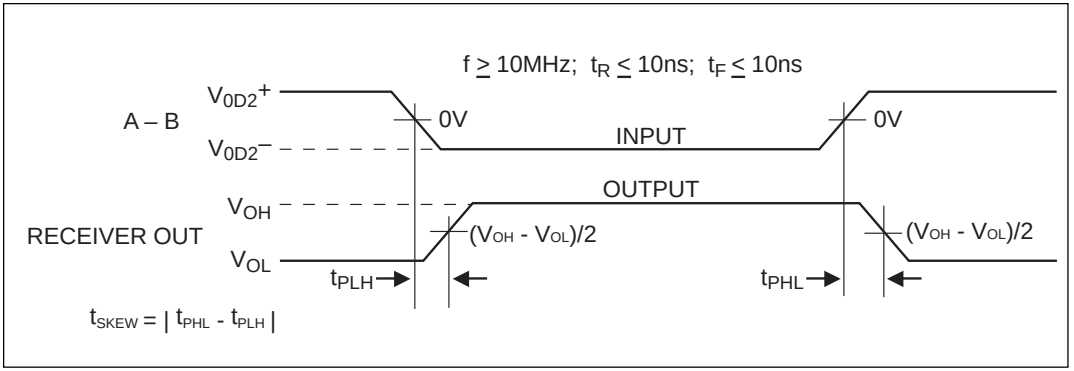


Figure 38. Receiver Propagation Delays

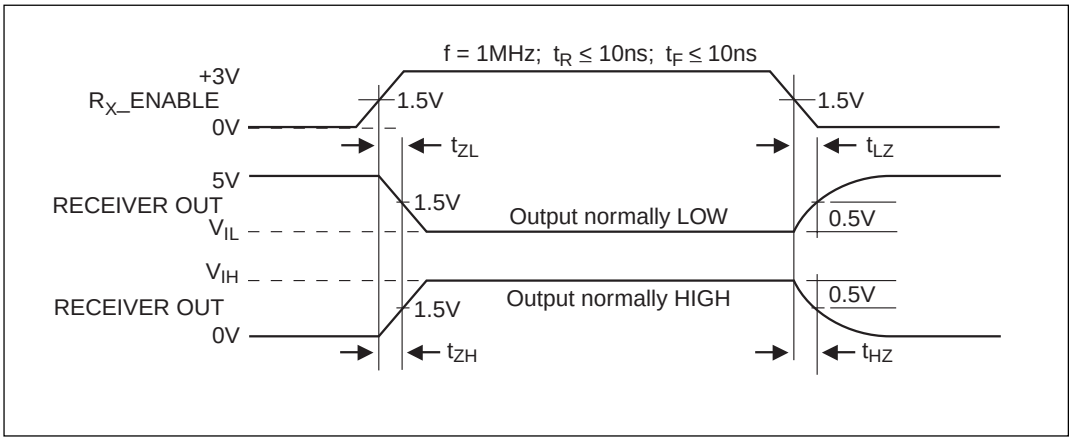


Figure 39. Receiver Enable and Disable Times

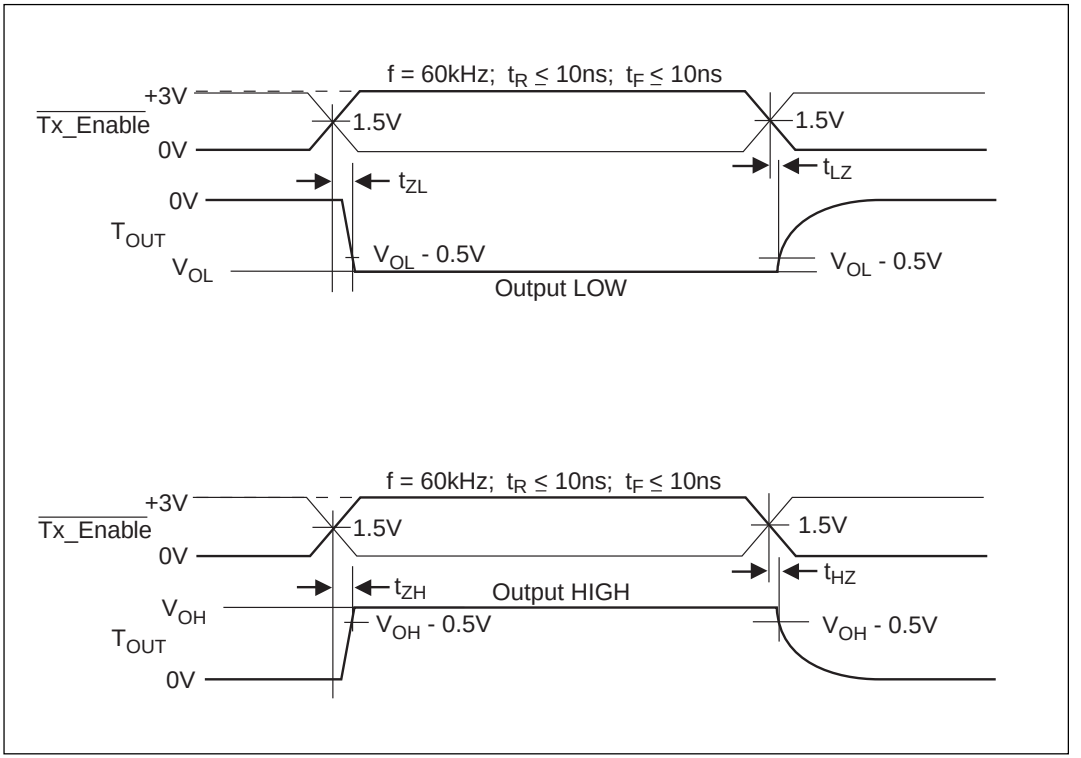


Figure 40. V.28 (RS-232) and V.10 (RS-423) Driver Enable and Disable Times

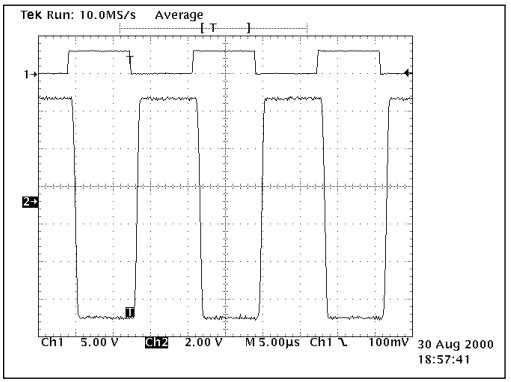


Figure 41. Typical V.28 Driver Output Waveform

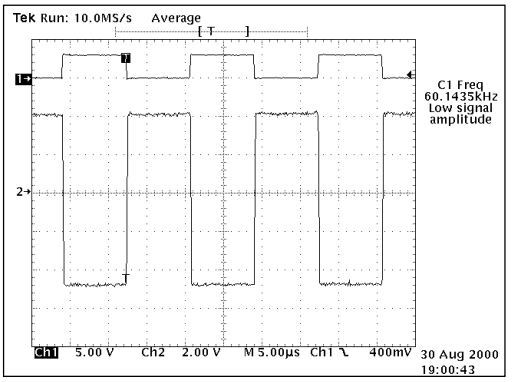


Figure 42. Typical V.10 Driver Output Waveform

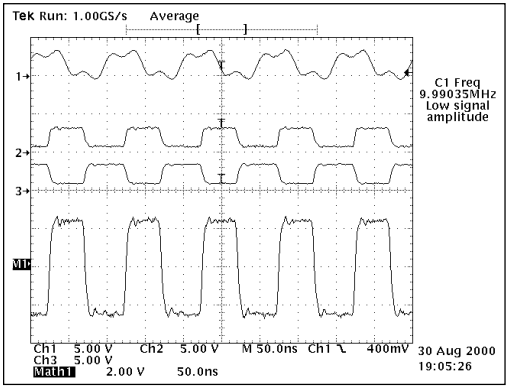


Figure 43. Typical V.11 Driver Output Waveform

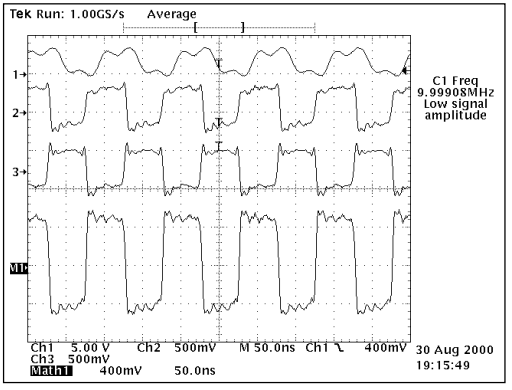
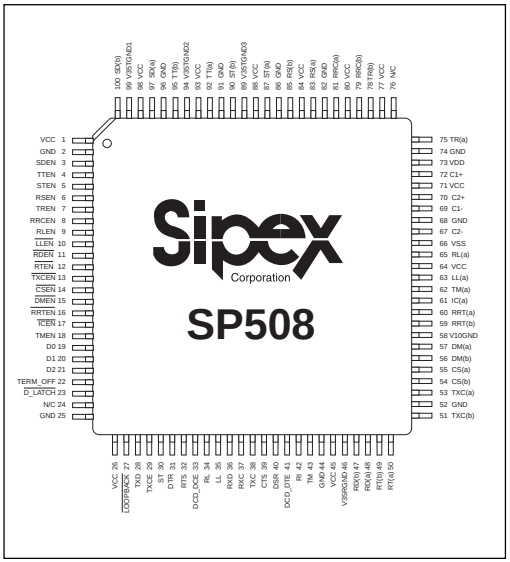


Figure 44. Typical V.35 Driver Output Waveform

PRELIMINARY INFORMATION

PINOUT



PIN ASSIGNMENTS

Pin 1 — V_{CC} — +5V Power Supply Input.

Pin 2 — GND — Signal Ground.

Pin 3 — SDEN — T_XD Driver Enable Input.

Pin 4 — TTEN — TXCE Driver Enable Input.

Pin 5 — STEN — ST Driver Enable Input.

Pin 6 — RSEN — RTS Driver Enable Input.

Pin 7 — TREN — DTR Driver Enable Input.

Pin 8 — RRCEN — DCD_{DCE} Driver Enable Input.

Pin 9 — RLEN — RL Driver Enable Input.

Pin 10 — $\overline{\text{LLEN}}$ — LL Driver Enable Input.

Pin 11 — $\overline{\text{RDEN}}$ — R_XD Receiver Enable Input.

Pin 12 — $\overline{\text{RTEN}}$ — R_XT Receiver Enable Input.

Pin 13 — $\overline{T_XCEN}$ — T_XC Receiver Enable Input.

Pin 14 — $\overline{\text{CSEN}}$ — CTS Receiver Enable Input.

Pin 15 — $\overline{\text{DMEN}}$ — DSR Receiver Enable Input.

Pin16 — $\overline{\text{RRTEN}}$ — DCD_{DTE} Receiver Enable Input.

Pin 17 — $\overline{\text{ICEN}}$ — RI Receiver Enable Input.

Pin 18 — TMEN — TM Receiver Enable Input.

Pin 19 — D0 — Mode Select Input.

Pin 20 — D1 — Mode Select Input.

Pin 21 — D2 — Mode Select Input.

Pin 22 — TERM_OFF — Termination Disable Input.

Pin 23 — $\overline{\text{D\_LATCH}}$ — Decoder Latch Input.

Pin 24 — N/C — No Connection.

Pin 25 — GND — Signal Ground.

Pin 26 — V_{CC} — +5V Power Supply Input.

Pin 27—$\overline{\text{LOOPBACK}}$—Loopback Mode Enable Input.

Pin 28 — TXD — TXD Driver TTL Input.

Pin 29 — TXCE — TXCE Driver TTL Input.

Pin 30 — ST — ST Driver TTL Input.

Pin 31 —RTS — RTS Driver TTL Input.

Pin 32 — DTR— DTR Driver TTL Input.

Pin 33 — DCD_DCE — DCD_{DCE} Driver TTL Input.

Pin 34 — RL — RL Driver TTL Input.

Pin 35 — LL — LL Driver TTL Input.

Pin 36 — RXD — RXD Receiver TTL Output.

Pin 37 — RXC — RXC Receiver TTL Output.

Pin 38 — TXC — TXC Receiver TTL Output.

Pin 39 — CTS — CTS Receiver TTL Output.

Pin 40 — DTR — DSR Receiver TTL Output.

Pin 41 — DCD_DTE — DCD_{DTE} Receiver TTL Output.

Pin 42 — RI — RI Receiver TTL Output.

Pin 43 — TM — TM Receiver TTL Output.

Pin 44 — GND — Signal Ground.

Pin 45 — V_{CC} — +5V Power Supply Input.

Pin 46 — V35RGND — Receiver Termination Reference.

Pin 47 — RD(b) — RXD Non-Inverting Input.

PRELIMINARY INFORMATION

Pin 48 — RD(a) — RXD Inverting Input.

Pin 49 — RT(b) — RXT Non-Inverting Input.

Pin 50 — RT(a) — RXT Inverting Input.

Pin 51 — TXC(b) — TXC Non-Inverting Input.

Pin 52 — GND — Signal Ground.

Pin 53 — TXC(a) — TXC Inverting Input.

Pin 54 — CS(b) — CTS Non-Inverting Input.

Pin 55 — CS(a) — CTS Inverting Input.

Pin 56 — DM(b) — DSR Non-Inverting Input.

Pin 57 — DM(a) — DSR Inverting Input.

Pin 58 — V10GND — V.10 R_X Reference Node.

Pin 59 — RRT(b) — DCD_{DTE} Non-Inverting Input.

Pin 60 —RRT(a) — DCD_{DTE} Inverting Input.

Pin 61 — IC(a) — RI Receiver Input.

Pin 62 — TM(a) — TM Receiver Input.

Pin 63 — LL(a) — LL Driver Output.

Pin 64 — V_{CC} — +5V Power Supply Input.

Pin 65 — RL(a) — RL Driver Output.

Pin 66 — V_{SS} — $-2_X V_{CC}$ Charge Pump Output.

Pin 67 — C2- — Charge Pump Capacitor.

Pin 68 — GND — Signal Ground.

Pin 69 — C1- — Charge Pump Capacitor.

Pin 70 — C2+ — Charge Pump Capacitor.

Pin 71 — V_{CC} — +5V Power Supply Input.

Pin 72 — C1+ — Charge Pump Capacitor.

Pin 73 — V_{DD} — $2_X V_{CC}$ Charge Pump Output.

Pin 74 — GND — Signal Ground.

Pin 75 — TR(a) — DTR Inverting Output.

Pin 76 — N/C — No Connection.

Pin 77 — V_{CC} — +5V Power Supply Input.

Pin 78 — TR(b) — DTR Non-Inverting Output.

Pin 79 — RRC(b) — DCD_{DCE} Non-Inverting Output.

Pin 80 — V_{CC} — +5V Power Supply Input.

Pin 81 — RRC(a) — DCD_{DCE} Inverting Output.

Pin 82 — GND — Signal Ground.

Pin 83 — RS(a) — RTS Inverting Output.

Pin 84 — V_{CC} — +5V Power Supply Input.

Pin 85 — RS(b) — RTS Non-Inverting Output.

Pin 86 — GND — Signal Ground.

Pin 87 — ST(a) — ST Inverting Output.

Pin 88 — V_{CC} — +5V Power Supply Input.

Pin 89 — V35TGND3 — ST Termination Reference.

Pin 90 — ST(b) — ST Non-Inverting Output.

Pin 91 — GND — Signal Ground.

Pin 92 — TT(a) — TXCE Inverting Output.

Pin 93 — V_{CC} — +5V Power Supply Input.

Pin 94 — V35TGND2 — TXCE Termination Reference.

Pin 95 — TT(b) — TXCE Non-Inverting Output.

Pin 96 — GND — Signal Ground.

Pin 97 — SD(a) — TXD Inverting Output.

Pin 98 — V_{CC}- — +5V Power Supply Input.

Pin 99 — V35TGND1 — TXD Termination Reference.

Pin 100 — SD(b) — TXD Non-Inverting Output.

SP508 Driver Table

Driver Output Pin	V.35 Mode	EIA-530 Mode	RS-232 Mode (V.28)	EIA-530A Mode	RS-449 Mode (V.36)	X.21 Mode (V.11)	Shutdown	Suggested Signal
MODE (D0, D1, D2)	001	010	011	100	101	110	111	
$T_1OUT(a)$	V.35	V.11	V.28	V.11	V.11	V.11	High-Z	TxD(a)
$T_1OUT(b)$	V.35	V.11	High-Z	V.11	V.11	V.11	High-Z	TxD(b)
$T_2OUT(a)$	V.35	V.11	V.28	V.11	V.11	V.11	High-Z	TxCE(a)
$T_2OUT(b)$	V.35	V.11	High-Z	V.11	V.11	V.11	High-Z	TxCE(b)
$T_3OUT(a)$	V.35	V.11	V.28	V.11	V.11	V.11	High-Z	TxC_DCE(a)
$T_3OUT(b)$	V.35	V.11	High-Z	V.11	V.11	V.11	High-Z	TxC_DCE(b)
$T_4OUT(a)$	V.28	V.11	V.28	V.11	V.11	V.11	High-Z	RTS(a)
$T_4OUT(b)$	High-Z	V.11	High-Z	V.11	V.11	V.11	High-Z	RTS(b)
$T_5OUT(a)$	V.28	V.11	V.28	V.10	V.11	V.11	High-Z	DTR(a)
$T_5OUT(b)$	High-Z	V.11	High-Z	High-Z	V.11	V.11	High-Z	DTR(b)
$T_6OUT(a)$	V.28	V.11	V.28	V.11	V.11	V.11	High-Z	DCD_DCE(a)
$T_6OUT(b)$	High-Z	V.11	High-Z	V.11	V.11	V.11	High-Z	DCD_DCE(b)
$T_7OUT(a)$	V.28	V.10	V.28	V.10	V.10	High-Z	High-Z	RL
$T_8OUT(a)$	V.28	V.10	V.28	V.10	V.10	High-Z	High-Z	LL

Table 1. Driver Mode Selection

SP508 Receiver Table

Receiver Input Pin	V.35 Mode	EIA-530 Mode	RS-232 Mode (V.28)	EIA-530A Mode	RS-449 Mode (V.36)	X.21 Mode (V.11)	Shutdown	Suggested Signal
MODE (D0, D1, D2)	001	010	011	100	101	110	111	
$R_1IN(a)$	V.35	V.11	V.28	V.11	V.11	V.11	High-Z	RxD(a)
$R_1IN(b)$	V.35	V.11	High-Z	V.11	V.11	V.11	High-Z	RxD(b)
$R_2IN(a)$	V.35	V.11	V.28	V.11	V.11	V.11	High-Z	RxC(a)
$R_2IN(b)$	V.35	V.11	High-Z	V.11	V.11	V.11	High-Z	RxC(b)
$R_3IN(a)$	V.35	V.11	V.28	V.11	V.11	V.11	High-Z	TxC_DTE(a)
$R_3IN(b)$	V.35	V.11	High-Z	V.11	V.11	V.11	High-Z	TxC_DTE(b)
$R_4IN(a)$	V.28	V.11	V.28	V.11	V.11	V.11	High-Z	CTS(a)
$R_4IN(b)$	High-Z	V.11	High-Z	V.11	V.11	V.11	High-Z	CTS(b)
$R_5IN(a)$	V.28	V.11	V.28	V.10	V.11	V.11	High-Z	DSR(a)
$R_5IN(b)$	High-Z	V.11	High-Z	High-Z	V.11	V.11	High-Z	DSR(b)
$R_6IN(a)$	V.28	V.11	V.28	V.11	V.11	V.11	High-Z	DCD_DTE(a)
$R_6IN(b)$	High-Z	V.11	High-Z	V.11	V.11	V.11	High-Z	DCD_DTE(b)
$R_7IN(a)$	V.28	V.10	V.28	V.10	V.10	High-Z	High-Z	RI
$R_8IN(a)$	V.28	V.10	V.28	V.10	V.10	High-Z	High-Z	TM

Table 2. Receiver Mode Selection

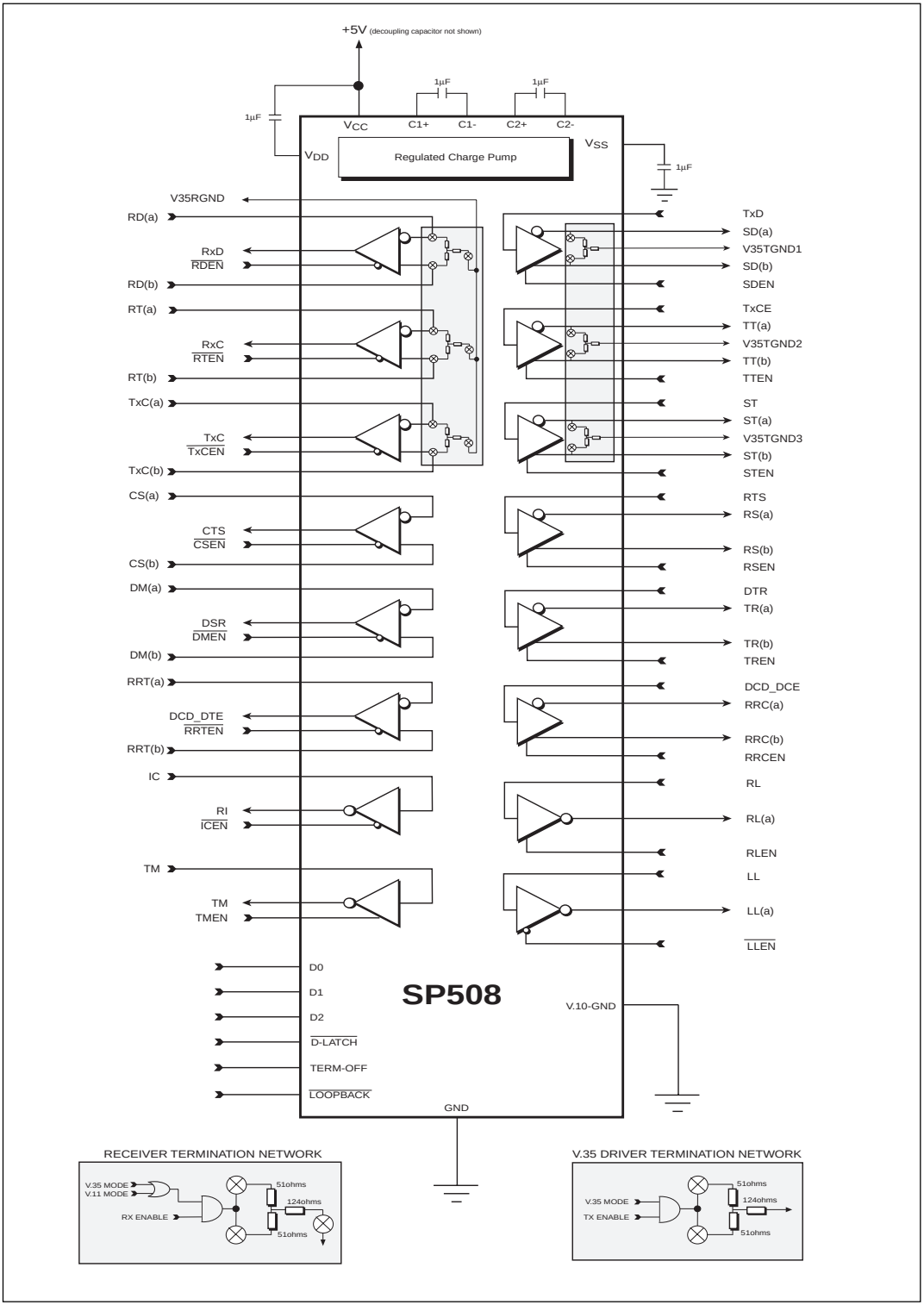


Figure 45. SP508 Block Diagram

PRELIMINARY INFORMATION

FEATURES

The **SP508** contains highly integrated serial transceivers that offer programmability between interface modes through software control. The **SP508** offers the hardware interface modes for RS-232 (V.28), RS-449/V.36 (V.11 and V.10), EIA-530 (V.11 and V.10), EIA-530A (V.11 and V.10), V.35 (V.35 and V.28) and X.21(V.11). The interface mode selection is done via three control pins, which can be latched via microprocessor control.

The **SP508** has eight drivers, eight receivers, and **Sipex's** patented on-board charge pump (5,306,954) that is ideally suited for wide area network connectivity and other multi-protocol applications. Other features include digital and line loopback modes, individual enable/disable control lines for each driver and receiver, fail-safe when inputs are either open or shorted, individual termination resistor ground paths, separate driver and receiver ground outputs, enhanced ESD protection on driver outputs and receiver inputs.

THEORY OF OPERATION

The **SP508** device is made up of 1) the drivers, 2) the receivers, 3) a charge pump, 4) DTE/DCE switching algorithm, and 5) control logic.

Drivers

The **SP508** has eight enhanced independent drivers. Control for the mode selection is done via a three-bit control word into D0, D1, and D2. The drivers are prearranged such that for each mode of operation, the relative position and functionality of the drivers are set up to accommodate the selected interface mode. As the mode of the drivers is changed, the electrical characteristics will change to support the required signal levels. The mode of each driver in the different interface modes that can be selected is shown in ***Table 1***.

There are four basic types of driver circuits – ITU-T-V.28 (RS-232), ITU-T-V.10 (RS-423), ITU-T-V.11 (RS-422), and CCITT-V.35.

The V.28 (RS-232) drivers output single-ended signals with a minimum of $\pm$5V (with 3kΩ & 2500pF loading), and can operate over 120kbps. Since the **SP550** uses a charge pump to generate the RS-232 output rails, the driver outputs will never exceed $\pm$10V. The V.28 driver architecture is similar to **Sipex's** standard line of RS-232 transceivers.

The RS-423 (V.10) drivers are also single-ended signals which produce open circuit V_{OL} and V_{OH} measurements of $\pm$4.0V to $\pm$6.0V. When terminated with a 450Ω load to ground, the driver output will not deviate more than 10% of the open circuit value. This is in compliance of the ITU V.10 specification. The V.10 (RS-423) drivers are used in RS-449/V.36, EIA-530, and EIA-530A modes as Category II signals from each of their corresponding specifications. The V.10 driver can transmit over 1Mbps if necessary.

The third type of drivers are V.11 (RS-422) differential drivers. Due to the nature of differential signaling, the drivers are more immune to noise as opposed to single-ended transmission methods. The advantage is evident over high speeds and long transmission lines. The strength of the driver outputs can produce differential signals that can maintain $\pm$2V differential output levels with a load of 100Ω. The signal levels and drive capability of these drivers allow the drivers to also support RS-485 requirements of $\pm$1.5V differential output levels with a 54Ω load. The strength allows the **SP508** differential driver to drive over long cable lengths with minimal signal degradation. The V.11 drivers are used in RS-449, EIA-530, EIA-530A and V.36 modes as Category I signals which are used for clock and data. **Sipex's** new driver design over its predecessors allow the **SP508** to operate over 40Mbps for differential transmission.

The fourth type of drivers are V.35 differential drivers. There are only three available on the SP550 for data and clock (TxD, TxCE, and TxC in DCE mode). These drivers are current sources that drive loop current through a differential pair resulting in a 550mV differential voltage at the receiver. These drivers also incorporate fixed termination networks for each driver in order to set the V_{OH} and V_{OL} depending on load conditions. This termination network is basically a "Y" configuration consisting of two 51Ω resistors connected in series and a 124Ω resistor connected between the two 50Ω resistors and a V35TGND output. Each of the three drivers and its associated termination will have its own V35TGND output for grounding convenience. Filtering can be done on these pins to reduce common mode noise transmitted over the transmission line by connecting a capacitor to ground.

The drivers also have separate enable pins which simplifies half-duplex configurations for some applications, especially programmable DTE/DCE. The enable pins will either enable or disable the output of the drivers according to the appropriate active logic illustrated on ***Figure 45***. The enable pins have internal pull-up and pull-down devices, depending on the active polarity of the receiver, that enable the driver upon power if the enable lines are left floating. During disabled conditions, the driver outputs will be at a high impedance 3-state.

The driver inputs are both TTL or CMOS compatible. All driver inputs have an internal pull-up resistor so that the output will be at a defined state at logic LOW ("0"). Unused driver inputs can be left floating. The internal pull-up resistor value is approximately 500kΩ.

Receivers

The **SP508** has eight enhanced independent receivers. Control for the mode selection is done via a three-bit control word that is the same as the driver control word. Therefore, the modes for the drivers and receivers are identical in the application.

Like the drivers, the receivers are prearranged for the specific requirements of the synchronous serial interface. As the operating mode of the receivers is changed, the electrical characteristics will change to support the required serial interface protocols of the receivers. ***Table 1*** shows the mode of each receiver in the different interface modes that can be selected. There are two basic types of receiver circuits—ITU-T-V .28 (RS-232) and ITU-T-V.11, (RS-422).

The RS-232 (V.28) receiver is single-ended and accepts RS-232 signals from the RS-232 driver. The RS-232 receiver has an operating voltage range of ±15V and can receive signals downs to ±3V. The input sensitivity complies with RS-232 and V .28 at ±3V. The input impedance is 3Ω to 7KΩ in accordance to RS-232 and V .28. The receiver output produces a TTL/CMOS signal with a +2.4V minimum for a logic "1" and a +0.8V maximum for a logic "0". The RS-232 (V.28) protocol uses these receivers for all data, clock and control signals. They are also used in V.35 mode for control line signals: CTS, DSR, LL, and RL. The RS-232 receivers can operate over 120kbps.

The second type of receiver is a differential type that can be configured internally to support ITU-T-V.10 and CCITT-V.35 depending on its input conditions. This receiver has a typical input impedance of 10kΩ and a differential threshold of less than ±100mV, which complies with the ITU-T-V.11 (RS-422) specifications. V.11 receivers are used in RS-449/V.36, EIA-530, EIA-530A and X.21 as Category I signals for receiving clock, data, and some control line signals not covered by Category II V.10 circuits. The differential V.11 transceiver has improved architecture that allows over 40Mbps transmission rates.

For receivers dedicated for data and clock (RxD, RxC, TxC) incorporate internal termination for V.11. The termination resistor is typically 120Ω connected between the A and B inputs. The termination is essential for minimizing crosstalk and signal reflection over the transmission line . The minimum value is guaranteed to exceed 100Ω, thus complying with the V.11 and RS-422 specifications. This resistor is invoked when the receiver is operating as a V.11 receiver, in modes EIA-530, EIA-530A, RS-449/V.36, and X.21.

The same receivers also incorporate a termination network internally for V.35 applications. For V.35, the receiver input termination is a "Y" termination consisting of two 51Ω resistors connected in series and a 124Ω resistor connected between the two 50Ω resistors and V35RGND output. The V35RGND is usually grounded. The receiver itself is identical to the V.11 receiver.

The differential receivers can be configured to be ITU-T-V.10 single-ended receivers by internally connecting the non-inverting input to ground. This is internally done by default from the decoder. The non-inverting input is rerouted to V10GND and can be grounded separately. The ITU-T-V.10 receivers can operate over 1Mbps and are used in RS-449/V.36, E1A-530, E1A-530A and X.21 modes as Category II signals as indicated by their corresponding specifications. All receivers include an enable/disable line for disabling the receiver output allowing convenient half-duplex configurations. The enable pins will either enable or disable the output of the receivers according to the appropriate active logic illustrated on ***Figure 45***. The receiver's enable lines include an internal pull-up or pull-down device, depending on the active polarity of the receiver, that enables the receiver upon power up if the enable lines are left floating. During disabled conditions, the receiver outputs will be at a high impedance state. If the receiver is disabled any associated termination is also disconnected from the inputs.

All receivers include a fail-safe feature that outputs a logic high when the receiver inputs are open, terminated but open, or shorted together. For single-ended V.28 and V.10 receivers, there are internal 5kΩ pull-down resistors on the inputs which produces a logic high ("1") at the receiver outputs. The differential receivers have a proprietary circuit that detect open or shorted inputs and if so, will produce a logic HIGH ("1") at the receiver output.

CHARGE PUMP

The charge pump is a **Sipex**-patented design (5,306,954) and uses a unique approach compared to older less-efficient designs. The charge pump still requires four external capacitors, but uses four-phase voltage shifting technique to attain symmetrical power supplies. The charge pump V_{DD} and V_{SS} outputs are regulated to +5.8V and -5.8V, respectively. There is a free-running oscillator that controls the four phases of the voltage shifting. A description of each phase follows.

Phase 1

—V_{SS} charge storage ——During this phase of the clock cycle, the positive side of capacitors C_1 and C_2 are initially charged to V_{CC}. C+ is then switched to ground and the charge in C_1- is transferred to C_2-. Since C_2+ is connected to V_{CC}, the voltage potential across capacitor C_2 is now $2_X V_{CC}$.

Phase 2

—V_{SS} transfer—Phase two of the clock connects the negative terminal of C_2 to the V_{SS} storage capacitor and the positive terminal of C_2 to ground, and transfers the negative generated voltage to C_3. This generated voltage is regulated to –5.8V. Simultaneously, the positive side of the capacitor C_1 is switched to V_{CC} and the negative side is connected to ground.

Phase 3

—V_{DD} charge storage —The third phase of the clock is identical to the first phase—the charge transferred in C_1 produces $-V_{CC}$ in the negative terminal of C_1 which is applied to the negative side of the capacitor C_2 . Since C_2+ is at V_{CC}, the voltage potential across C_2 is $2_X V_{CC}$.

Phase 4

—V_{DD} transfer —The fourth phase of the clock connects the negative terminal of C_2 to ground, and transfers the generated 5.8V across C_2 to C_4, the V_{DD} storage capacitor. This voltage is regulated to +5.8V. At the regulated voltage, the internal oscillator is disabled and simultaneously with this, the positive side of capacitor C_1 is switched to V_{CC} and the negative side is connected to ground, and the cycle begins again. The charge pump cycle will continue as long as the operational conditions for the internal oscillator are present.

Since both V^+ and V^- are separately generated from V_{CC}; in a no-load condition V^+ and V^- will be symmetrical. Older charge pump approaches that generate V^- from V^+ will show a decrease in the magnitude of V^- compared to V^+ due to the inherent inefficiencies in the design.

The clock rate for the charge pump typically operates at 250kHz. The external capacitors can be as low as 1µF with a 16V breakdown voltage rating.

TERM_OFF FUNCTION

The **SP508** contains a TERM_OFF pin that disables all three receiver input termination networks regardless of mode. This allows the device to be used in monitor mode applications typically found in networking test equipment. The TERM_OFF pin internally contains a pull-down device with an impedance of over 500kΩ, which will default in a "ON" condition during power-up if V.35 receivers are used. The individual receiver enable line and the SHUTDOWN mode from the decoder will disable the termination regardless of TERM_OFF.

LOOPBACK FUNCTION

The **SP508** contains a LOOPBACK pin that invokes a loopback path. This loopback path is illustrated in ***Figure 50***. LOOPBACK has an internal pull-up resistor that defaults to normal mode during power up or if the pin is left floating. During loopback, the driver output and receiver input characteristics will still adhere to its appropriate specifications.

DECODER AND D_LATCH FUNCTION

The **SP508** contains a D_LATCH pin that latches the data into the D0, D1, and D2 decoder inputs. If tied to a logic LOW ("0"), the latch is transparent, allowing the data at the decoder inputs to propagate through and program the **SP508** accordingly. If tied to a logic HIGH("1"), the latch locks out the data and prevents the mode from changing until this pin is brought to a logic LOW.

There are internal pull-up devices on D0, D1, and D2, which allow the device to be in SHUTDOWN mode ("111") upon power up. However , if the device is powered -up with the D_LATCH at a logic HIGH, the decoder state of the **SP508** will be undefined.

ESD TOLERANCE

The **SP508** device incorporates ruggedized ESD cells on all driver output and receiver input pins. The ESD structure is improved over our previous family for more rugged applications and environments sensitive to electrostatic discharges and associated transients. Actual ESD figures will be disclosed in the final data sheet.

CTR1/CTR2 EUROPEAN COMPLIANCY

As with all of **Sipex's** previous multi-protocol serial transceiver IC's the drivers and receivers have been designed to meet all the requirements to NET1/NET2 and TBR2 in order to meet CTR1/CTR2 compliancy. The **SP508** is also tested in-house at **Sipex** and adheres to all the NET1/2 physical layer testing and the ITU Series V specifications before shipment. Please note that although the **SP508**, as with its predecessors, adhere to CTR1/CTR2 compliancy testing, any complex or unusual configuration should be double-checked to ensure CTR1/CTR2 compliance. Consult the factory for details.

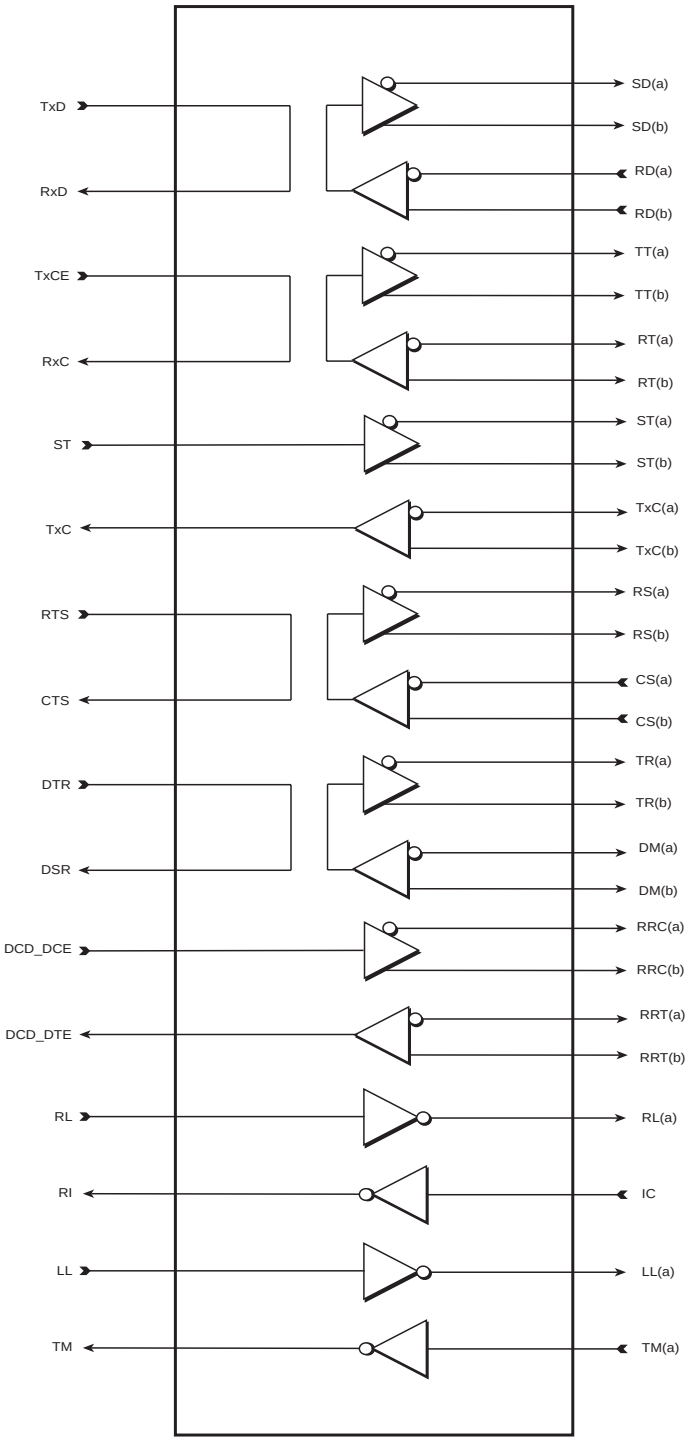


Figure 46. SP508 Loopback Path

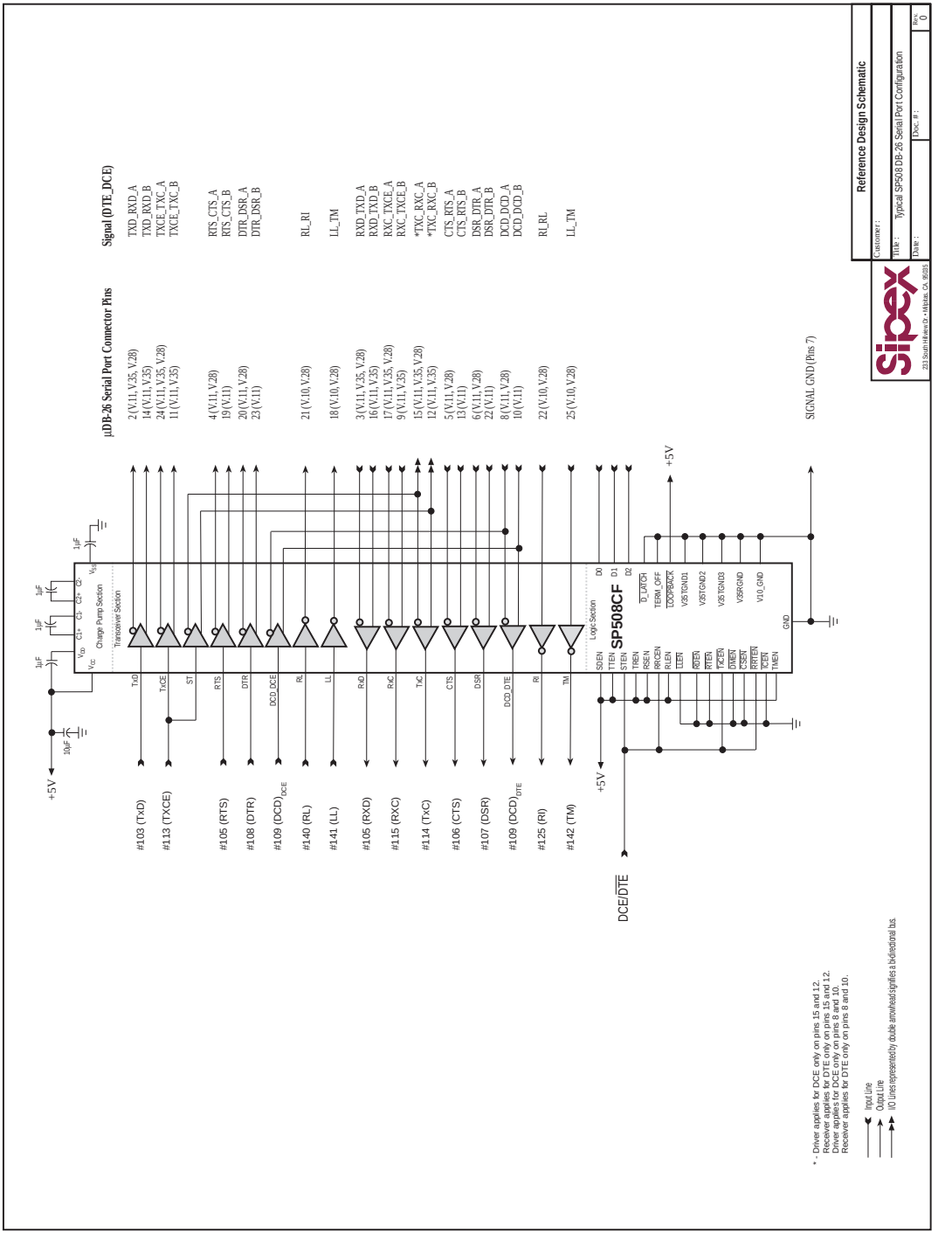
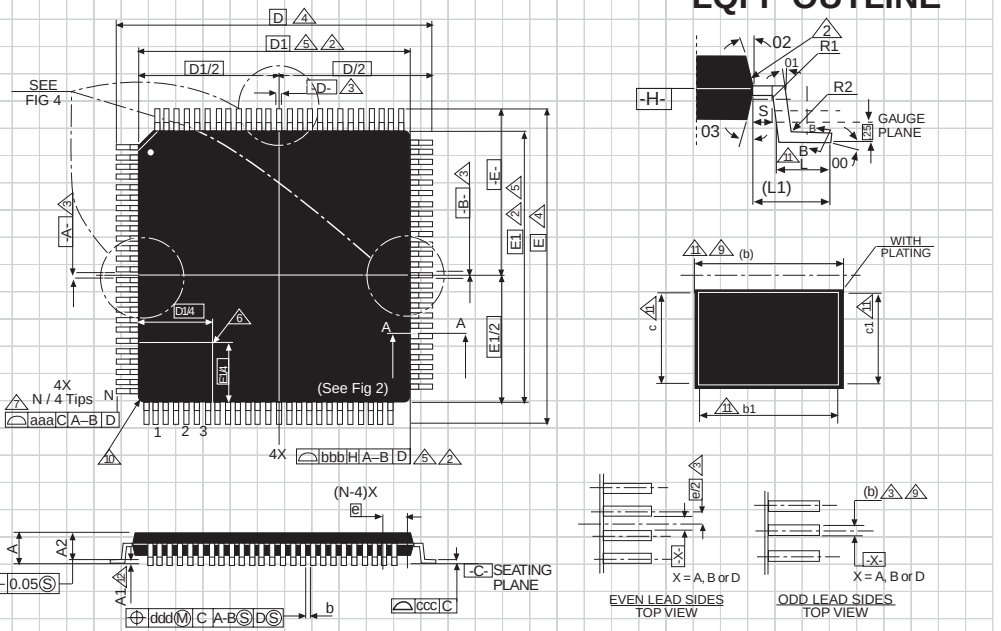


Figure 47. SP508 Typical Operating Configuration to Serial Port Connector with DCE/DTE programmability

PRELIMINARY INFORMATION

PACKAGE: QUAD FLATPACK LQFP OUTLINE



1. ALL DIMENSIONING AND TOLERANCING CONFORMS TO ANSI Y14.5M-1982.
2. THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM PACKAGE BODY SIZE BY AS MUCH AS 0.15mm.
3. DATUMS A – B AND – D – TO BE DETERMINED AT DATUM PLANE – H –
4. TO BE DETERMINED AT SEATING PLANE – C –
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. RECTANGULAR VARIATIONS AHA AND BHA HAVE 38 AND 26 LEADS ON SIDES D AND E RESPECTIVELY. RECTANGULAR VARIATIONS AHB AND BHB HAVE 30 AND 20 LEADS ON SIDES D AND E RESPECTIVELY.
8. ALL DIMENSIONS ARE IN MILLIMETER.
9. DIMENSIONS b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm FOR 0.4mm AND 0.5mm PITCH PACKAGES.
10. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
11. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
12. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

SYMBOL	MS-026 *BED* SQUARE MIN	NOM	MAX	NOTE
A	1.40	1.50	1.60	
A1	0.05	0.10	0.15	
A2	1.35	1.40	1.45	
D		16.00 BSC		4
D1		14.00 BSC		5, 2
E		16.00 BSC		4
E1		14.00 BSC		5, 2
N		*100*		
e		0.50 BSC		
b	0.17	0.22	0.27	9
b1	0.17	0.20	0.23	
R2	0.08	–	0.20	
R1	0.08	–	–	
00	0°	3.5°	7°	
01	0°	–	–	
02	11°	12°	13°	
03	11°	12°	13°	
S	0.20	–	–	
c	0.09	–	0.20	
c1	0.09	–	0.16	
L	0.45	0.60	0.75	
L1		1.00 REF		
Tolerance of Form and Position				
aaa		0.20		
bbb		0.20		
ccc		0.08		
ddd		0.08		
NOTE		1, 8		
REF		11 - 411		
ISSUE		A		

PRELIMINARY INFORMATION

ORDERING INFORMATION

Model	Temperature Range	Package Types
SP508CF	0°C to +70°C	100–pin JEDEC LQFP

SIGNAL PROCESSING EXCELLENCE

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