NEC

CMOS DIGITAL INTEGRATED CIRCUITS

μPD2845GR

1 V, 1.3 mA, 94MHz PLL SYNTHESIZER LSI FOR PAGER SYSTEM

DESCRIPTION

μPD2845GR is a PLL synthesizer LSI for pager system. This LSI is manufactured using low voltage CMOS process and therefore realized the low power consumption PLL operated on 1 V, 1.3 mA. This LSI is packaged in 16 pin plastic SSOP suitable for high-density surface mounting. So, this product contributes to produce a long-life-battery and physically-small pager system.

FEATURES

- Operating frequency : · Input frequency : f_{in} = 10 MHz to 94 MHz
  · Reference oscillating frequency : $f_{x'tal}$ = 12.8 MHz
- Low Supply voltage : · PLL block : V_{DD1} = 1.00 V to 1.15 V @ f_{in} = 10 MHz to 70 MHz
  V_{DD1} = 1.05 V to 1.15 V @ f_{in} = 10 MHz to 94 MHz
  · Charge pump block: V_{DD2} = 3.0 V ± 300 mV
- Low power consumption — I_{DD} = 1.3 mA TYP. @ f_{in} = 70 MHz, $f_{x'tal}$ = 12.8 MHz
- Equipped with power-save function — Serial data can be received in power-save mode.
- Packaged in 16 pin plastic SSOP suitable for high-density surface mounting.

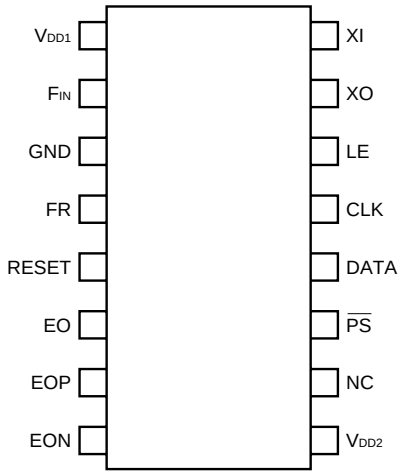
ORDERING INFORMATION

PART NUMBER	PACKAGE	SUPPLYING FORM
μPD2845GR-E1	16 pin plastic SSOP (225 mil)	Embossed tape 12 mm wide. QTY 2.5 k/reel Pin 1 is in tape pull-out direction.
μPD2845GR-E2	16 pin plastic SSOP (225 mil)	Embossed tape 12 mm wide. QTY 2.5 k/reel Pin 1 is in tape roll-in direction.

* To order evaluation samples, please contact your local NEC sales office (Order number : μPD2845GR).

PIN ASSIGNMENT

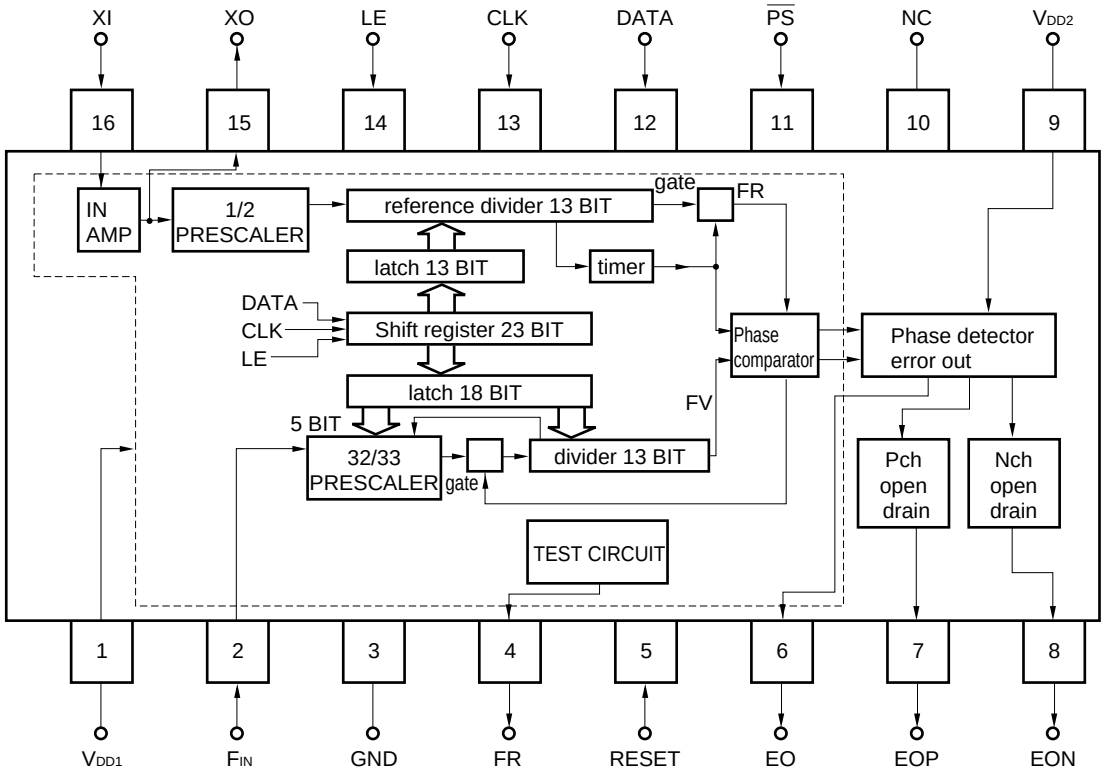
(Top View)



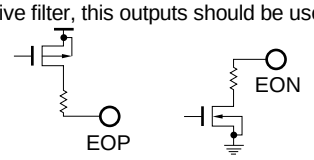
Caution Electro-static sensitive devices

Document No. P12150EJ2V0DS00 (2nd edition)
(Previous No. IC-3291)
Date Published February 1997 N

INTERNAL BLOCK DIAGRAM



PIN EXPLANATION

PIN No.	PIN NAME	I/O	EXPLANATION FOR FUNCTION
1	V_{DD1}	—	Supply voltage to PLL block
2	F_{IN}	I	Frequency Input
3	GND	—	Ground
4	FR	O	Test pin for monitor. Normally used as PLL, output L should be selected by test bit and this pin should be opened. (Refer to setting for reference counter on 11 page)
5	RESET	I	Test pin for monitor reset. (Refer to RESET on 12 page) Normally used as PLL, this pin should be grounded.
6	EO	O	Internal charge pump output. In the case of passive filter, this output should be used. Input signal phase f_p vs. reference signal f_r $f_p > f_r$: Low output $f_p < f_r$: High output $f_p = f_r$: High-impedance
7 8	EOP EON	O O	Outputs for external charge pump. In the case of active filter, this outputs should be used. EOP : PCH open drain EON : NCH open drain 
9	V_{DD2}	—	Supply voltage to charge pump.
10	NC	—	Non Connection.
11	$\overline{PS}$	I	Control bias input for power-save (Refer to Power-save on 12 page).
12	DATA	I	Data input for divided ratio.
13	CLK	I	Clock input for shift register.
14	LE	I	Latch enable input.
15 16	XO XI	O I	X'tal oscillator connection pin.

ABSOLUTE MAXIMUM RATINGS (UNLESS OTHERWISE SPECIFIED, T_A = +25 °C)

Supply Voltage	V_{DD1}	–0.3 to 2.0	V
	V_{DD2}	–0.3 to 6.0	V
Input Voltage	V_{I1}	–0.3 to V_{DD1} +0.3 (Except for DATA, CLK, LE, $\overline{PS}$ pin)	V
	V_{I2}	–0.3 to 6.0 (DATA, CLK, LE, $\overline{PS}$)	V
Output Voltage	V_{O1}	–0.3 to V_{DD1} +0.3 (XO, FR)	V
	V_{O2}	–0.3 to V_{DD2} +0.3 (EO, EOP, EON)	V
Output Current	I_O	10	mA
Operating Ambient Temperature	T_A	–10 to +50	°C
Storage Temperature	T_{stg}	–55 to +125	°C

RECOMMENDED OPERATING RANGE

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD1}	1.0	1.05	1.1	V
	V_{DD2}	2.85	3.0	3.15	V
Operating Ambient Temperature	T_A	–10	+25	+50	°C

ELECTRICAL CHARACTERISTICS

DC PERFORMANCE (Unless otherwise specified, V_{DD1} = 1.00 V to 1.15 V, V_{DD2} = 2.70 to 3.30 V, T_A = –10 to +50 °C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Supply Voltage	V_{DD1}	1.00	1.05	1.15	V	PLL Operation
	V_{DD2}	2.70	3.0	3.30	V	P/D Charge pump block
Circuit Current	I_{DD1}		1.3	2.2	mA	f_{in} = 70 MHz, 0.2 V_{P-P}. fx'tal = 12.8 MHz X'tal OSC IN. V_{DD1} = 1.0 V to 1.1 V V_{DD2} = 2.85 V to 3.15 V
Data Retain Current	I_{DR}		1.0	10	μA	No Input Signal, V_{DD1} = 1.1 V
High Level Output Current1[*1]	I_{OH1}	–1.0			mA	EO, EOP pin. V_{DD2} = 2.85 V V_{OH} = V_{DD2} –0.5 V
High Level Output Current2[*1]	I_{OH2}	–0.5			mA	XO pin. V_{OH} = V_{DD1} –0.5 V
High Level Output Current3[*1]	I_{OH3}	–0.1			mA	FR pin. V_{OH} = V_{DD1} –0.5 V
Low Level Output Current1[*2]	I_{OL1}	1.0			mA	EO, EON pin. V_{DD2} = 2.85 V V_{OL} = 0.5 V
Low Level Output Current2[*2]	I_{OL2}	0.4			mA	XO pin. V_{OL} = 0.5 V
Low Level Output Current3[*2]	I_{OL3}	0.4			mA	FR pin. V_{OL} = 0.5 V
High Level Input Current1[*2]	I_{IH1}	0.4			μA	F_{IN}, XI pin. V_{IH} = V_{DD1} 1.0 V
Low Level Input Current1[*1]	I_{IL1}	–0.4			μA	F_{IN}, XI pin. V_{IL} = 0 V, V_{DD1} 1.0 V
High Level Input Current2[*2]	I_{IH2}			1.0	μA	DATA, CLK, LE, $\overline{PS}$ pin. V_{IH1} = 3.85 V
High Level Input Voltage1	V_{IH1}	0.8 × V_{DD1}		4.0	V	DATA, CLK, LE, PS pin.
Low Level Input Voltage1	V_{IL1}	0		0.2 × V_{DD1}	V	DATA, CLK, LE, PS pin.
High Level Input Voltage2	V_{IH2}	0.8 × V_{DD1}		V_{DD1}	V	RESET pin.
Low Level Input Voltage2	V_{IL2}	0		0.2 × V_{DD1}	V	RESET pin.
Output Leak Current	I_L		10^{-4}	±1.0	μA	EO, EOP, EON pin. V_{DD1} = 1.0 V to 1.1 V V_{DD2} = 2.85 V to 3.15 V

***1** Current from IC

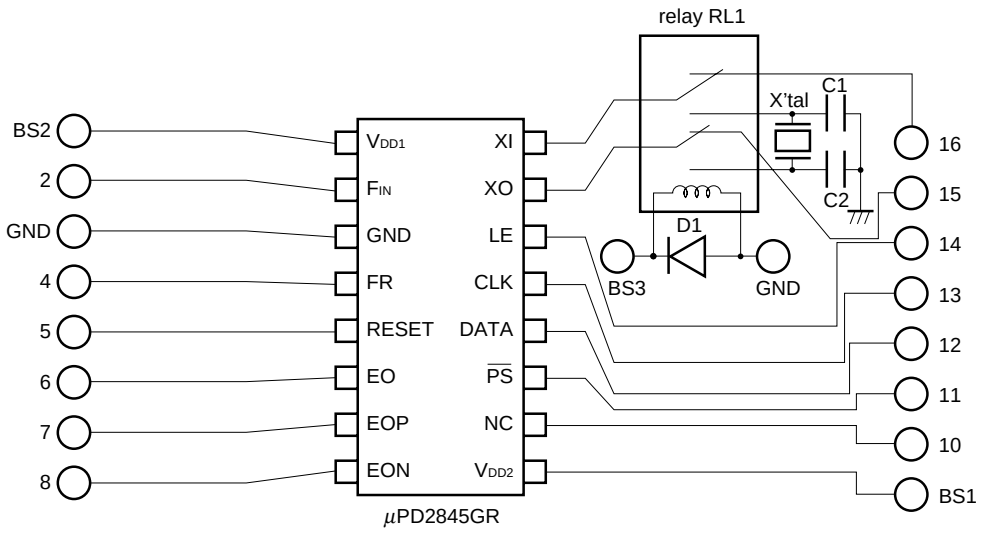
***2** Current into IC

AC PERFORMANCE (Unless otherwise specified, V_{DD1} = 1.00 V to 1.15 V, V_{DD2} = 2.70 to 3.30 V, T_A = –10 to +50 °C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Input frequency 1	f_{in1}	10		70	MHz	F_{IN} pin, V_{in} = 0.2 V_{P-P}
Input frequency 2	f_{in2}	10		94	MHz	F_{IN} pin, V_{in} = 0.2 V_{P-P}, V_{DD1} = 1.05 V to 1.15 V
Reference Oscillating Frequency	$f_{x'tal}$		12.8		MHz	XI, XO pin

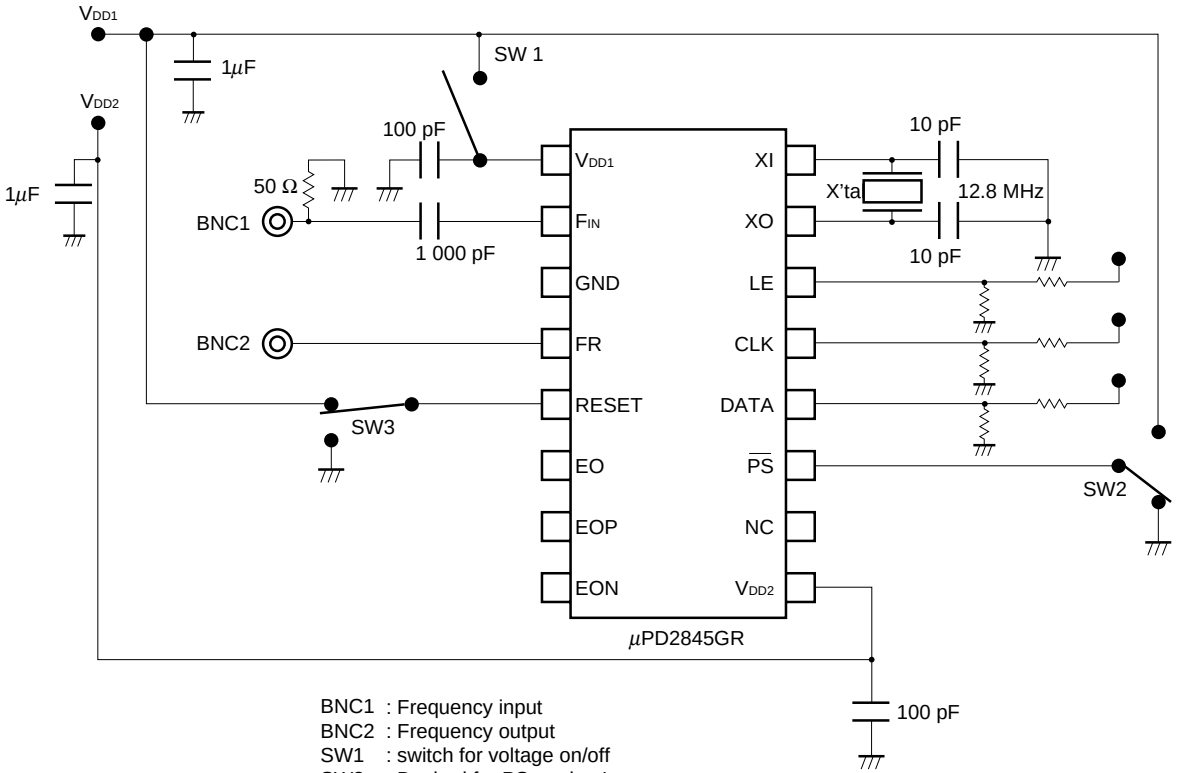
TEST CIRCUIT

DC measurement



relay RL1 : SRR-204
Diode D1 : 1S945
Capacitor C1,C2 : 18 pF
X'tal : 12.8 MHz

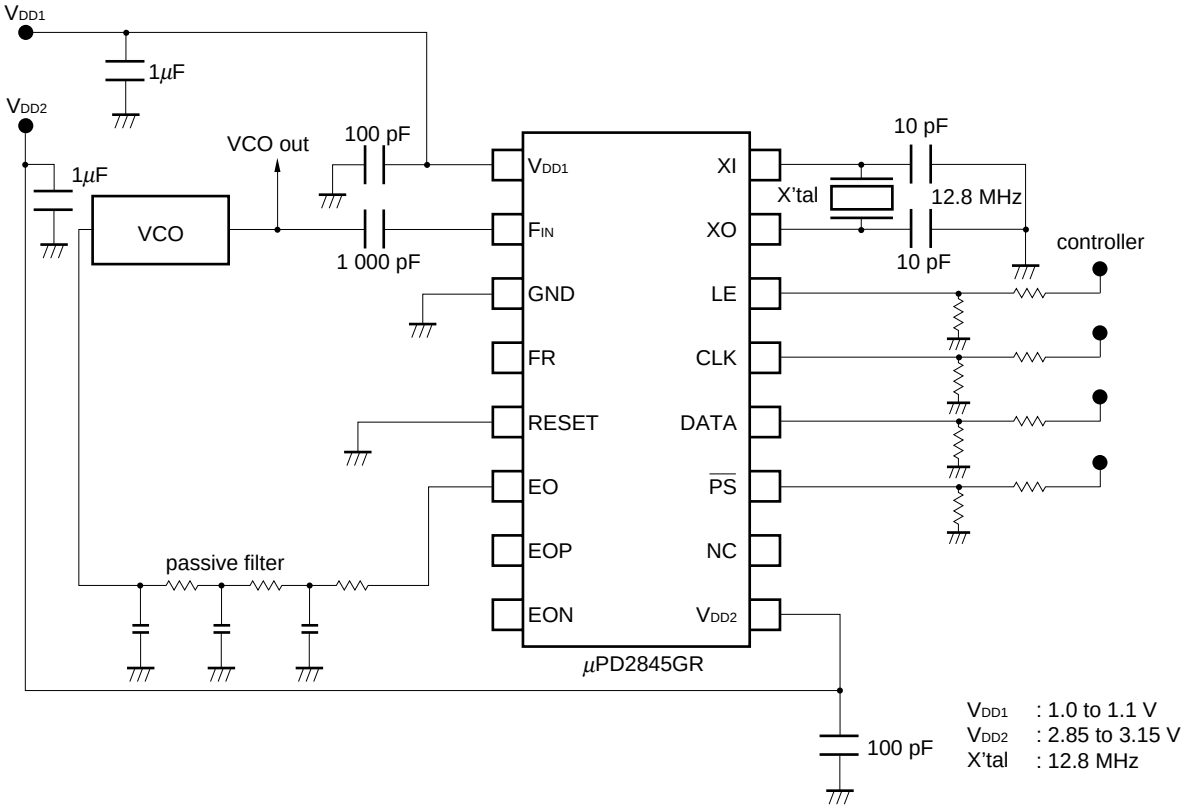
AC measurement



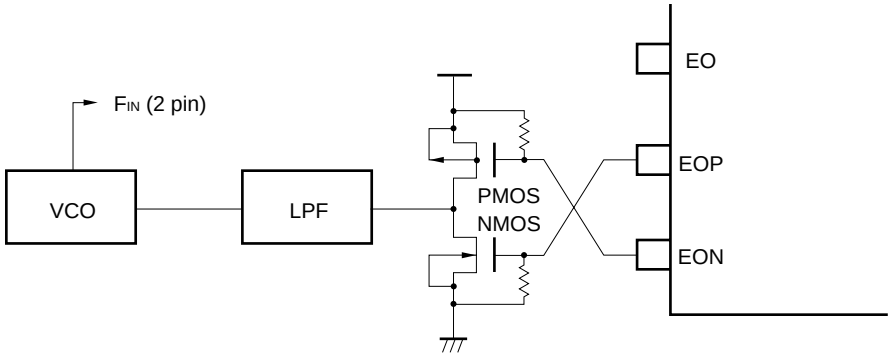
BNC1 : Frequency input
BNC2 : Frequency output
SW1 : switch for voltage on/off
SW2 : Desired for PS mode : Low
SW3 : Desired for reset mode : High

APPLICATION CIRCUIT EXAMPLES

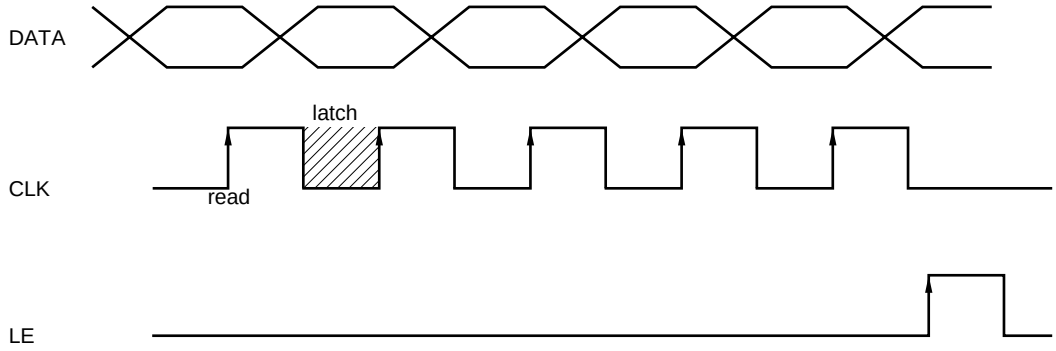
Passive filter application example (using internal charge pump)



Active filter application example (using external charge pump)



INPUT TIMING OF SERIAL DATA



This logic circuit is controlled by a 3-wire serial bus interface with DATA (12 pin), CLK (13 pin) and LE (14 pin).

On the control setting, Binary-coded serial data is input to DATA pin. This data is read into the shift register at the rising edge of the CLK signal input to the CLK pin. When the LE signal is at the low level, DATA CLK are received into the LSI to be latched at the rising edge of the LE signal.

While the LE signal is at the high level, neither DATA nor CLK signals can be received.

CAUTION At the initial V_{CC} supplied time, serial data must be input, because the IC output is unstable on the non-data input stage. [Refer to 'Power-save (pin 11)' on 12 page]

INPUT SIGNAL DIVIDER

INPUT SIGNAL DIVIDER obtain the frequency: f_p input to phase comparator. This circuit divides input frequency: f_{in} to obtain f_p. This block consists of prescaler, 5 bit swallow counter, 13 bit main counter and divide-ratio control circuit.

Setting numbers

- Main counter M = 32 to 8 191
- Swallow counter S = 0 to 31
- Prescaler P = 32, P+1 = 33

Total divide ratio

$NT = S(P+1) + P(M-S) = PM+S = 32\,M+S\ (M \geq S)$

$\therefore NT = 1\,024$ to 262 143

Relation between f_p and f_{in}

$f_p = f_{in}/(32\,M+S)$

(ex)

At f_p = 5 kHz fin = 70 MHz

NT = 70 M/5 k = 14 000

Therefore 14 000 32 = 437 • • • 16

↑ ↑

M S

Reference Counter

Reference Counter obtain the frequency: f_r input to phase comparater. This circuit divides the reference oscillating frequency: $f_{X'tal}$ of X'tal or TCXO to obtain f_r. This block consists of 13 bit programmable reference counter and prescaler of divide-by-2.

Setting number

- 13 bit programmable reference counter R = 2 to 8 191

Total reference counter block divide ratio

$RT = 2 \times R$

$\therefore RT = 4$ to 16 382

Relation between f_r and $f_{X'tal}$

$f_r = (f_{X'tal}/2)/R$

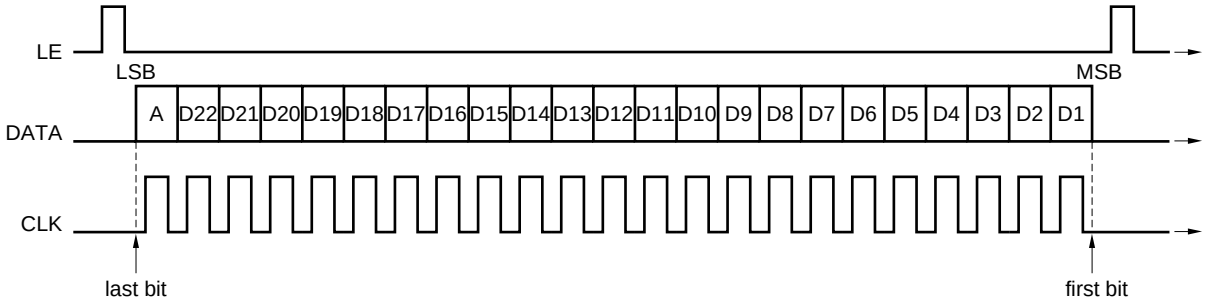
(ex)

f_r = 5 kHz $f_{X'tal}$ = 12.8 MHz

R = (12.8 MHz/2)/5 kHz = 1 280

Data format of shift register

Foundaly constraction of shift register



(1) Setting for data selection bit

Data selection bit: last A bit can govern the latch selection.

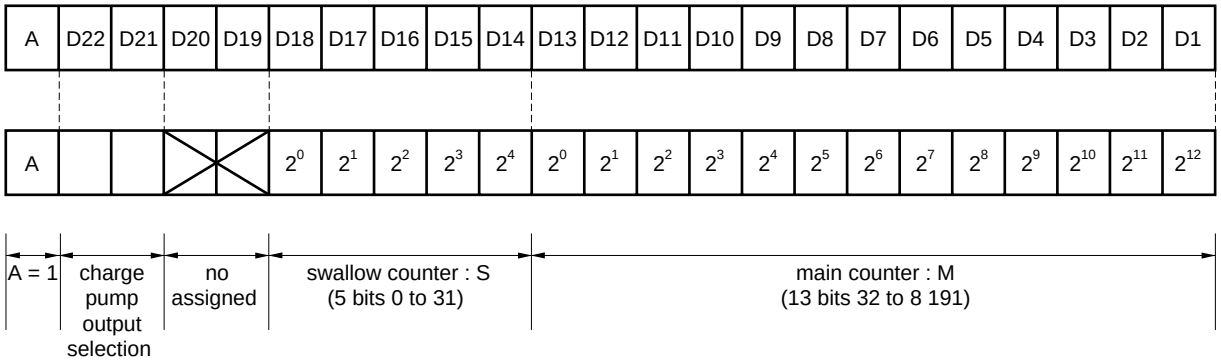
Data selection bit's construction and function

A	Function
1	Setting for swallow and main counter's divide ratio. Setting for charge pump output selection.
0	Setting for reference counter's divide ratio.

"0" = Low, "1" = High

(2) Setting for swallow/main counter's data and charge pump output selection

Bit constraction of setting for swallow/main counter and charge pump output selection



CAUTION D19, D20 are not assigned for setting but CLK signals must be input because of the bit construction.

- SWALLOW COUNTER DATA

  $S = (D14 \times 2^4) + (D15 \times 2^3) + (D16 \times 2^2) + (D17 \times 2^1) + (D18 \times 2^0)$

- MAIN COUNTER DATA

  $M = (D1 \times 2^{12}) + (D2 \times 2^{11}) + (D3 \times 2^{10}) + (D4 \times 2^9) + (D5 \times 2^8) + (D6 \times 2^7) + (D7 \times 2^6) + (D8 \times 2^5) + (D9 \times 2^4) + (D10 \times 2^3) + (D11 \times 2^2) + (D12 \times 2^1) + (D13 \times 2^0)$

NT = 32M + S

$= 32 \times \{(D1 \times 2^{12}) + (D2 \times 2^{11}) + (D3 \times 2^{10}) + (D4 \times 2^{9}) + (D5 \times 2^{8}) + (D6 \times 2^{7}) + (D7 \times 2^{6}) + (D8 \times 2^{5}) + (D9 \times 2^{4}) + (D10 \times 2^{3}) + (D11 \times 2^{2}) + (D12 \times 2^{1}) + (D13 \times 2^{0})\} + \{(D14 \times 2^{4}) + (D15 \times 2^{3}) + (D16 \times 2^{2}) + (D17 \times 2^{1}) + (D18 \times 2^{0})\}$

$\therefore NT = (D1 \times 2^{17}) + (D2 \times 2^{16}) + (D3 \times 2^{15}) + (D4 \times 2^{14}) + (D5 \times 2^{13}) + (D6 \times 2^{12}) + (D7 \times 2^{11}) + (D8 \times 2^{10}) + (D9 \times 2^{9}) + (D10 \times 2^{8}) + (D11 \times 2^{7}) + (D12 \times 2^{6}) + (D13 \times 2^{5}) + (D14 \times 2^{4}) + (D15 \times 2^{3}) + (D16 \times 2^{2}) + (D17 \times 2^{1}) + (D18 \times 2^{0})$

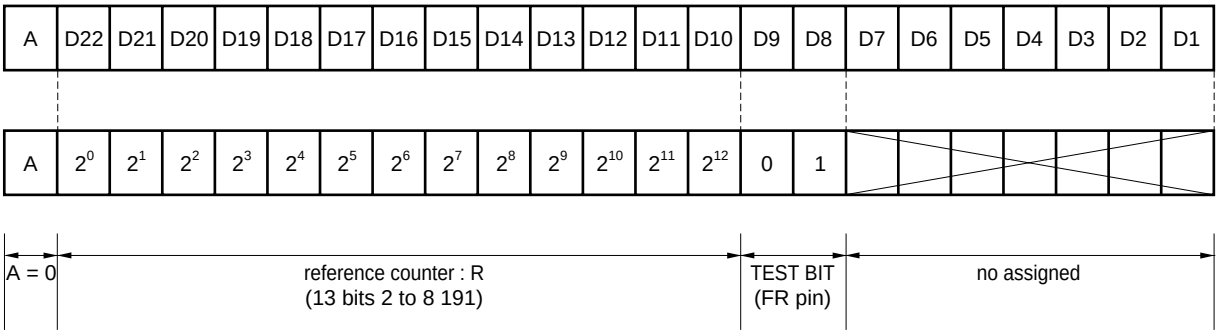
Thus, total divide ratio of input signal divider 'NT' can be transferred to binary-code in order to setting data 'D1 to D18' input. (D1 should be top digit and D18 should be bottom digit.)

- Charge pump output selection data

D22	D21	EO Pin (To use internal charge pump)	EOP, EO Pin (To use external charge pump)
0	0	Hi- Impedance	OFF
0	1	Hi-Impedance	OUTPUT
1	0	OUTPUT	OFF
1	1	OUTPUT	OUTPUT

"0" = Low, "1" = High

(3) Setting for reference counter



CAUTION D1 to D7 are not assigned for setting but CLK signals must be input because of the bit construction.

RT = 2 × R

$\therefore RT = 2 \times \{(D10 \times 2^{12}) + (D11 \times 2^{11}) + (D12 \times 2^{10}) + (D13 \times 2^{9}) + (D14 \times 2^{8}) + (D15 \times 2^{7}) + (D16 \times 2^{6}) + (D17 \times 2^{5}) + (D18 \times 2^{4}) + (D19 \times 2^{3}) + (D20 \times 2^{2}) + (D21 \times 2^{1}) + (D22 \times 2^{0})\}$

***TEST BIT:** for IC tester (FR pin) use or not use (PLL operation).
for normally PLL operation, input D9 = 0, D8 = 1 (FR pin = output L).

Power-save and RESET

Power-save (PIN 11)

Power-save-mode can be selected by input data to $\overline{PS}$ pin.

H; operation mode

L; power-save-mode

On the power-save-mode, reference oscillator and prescaler turn off and error-outs (EO, EOP, EON) output Hi-impedance but shift register data is remained. Serial data can be received in power-save-mode.

Note: Power-save usage for initial V_{CC} supplying

To prevent unstable mode at initial V_{CC} supplying, Power-save-mode must be selected. After counter data setting, normal operation mode can be selected.

RESET (PIN 5)

Reset-mode can be selected by input data to RESET pin.

H; reset-mode L(GND or Open); Normal operation.

On the reset-mode, reference oscillator/prescalers turn off and error-outs (EO, EOP, EON) output Hi-impedance.

Shift-register data is initialized.

This reset-mode should be used at LSI testing, normally use as PLL, RESET pin should be opened or grounded.

Supplementary explanation:

When RESET pin bias is switched from H to L, initial divide ratios can be set automatically as follows

- Input signal divider: NT = 10372
- 13 bit programmable reference counter: R = 1 280 (RT = 2 560)

These divide ratios make PLL loop without controller on condition as follows

f_{in} = 51.86 MHz

$f_{x'tal}$ = 12.8 MHz

$f_p = f_r$ = 5.0 kHz

PHASE COMPARATOR

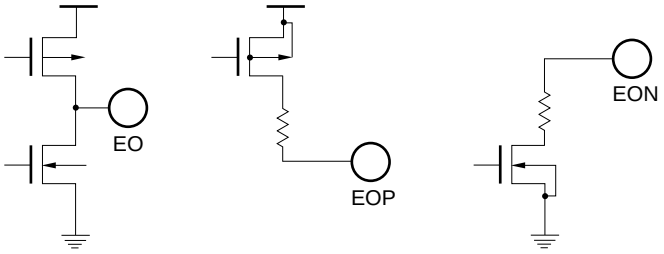
PHASE COMPARATOR compares the phase between divided input frequency (f_p) and reference frequency (f_r). This circuit make the change pump output signals according to following detection.

detection	EO*3	EOP*4	EON*4
$f_r > f_p$	H	H	OFF
$f_r = f_p$	Hi-Impedance	OFF	OFF
$f_r < f_p$	L	OFF	L

***3** To use internal charge pump (passive filter type)

***4** To use external charge pump (active filter type)

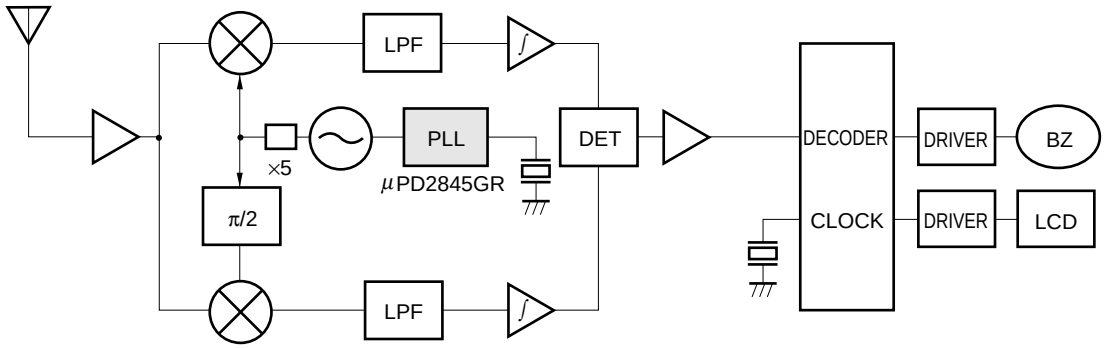
VCO should be used as type of 'higher voltage-higher frequency'.



EOP is Pch open drain, EON is Nch open drain. EO is output pin of internal charge pump.

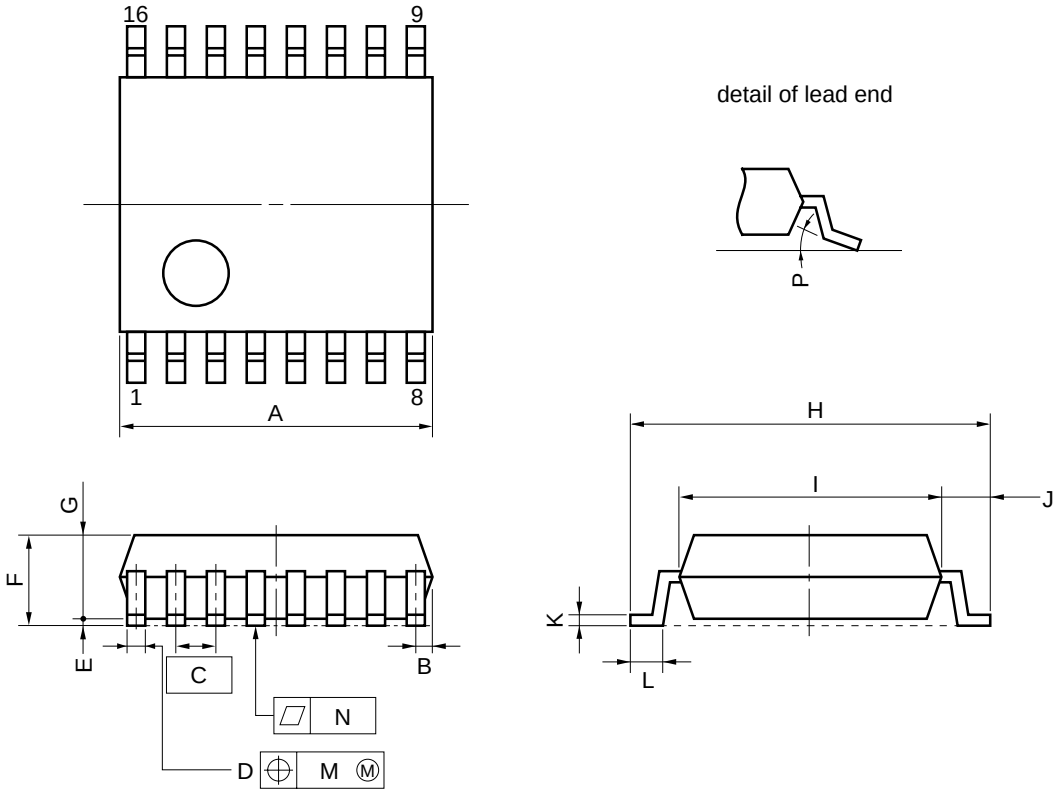
SYSTEM APPLICATION EXAMPLE

Pager block diagram of direct conversion type



PACKAGE DIMENSIONS

16 PIN PLASTIC SHRINK SOP (225 mil)



NOTE

Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	5.50 MAX.	0.217 MAX.
B	0.475 MAX.	0.019 MAX.
C	0.65 (T.P.)	0.026 (T.P.)
D	0.20±0.10	0.008±0.004
E	0.125±0.075	0.005±0.003
F	1.8 MAX.	0.071 MAX.
G	1.44	0.057
H	6.2±0.3	0.244±0.012
I	4.4±0.2	$0.173^{+0.009}_{-0.008}$
J	0.9±0.2	$0.035^{+0.009}_{-0.008}$
K	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.002}$
L	0.5±0.2	$0.020^{+0.008}_{-0.009}$
M	0.10	0.004
N	0.10	0.004
P	5°±5°	5°±5°

P16GM-65-225B-2

NOTE ON CORRECT USE

(1) Observe precautions for handling because of electrostatic sensitive devides.
(2) Form a ground pattern as wide as possible to minimize ground impedance.
(3) Connect a bypass capacitor (e. g. 1 000 pF) to the V_{DD} pin.
(4) The DC cut capacitor must be each attached to F_{IN}, XI and XO pin.
(5) External R, C values of loop filter should be determined according to the VCO specification.
(6) While VCO signal is not input to F_{IN} pin, power-save-mode must be set.
(7) After initially V_{CC}, V_{DD} are supplied, serial data should be input immediately. (Before serial data input, LSI operation is unstable or undesired.)

RECOMMENDED SOLDERING CONDITIONS

This product should be soldered in the following recommended conditions. Other soldering method and conditions than the recommended conditions are to be consulted with our sales representatives.

μPD2845GR

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak package's surface temperature: 235 °C or below, Reflow time: 30 seconds or below (210 °C or higher), Number of reflow process: 2, Exposure limit*: None	IR35-00-2
VPS	Peak package's surface temperature: 215 °C or below, Reflow time: 40 seconds or below (200 °C or higher), Number of reflow process: 2, Exposure limit*: None	VP15-00-2
Partial heating method	Terminal temperature: 300 °C or below, Flow time: 3 seconds or below, Exposure limit*: None	

*: Exposure limit before soldering after dry-package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Note Apply only a single process at once, except for "Partial heating method".
For details of recommended soldering conditions for surface mounting, refer to information document SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL (C10535E).

M4 96.5