1.1 Scope.

This specification covers the detail requirement for a monolithic CMOS 14-bit D/A converter, with output amplifier and operating off 5 V supplies. It has a fast parallel and serial microprocessor interface structure.

1.2 Part Number.

The complete part number is:

Device	Part Number[1]
−1	AD7840S(X)/883B

NOTE
[1]To complete the part number substitute the package identifier as shown in paragraph 1.2.3.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-24	24-Pin Cerdip, 0.3"
E	E-28A	28-Contact LCC

1.3 Absolute Maximum Ratings. (T_A = +25°C unless otherwise noted)

V_{DD} to AGND ..... −0.3 V to +7 V
V_{SS} to AGND ..... +0.3 V to −7 V
AGND to DGND ..... −0.3 V to V_{DD} +0.3 V
V_{OUT} to AGND ..... V_{SS} to V_{DD}
REF OUT to AGND ..... 0 V to V_{DD}
Digital Inputs to DGND ..... −0.3 V to V_{DD} +0.3 V
Operating Temperature Range ..... −55°C to +125°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering 10 sec) ..... +300°C
Power Dissipation (Any Package)
  Up to +75°C ..... 450 mW
  Derates above +75°C ..... 100 mW/°C

1.4 Recommended Operating Conditions.

Supply Voltage: V_{DD} = +5 V ±5%, V_{SS} = −5 V ±5%, AGND = DGND = 0 V.
Reference: REF IN = +3 V, R_L = 2 kΩ, C_L = 100 pF.

AD7840—SPECIFICATIONS

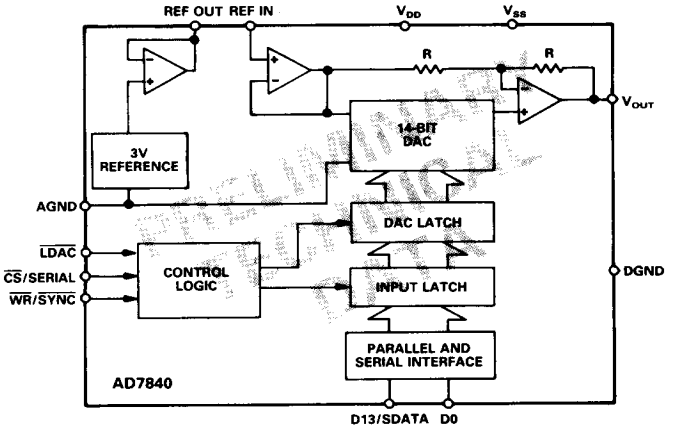
Table 1.

Test	Symbol	Device	Limits Min	Limits Max	Sub Groups	Test Condition[1] $-55°C \le T_A \le +125°C$ unless otherwise specified	Unit
Resolution	RES	−1	14		1, 2, 3	Guaranteed Minimum Resolution	Bits
Signal-to-Noise Ratio[2]	SNR	−1	76		4, 5, 6	V_{OUT} = 1.0 kHz Sine Wave f_{SAMPLE} = 100 kHz V_{OUT} = ±3.0 V p-p	dB
Total Harmonic Distortion	THD	−1		−78	4, 5, 6		dB
Peak Harmonic or Spurious Noise	HP	−1		−78	4, 5, 6		dB
Integral Nonlinearity	INL	−1		±2.0	1, 2, 3	Guaranteed Monotonic to 14 Bits	LSB
Differential Nonlinearity	DNL	−1		±0.9	1, 2, 3		LSB
Bipolar Zero Error	BZE	−1		±10	1, 2, 3		LSB
Positive Full-Scale Error[3]	+FSE	−1		±10	1, 2, 3		LSB
Negative Full-Scale Error[3]	−FSE	−1		±10	1, 2, 3		LSB
Reference Output Voltage[4]	V_{REF}	−1	2.99	3.01	1	T_A = +25°C	V
Reference Output Voltage Temperature Coefficient	ΔV_{OUT}	−1		±60	2, 3		ppm/°C
Reference Load Change	$\Delta V_{OUT}/\Delta I_{OUT}$	−1		−1.0	1, 2, 3	I_{OUT} = 0 μA to 500 μA	mV
Reference Input Voltage Range[5]	V_{REF}	−1	2.85	3.15	1, 2, 3		V
Reference Input Current	I_{REF}	−1		50	1, 2, 3	At 2.85 V to 3.15 V	μA
Input Logic High Voltage	V_{INH}	−1	2.4		7, 8		V
Input Logic Low Voltage	V_{INL}	−1		0.8	7, 8		V
Input Current	I_{IN}	−1		±10	1, 2, 3	V_{IN} = 0 V to V_{DD}	μA
Input Currrent ($\overline{CS}$) Input Only)	$I_{IN(\overline{CS})}$	−1		±10	1, 2, 3	V_{IN} = V_{SS} to V_{DD}	μA
Input Capacitance	C_{IN}	−1		10	4	T_A = +25°C	pF
Voltage Output Settling Time Positive Full-Scale Change[6, 7]	t_{S1}	−1		4.0	9	Settling Time to Within ±1/2 LSB LSB of Final Value, T_A = +25°C	μs
Voltage Output Settling Time Negative Full-Scale Change[6, 7]	t_{S2}	−1		4.0	9	Settling Time to Within ±1/2 LSB LSB of Final Value, T_A = +25°C	μs
Supply Current	I_{DD}	−1		15	1, 2, 3	Outputs Unloaded, SCLK = +5.0 V	mA
	I_{SS}			7.0			
$\overline{CS}$ to $\overline{WR}$ Setup Time[6, 7]	t_1	−1	0		9, 10, 11	Input tr = tf = 5.0 ns (10% to 90% of 5.0 V), Timing Voltage Reference Level = 1.6 V	ns
$\overline{CS}$ to $\overline{WR}$ Hold Time[6, 7]	t_2		0				
$\overline{WR}$ Pulse Width	t_3		50				
Data Valid to $\overline{WR}$ Setup Time	t_4		28				
Data Valid to $\overline{WR}$ Hold Time	t_5		15				
$\overline{LDAC}$ Pule Width[6, 7]	t_6		40				
$\overline{SYNC}$ to SCLK Falling Edge[6, 7]	t_7		50				
SCLK Cycle Time[6, 7]	t_8		200				
Data Valid to SCLK Setup Time[6, 7]	t_9		40				
Data Valid to SCLK Hold Time[6, 7]	t_{10}		100				
$\overline{SYNC}$ to SCLK Hold Time[6, 7]	t_{11}		100				

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

NOTES
[1]V_{DD} = +4.75 V to +5.25 V, V_{SS} = −4.75 V to −5.25 V; AGND = DGND = 0 V, REF IN = +3.0 V, R_L = 2.0 kΩ, and C_L = 100 pF unless otherwise specified.
[2]SNR calculation includes distortion and noise components.
[3]Measured with respect to REF IN and includes bipolar offset error.
[4]The maximum recommended capacitance on REF OUT for normal operation is 50 pF. If the reference is required for external use, it should be decoupled to AGND with a 200 Ω resistor in series with a parallel combination of a 10 μF tantalum capacitor and a 0.1 μF ceramic capacitor.
[5]This is the allowed range for REF IN. All tests are performed with REF IN = +3 V as described in Note 1.
[6]If not tested, shall be guaranteed to the limits specified in Table 1.
[7]Measured only for the initial die release and after process or design changes which might affect this parameter.

3.2.1 Functional Block Diagram and Terminal Assignments.

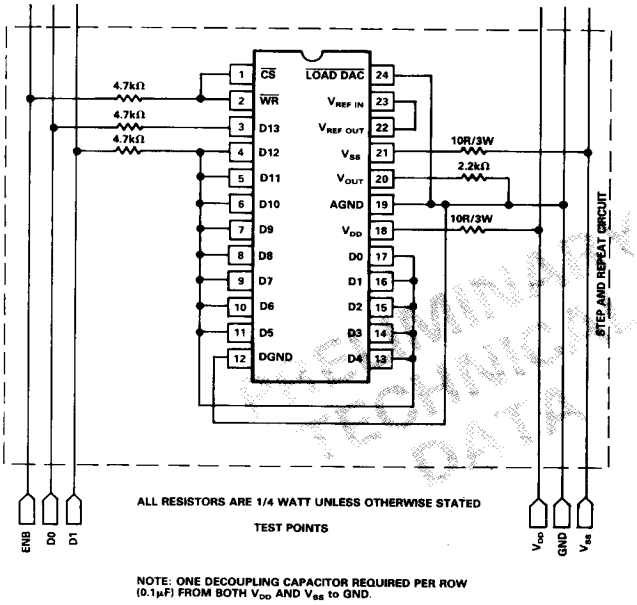


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (80).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



NOTE: ONE DECOUPLING CAPACITOR REQUIRED PER ROW (0.1μF) FROM BOTH V_{DD} AND V_{SS} to GND.

AD7840 BURN-IN PROCEDURE

POWER UP SEQUENCE

1. V_{DD}
2. V_{SS}

BURN-IN CONDITIONS (STATIC AND DYNAMIC)

1. V_{DD} = +5V
2. V_{SS} = −5V

I/P LOGIC LEVELS ARE 0 to 5V (ENB, D2, D1)