SRAM

512K x 8 SRAM

HIGH SPEED SRAM with
REVOLUTIONARY PINOUT

AVAILABLE AS MILITARY SPECIFICATIONS

•SMD 5962-95600
•MIL-STD-883

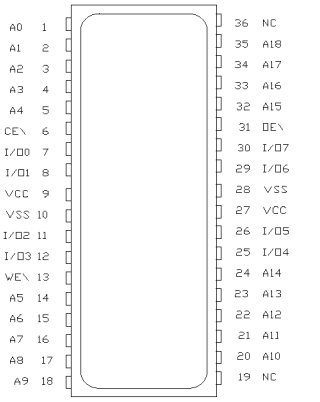
FEATURES

- Ultra High Speed Asynchronous Operation
- Fully Static, No Clocks
- Multiple center power and ground pins for improved noise immunity
- Easy memory expansion with CE\ and OE\ options
- All inputs and outputs are TTL-compatible
- Single +5V Power Supply +/- 10%
- Data Retention Functionality Testing (Contact Factory)
- Industrial and Military Temperature Range
  Military Range -55°C to + 125°C
  Industrial Range -40°C to + 85°C
- Cost Efficient Plastic Packaging
- Extended Testing Over -55°C to +125°C for plastics
- Plastic 36 pin PSOJ is fully compatible with the Ceramic 36 pin SOJ
- 3.3V Future Offering

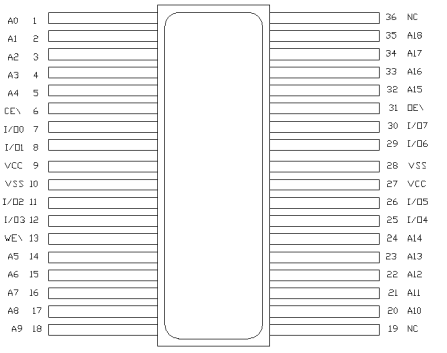
OPTIONS	MARKING	
• **Timing**		
12ns access	-12 (Consult Factory)	
15ns access	-15	
17ns access	-17	
20ns access	-20	
25ns access	-25	
35ns access	-35	
• **Package(s)**		
Ceramic LCC	EC	No. 210
Ceramic Flatpack	F	No. 307
Plastic SOJ	DJ	No. 903
Ceramic SOJ	ECJ	No.503
• 2V data retention/low power	L (Consult Factory)	
• Radiation Tolerant (EPI)	E (Consult Factory)	

PIN ASSIGNMENT (Top View)

36-Pin SOJ/LCC



36-Pin
Flat Pack



GENERAL DESCRIPTION

The AS5C512K8 offers flexibility in high-speed memory applications, with chip enable (CE\) and output enable (OE\) capabilities.

These features can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable (WE\) and CE\ inputs are both LOW. Reading is accomplished when WE\ remains HIGH and CE\ and OE\ go LOW.

As a option, the device can be supplied offering a reduced power standby mode. This allows system designer to meet low standby power requirements.

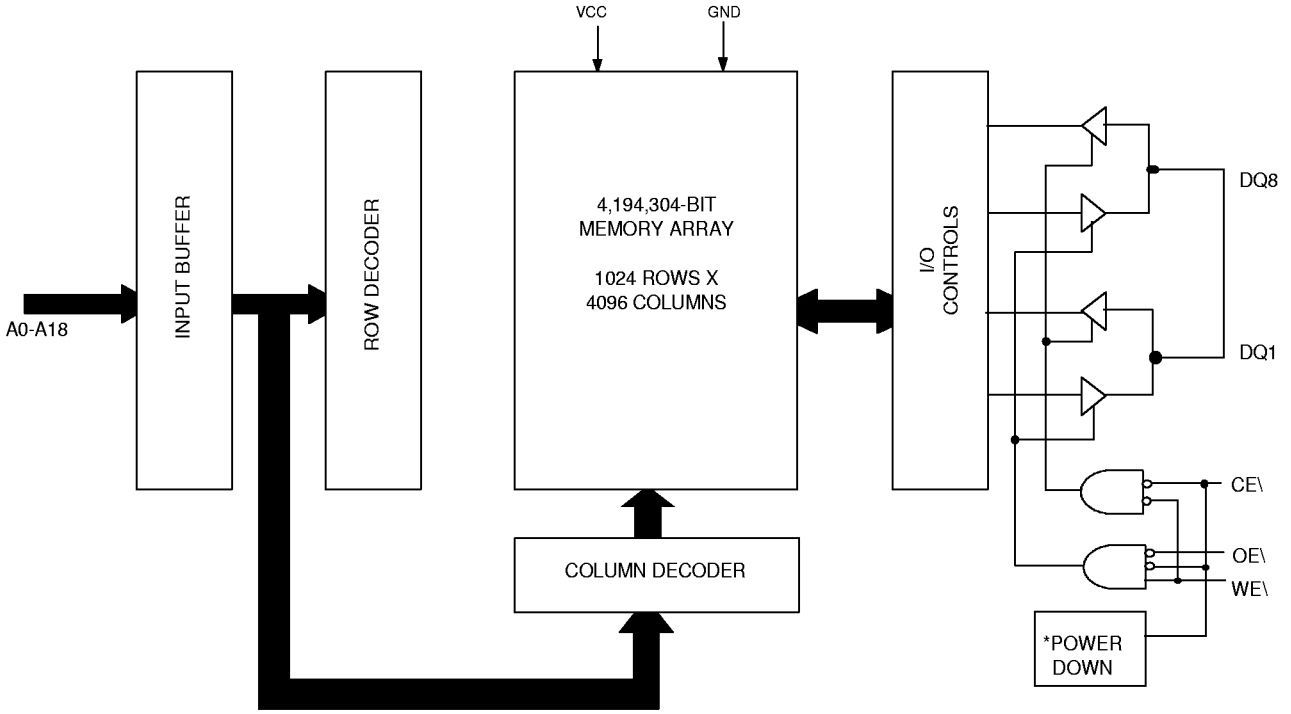
All devices operate from a single +5V power supply and all inputs and outputs are fully TTL-compatible.

The AS5C512K8DJ offers the convenience and reliability of the AS5C512K8 SRAM and has the cost advantage of a durable plastic.

The AS5C512K8DJ is tested to military specifications. When a device is operated beyond commercial temperatures the overall characteristics of the device will change. ASI ensures that this device will behave in an expected manner in military applications due to the extensive characterizations performed to meet military standards.

The AS5C512K8DJ is footprint compatible with 36 pin CSOJ package of the SMD 5692-95600.

FUNCTIONAL BLOCK DIAGRAM



**On the low voltage Data Retention option.*

TRUTH TABLE

MODE	OE\	CE\	WE\	I/O	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

X = Don't Care

PIN FUNCTIONS

A0 - A18	Address Inputs
WE\	Write Enable
CE\	Chip Enable
OE\	Output Enable
I/O_0 - I/O_7	Data Inputs/Outputs
V_{CC}	Power
V_{SS}	Ground
NC	No Connection

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss
Vcc .....-.5V to +7.0V
Storage Temperature .....-65°C to +150°C
Short Circuit Output Current (per I/O).....20mA
Voltage on any Pin Relative to Vss.....-.5V to Vcc+1 V
Junction Temperature**.....+150°C
Power Dissipation .....1 W

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
** Maximum junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow, and humidity.

MILITARY CONDITIONS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS
(-55°C ≤ T A ≤ 125°C; Vcc = 5V ±10%)- Military Temps

SYMBOL	DESCRIPTION	CONDITIONS		-12	-15	-17	-20	-25	-35	UNITS	NOTES
I_{CC}	Power Supply Current: Operating	CE\ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^{t}RC OUTPUTS OPEN	MAX	220	215	215	215	195	175	mA	3
I_{SBT1}	Power Supply Current: Standby	CE\ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^{t}RC OUTPUTS OPEN	MAX	65	60	60	60	50	40	mA	
I_{SBC}		CE\ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	MAX	20	20	20	20	20	20	mA	

SYMBOL	DESCRIPTION	CONDITIONS	MIN	MAX	UNITS	NOTES
V_{IH}	Input High (Logic 1) Voltage		2.2	VCC+.5	V	1
V_{IL}	Input Low (Logic 0) Voltage		-0.5	0.8		1,2
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	-5	5	µA	
I_{LO}	Output Leakage Current	Output(s) disabled 0V ≤ V_{OUT} ≤ V_{CC}	-5	5	µA	
V_{OH}	Output High Voltage	I_{OH} = -4.0 mA	2.4		V	1
V_{OL}	Output Low Voltage	I_{OL} =8 mA		0.4	V	1
V_{CC}	Supply Voltage		4.5	5.5	V	1

INDUSTRIAL CONDITIONS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS
(-40°C ≤ T A ≤ 85°C; Vcc = 5V ±10%)- Industrial Temps

SYMBOL	DESCRIPTION	CONDITIONS		-12	-15	-17	-20	-25	-35	UNITS	NOTES
I_{CC}	Power Supply Current: Operating	CE\ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^{t}RC OUTPUTS OPEN	MAX	210	205	195	185	175	165	mA	3
I_{SBT1}	Power Supply Current: Standby	CE\ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^{t}RC OUTPUTS OPEN	MAX	50	50	50	50	50	40	mA	
I_{SBC}		CE\ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	MAX	10	10	10	10	10	10	mA	

SYMBOL	DESCRIPTION	CONDITIONS	MIN	MAX	UNITS	NOTES
V_{IH}	Input High (Logic 1) Voltage		2.2	VCC+.5	V	1
V_{IL}	Input Low (Logic 0) Voltage		-0.5	0.8		1,2
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	-2	2	µA	
I_{LO}	Output Leakage Current	Output(s) disabled 0V ≤ V_{OUT} ≤ V_{CC}	-2	2	µA	
V_{OH}	Output High Voltage	I_{OH} = -4.0mA	2.4		V	1
V_{OL}	Output Low Voltage	I_{OL} = 8 mA		0.4	V	1
V_{CC}	Supply Voltage		4.5	5.5	V	1

Military and Industrial Conditions

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; 1 = MHz	C_I	8	pF	4
Output Capacitance	V_{CC} = 5V	C_O	10	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 5) (-55°C ≤ T_A ≤ 125°C; V_{CC} = 5V ±10%)

DESCRIPTION		-12		-15		-17		-20		-25		-35			
	SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle Time	^tRC	12		15		17		20		25		35		ns	
Address access time	^tAA		12		15		17		20		25		35	ns	
Chip Enable access time	^tACE		12		15		17		20		25		35	ns	
Output hold from address change	^tOH	2		2		2		2		2		2		ns	
Chip Enable to output in Low-Z	^tLZCE	2		2		2		2		2		2		ns	4, 6, 7
Chip disable to output in High-Z	^tHZCE		6		7		8		9		10		12	ns	4, 6, 7
Output Enable access time	^tAOE		6		7		8		8		10		12	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		0		0		ns	4, 6, 7
Output disable to output in High-Z	^tHZOE		6		7		8		9		10		12	ns	4, 6, 7
WRITE Cycle															
WRITE cycle time	^tWC	12		15		17		20		25		35		ns	
Chip Enable to end of write	^tCW	9		10		11		15		17		20		ns	
Address valid to end of write	^tAW	9		10		11		15		17		20		ns	
Address setup time	^tAS	0		0		0		0		0		0		ns	
Address hold from end of write	^tAH	1		1		1		1		1		1		ns	
WRITE pulse width (OE\ High)	$^tWP1$	9		10		11		15		17		20		ns	
WRITE pulse width (OE\ Low)	$^tWP2$	12		13		14		15		17		20		ns	
Data setup time	^tDS	6		7		7		10		12		15		ns	
Data hold time	^tDH	0		0		0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	2		2		2		2		2		2		ns	4, 6, 7
Write Enable to output in High-Z	^tHZWE		6		7		8		10		12		15	ns	4, 6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

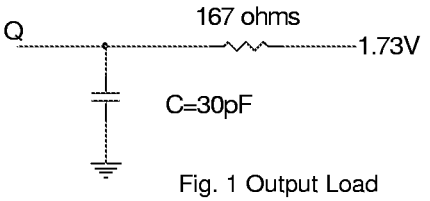


Fig. 1 Output Load Equivalent

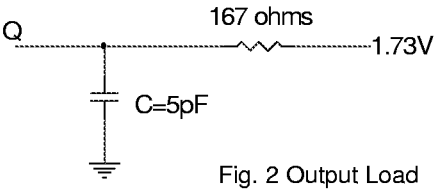


Fig. 2 Output Load Equivalent

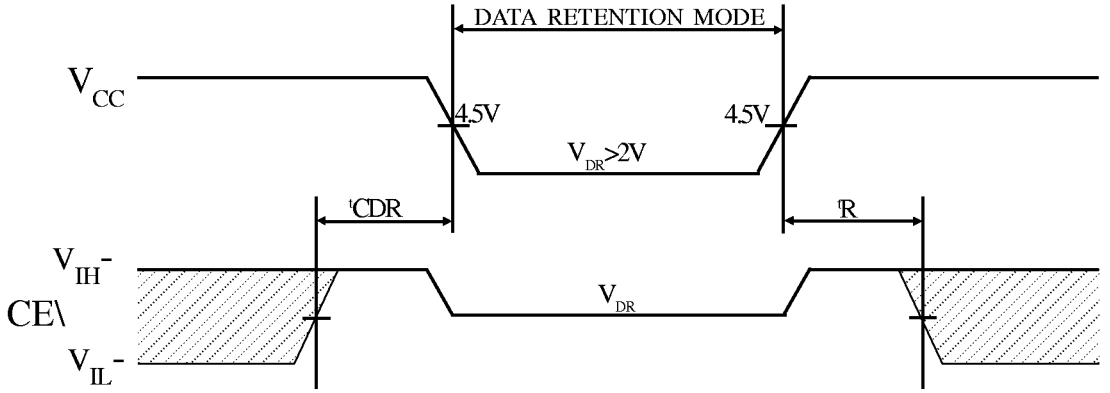
NOTES

1. All voltages referenced to V_{SS} (GND).
2. -2V for pulse width < 20ns
3. I_{CC} is dependent on output loading and cycle rates.
4. This parameter is guaranteed but not tested.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^tLZCE, ^tLZWE, ^tLZOE, ^tHZCE, ^tHZOE and ^tHZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±200mV from steady state voltage.
7. At any given temperature and voltage condition, ^tHZCE is less than ^tLZCE, and ^tHZWE is less than ^tLZWE.
8. WE\ is HIGH for READ cycle.
9. Device is continuously selected. Chip enables and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^tRC = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Output enable (OE\) is inactive (HIGH).
14. Output enable (OE\) is active (LOW).
15. ASI does not warrant functionality nor reliability of any product in which the junction temperature exceeds 150°C. Care should be taken to limit power to acceptable levels.

DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

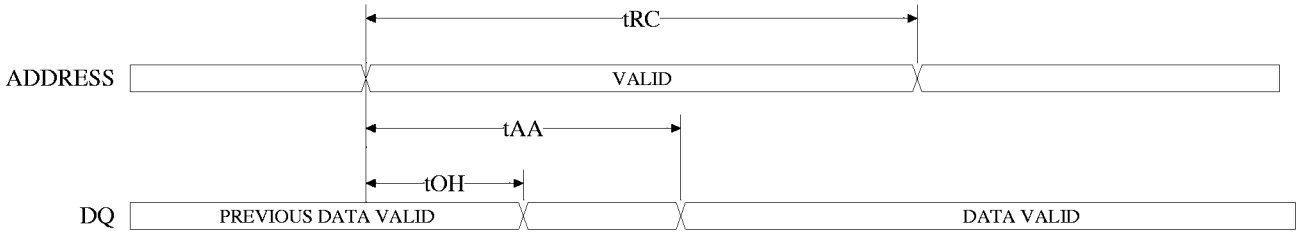
DESCRIPTION	CONDITIONS		SYMBOL	MIN	MAX	UNITS	NOTES
V_{CC} for Retention Data			V_{DR}	2		V	
Data Retention Current	CE\ ≥ V_{CC} - 0.2 V	V_{CC} = 2.0V	I_{CCDR}		20	mA	
	V_{IN} ≥ V_{CC} - 0.2 V	V_{CC} = 3.0V	I_{CCDR}		28	mA	
Chip Deselect to Data			t_{CDR}	0		ns	4
Retention Time							
Operation Recovery Time			t_R	t_{RC}		ns	4,11

LOW V_{CC} DATA RETENTION WAVEFORM



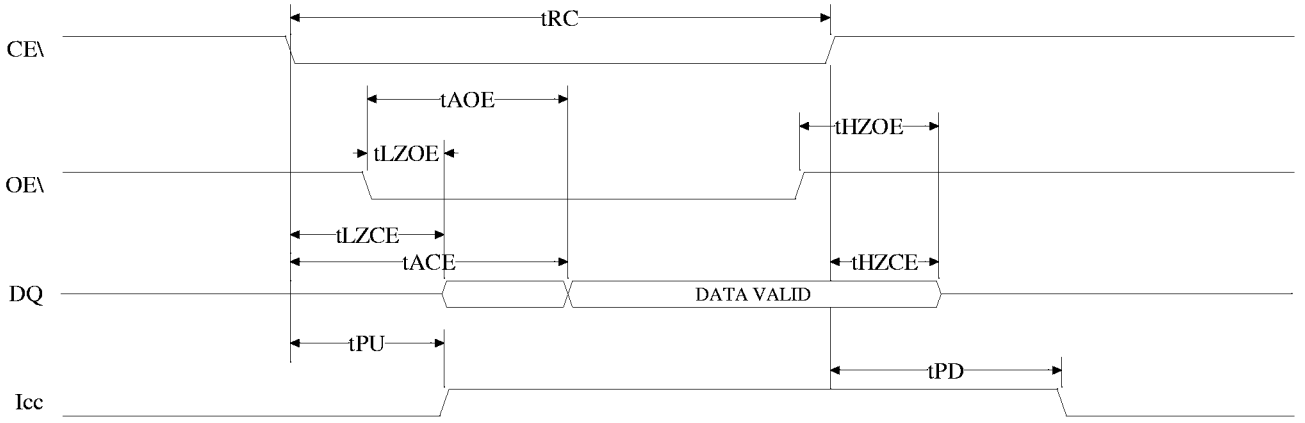
READ CYCLE NO. 1 [8,9]

(Address Controlled, CS\ = OE\ = V_{IL}, WE\ = V_{IH})



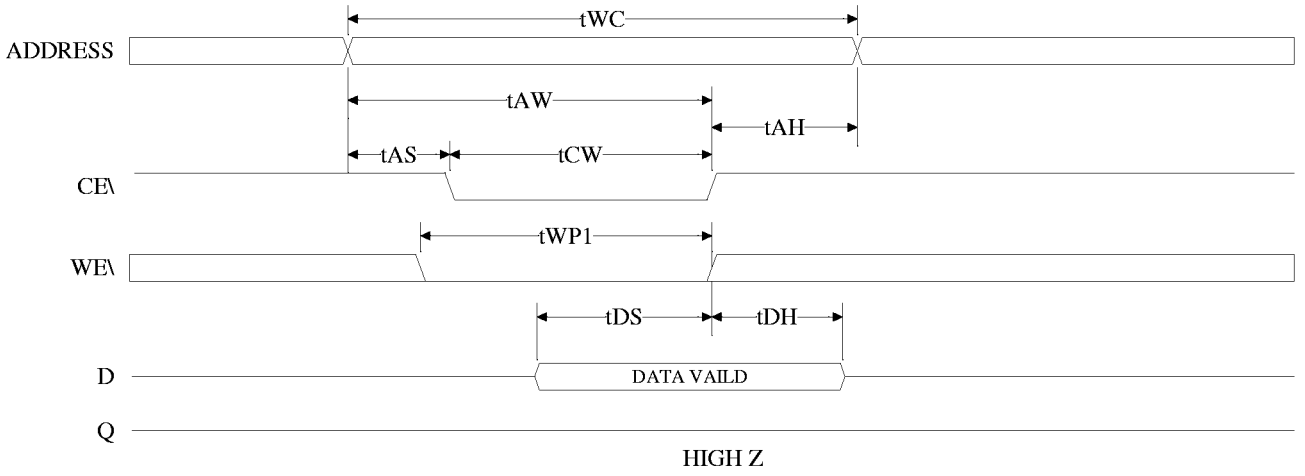
READ CYCLE NO. 2 [7,8,10]

(WE\ = V_{IH})



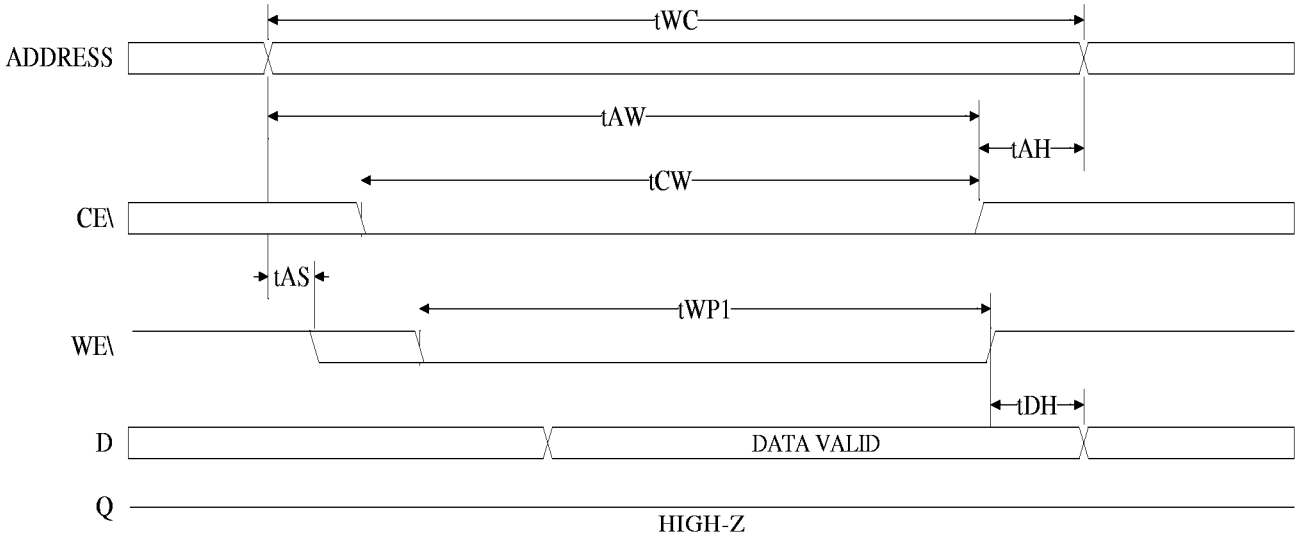
WRITE CYCLE NO. 1 [12]

(Chip Enabled Controlled)



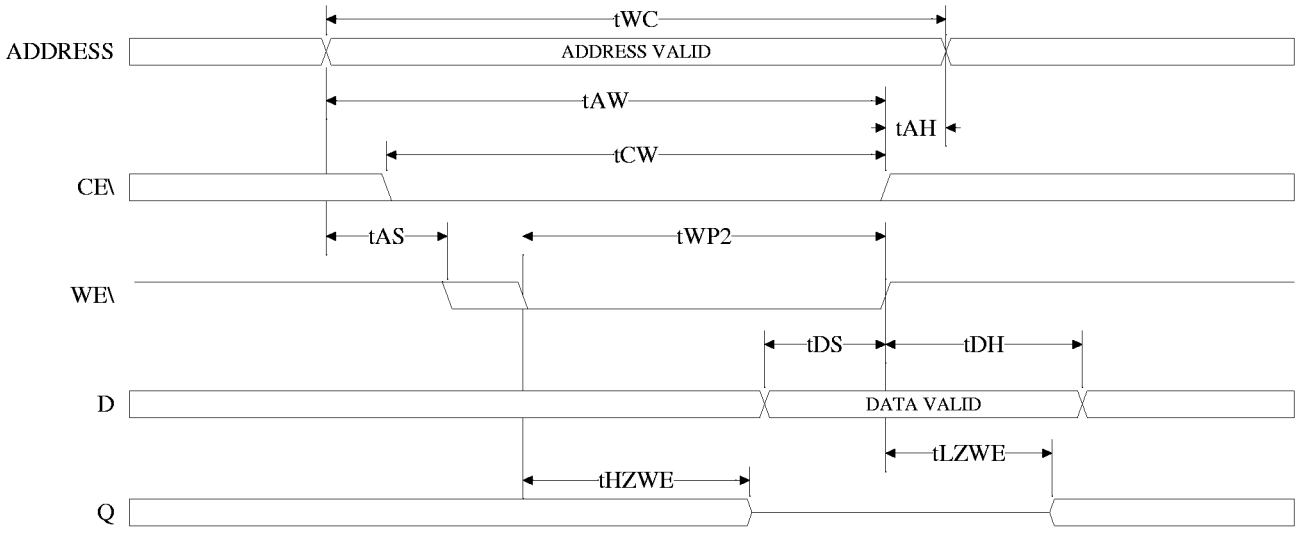
WRITE CYCLE NO. 2 [12, 13]

(Write Enabled Controlled)



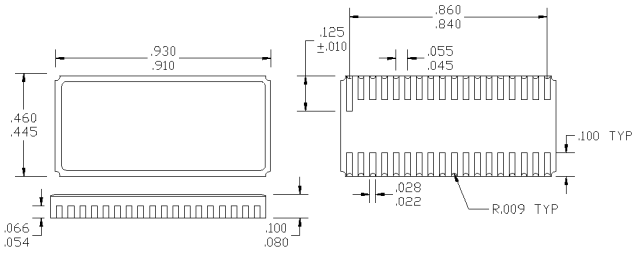
WRITE CYCLE NO. 3 [7, 12, 14]

(Write Enabled Controlled)

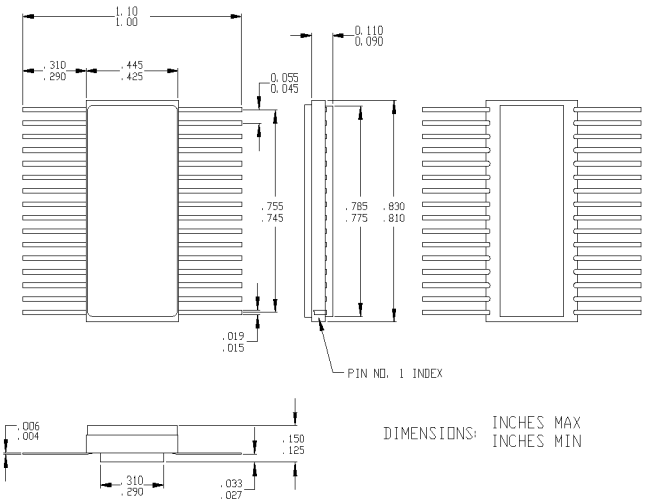


MECHANICAL DEFINITION

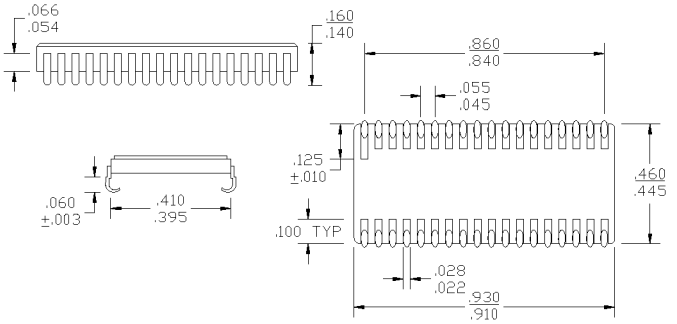
Package 210 / 36 Lead CLCC



Package 307 / 36 Lead FP



Package 503 / 36 Lead SOJ



Package 903 / 36 Lead Plastic SOJ