Features

- Fast Read Access Time - 120 ns
- Five Volt Only Reprogramming
- Page Program Operation
  - Single Cycle Reprogram (Erase and Program)
  - Internal Address and Data Latches for 64 Bytes
- Fast Program Cycle Times
  - Page (64 Byte) Program Time - 10 ms
  - Chip Erase Time - 10 ms
- Internal Program Control Timer
- Low Power Dissipation
  - 80 mA Active Current
  - 300 µA CMOS Standby Current
- Hardware and Software Data Protection
- DATA Polling for End of Program Detection
- High Reliability CMOS Technology
  - 1000 Erase/Program Cycles
  - 10 Year Data Retention
- Single 5V ± 10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- Full Military, Commercial, and Industrial Temperature Ranges
- Pin-Compatible with 29C010 and 29C512 for Easy System Upgrades

256K (32K x 8) 5-Volt Only CMOS PEROM

Description

The AT29C257 is a 5-volt-only in-system Programmable and Erasable Read Only Memory (PEROM). Its 256k of memory is organized as 32,768 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 120 ns with power dissipation of just 440 mW. When the device is deselected, the CMOS standby current is less than 300 µA.

To allow for simple in-system reprogrammability, the AT29C257 does not require high input voltages for programming. Five volt only commands determine the operation of the device. Reading data out of the device is similar to reading from a static RAM. Reprogramming the AT29C257 is performed on a page basis; 64 bytes of data are loaded into the device and then simultaneously programmed. The contents of the entire device may be erased by using a six-byte software code (although erasure before programming is not needed).

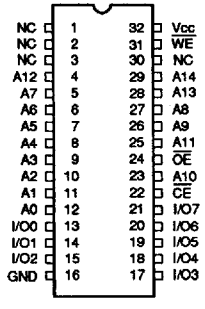
During a reprogram cycle, the address locations and 64 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a program cycle, the device will automatically erase the page and then program the latched data using an internal control timer. The end of a program cycle can be detected by $\overline{\text{DATA}}$ polling of I/O7. Once the end of a program cycle has been detected a new access for a read, program or chip erase can begin.

Pin Configurations

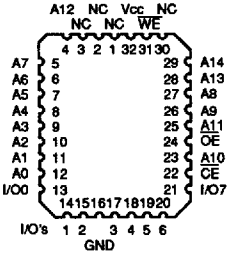
Pin Name	Function
A0 - A14	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect

Notes:
1. PLCC package pin 30 is a DON'T CONNECT.
2. To upgrade to the 1-Mbit 29C010, pin 3 is A15 and pin 2 is A16.

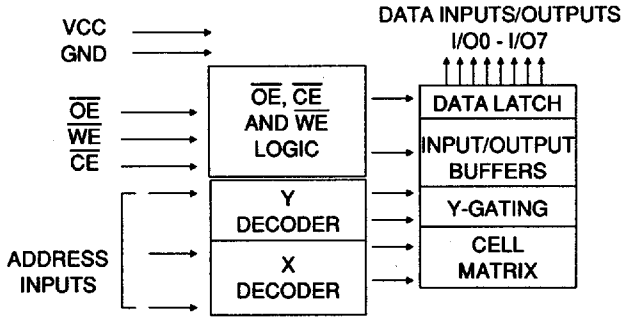
DIP Top View



PLCC and LCC Top View



Block Diagram



Device Operation

READ: The AT29C257 is accessed like a static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers flexibility in preventing bus contention.

BYTE LOAD: A byte load is performed by applying a low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Byte loads are used to enter the 64 bytes of a page to be programmed or the software codes for data protection and chip erasure.

PROGRAM: The device is reprogrammed on a page basis. If a byte of data within a page is to be changed, data for the entire page must be loaded into the device. Any byte that is not loaded during the programming of its page will be erased to read FFh. Once the bytes of a page are loaded into the device, they are simultaneously programmed during the internal programming period. After the first data byte has been loaded into the device, successive bytes are entered in the same manner. Each new byte to be programmed must have its high to low transition on $\overline{WE}$ (or $\overline{CE}$) within 150 µs of the low to high transition of $\overline{WE}$ (or $\overline{CE}$) of the preceding byte. If a high to low transition is not detected within 150 µs of the last low to high transition, the load period will end and the internal programming period will start. A6 to A14 specify the page address. The page address must be valid during each high to low transition of $\overline{WE}$ (or $\overline{CE}$). A0 to A5 specify the byte address within the page. The bytes may be loaded in any order; sequential loading is not required.

SOFTWARE DATA PROTECTION: A software controlled data protection feature is available on the AT29C257. Once the software protection is enabled a software algorithm must be issued to the device before a program may be performed. The software protection feature may be enabled or disabled by the user; when shipped from Atmel, the software data protection feature is disabled. To enable the software data protection, a series of three program commands to specific addresses with specific data must be performed. After the software data protection is enabled the same three program commands must begin each program cycle in order for the programs to occur. All software program commands must obey the page program timing specifications. Once set, the software data protection feature remains active unless its disable command is issued. Power transitions will not reset the software data protection feature, however the software feature will guard against inadvertent program cycles during power transitions.

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent programs to the AT29C257 in the following ways: (a) V_{CC} sense— if V_{CC} is below 3.8 V (typical), the program function is inhibited. (b) V_{CC} power on delay— once V_{CC} has reached the V_{CC} sense level, the device will automatically time out 5 ms (typical) before programming. (c) Program inhibit— holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits program cycles. (d) Noise filter— pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a program cycle.

PRODUCT IDENTIFICATION: The product identification mode identifies the device and manufacturer and may be ac-

continued on next page

Device Operation (Continued)

cessed by a hardware or software operation. For details, see Operating Modes or Software Product Identification.

$\overline{\text{DATA}}$ POLLING: The AT29C257 features $\overline{\text{DATA}}$ polling to indicate the end of a program cycle. During a program cycle an attempted read of the last byte loaded will result in the complement of the loaded data on I/O7. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. $\overline{\text{DATA}}$ polling may begin at any time during the program cycle.

TOGGLE BIT: In addition to $\overline{\text{DATA}}$ polling the AT29C257 provides another method for determining the end of a program or erase cycle. During a program or erase operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the program cycle has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a program cycle.

5-VOLT CHIP ERASE: The entire device may be erased at one time by using a six byte software code. The erase code consists of six byte load commands to specific address locations with specific data patterns. Once the code has been entered, the device will set each byte to the high state (FFh). After the software chip erase has been initiated, the device will internally time the erase operation so that no external clocks are required.

HIGH VOLTAGE CHIP ERASE: The contents of the entire device may be set to the high state by using an externally timed high voltage operation. $\overline{\text{OE}}$ is first raised to 12 volts with $\overline{\text{CE}}$ low and $\overline{\text{WE}}$ high; when $\overline{\text{WE}}$ is pulsed low for a minimum of 10 ms, the contents of the entire device is erased.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including N.C. Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} +0.6V
Voltage on $\overline{\text{OE}}$ with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Pin Capacitance (f=1MHz T=25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note: 4. This parameter is characterized and is not 100% tested.

D.C. and A.C. Operating Range

		AT29C257-12	AT29C257-15	AT29C257-20	AT29C257-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5V±10%	5V±10%	5V±10%	5V±10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Ai	I/O
Read	V_{IL}	V_{IL}	V_{IH}	Ai	D_{OUT}
Program[2]	V_{IL}	V_{IH}	V_{IL}	Ai	D_{IN}
5V Chip Erase	V_{IL}	V_{IH}	V_{IL}	Ai	
Standby/Write Inhibit	V_{IH}	X[1]	X	X	High Z
Write Inhibit	X	X	V_{IH}		
Write Inhibit	X	V_{IL}	X		
Output Disable	X	V_{IH}	X		High Z
High Voltage Chip Erase	V_{IL}	V_H [3]	V_{IL}	X	High Z
Product Identification	V_{IL}	V_{IL}	V_{IH}	A1-A14 = V_{IL}, A9 = V_H, A0 = V_{IL}	Manufacturer Code[4]
				A1-A14 = V_{IL}, A9 = V_H, A0 = V_{IH}	Device Code[4]

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to A.C. Programming Waveforms.
3. $V_H = 12.0V \pm 0.5V$.
4. Manufacturer Code: 1F, Device Code: DC

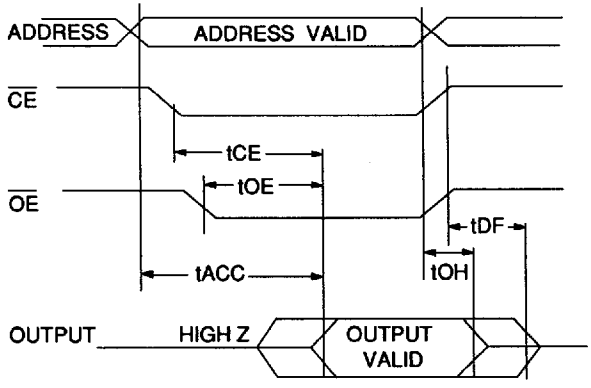
D.C. Characteristics

Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}		10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC}-0.3V to V_{CC}		300	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC}		3	mA
I_{CC}	V_{CC} Active Current	f= 5 MHz; I_{OUT} = 0 mA		50	mA
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		.45	V
V_{OH1}	Output High Voltage	I_{OH} = -400 µA	2.4		V
V_{OH2}	Output High Voltage CMOS	I_{OH} = -100 µA; V_{CC} = 4.5V	4.2		V

A.C. Read Characteristics

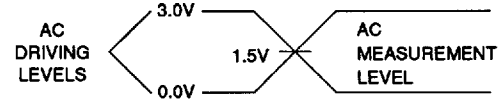
Symbol	Parameter	AT29C257-12		AT29C257-15		AT29C257-20		AT29C257-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		120		150		200		250	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		120		150		200		250	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	0	50	0	70	0	80	0	100	ns
t_{DF} (3,4)	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	40	0	50	0	55	0	60	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		0		ns

A.C. Read Waveforms



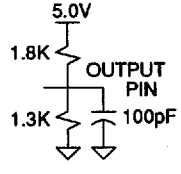
Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5ns

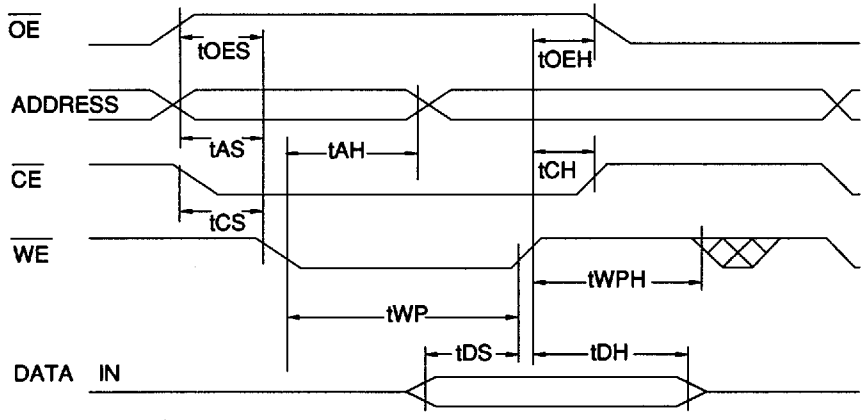
Output Test Load



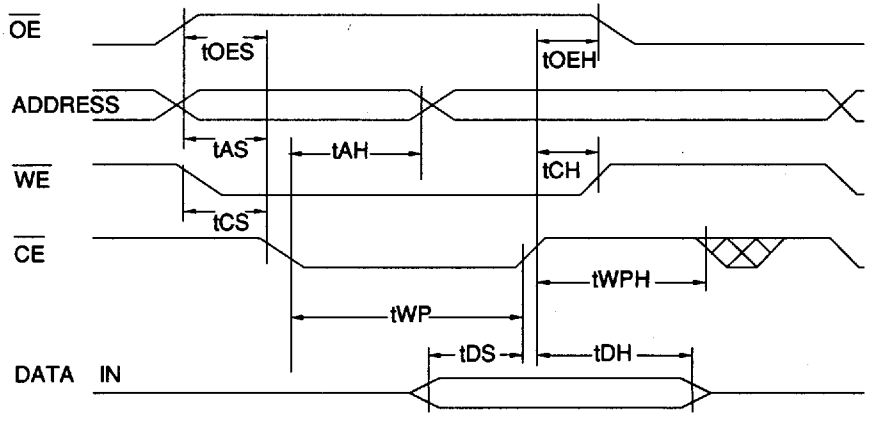
A.C. Byte Load Characteristics

Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	120		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH},t_{OEH}	Data, $\overline{OE}$ Hold Time	0		ns
t_{WC}	Write Cycle Time		10	ms

A.C. Byte Load Waveforms- $\overline{WE}$ Controlled



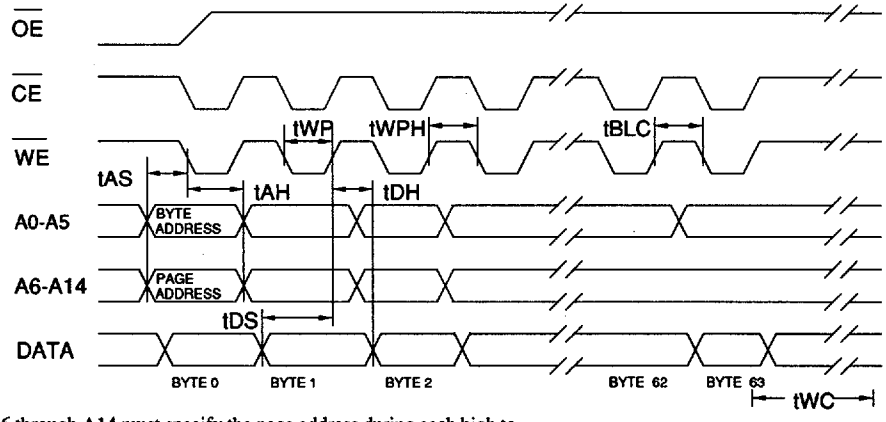
A.C. Byte Load Waveforms- $\overline{CE}$ Controlled



Program Cycle Characteristics

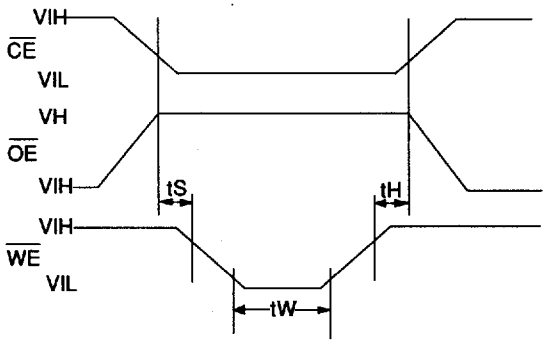
Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		10	ms
t_{AS}	Address Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}	Data Hold Time	0		ns
t_{WP}	Write Pulse Width	120		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	100		ns

Program Cycle Waveforms



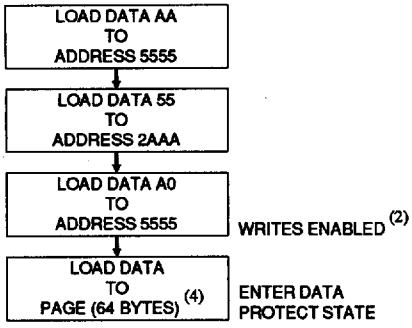
Notes: A6 through A14 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
$\overline{OE}$ must be high when $\overline{WE}$ and $\overline{CE}$ are both low.
All bytes that are not loaded within the page being programmed will be erased to FF.

High Voltage Chip Erase Waveforms

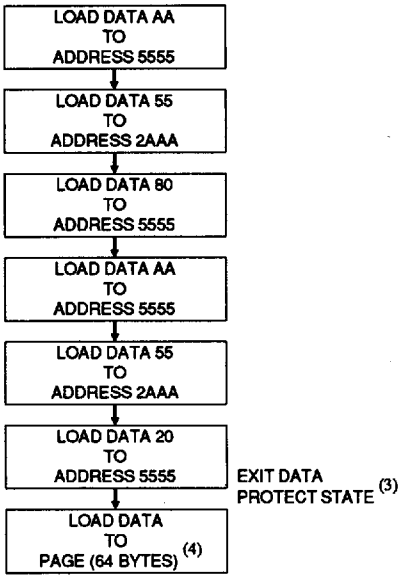


t_S = 5µsec (min.)
$t_W = t_H$ = 10msec (min.)
V_H = 12.0V ± 0.5V

Software Data Protection Enable Algorithm [1]

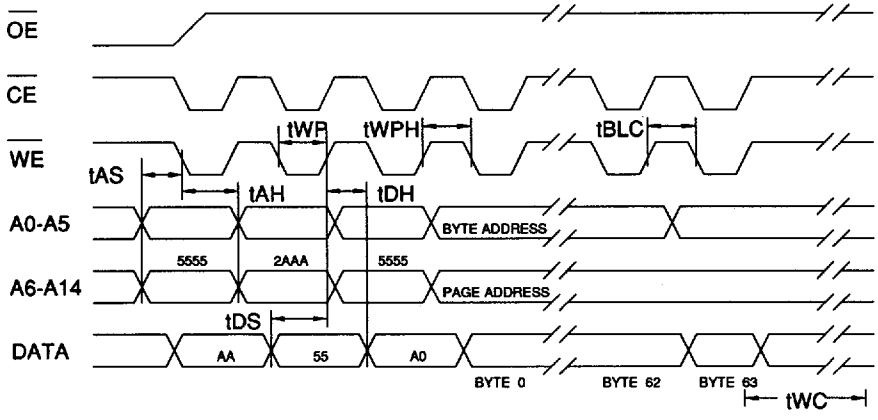


Software Data Protection Disable Algorithm [1]



Notes for software program code:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Data Protect state will be activated at end of program cycle.
3. Data Protect state will be deactivated at end of program period.
4. 64 bytes of data must be loaded.

Software Protected Program Cycle Waveform

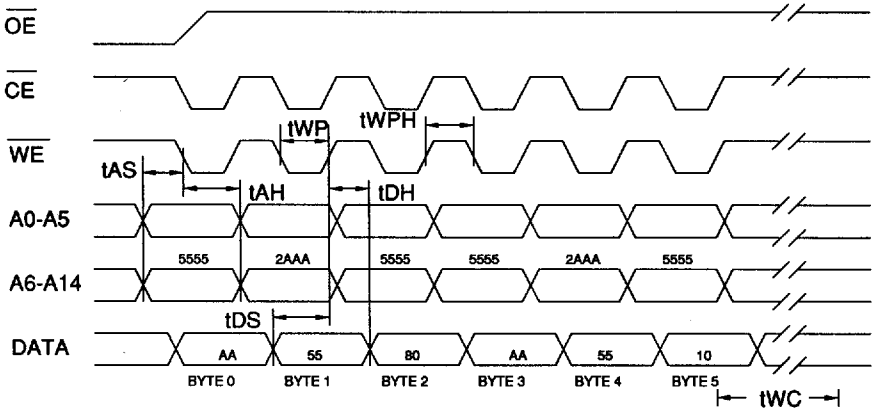


Notes: A6 through A14 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.
$\overline{OE}$ must be high when $\overline{WE}$ and $\overline{CE}$ are both low.
All bytes that are not loaded within the page being programmed will be erased to FF.

Chip Erase Cycle Characteristics

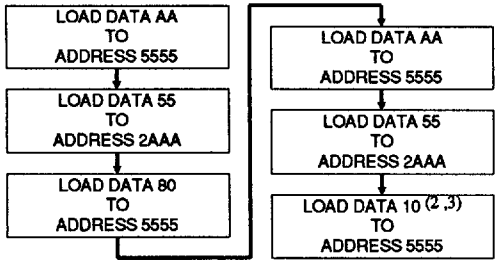
Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		10	ms
t_{AS}	Address Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}	Data Hold Time	0		ns
t_{WP}	Write Pulse Width	120		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	100		ns

Chip Erase Cycle Waveforms



Note: $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

Chip Erase Software Algorithm[1]



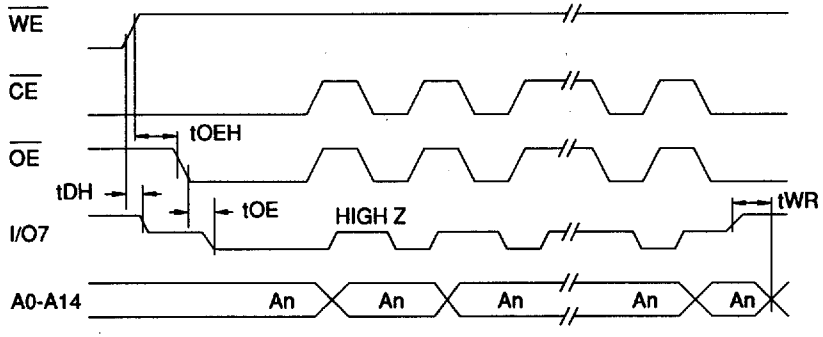
Notes for software erase code:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. $\overline{DATA}$ polling may be used to determine the end of the erase cycle by checking any address for data equal to FF.
3. After loading the six byte code, no byte loads are allowed until the completion of the erase cycle. The erase cycle will time itself to completion within twc.

$\overline{\text{Data}}$ Polling Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	0			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay			100	ns
t_{WR}	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

$\overline{\text{Data}}$ Polling Waveforms

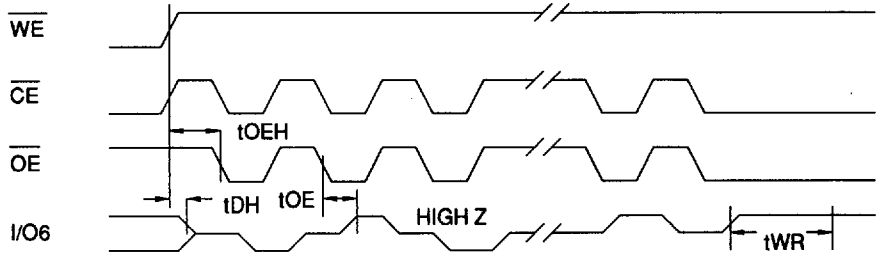


Toggle Bit Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	0			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay			100	ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

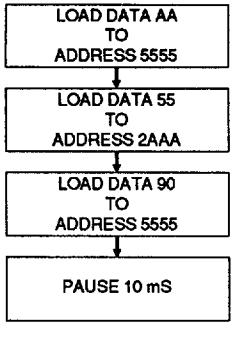
Note: 1. These parameters are characterized and not 100% tested.

Toggle Bit Waveforms

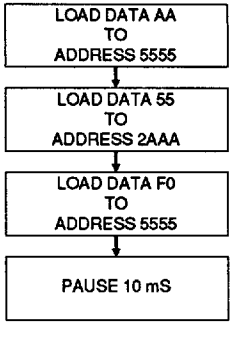


Notes:
1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

Software Product Identification Entry (1)

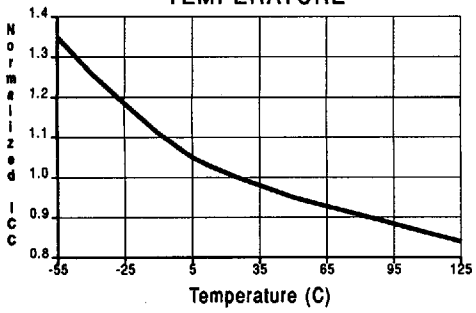


Software Product Identification Exit (1)

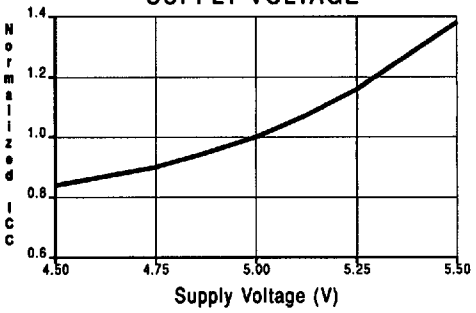


Notes for software product identification:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. A1 - A14 = V_{IL}.
   Manufacture Code is read for A0 = V_{IL};
   Device Code is read for A0 = V_{IH}.
3. The device does not remain in identification mode if powered down.
4. The device returns to standard operation mode.

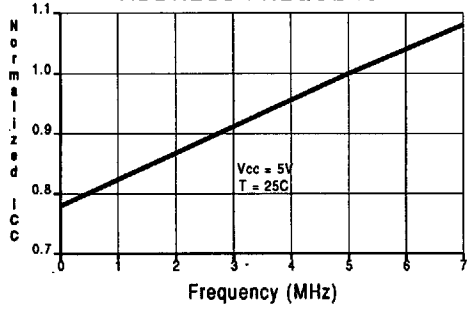
NORMALIZED SUPPLY CURRENT vs. TEMPERATURE



NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



NORMALIZED SUPPLY CURRENT vs. ADDRESS FREQUENCY



Ordering Information

tACC (ns)	ICC (mA) Active	ICC (mA) Standby	Ordering Code	Package	Operation Range
120	80	0.3	AT29C257-12DC AT29C257-12JC AT29C257-12LC AT29C257-12PC	32D6 32J 32L 32P6	Commercial (0° to 70°C)
			AT29C257-12DI AT29C257-12JI AT29C257-12LI AT29C257-12PI	32D6 32J 32L 32P6	Industrial (-40° to 85°C)
			AT29C257-12DM	32D6	Military (-55°C to 125°C)
			AT29C257-12DM/883	32D6	Military/883C Class B, Fully Compliant (-55°C to 125°C)
150	80	0.3	AT29C257-15DC AT29C257-15JC AT29C257-15LC AT29C257-15PC	32D6 32J 32L 32P6	Commercial (0° to 70°C)
			AT29C257-15DI AT29C257-15JI AT29C257-15LI AT29C257-15PI	32D6 32J 32L 32P6	Industrial (-40° to 85°C) (-40° to 85°C)
			AT29C257-15DM	32D6	Military (-55°C to 125°C)
			AT29C257-15DM/883	32D6	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	80	0.3	AT29C257-20DC AT29C257-20JC AT29C257-20LC AT29C257-20PC	32D6 32J 32L 32P6	Commercial (0° to 70°C)
			AT29C257-20DI AT29C257-20JI AT29C257-20LI AT29C257-20PI	32D6 32J 32L 32P6	Industrial (-40° to 85°C)
			AT29C257-20DM	32D6	Military (-55°C to 125°C)
			AT29C257-20DM/883	32D6	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	80	0.3	AT29C257-25DC AT29C257-25JC AT29C257-25LC AT29C257-25PC	32D6 32J 32L 32P6	Commercial (0° to 70°C)
			AT29C257-25DI AT29C257-25JI AT29C257-25LI AT29C257-25PI	32D6 32J 32L 32P6	Industrial (-40° to 85°C)

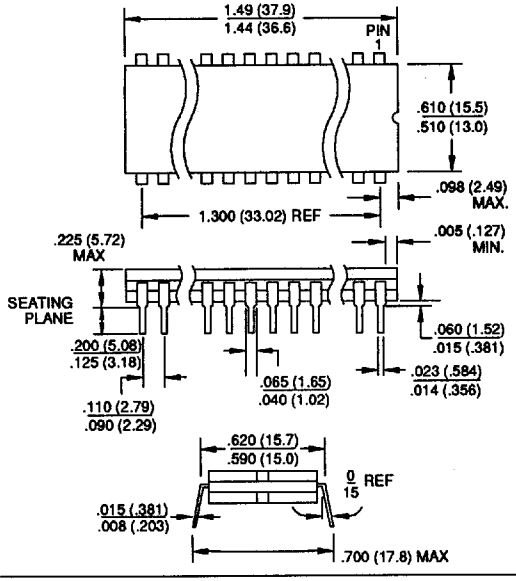
Ordering Information

tACC (ns)	ICC (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
250	80	0.3	AT29C257-25DM	32D6	Military (-55°C to 125°C)
			AT29C257-25DM/883	32D6	Military/883C Class B, Fully Compliant (-55°C to 125°C)

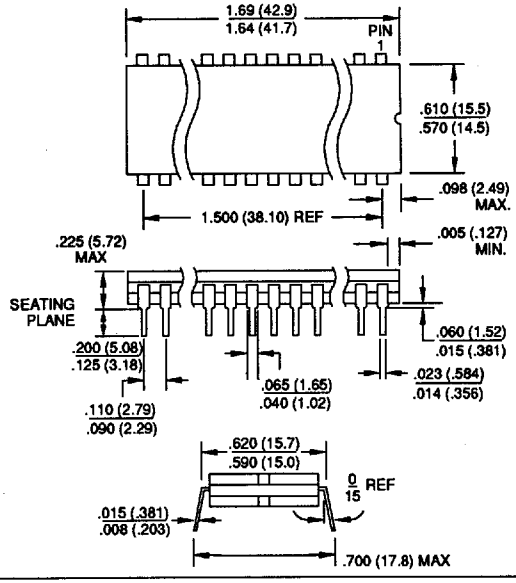
Package Type	
32D6	32 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32L	32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
32P6	32 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)

Packaging Information

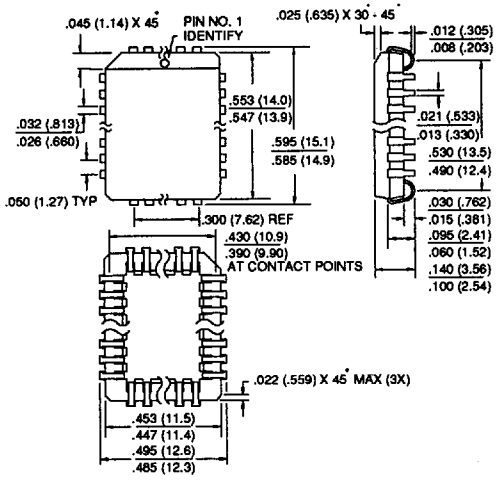
28D6, 28 Lead, 0.600" Wide, Non-Windowed,
Ceramic Dual Inline Package (Cerdip)
Dimensions in Inches and (Millimeters)
MIL-M-38510 D-10 CONFIG 1



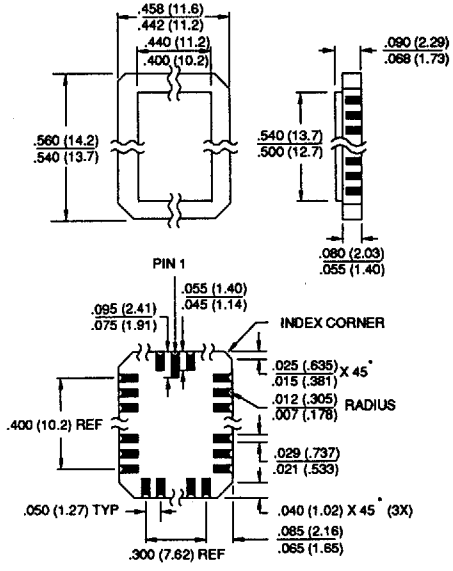
32D6, 32 Lead, 0.600" Wide, Non-Windowed,
Ceramic Dual Inline Package (Cerdip)
Dimensions in Inches and (Millimeters)



32J, 32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC OUTLINE MO-052 AE

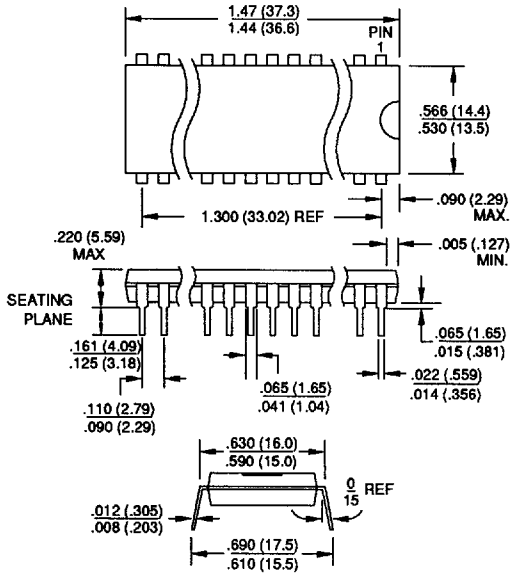


32L, 32 Pad, Non-Windowed,
Ceramic Leadless Chip Carrier (LCC)
Dimensions in Inches and (Millimeters)
MIL-M-38510 C-12

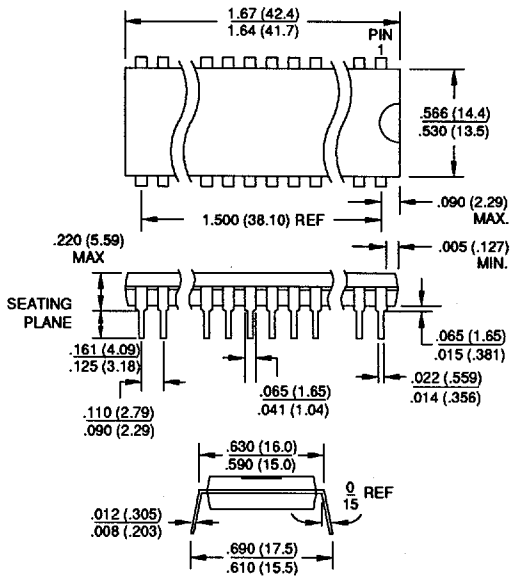


Packaging Information

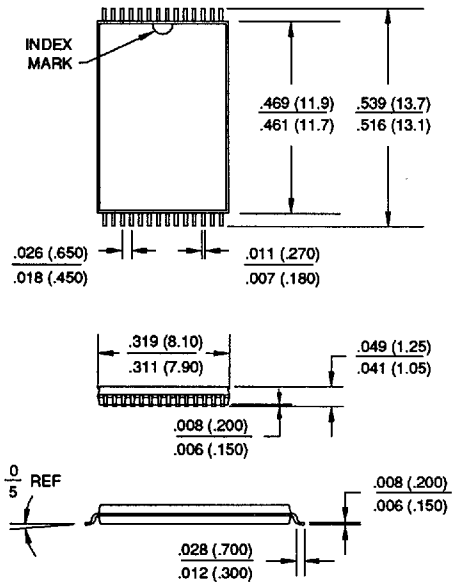
28P6, 28 Lead, 0.600" Wide,
Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)



32P6, 32 Lead, 0.600" Wide,
Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)



28T, 28 Lead, Thin Small Outline Package (TSOP)
Dimensions in Inches and (Millimeters)



32T, 32 Lead, Thin Small Outline Package (TSOP)
Dimensions in Inches and (Millimeters)