CS8151

5.0 V, 100 mA Low Dropout Linear Regulator with Watchdog, $\overline{\text{RESET}}$, and Wake Up

The CS8151 is a precision 5.0 V, 100 mA micro−power voltage regulator with very low quiescent current (400 μA typical at 200 μA load). The 5.0 V output is accurate within ±2% and supplies 100 mA of load current with a typical dropout voltage of 400 mV. Microprocessor control logic includes Watchdog, Wake Up and $\overline{\text{RESET}}$. This unique combination of low quiescent current and full microprocessor control makes the CS8151 ideal for use in battery operated, microprocessor controlled equipment.

The CS8151 Wake Up function brings the microprocessor out of Sleep mode. The microprocessor in turn, signals its Wake Up status back to the CS8151 by issuing a Watchdog signal.

The Watchdog logic function monitors an input signal (WDI) from the microprocessor. The CS8151 responds to the falling edge of the Watchdog signal which it expects at least once during each wake−up period. When the correct Watchdog signal is received, a falling edge is issued on the wake−up signal line.

$\overline{\text{RESET}}$ is independent of V_{IN} and operates correctly to an output voltage as low as 1.0 V. A $\overline{\text{RESET}}$ signal is issued in any of three situations. During power up the $\overline{\text{RESET}}$ is held low until the output voltage is in regulation. During operation if the output voltage shifts below the regulation limits, the $\overline{\text{RESET}}$ toggles low and remains low until proper output voltage regulation is restored. And finally, a $\overline{\text{RESET}}$ signal is issued if the regulator does not receive a Watchdog signal within the Wake Up period.

The $\overline{\text{RESET}}$ pulse width, Wake Up signal frequency, and Wake Up delay time are all set by one external capacitor C_{Delay}.

The regulator is protected against short circuit, over voltage, and thermal runaway conditions. The device can withstand 74 V peak transients, making it suitable for use in automotive environments.

Features

- 5.0 V ± 2%/100 mA Output Voltage
- Micropower Compatible Control Functions
  - Wake Up
  - Watchdog
  - $\overline{\text{RESET}}$
- Low Dropout Voltage: 400 mV @ 100 mA
- Low Sleep Mode Quiescent Current (400 μA Typ)
- Protection Features
  - Thermal Shutdown
  - Short Circuit
  - 74 V Peak Transient Capability
  - Reverse Transient (−50 V)
- Internally Fused Leads in PDIP−16 and SO−16L Packages
- Pb−Free Packages are Available

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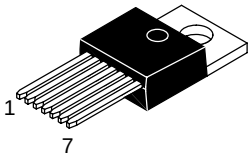
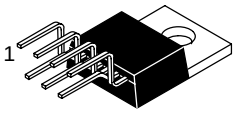
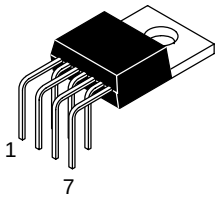


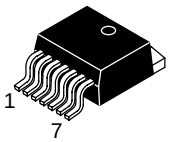
TO−220−7
T SUFFIX
CASE 821E



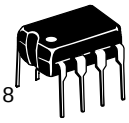
TO−220−7
TVA SUFFIX
CASE 821J



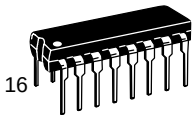
TO−220−7
THA SUFFIX
CASE 821H



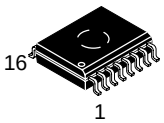
D²PAK−7
DPS SUFFIX
CASE 936AB



PDIP−8
N SUFFIX
CASE 626



PDIP−16
NF SUFFIX
CASE 648



SO−16L
DWF SUFFIX
CASE 751G

DEVICE MARKING INFORMATION

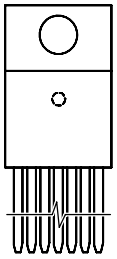
See general marking information in the device marking section on page 10 of this data sheet.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 11 of this data sheet.

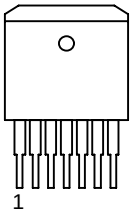
PIN CONNECTIONS

TO−220
SEVEN LEAD

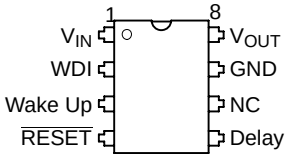


Tab = GND
Pin 1. V_{OUT}
2. V_{IN}
3. WDI
4. GND
5. Wake Up
6. $\overline{RESET}$
7. Delay

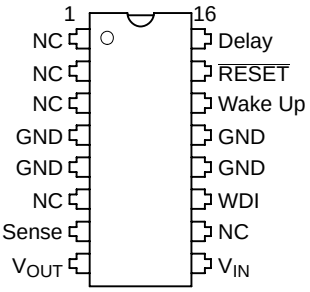
D^2PAK
7−PIN



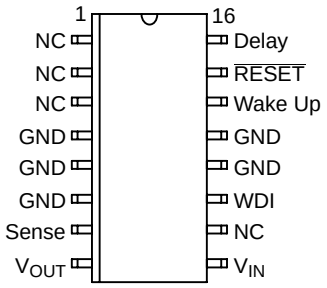
PDIP−8



PDIP−16



SO−16L



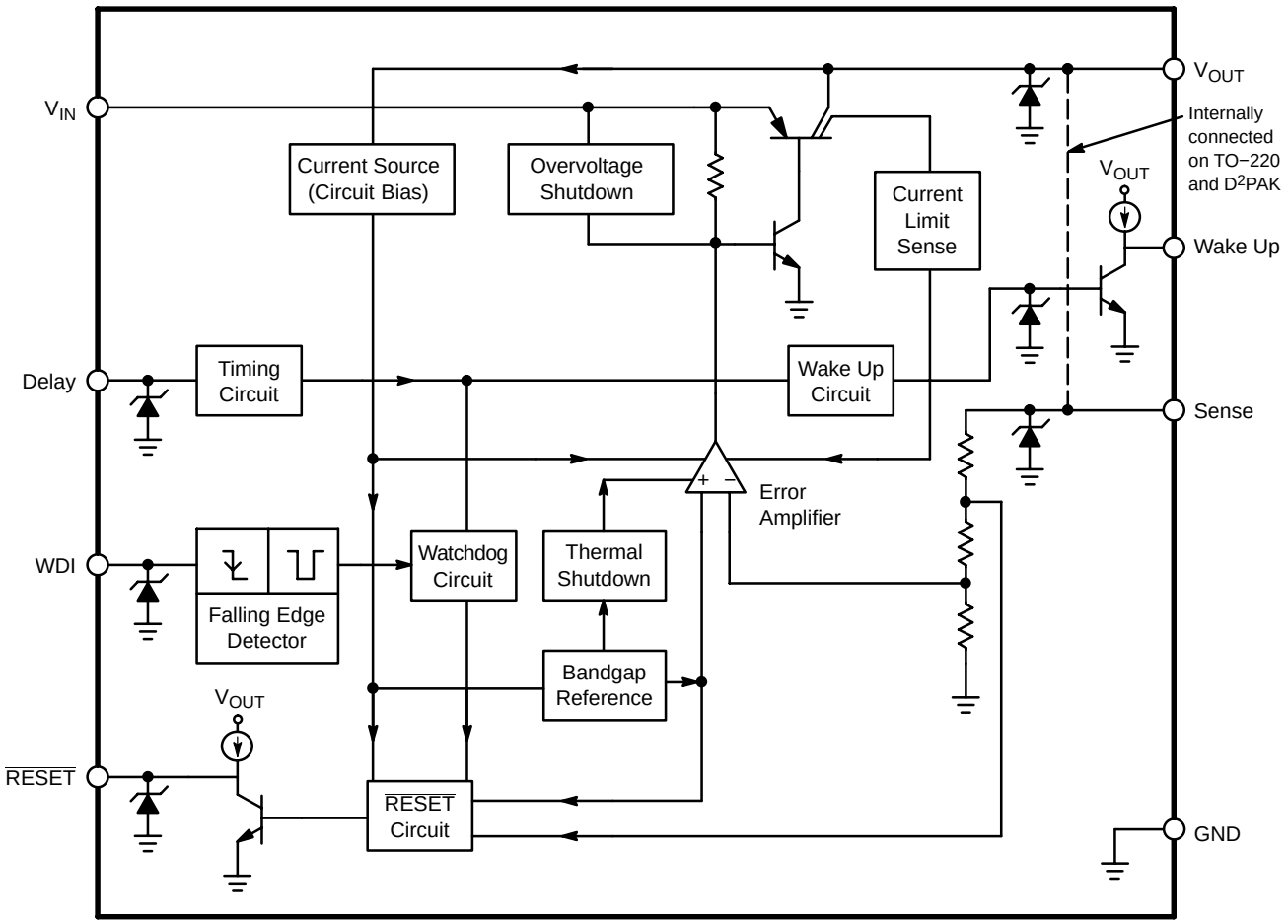


Figure 1. Block Diagram

MAXIMUM RATINGS*

Rating		Value	Unit
Power Dissipation		Internally Limited	−
Output Current (V_{OUT}, $\overline{RESET}$, Wake Up)		Internally Limited	−
Reverse Battery		−15	V
Peak Transient Voltage (60 V Load Dump @ V_{IN} = 14 V)		+74	V
Maximum Negative Transient (t < 2.0 ms)		−50	V
ESD Susceptibility (Human Body Model)		2.0	kV
ESD Susceptibility (Machine Model)		200	V
Logic Inputs/Outputs		−0.3 to +6.0	V
Storage Temperature Range		−55 to +150	°C
Lead Temperature Soldering	Wave Solder (through hole styles only) (Note 1) Reflow (SMD styles only) (Notes 2 & 3)	260 peak 240 peak	°C °C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. 10 seconds max
2. 60 seconds max above 183°C
3. −5°C / +0°C allowable conditions

*The maximum package power dissipation must be observed

ELECTRICAL CHARACTERISTICS (−40°C ≤ T_A ≤ 125°C, −40°C ≤ T_J ≤ 150°C, 6.0 V ≤ V_{IN} ≤ 26 V, 100 μA ≤ I_{OUT} ≤ 100 mA, C_2 = 47 μF (ESR < 8.0 Ω), C_{Delay} = 0.1 μF; unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Output Section					
Output Voltage, V_{OUT}	9.0 V < V_{IN} < 16 V 6.0 V < V_{IN} < 26 V, 0 < I_{OUT} < 100 mA	4.90 4.85	5.0 5.0	5.10 5.15	V V
Dropout Voltage (V_{IN} − V_{OUT})	I_{OUT} = 100 mA I_{OUT} = 100 μA	− −	400 100	600 150	mV mV
Load Regulation	V_{IN} = 14 V, 100 μA < I_{OUT} < 100 mA	−	10	50	mV
Line Regulation	I_{OUT} = 1.0 mA, 6.0 V < V_{IN} < 26 V	−	10	50	mV
Ripple Rejection	7.0 V < V_{IN} < 17 V @ f = 120 Hz, I_{OUT} = 100 mA	60	75	−	dB
Current Limit	V_{OUT} = 4.5 V	100	250	−	mA
Thermal Shutdown	−	150	180	210	°C
Overvoltage Shutdown	V_{OUT} < 1.0 V	50	56	62	V
Quiescent Current	I_{OUT} = 200 μA (Sleep) I_{OUT} = 50 mA I_{OUT} = 100 mA (Wake Up)	− − −	0.4 4.0 12	0.75 − 20	mA mA mA
Reverse Current	V_{OUT} = 5.0 V, V_{IN} = 0 V	−	1.0	1.5	mA
$\overline{RESET}$					
Threshold High (RTH)	RTH V_{OUT} Increasing	V_{OUT} − 0.3	−	V_{OUT} − 0.04	V
Threshold Low (RTL)	RTL V_{OUT} Decreasing	4.5	4.7	4.91	V
Hysteresis	RTH − RTL	150	200	250	mV
Output Low	1.0 V < V_{OUT} RTL, I_{OUT} = 25 μA	−	0.2	0.8	V
Output High	I_{OUT} = 25 μA, V_{OUT} > RTH	3.8	4.2	5.1	V
Current Limit	$\overline{RESET}$ = 0 V, V_{OUT} > V_{RTH} (Sourcing) $\overline{RESET}$ = 5.0 V, V_{OUT} > 1.0 V (Sinking)	0.025 0.1	0.5 12	1.30 80	mA mA
Delay Time	POR Mode	3.0	5.0	7.0	ms

ELECTRICAL CHARACTERISTICS ($-40°C \le T_A \le 125°C$, $-40°C \le T_J \le 150°C$, $6.0\ V \le V_{IN} \le 26\ V$, $100\ \mu A \le I_{OUT} \le 100\ mA$, $C_2 = 47\ \mu F$ (ESR < 8.0 Ω), $C_{Delay} = 0.1\ \mu F$; unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Watchdog Input					
Threshold High	–	–	1.4	2.0	V
Threshold Low	–	0.8	1.3	–	V
Hysteresis	–	25	100	–	mV
Input Current	0 < WDI < 6.0 V	−10	0	+10	μA
Pulse Width	50% WDI Falling Edge to 50% WDI Rising Edge and 50% WDI Rising Edge to 50% WDI Falling Edge (see Figures 2, 3, and 4)	5.0	–	–	μs
Wake Up Output					
Wake Up Period	See Figure 2	30	40	50	ms
Wake Up Duty Cycle Nominal	See Figure 4	40	50	60	%
$\overline{\text{RESET}}$ High to Wake Up Rising Delay Time	50% $\overline{\text{RESET}}$ Rising Edge to 50% Wake Up Edge (see Figures 2, 3, and 4)	15	20	25	ms
Wake Up Response to Watchdog Input	50% WDI Falling Edge to 50% Wake Up Falling Edge	–	2.0	10	μs
Wake Up Response to $\overline{\text{RESET}}$	50% $\overline{\text{RESET}}$ Falling Edge to 50% Wake Up Falling Edge, $V_{OUT} = 5.0\ V \rightarrow 4.5\ V$	–	2.0	10	μs
Output Low	$I_{OUT} = 25\ \mu A$ (Sinking)	–	0.2	0.8	V
Output High	$I_{OUT} = 25\ \mu A$ (Sourcing)	3.8	4.2	5.1	V
Current Limit	Wake Up = 5.0 V Wake Up = 0 V	0.025 0.05	1.0 –	7.0 3.5	mA mA

PACKAGE PIN DESCRIPTION

PACKAGE PIN # TO−220 & D²PAK	PACKAGE PIN # DIP−16	PACKAGE PIN # SO−16L	PIN SYMBOL	FUNCTION
1	8	8	V_{OUT}	Regulated output voltage 5.0 V ± 2%.
2	9	9	V_{IN}	Supply voltage to the IC.
3	11	11	WDI	CMOS/TTL compatible input lead. The Watchdog function monitors the falling edge of the incoming signal.
4	4, 5, 12, 13	4, 5, 6, 12, 13*	GND	Ground connection.
5	14	14	Wake Up	CMOS/TTL compatible output consisting of a continuously generated signal used to Wake Up the microprocessor from sleep mode.
6	15	15	$\overline{\text{RESET}}$	CMOS/TTL compatible output lead $\overline{\text{RESET}}$ goes low whenever V_{OUT} drops by more than 6.0% from nominal, or during the absence of a correct watchdog signal.
7	16	16	Delay	Input lead from timing capacitor for $\overline{\text{RESET}}$ and Wake Up signal.
−	7	7	Sense	Kelvin connection which allows remote sensing of the output voltage for improved regulation. If remote sensing is not required, connect to V_{OUT}.

*Pin 6 GND is not directly shorted to the fused paddle GND. The fused paddle GND (pins 4, 5, 12, 13) is connected through the substrate. Pin 6 must be electrically connected to at least one of the fused paddle GND's on the PC board.

PACKAGE PIN DESCRIPTION

PACKAGE PIN # PDIP−8	PIN SYMBOL	FUNCTION
1	V_{IN}	Supply voltage to the IC.
2	WDI	CMOS/TTL compatible input lead. The Watchdog function monitors the falling edge of the incoming signal.
3	Wake Up	CMOS/TTL compatible output consisting of a continuously generated signal used to Wake Up the microprocessor from sleep mode.
4	$\overline{\text{RESET}}$	CMOS/TTL compatible output lead $\overline{\text{RESET}}$ goes low whenever V_{OUT} drops by more than 6.0% from nominal, or during the absence of a correct watchdog signal.
5	Delay	Input lead from timing capacitor for $\overline{\text{RESET}}$ and Wake Up signal.
6	NC	No connection.
7	GND	Ground connection.
8	V_{OUT}	Regulated output voltage 5.0 V ± 2%.

TIMING DIAGRAMS

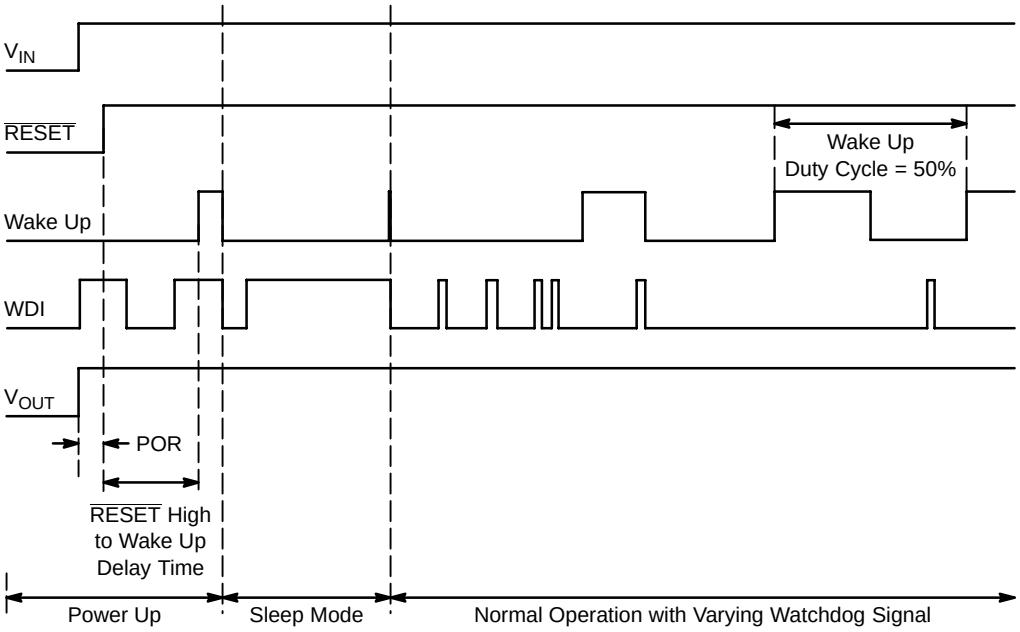


Figure 2. Power Up, Sleep Mode and Normal Operation

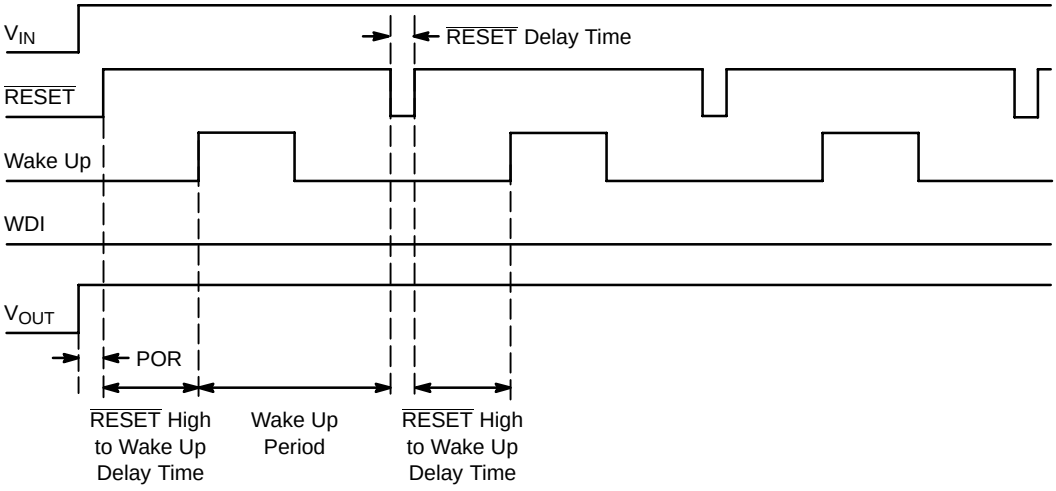


Figure 3. Error Condition: Watchdog Remains Low and a $\overline{\text{RESET}}$ Is Issued

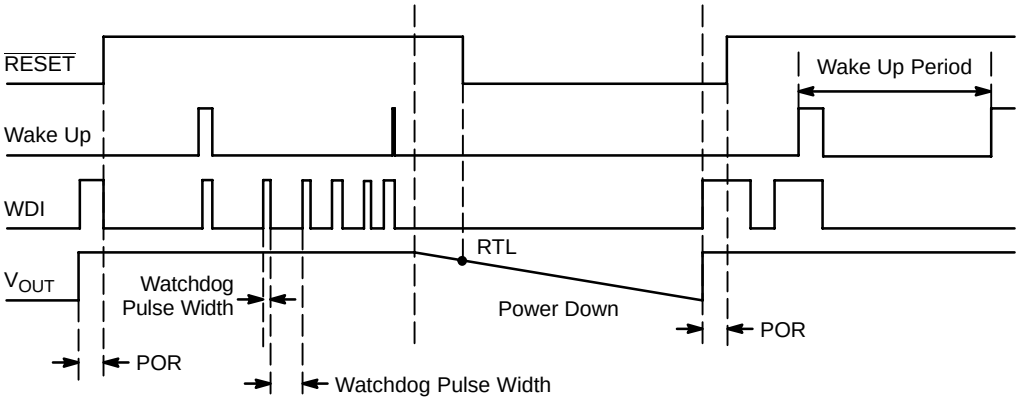


Figure 4. Power Down and Restart Sequence

DEFINITION OF TERMS

Dropout Voltage: The input−output voltage differential at which the circuit ceases to regulate against further reduction in input voltage. Measured when the output voltage has dropped 100mV from the nominal value obtained at 14V input, dropout voltage is dependent upon load current and junction temperature.

Input Voltage: The DC voltage applied to the input terminals with respect to ground.

Line Regulation: The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation: The change in output voltage for a change in load current at constant chip temperature.

Quiescent Current: The part of the positive input current that does not contribute to the positive load current. The regulator ground lead current.

Ripple Rejection: The ratio of the peak−to−peak input ripple voltage to the peak−to−peak output ripple voltage.

Current Limit: Peak current that can be delivered to the output.

CIRCUIT DESCRIPTION

Functional Description

To reduce the drain on the battery a system can go into a low current consumption mode when ever its not performing a main routine. The Wake Up signal is generated continuously and is used to interrupt a microcontroller that is in sleep mode. The nominal output is a 5.0 V square wave with a duty cycle of 50% at a frequency that is determined by a timing capacitor, C_{Delay}.

When the microprocessor receives a rising edge from the Wake Up output, it must issue a watchdog pulse and check its inputs to decide if it should resume normal operations or remain in the sleep mode.

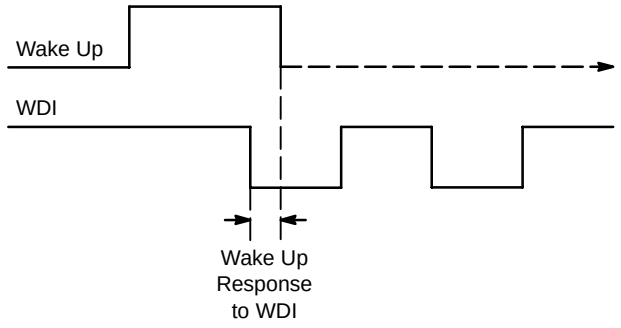


Figure 5. Wake Up Response to WDI

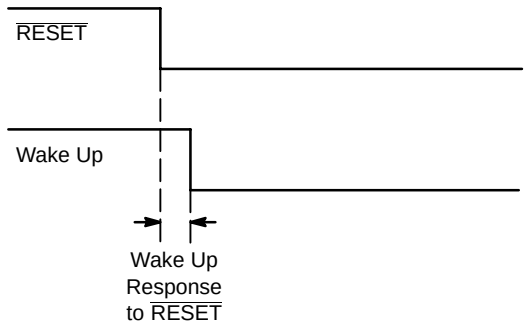


Figure 6. Wake Up Response to $\overline{\text{RESET}}$ (Low Voltage)

The first falling edge of the watchdog signal causes the Wake Up to go low within 2.0 μs (Typ) and remain low until the next Wake Up cycle (see Figure 5). Other watchdog pulses received within the same cycle are ignored (Figures 2, 3, and 4).

During power up, $\overline{\text{RESET}}$ is held low until the output voltage is in regulation. During operation, if the output voltage shifts below the regulation limits, the $\overline{\text{RESET}}$ toggles low and remains low until proper output voltage regulation is restored. After the $\overline{\text{RESET}}$ delay, $\overline{\text{RESET}}$ returns high.

The Watchdog circuitry continuously monitors the input watchdog signal (WDI) from the microprocessor. The absence of a falling edge on the Watchdog input during one Wake Up cycle will cause a $\overline{\text{RESET}}$ pulse to occur at the end of the Wake Up cycle (see Figure 3).

The Wake Up output is pulled low during a $\overline{\text{RESET}}$ regardless of the cause of the $\overline{\text{RESET}}$. After the $\overline{\text{RESET}}$ returns high, the Wake Up cycle begins again (see Figure 3).

The $\overline{\text{RESET}}$ pulse width, Wake Up signal frequency and $\overline{\text{RESET}}$ high to Wake Up delay time are all set by one external capacitor C_{Delay}.

Wake Up Period = $(4 \times 10^5)C_{Delay}$

$\overline{\text{RESET}}$ Delay Time = $(5 \times 10^4)C_{Delay}$

$\overline{\text{RESET}}$ High to Wake Up Delay Time = $(2 \times 10^5)C_{Delay}$

Capacitor temperature coefficient and tolerance as well as the tolerance of the CS8151 must be taken into account in order to get the correct system tolerance for each parameter.

APPLICATION NOTES

Output Stage Protection

The output stage is protected against overvoltage, short circuit and thermal runaway conditions (see Figure 7).

If the input voltage rises above the overvoltage shutdown threshold (e.g. load dump), the output shuts down. This response protects the internal circuitry and enables the IC to survive unexpected voltage transients.

Should the junction temperature of the power device exceed 180°C (Typ) the power transistor is turned off. Thermal shutdown is an effective means to prevent die overheating since the power transistor is the principle heat source in the IC.

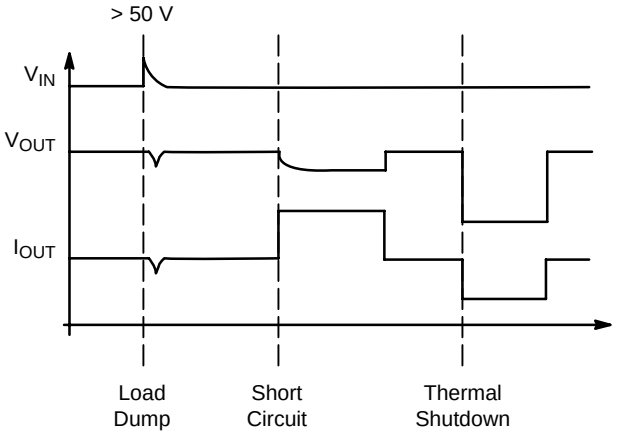
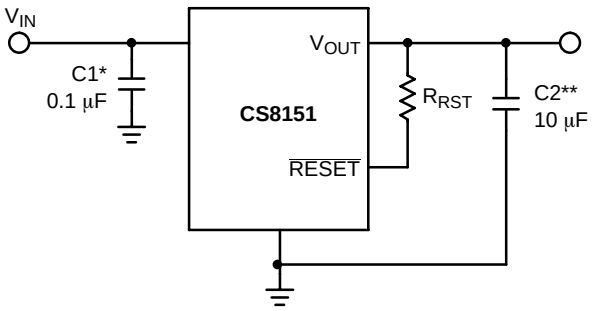


Figure 7. Typical Circuit Waveforms for Output Stage Protection

Stability Considerations

The output or compensation capacitor C2 (see Figure 8) helps determine three main characteristics of a linear regulator: startup delay, load transient response and loop stability.



*C1 required if regulator is located far from the power supply filter.
**C2 required for stability.

Figure 8. Test and Application Circuit Showing Output Compensation

The capacitor value and type should be based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR can cause instability. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures (−25°C to −40°C), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturers data sheet usually provide this information.

The value for the output capacitor C2 shown in the test and applications circuit should work for most applications, however it is not necessarily the optimized solution.

To determine an acceptable value for C2 for a particular application, start with a tantalum capacitor of the recommended value and work towards a less expensive alternative part.

Step 1: Place the completed circuit with a tantalum capacitor of the recommended value in an environmental chamber at the lowest specified operating temperature and monitor the outputs with an oscilloscope. A decade box connected in series with the capacitor will simulate the higher ESR of an aluminum capacitor. Leave the decade box outside the chamber, the small resistance added by the longer leads is negligible.

Step 2: With the input voltage at its maximum value, increase the load current slowly from zero to full load while observing the output for any oscillations. If no oscillations are observed, the capacitor is large enough to ensure a stable design under steady state conditions.

Step 3: Increase the ESR of the capacitor from zero using the decade box and vary the load current until oscillations appear. Record the values of load current and ESR that cause the greatest oscillation. This represents the worst case load conditions for the regulator at low temperature.

Step 4: Maintain the worst case load conditions set in step 3 and vary the input voltage until the oscillations increase. This point represents the worst case input voltage conditions.

Step 5: If the capacitor is adequate, repeat steps 3 and 4 with the next smaller valued capacitor. A smaller capacitor will usually cost less and occupy less board space. If the output oscillates within the range of expected operating conditions, repeat steps 3 and 4 with the next larger standard capacitor value.

Step 6: Test the load transient response by switching in various loads at several frequencies to simulate its real working environment. Vary the ESR to reduce ringing.

Step 7: Raise the temperature to the highest specified operating temperature. Vary the load current as instructed in step 5 to test for any oscillations.

Once the minimum capacitor value with the maximum ESR is found, a safety factor should be added to allow for the tolerance of the capacitor and any variations in regulator performance. Most good quality aluminum electrolytic capacitors have a tolerance of ±20% so the minimum value found should be increased by at least 50% to allow for this tolerance plus the variation which will occur at low

temperatures. The ESR of the capacitor should be less than 50% of the maximum allowable ESR found in step 3 above.

Calculating Power Dissipation In a Single Output Linear Regulator

The maximum power dissipation for a single output regulator (Figure 9) is:

$$P_{D(max)} = (V_{IN(max)} - V_{OUT(min)})I_{OUT(max)} + V_{IN(max)}I_Q \quad (1)$$

where:

$V_{IN(max)}$ is the maximum input voltage,

$V_{OUT(min)}$ is the minimum output voltage,

$I_{OUT(max)}$ is the maximum output current for the application, and

I_Q is the quiescent current the regulator consumes at $I_{OUT(max)}$.

Once the value of $P_{D(max)}$ is known, the maximum permissible value of $R_{\theta JA}$ can be calculated:

$$R_{\theta JA} = \frac{150^\circ C - T_A}{P_D} \quad (2)$$

The value of $R_{\theta JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{\theta JA}$'s less than the calculated value in equation 2 will keep the die temperature below 150°C.

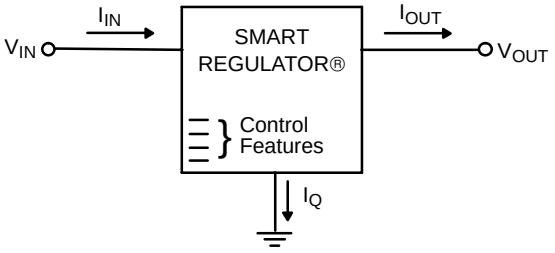


Figure 9. Single Output Regulator with Key Performance Parameters Labeled

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Heat Sinks

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\theta JA}$:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \quad (3)$$

where:

$R_{\theta JC}$ = the junction−to−case thermal resistance,

$R_{\theta CS}$ = the case−to−heatsink thermal resistance, and

$R_{\theta SA}$ = the heatsink−to−ambient thermal resistance.

$R_{\theta JC}$ appears in the package section of the data sheet. Like $R_{\theta JA}$, it too is a function of package type. $R_{\theta CS}$ and $R_{\theta SA}$ are functions of the package type, heatsink and the interface between them. These values appear in heatsink data sheets of heatsink manufacturers.

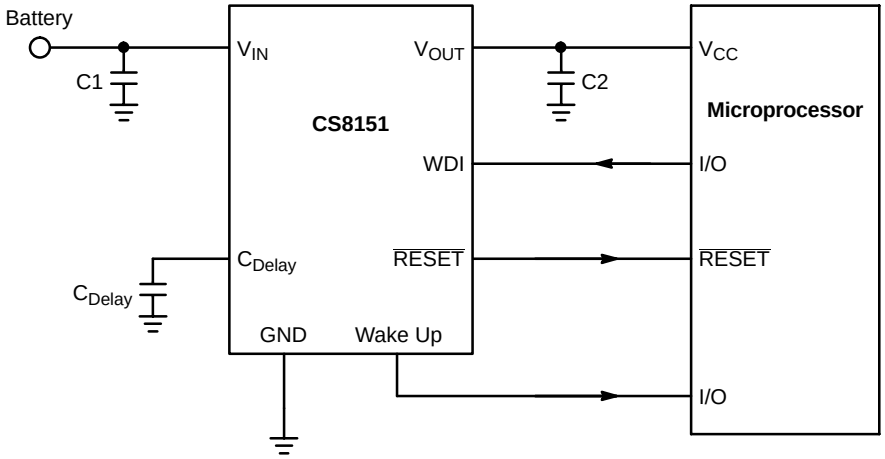


Figure 10. Application Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

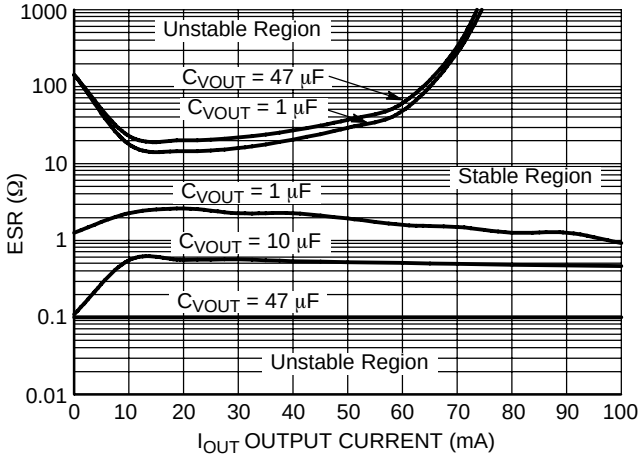


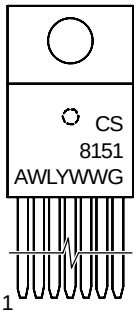
Figure 11. CS8151 Output Stability with Output Capacitor Change

MARKING DIAGRAMS

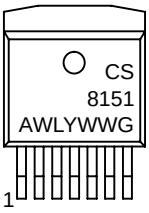
TO−220 SEVEN LEAD T SUFFIX CASE 821E

TO−220 SEVEN LEAD TVA SUFFIX CASE 821J

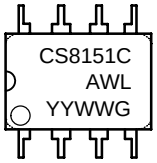
TO−220 SEVEN LEAD THA SUFFIX CASE 821H



D^2PAK 7−PIN DPS SUFFIX CASE 936AB

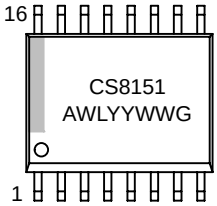


PDIP−8 N SUFFIX CASE 626



PDIP−16 NF SUFFIX CASE 648

SO−16L DWF SUFFIX CASE 751G



A	= Assembly Location
WL	= Wafer Lot
Y, YY	= Year
WW	= Work Week
G	= Pb−Free Package

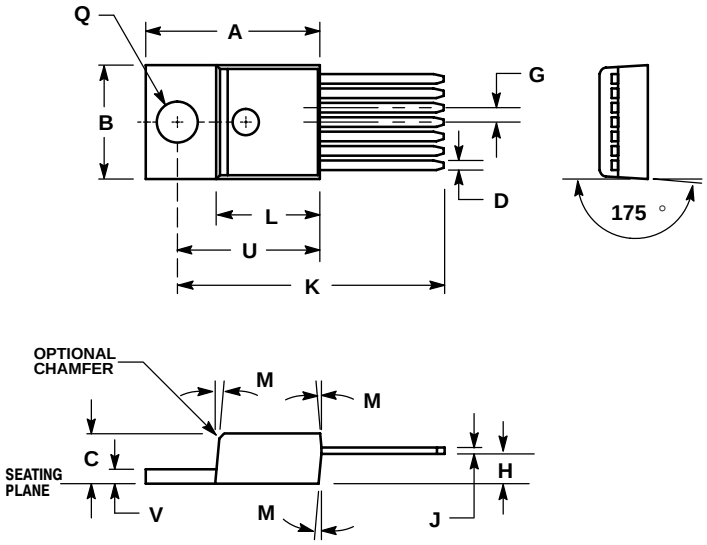
ORDERING INFORMATION

Device	Package	Shipping†
CS8151YT7	TO−220−7	50 Units / Rail
CS8151YT7G	TO−220−7 (Pb−Free)	50 Units / Rail
CS8151YTVA7	TO−220−7	50 Units / Rail
CS8151YTVA7G	TO−220−7 (Pb−Free)	50 Units / Rail
CS8151YTHA7	TO−220−7	50 Units / Rail
CS8151YTHA7G	TO−220−7 (Pb−Free)	50 Units / Rail
CS8151YDPS7	D^2PAK−7	50 Units / Rail
CS8151YDPS7G	D^2PAK−7 (Pb−Free)	50 Units / Rail
CS8151YDPSR7	D^2PAK−7	750 Units / Tape & Reel
CS8151YDPSR7G	D^2PAK−7 (Pb−Free)	750 Units / Tape & Reel
CS8151CGN8	PDIP−8	50 Units / Rail
CS8151CGN8G	PDIP−8 (Pb−Free)	50 Units / Rail
CS8151YNF16	PDIP−16	25 Units / Rail
CS8151YNF16G	PDIP−16 (Pb−Free)	25 Units / Rail
CS8151YDWF16	SO−16L	47 Units / Rail
CS8151YDWF16G	SO−16L (Pb−Free)	47 Units / Rail
CS8151YDWFR16	SO−16L	1000 Units / Tape & Reel
CS8151YDWFR16G	SO−16L (Pb−Free)	1000 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

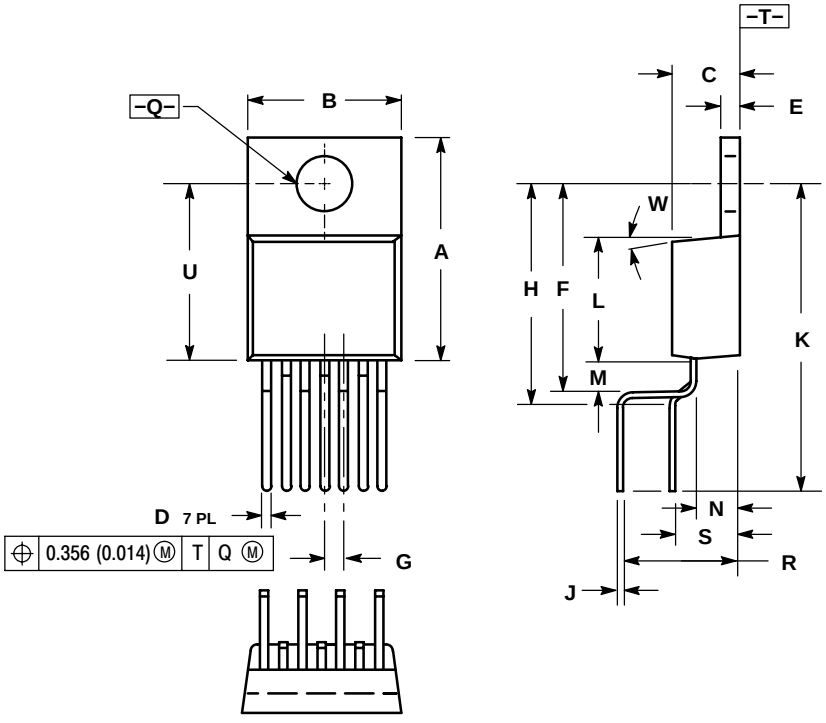
TO−220−7
T SUFFIX
CASE 821E−04
ISSUE D



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.003 (0.076) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
4. 821E−01 THRU 821−03 OBSOLETE, NEW STANDARD 821E−04.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.600	0.610	15.24	15.49
B	0.386	0.403	9.80	10.23
C	0.170	0.180	4.32	4.56
D	0.028	0.037	0.71	0.94
G	0.045	0.055	1.15	1.39
H	0.088	0.102	2.24	2.59
J	0.018	0.026	0.46	0.66
K	1.028	1.042	26.11	26.47
L	0.355	0.365	9.02	9.27
M	5 ° NOM		5 ° NOM	
Q	0.142	0.148	3.61	3.75
U	0.490	0.501	12.45	12.72
V	0.045	0.055	1.15	1.39

TO−220−7
TVA SUFFIX
CASE 821J−02
ISSUE A

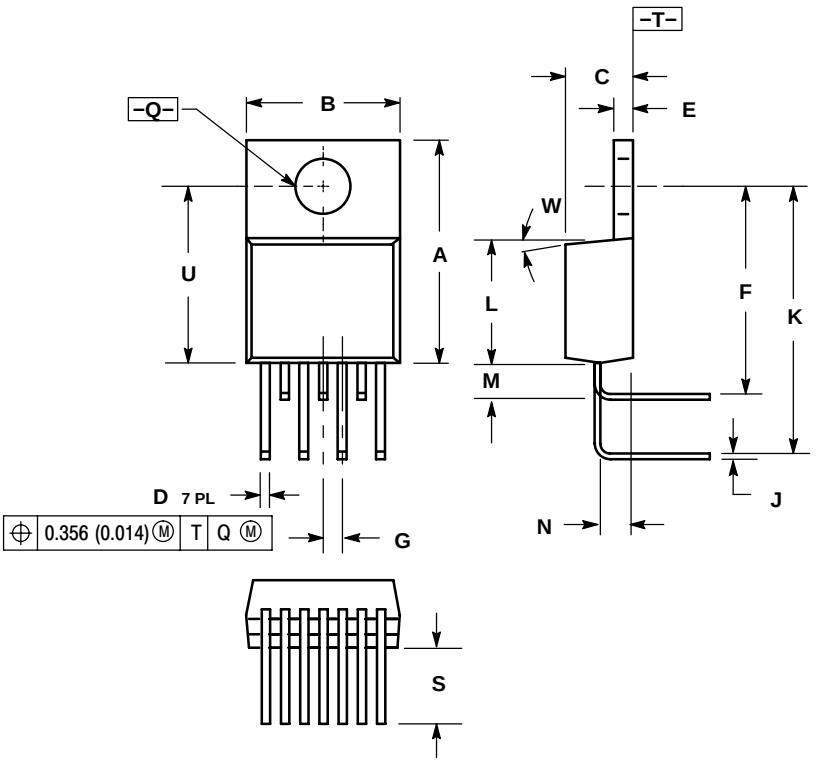


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION D DOES NOT INCLUDE INTERCONNECT BAR (DAMBAR) PROTRUSION. DIMENSION D INCLUDING PROTRUSION SHALL NOT EXCEED 10.92 (0.043) MAXIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.560	0.590	14.22	14.99
B	0.385	0.415	9.77	10.54
C	0.160	0.190	4.06	4.82
D	0.023	0.037	0.58	0.94
E	0.045	0.055	1.14	1.40
F	0.540	0.555	13.72	14.10
G	0.050 BSC		1.27 BSC	
H	0.570	0.595	14.48	15.11
J	0.014	0.022	0.36	0.56
K	0.785	0.800	19.94	20.32
L	0.322	0.337	8.18	8.56
M	0.073	0.088	1.85	2.24
N	0.090	0.115	2.28	2.91
Q	0.146	0.156	3.70	3.95
R	0.289	0.304	7.34	7.72
S	0.164	0.179	4.17	4.55
U	0.460	0.475	11.68	12.07
W	3 °		3 °	

PACKAGE DIMENSIONS

TO−220−7
THA SUFFIX
CASE 821H−02
ISSUE A



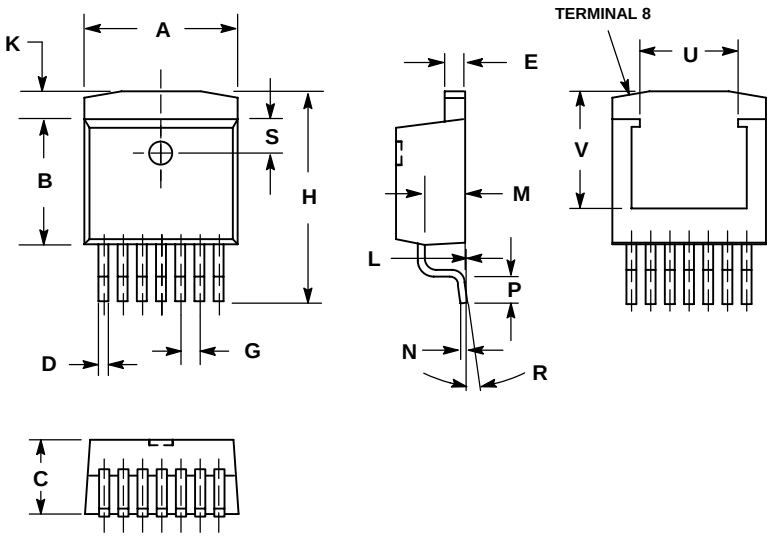
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION D DOES NOT INCLUDE INTERCONNECT BAR (DAMBAR) PROTRUSION. DIMENSION D INCLUDING PROTRUSION SHALL NOT EXCEED 10.92 (0.043) MAXIMUM.

1. LEADS MAINTAIN A RIGHT ANGLE WITH RESPECT TO THE PACKAGE BODY TO WITH ±0.020".

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.560	0.590	14.22	14.99
B	0.385	0.415	9.77	10.54
C	0.160	0.190	4.06	4.82
D	0.023	0.037	0.58	0.94
E	0.045	0.055	1.14	1.40
F	0.568	0.583	14.43	14.81
G	0.050 BSC		1.27 BSC	
J	0.015	0.022	0.38	0.56
K	0.728	0.743	18.49	18.87
L	0.322	0.337	8.18	8.56
M	0.101	0.116	2.57	2.95
N	0.090	0.115	2.28	2.91
Q	0.146	0.156	3.70	3.95
S	0.150	0.200	3.81	5.08
U	0.460	0.475	11.68	12.07
W	3 °		3 °	

PACKAGE DIMENSIONS

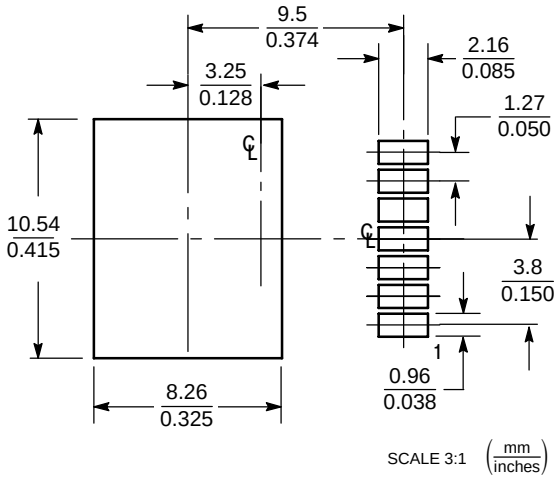
D²PAK−7 (SHORT LEAD)
DPS SUFFIX
CASE 936AB−01
ISSUE A



NOTES:
1. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.396	0.406	10.05	10.31
B	0.326	0.336	8.28	8.53
C	0.170	0.180	4.31	4.57
D	0.026	0.036	0.66	0.91
E	0.045	0.055	1.14	1.40
G	0.050 REF		1.27 REF	
H	0.539	0.579	13.69	14.71
K	0.055	0.066	1.40	1.68
L	0.000	0.010	0.00	0.25
M	0.100	0.110	2.54	2.79
N	0.017	0.023	0.43	0.58
P	0.058	0.078	1.47	1.98
R	0 °	8 °	0 °	8 °
S	0.095	0.105	2.41	2.67
U	0.256 REF		6.50 REF	
V	0.305 REF		7.75 REF	

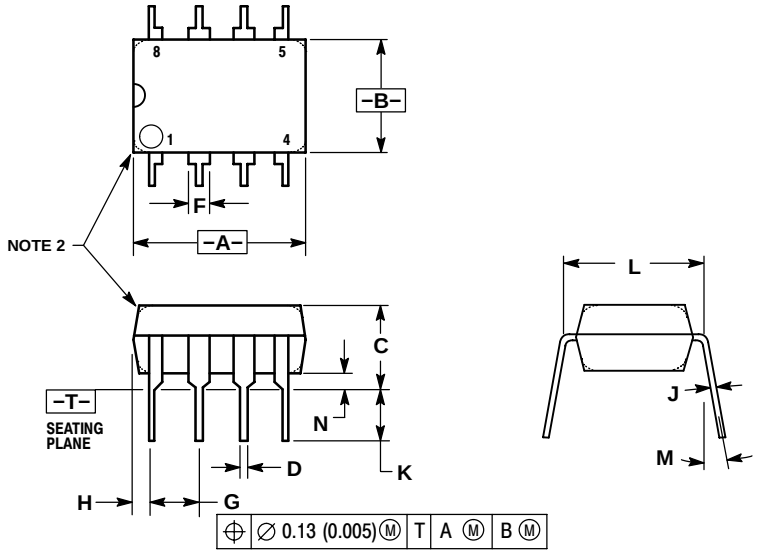
SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

PDIP−8
N SUFFIX
CASE 626−05
ISSUE L



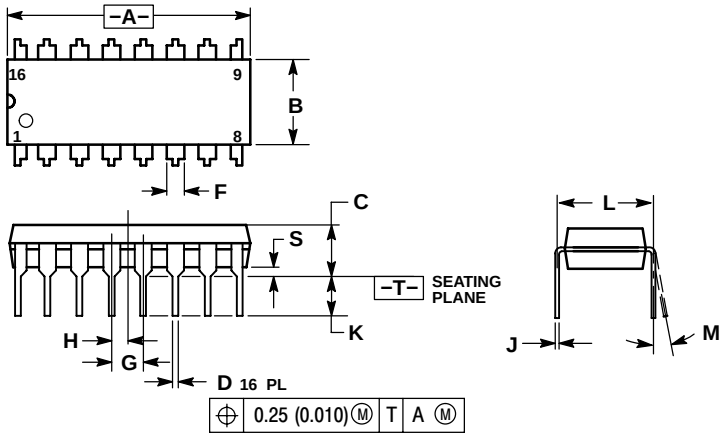
NOTES:
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	---	10°	---	10°
N	0.76	1.01	0.030	0.040

PACKAGE THERMAL DATA

Parameter		DIP−8	Unit
$R_{\Theta JC}$	Typical	52	°C/W
$R_{\Theta JA}$	Typical	100	°C/W

PDIP−16
NF SUFFIX
CASE 648−08
ISSUE T

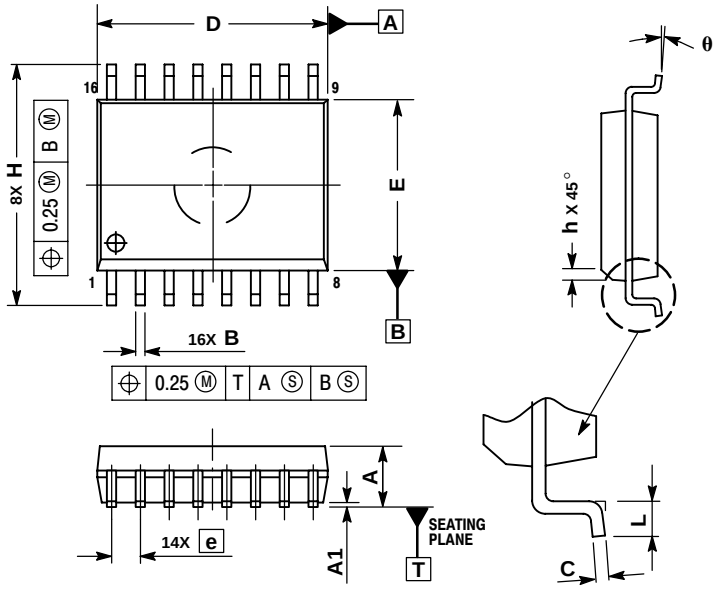


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

PACKAGE DIMENSIONS

SO−16L
DWF SUFFIX
CASE 751G−03
ISSUE C



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INLCUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

PACKAGE THERMAL DATA

Parameter		TO−220−7	D²PAK−7	DIP−16	SO−16L	Unit
$R_{\theta JC}$	Typical	1.8	1.8	15	18	°C/W
$R_{\theta JA}$	Typical	50	10−50*	50	75	°C/W

*Depending on thermal properties of substrate. $R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$.

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