SONY CXK581100TM/YM -10LX/12LX/15LX -10LLX/12LLX/15LLX

131072-word × 8-bit High Speed CMOS Static RAM

Description

CXK581100TM/YM is a 1M bits, 131,072 words by 8 bits, CMOS static RAM. It is suitable for portable and battery back-up systems by adopting TSOP packages correspond to extending operating temperature range and low power consumption.

Features

- Extended operating temperature range (–25 to +85 °C)
- Thin small-outline packages of EIAJ standard:
  CXK581100TM:
  8mm × 20mm 32 pin TSOP
  CXK581100YM:
  8mm × 20mm 32 pin TSOP (Mirror image pinout)
- Low stand-by current:
  LX-Version:
  200 µA (Max.) @Vcc=5.5V, Ta=–25 to +85 °C
  LLX-Version:
  40 µA (Max.) @Vcc=5.5V, Ta=–25 to +85 °C
- Low voltage data retention: 2.2V (Min.)
- Fast access time: (Access time)
  CXK581100TM/YM-10LX, -10LLX 100ns (Max.)
  CXK581100TM/YM-12LX, -12LLX 120ns (Max.)
  CXK581100TM/YM-15LX, -15LLX 150ns (Max.)
- Single +5V Supply: +5V ± 10%

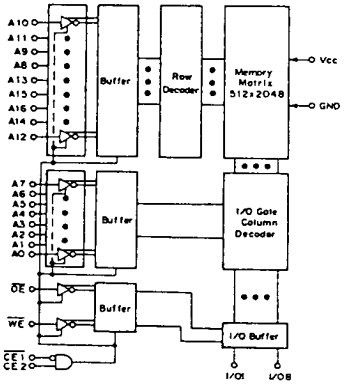
Function

131072-word × 8-bit static RAM

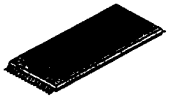
Structure

Silicon gate CMOS IC

Block Diagram



CXK581100TM
32 pin TSOP (Plastic)

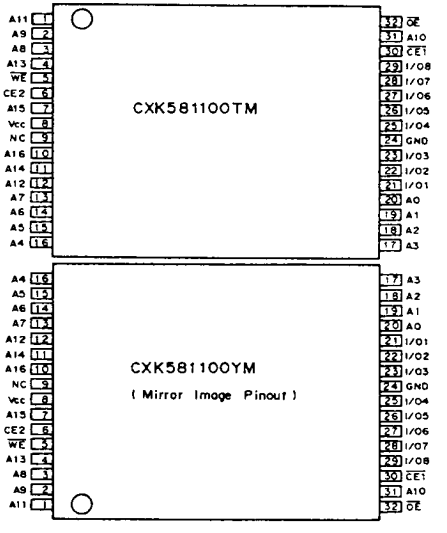


CXK581100YM
32 pin TSOP (Plastic)

Pin Description

Symbol	Description
A0 to A16	Address input
I/O1 to I/O8	Data input/output
$\overline{CE1}$, CE2	Chip enable 1, 2 input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
Vcc	+5V power supply
GND	Ground
NC	No connection

Pin Configuration (Top View)



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Absolute Maximum Ratings

(Ta=25°C, GND=0V)

Item	Symbol	Rating	Unit
Supply voltage	Vcc	−0.5 to +7.0	V
Input voltage	V_{IN}	−0.5 * to Vcc+0.5	V
Input and output voltage	$V_{I/O}$	−0.5 * to Vcc+0.5	V
Allowable power dissipation	P_D	0.7	W
Operating temperature	Topr	−25 to +85	°C
Storage temperature	Tstg	−55 to +150	°C
Soldering temperature • time	Tsolder	235 • 10	°C • sec

* V_{IN}, $V_{I/O}$=−3.0V Min. for pulse width less than 50ns.

Truth Table

$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	Mode	I/O1 to I/O8	Vcc Current
H	×	×	×	Not selected	High Z	I_{SB1}, I_{SB2}
×	L	×	×	Not selected	High Z	I_{SB1}, I_{SB2}
L	H	H	H	Output disable	High Z	I_{CC1}, I_{CC2}, I_{CC3}
L	H	L	H	Read	Data out	I_{CC1}, I_{CC2}, I_{CC3}
L	H	×	L	Write	Data in	I_{CC1}, I_{CC2}, I_{CC3}

× : "H" or "L"

DC Recommended Operating Conditions

(Ta=−25 to +85°C, GND=0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.4	—	Vcc+0.3	V
Input low voltage	V_{IL}	−0.3 *	—	0.6	V

* V_{IL}=−3.0V Min. for pulse width less than 50ns.

5

Electrical Characteristics

• DC and operating characteristics

(Vcc=5V ± 10%, GND=0V, Ta=–25 to +85 °C)

Item	Symbol	Test conditions		–10LX/12LX/15LX			–10LLX/12LLX/15LLX			Unit
				Min.	Typ. *	Max.	Min.	Typ. *	Max.	
Input leakage current	I_{LI}	V_{IN}=GND to Vcc		–1	—	1	–1	—	1	µA
Output leakage current	I_{LO}	$\overline{CE1}$=V_{IH} or CE2=V_{IL} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, $V_{I/O}$=GND to Vcc		–1	—	1	–1	—	1	µA
Operating power supply current	I_{CC1}	$\overline{CE1}$=V_{IL}, CE2=V_{IH}, V_{IN}=V_{IH} or V_{IL}, I_{OUT}=0mA		—	7	15	—	7	15	mA
Average operating current	I_{CC2}	Cycle=Min. Duty=100%, I_{OUT}=0mA	Write cycle	—	35	60	—	35	60	mA
			Read cycle	—	25	40	—	25	40	
	I_{CC3}	Cycle time 1 µs Duty=100%, I_{OUT}=0mA $\overline{CE1}$ ≦ 0.2V, CE2 ≧ Vcc–0.2V V_{IL} ≦ 0.2V, V_{IH} ≧ Vcc–0.2V	Write cycle	—	10	20	—	10	20	mA
			Read cycle	—	5	10	—	5	10	
Standby current	I_{SB1}	CE2 ≦ 0.2V or $\overline{CE1}$ ≧ Vcc–0.2V CE2 ≧ Vcc–0.2V	–25 to +85 °C	—	—	200	—	—	40	µA
			–25 to +70 °C	—	—	100	—	—	20	
			–25 to +40 °C	—	—	20	—	—	4	
			+25 °C	—	2	8	—	0.7	2	
	I_{SB2}	$\overline{CE1}$=V_{IH} or CE2=V_{IL}		—	0.6	3	—	0.6	3	mA
Output high voltage	V_{OH}	I_{OH}=–1.0mA		2.4	—	—	2.4	—	—	V
Output low voltage	V_{OL}	I_{OL}=2.1mA		—	—	0.4	—	—	0.4	V

* Vcc=5V, Ta=25 °C

I/O Capacitance

(Ta=25 °C, f=1MHz)

Item	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Input capacitance	C_{IN}	V_{IN}=0V	—	—	6	pF
I/O capacitance	$C_{I/O}$	$V_{I/O}$=0V	—	—	8	pF

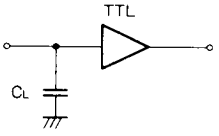
Note) This parameter is sampled and is not 100% tested.

AC Characteristics

• AC test conditions

(Vcc=5V ± 10%, Ta=–25 to +85 °C)

Item	Conditions
Input pulse high level	V_{IH}=2.4V
Input pulse low level	V_{IL}=0.6V
Input rise time	tr=5ns
Input fall time	tf=5ns
Input and output reference level	1.5V
Output load conditions	C_L * =100pF, 1TTL



* C_L includes scope and jig capacitances

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• Read cycle ($\overline{WE}$="H")

Item	Symbol	-10LX/10LLX		-12LX/12LLX		-15LX/15LLX		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	100	—	120	—	150	—	ns
Address access time	t_{AA}	—	100	—	120	—	150	ns
Chip enable access time ($\overline{CE1}$)	t_{CO1}	—	100	—	120	—	150	ns
Chip enable access time (CE2)	t_{CO2}	—	100	—	120	—	150	ns
Output enable to output valid	t_{OE}	—	50	—	60	—	70	ns
Output hold from address change	t_{OH}	10	—	10	—	10	—	ns
Chip enable to output in low Z ($\overline{CE1}$, CE2)	t_{LZ1}, t_{LZ2}	10	—	10	—	10	—	ns
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}	5	—	5	—	5	—	ns
Chip disable to output in high Z ($\overline{CE1}$, CE2)	t_{HZ1}*, t_{HZ2}*	—	35	—	40	—	50	ns
Chip disable to output in high Z ($\overline{OE}$)	t_{OHZ}*	—	35	—	40	—	50	ns

* t_{HZ1}, t_{HZ2} and t_{OHZ} are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

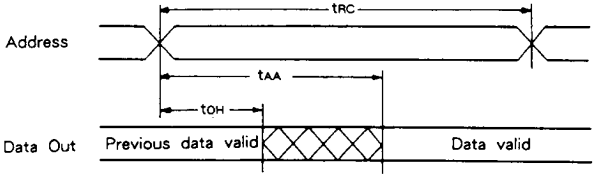
• Write cycle

Item	Symbol	-10LX/10LLX		-12LX/12LLX		-15LX/15LLX		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	100	—	120	—	150	—	ns
Address valid to end of write	t_{AW}	70	—	85	—	100	—	ns
Chip enable to end of write	t_{CW}	70	—	85	—	100	—	ns
Data to write time overlap	t_{DW}	40	—	50	—	60	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	70	—	80	—	90	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	ns
Write recovery time ($\overline{WE}$)	t_{WR}	5	—	5	—	5	—	ns
Write recovery time ($\overline{CE1}$, CE2)	t_{WR1}	0	—	0	—	0	—	ns
Output active from end of write	t_{OW}	10	—	10	—	10	—	ns
Write to output in high Z	t_{WHZ}*	—	30	—	30	—	30	ns

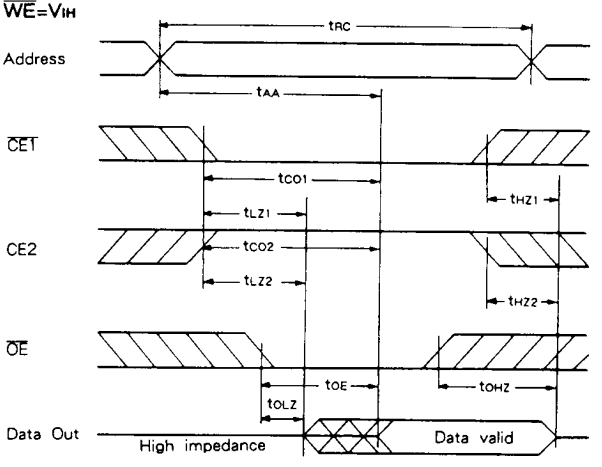
* t_{WHZ} is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

Timing Waveform

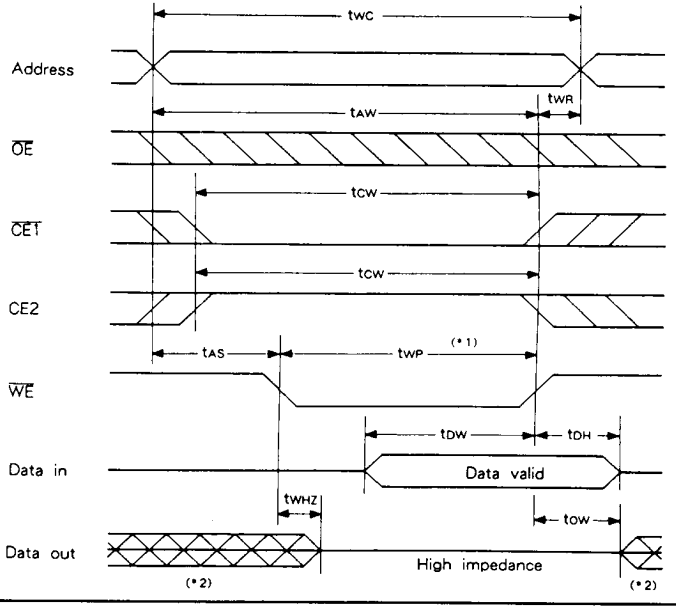
• Read cycle (1) : $\overline{CE1}$=$\overline{OE}$=V_{IL}, CE2=V_{IH}, $\overline{WE}$=V_{IH}



• Read cycle (2) : $\overline{WE}$=V_{IH}



• Write cycle (1) : $\overline{WE}$ control



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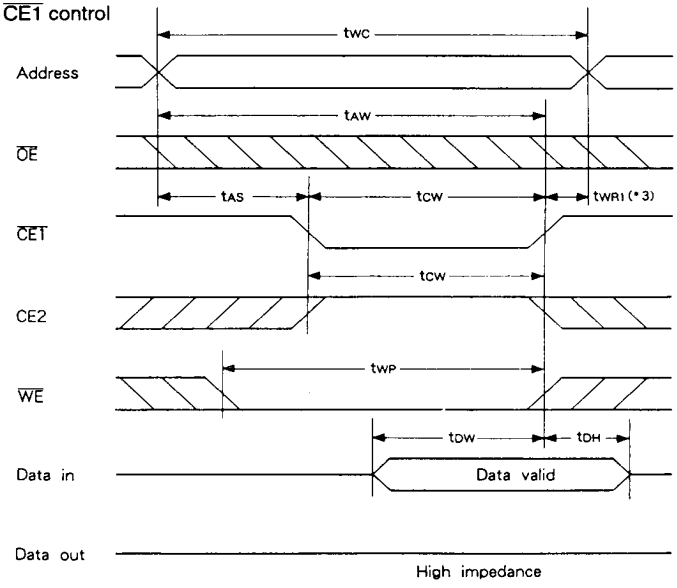
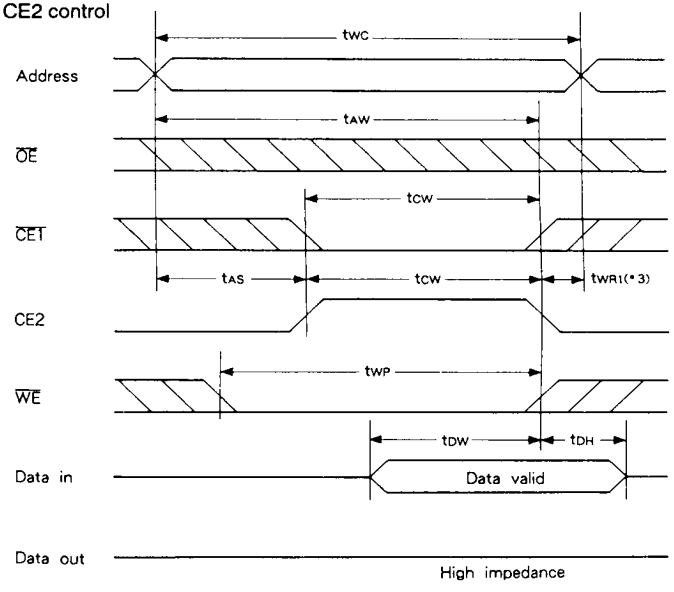
• Write cycle (2) : $\overline{CE1}$ control



• Write cycle (3) : CE2 control



*1. Write is executed when both $\overline{CE1}$ and $\overline{WE}$ are at low and CE2 is at high simultaneously.
*2. Do not apply the data input valtage of the opposite phase to the output while I/O pin is in output condition.
*3. t_{WR1} is tested from either the rising edge of $\overline{CE1}$ or the falling edge of CE2, whichever comes earlier, until the end of the write cycle.

Data Retention Characteristics

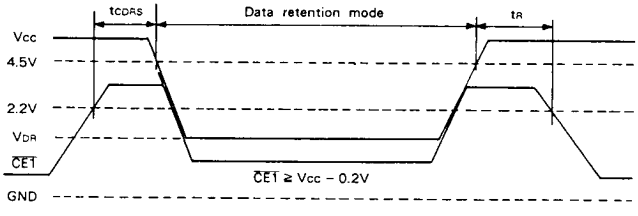
(Ta=−25 to +85 °C)

Item	Symbol	Test conditions		−10LX/12LX/15LX			−10LLX/12LLX/15LLX			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
Data retention voltage	V_{DR}	*1		2.2	—	5.5	2.2	—	5.5	V
Data retention current	I_{CCDR1}	Vcc=3.0V *1	−25 to +85 °C	—	—	100	—	—	24	µA
			−25 to +70 °C	—	—	50	—	—	12	
			−25 to +40 °C	—	—	10	—	—	2.4	
			+25 °C	—	1	4	—	0.4	1.2	
	I_{CCDR2}	Vcc=2.2 to 5.5V *1		—	2*3	200	—	0.7*3	40	µA
Data retention setup time	t_{CDRS}	Chip disable to data retention mode		0	—	—	0	—	—	ns
Recovery time	t_R			t_{RC} *2	—	—	t_{RC} *2	—	—	ns

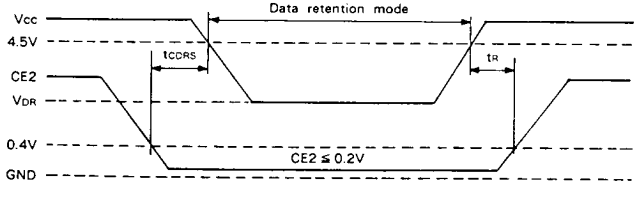
*1. $\overline{CE1} \geqq Vcc-0.2V$, $CE2 \geqq Vcc-0.2V$ ($\overline{CE1}$ control) or $CE2 \leqq 0.2V$ (CE2 control)
*2. t_{RC}: Read cycle time
*3. Vcc=5V, Ta=25 °C

Data Retention Waveform

- Low supply voltage data retention waveform (1) : $\overline{CE1}$ control



- Low supply voltage data retention waveform (2) : CE2 control



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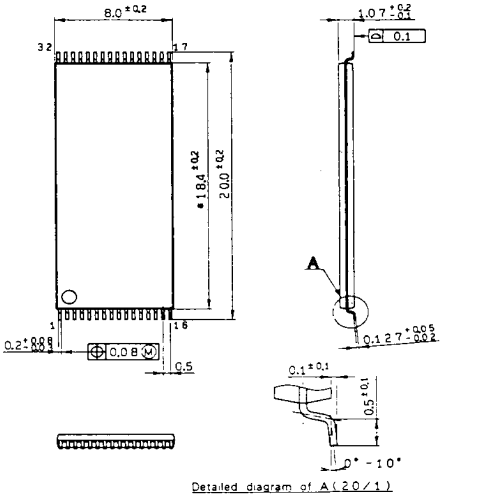
Package Outline Unit : mm

CXK581100TM

32pin TSOP (Plastic)



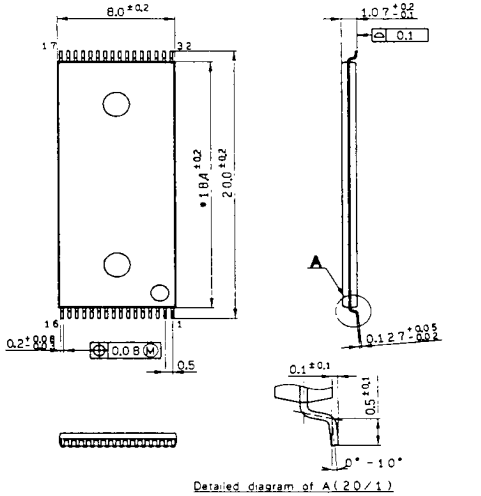
Detailed diagram of A (20/1)

Note) Dimensions marked with * does not include resin residue.

SONY NAME	TSOP-32P-L01
EIAJ NAME	TSOP032-P-0820-A
JEDEC CODE	

CXK581100YM

32pin TSOP (Plastic)



Detailed diagram of A (20/1)

Note) Dimensions marked with * does not include resin residue.

SONY NAME	TSOP-32P-L01R
EIAJ NAME	TSOP032-P-0820-B
JEDEC CODE	