Genesys Logic, Inc.

GL816 -
USB 2.0 Flash Card Reader Controller

Specification 1.2

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Contents

1. General Description

The GL816 is a highly integrated, flexible application USB 2.0 Multi-Interface Flash Card Reader controller. It supports USB 2.0 high-speed transmission to PCMCIA, CompactFlash ™ (CF), Micro Drive, SmartMedia™ (SM), Secure Digital ™ (SD), Multi Media Card ™ (MMC), and MemoryStick ™ (MS) interface on one chip. Besides the flash card interface controller each, the GL816 integrates Genesys Logic own design USB 2.0 high-speed UTMI (**U**SB 2.0 **T**ransceiver **M**acrocell **I**nterface) transceiver. As a single chip solution for USB 2.0 multi flash card reader, the GL816 complies with Universal Serial Bus specification rev. 2.0, USB Storage Class specification ver.1.0, and flash card interface specification each.

The GL816 can support different kinds of multi-interface combinations. For the best performance consideration, the GL816 integrates high efficiency card interface hardware engine for data transfer, and the 48MHz feature-enhanced 8051 micro-controller. The GL816 also supports firmware upgrade via USB interface, and external flash read/ write for firmware upgrade and other applications. With the advanced mobile consideration in the IA application, the GL816 can support **Inter-Media** transfer, it means that the data transfer between different cards doesn't need the support of USB host in PC system.

The GL816 equips dedicated power control pins for different cards and power / busy indication. And the pin assignment design fits to card sockets to provide easier PCB layout. With 8 additional GPIOs, and firmware controllable CD, CE pins, the GL816 can be programmed to fit your various design in USB 2.0 high speed multi-interface flash card reader applications.

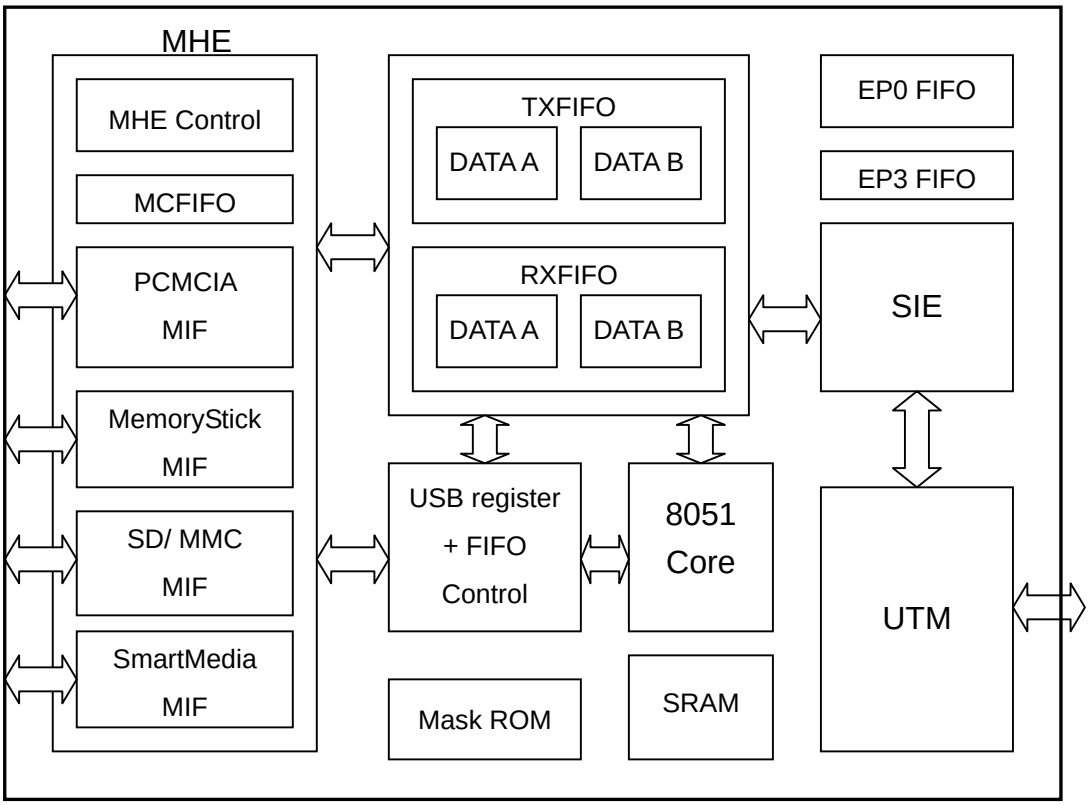
2. Features

- Supports PCMCIA, CompactFlash ™ (CF), SmartMedia ™ (SM), MemoryStick ™ (MS), Secure Digital ™ (SD) and Multi Media Card ™ (MMC) interface on one chip.
- Complies with 480Mbps Universal Serial Bus specification rev. 2.0.
- Complies with USB Storage Class specification rev. 1.0. (Bulk only protocol).
- Operating System supported: Win XP/ 2000/ Me/ 98/ 98SE; Mac OS 9.x/ X.
- Supports 1 device address and up to 10 endpoints: Control (0)/ Bulk Read (1)/ Bulk Write (2)/ Interrupt (3), and 3 optional Bulk Read/ Write endpoints pair.
- Integrated USB 2.0 Transceiver Macrocell Interface (UTMI) transceiver and Serial Interface Engine (SIE).
- Integrated 8051 micro-controller with enhanced feature:
  - Supports 48MHz clock rate.
  - 12 clocks per instruction cycle.
  - Embedded 24KB Mask ROM and 2KB+256B SRAM.
  - Supports external 64KB ROM/ Flash for design flexibility.
- Supports firmware upgrade via USB interface.
- Supports external flash read/ write for firmware upgrade and other applications.
- Supports serial EEPROM 93C86 interface for the flexibility of vendor or firmware parameters, EEPROM size up to 2KB.
- High efficiency card interface hardware engine for data transfer.
- Shared pins between PCMCIA and SmartMedia™ interface.
- PCMCIA interface:
  - Supports address up to 16 bits, with fix and incremental mode.
  - Supports 8 / 16 bit data mode and different timing.
  - Supports WAIT# detection.
  - Supports multi signal level (3.3 / 5V).
  - Other control signals like CD1#, CD2#, CE1#, CE2# … etc.
- SmartMedia™ interface:
  - Supports address up to 4 bytes, 8 bit data width and different speed.
  - Supports different page size, and automatic append redundant area data (8/16 bytes).
  - Hardware ECC generation and verification.
  - Supports firmware correct page ECC error capability.
  - Supports automatic page copy (source page read + destination page write).

- MemoryStick™ interface
  - Complies with MemoryStick interface specification.
  - Supports hardware BS/SDIO/SCLK signals.
  - Supports INS signal.
  - Supports automatic CRC16 generation and verification.
  - Supports hardware CMD timeout detection.
  - Supports different clock rate up to 24 MHz.
- Secure Digital™/ Multi Media Card™ interface
  - Complies with Secure Digital / MMC interface specification.
  - Supports both SD / MMC mode access: CLK/CMD/DAT0/DAT1/DAT2/DAT3.
  - Command transmit and response receive can be enabled separately.
  - Automatic CRC7 generation for command and CRC7 verification for response on CMD.
  - Supports automatic CRC16 generation and verification on DAT3-0.
  - In addition to full packet transaction, optional single byte/ bit operation on both CMD and DAT line/ lines.
  - Data processing in block or byte.
  - Supports different clock rate from 375 KHz to 24 MHz.
- Dedicated power control pins for different cards and power / busy indication.
- Build-in power-on reset (POR) and low-voltage detector (LVD).
- 3.3 Volt operation.
- Pin assignment fits to card sockets to provide easier PCB layout.
- Supports 8 additional GPIOs and firmware controllable CD, CE pins.
- Available in 128-pin LQFP package.

3. Function Block

3.1 Block Diagram



3.2 Functional Overview

3.2.1 UTM

The USB 2.0 Transceiver Macrocell, it's the analog circuitry that handles the low level USB protocol and signaling, and shifts the clock domain of the data from the USB 2.0 rate to one that is compatible with the general logic.

3.2.2 SIE

The Serial Interface Engine, which contains the USB PID and address recognition logic, and other sequencing and state machine logic to handle USB packets and transactions.

3.2.3 EP0 FIFO

It is composed of TX0FIFO and RX0FIFO, with 64-byte FIFO each, and it is used for endpoint 0 data transfer.

3.2.4 EP3 FIFO

It's an 8-byte FIFO for endpoint 3.

3.2.5 Bulk FIFO

It is composed of TXFIFO and RXFIFO for data transmission and receiving respectively, also with different modes support:

3.2.5.1 TXFIFO:

1. To ensure the continuous data transmission, TXFIFO includes 512 bytes DATA-A FIFO, 512 bytes DATA-B FIFO, and two 16 bytes corresponding redundant areas. All can be directly accessed by 8051 µC.
2. Normally SIE popes data, MHE pushes data for DATA A/B FIFOs, and redundant area is pushed by MHE when SmartMedia MIF is enabled and popped by uC.
3. Supports uC single byte access for SmartMedia ECC error correction.
4. At transmit mode SIE won't transmit data filled in TXFIFO before uC complete the data integrity checking.

3.2.5.2 RXFIFO:

1. To ensure the continuous data transmission, RXFIFO includes 512 bytes DATA-A FIFO, 512 bytes DATA-B FIFO, and 16 bytes single redundant area. All can be directly accessed by 8051 µC.

2. Normally MHE popes data, SIE pushes data for DATA A/B FIFOs, and redundant area is pushed by uC and popped by MHE when SmartMedia MIF is enabled.

3.2.5.3 Buffer Mode:

1. Buffer mode is enabled by firmware and is used to copy data block from source to destination in same card for SmartMedia or MemoryStick applications.
2. Under Buffer mode, firmware can enable MIF to read source data block to TXFIFO, check the data integrity, then enable MIF to write data in TXFIFO to destination data block space on memory card.
3. For SmartMedia application, the redundant data write to destination data block space is from redundant area of RXFIFO.

3.2.6 MHE (Media Hardware Engine)

The Media Hardware Engine contains 4 MIF (Media Interface), MHE control and MCFIFO.

3.2.6.1 MIF (Media Interface):

There are PCMCIA MIF, SmartMedia MIF, MemoryStick MIF, and Secure Digital/ Multi Media Card MIF in MHE.

3.2.6.2 MCFIFO (Media Control FIFO):

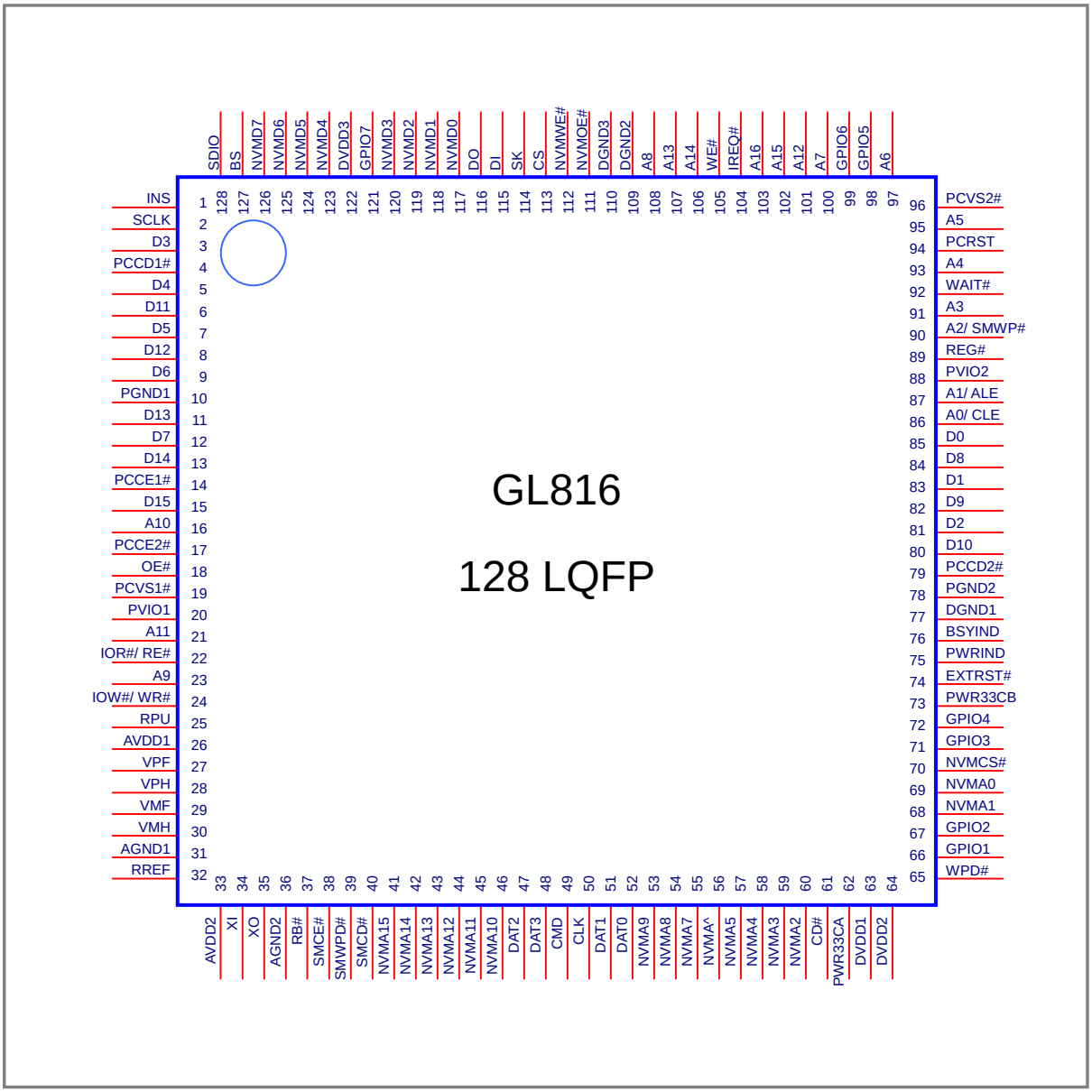
It's a 64-byte FIFO that shared by MemoryStick and SD/ MMC MIF. In MemoryStick application, the MCFIFO is used for register read and write function; In SD/ MMC application, it is used for command and response.

3.2.6.3 SMAFIFO (SmartMedia™ Address FIFO)

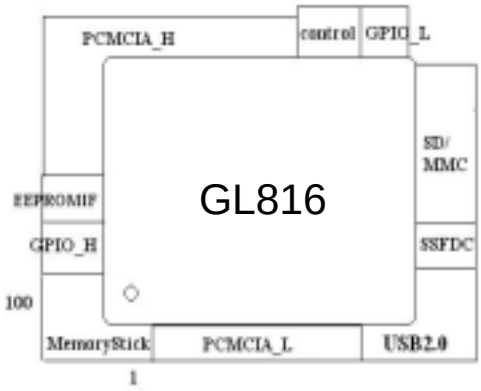
It's a 4-byte FIFO for SmartMedia address only.

4. Pinning Information

4.1 Pin Assignment



4.2 Pin Description



Pin#	Name	I/O	Description	Note
1	INS	B/I	MemoryStick INS	pu
2	SCLK	O	MemoryStick SCLK	
3	D3	B	PCMCIA data 3 / SmartMedia data 3	
4	PCCD1#	B/I	PCMCIA CD1#	pu
5	D4	B	PCMCIA data 4 / SmartMedia data 4	
6	D11	B	PCMCIA data 11	
7	D5	B	PCMCIA data 5 / SmartMedia data 5	
8	D12	B	PCMCIA data 12	
9	D6	B	PCMCIA data 6 / SmartMedia data 6	
10	PGND1	P	Pad GND #1	
11	D13	B	PCMCIA data 13	
12	D7	B	PCMCIA data 7 / SmartMedia data 7	

Pin#	Name	I/O	Description	Note
13	D14	B	PCMCIA data 14	
14	PCCE1#	B/O	PCMCIA CE1#	pu
15	D15	B	PCMCIA data 15	
16	A10	O	PCMCIA address 10	
17	PCCE2#	B/O	PCMCIA CE2#	pu
18	OE#	O	PCMCIA OE#	
19	PCVS1#	B/I	PCMCIA VS1# ATAPI DMARQ	
20	PVIO1	P	Power (5 / 3.3V) for pin 3-24	
21	A11	O	PCMCIA address 11	
22	IOR# / RE#	O	PCMCIA IOR# / SmartMedia RE#	
23	A9	O	PCMCIA address 9	
24	IOW# / WR#	O	PCMCIA IOW# / SmartMedia WR#	
25	RPU	A	USB resistor pull up	
26	AVDD1	P	Analog VDD #1	
27	VPF	B	FS D+	
28	VPH	B	HS D+	
29	VMF	B	FS D-	
30	VMH	B	HS D-	
31	AGND1	P	Analog GND #1	
32	RREF	A	Reference resistor	
33	AVDD2	P	Analog VDD #2	
34	XI	I	Crystal input	
35	XO	B	Crystal input	
36	AGND2	P	Analog GND #2	

Pin#	Name	I/O	Description	Note
37	RB#	B/I	SmartMedia RDY/BSY#	pu
38	SMCE#	B/O	SmartMedia CE#	pu
39	SMWPD#	B/I	SmartMedia Write Protect Detect	pu
40	SMCD#	B/I	SmartMedia CD#	pu
41	NVMA15	O	Ext. flash address 15	
42	NVMA14	O	Ext. flash address 14	
43	NVMA13	O	Ext. flash address 13	
44	NVMA12	O	Ext. flash address 12	
45	NVMA11	O	Ext. flash address 11	
46	NVMA10	O	Ext. flash address 10	
47	DAT2	B/SO	SD DAT2	pu
48	DAT3	B/SO	SD DAT3	pu
49	CMD	B/SO	SD/MMC CMD	pu
50	CLK	O	SD/MMC CLK	
51	DAT1	B/SO	SD DAT1	pu
52	DAT0	B/SO	SD/MMC DAT0	pu
53	NVMA9	O	Ext. flash address 9	
54	NVMA8	O	Ext. flash address 8	
55	NVMA7	O	Ext. flash address 7	
56	NVMA6	O	Ext. flash address 6	
57	NVMA5	O	Ext. flash address 5	
58	NVMA4	O	Ext. flash address 4	
59	NVMA3	O	Ext. flash address 3	
60	NVMA2	O	Ext. flash address 2	
61	CD#	B/I	SD/MMC CD#	pu
62	PWR33CA	O	PCMCIA 3.3V power control	pd
63	DVDD1	P	Digital VDD #1	

Pin#	Name	I/O	Description	Note
64	DVDD2	P	Digital VDD #2	
65	WPD#	B/I	SD/MMC Write Protect Detect	pu
66	GPIO1	B	GPIO1	odpu
67	GPIO2	B	GPIO2	odpu
68	NVMA1	O	Ext. flash address 1	
69	NVMA0	O	Ext. flash address 0	
70	NVMCS#	O	Ext. flash CS#	pu
71	GPIO3	B	GPIO3	odpu
72	GPIO4	B	GPIO4	odpu
73	PWR33CB	O	Card 3.3V power control	pd
74	EXTRST#	I	External reset	pu
75	PWRIND	O	Power indicator	pd
76	BSYIND	O	Busy indicator	pd
77	DGND1	P	Digital GND #1	pu
78	PGND2	P	Pad GND #2	
79	PCCD2#	B/I	PCMCIA CD2#	
80	D10	B	PCMCIA data 10	
81	D2	B	PCMCIA data 2 / SmartMedia data 2	
82	D9	B	PCMCIA data 9	
83	D1	B	PCMCIA data 1 / SmartMedia data 1	
84	D8	B	PCMCIA data 8	
85	D0	B	PCMCIA data 0 / SmartMedia data 0	
86	A0 / CLE	O	PCMCIA address 0 / SmartMedia CLE	

Pin#	Name	I/O	Description	Note
87	A1 / ALE	O	PCMCIA address 1 / SmartMedia ALE	
88	PVIO2	P	Power (3.3 / 5V) for pin 79-108	
89	REG#	B/O	PCMCIA REG#	pu
90	A2 / SMWP#	O	PCMCIA address 2 / SmartMedia WP#	
91	A3	O	PCMCIA address 3	
92	WAIT#	I/SO	PCMCIA WAIT#	pu
93	A4	O	PCMCIA address 4	
94	PCRST	B	PCMCIA RESET	pd
95	A5	O	PCMCIA address 5	
96	PCVS2#	B/I	PCMCIA VS2#	pu
97	A6	O	PCMCIA address 6	
98	GPIO5	B	GPIO5	odpu
99	GPIO6	B	GPIO6	odpu
100	A7	O	PCMCIA address 7	
101	A12	O	PCMCIA address 12 / ATAPI DMACK#	
102	A15	O	PCMCIA address 15	
103	A16	O	PCMCIA address 16	
104	IREQ#	B/I	PCMCIA IREQ#	pu
105	WE#	O	PCMCIA WE#	
106	A14	O	PCMCIA address 14 / MCS0#	
107	A13	O	PCMCIA address 13 / MCS1#	
108	A8	O	PCMCIA address 8	
109	DGND2	P	Digital GND #2	
110	DGND3	P	Digital GND #3	

Pin#	Name	I/O	Description	Note
111	NVMOE#	O	Ext. flash OE#	
112	NVMWE#	O	Ext. flash WE#	
113	CS	O	93C86 CS	
114	SK	O	93C86 Clock	
115	DI	O	93C86 Data in	
116	DO	I/SO	93C86 Data out	pd
117	NVMD0	B	Ext. flash Data 0	pd
118	NVMD1	B	Ext. flash Data 1	pd
119	NVMD2	B	Ext. flash Data 2	pd
120	NVMD3	B	Ext. flash Data 3	pd
121	GPIO7	B	GPIO7	odpu
122	DVDD3	P	Digital VDD #3	
123	NVMD4	B	Ext. flash Data 4	pd
124	NVMD5	B	Ext. flash Data 5	pd
125	NVMD6	B	Ext. flash Data 6	pd
126	NVMD7	B	Ext. flash Data 7	pd
127	BS	O	MemoryStick BS	
128	SDIO	B	MemoryStick SDIO	pd

Notation:

Description	**O**	Output
	I	Input
	B	Bi-directional
	B/I	Bi-directional, default input
	B/O	Bi-directional, default output
	P	Power
	A	Analog
	SO	Automatic output low when suspend
Note	**pu**	Internal pull up
	pd	Internal pull down
	odpu	Open drain with internal pull up

5. Electrical Characteristics

5.1 Recommended Operation Conditions

Item	Value
T_A (Ambient Temperature under bias)	0°C to 70°C
Supply Voltage	+3.0V to +3.6V
Ground Voltage	0V
F_{OSC}	12 MHz ± 100ppm

5.2 DC Characteristics

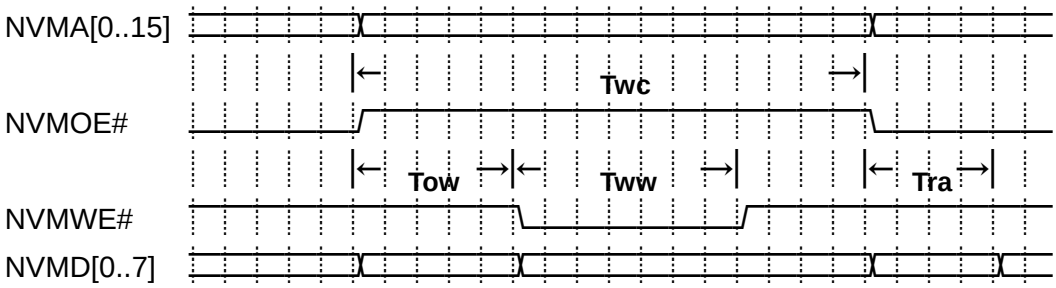
Parameter	Description	Condition	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		3.0		3.6	V
V_{IH}	Input High Voltage		2.6		5	V
V_{IL}	Input Low Voltage		0.0		0.7	V
I_I	Input Leakage current	$0 < V_{IN} < V_{CC}$				μA
V_{OH}	Output High Voltage		3.0			V
V_{OL}	Output Low Voltage				0.2	V
I_{OH}	Output Current High					mA
I_{OL}	Output Current Low					mA
C_{IN}	Input Pin Capacitance				2.0	pF
I_{SUSP}	Suspend current	1.5K external pull-up included				μA
I_{CC}	Supply current	Connect to USB with 8051 operating				mA

5.3 AC Electrical Characteristics

5.3.1 UTMI Transceiver

The GL816 is fully compatible with Universal Serial Bus specification rev. 2.0 and USB 2.0 Transceiver Macercell Interface (UTMI) specification rev. 1.01. Please refer to the specifications for more information.

5.3.2 External Flash

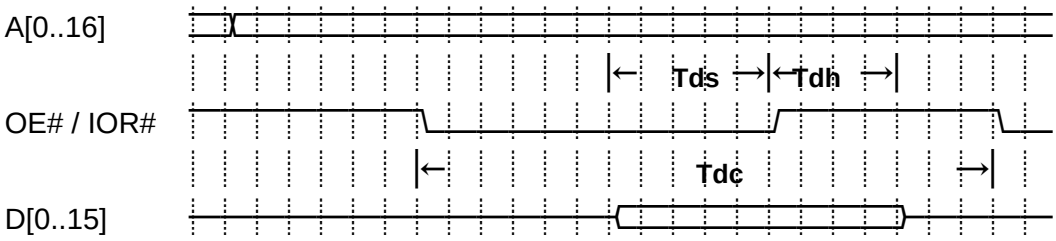


Parameter	Description	Min	Typ	Max
T_{WC}	Write data cycle time		102.5	
T_{WW}	Write pulse width		41.6	
T_{OW}	OE# to WE# time		38.6	
T_{RA}	Read Access time			90

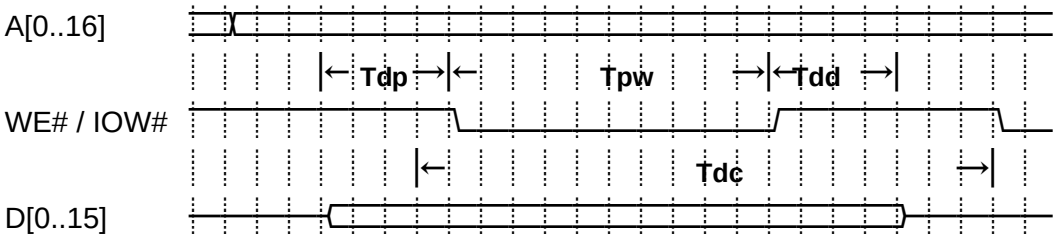
Unit: ns

5.3.3 PCMCIA

Read



Write

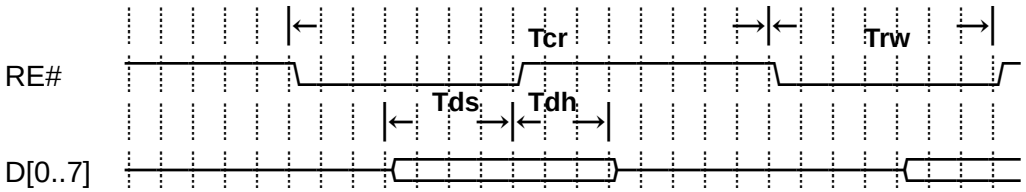


Parameter	Description	Mode	Min	Typ	Max
Tds	Data setup time (read)	0, 1		88.3	
		2, 3		38.3	
Tdh	Data hold time (read)	0, 1		2	
		2, 3		2	
Tdc	Access cycle time (read / write)	0		666.4	
		1		416.5	
		2		222.1	
		3		166.5	
Tpw	Control pulse width (read / write)	0		333.2	
		1		166.6	
		2		133.2	
		3		66.6	
Tdp	Data pre-output time (write)	0, 1		26.6	
		2, 3		1.6	
Tdd	Data delay time (write)	0, 1		41.6	
		2, 3		16.6	

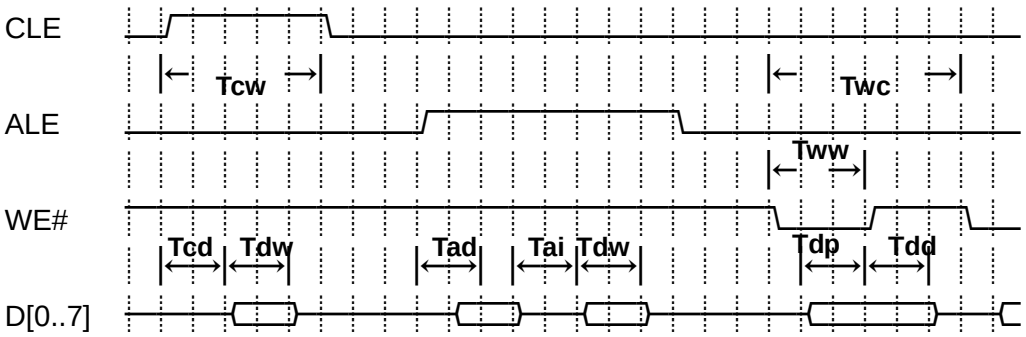
Unit: ns

5.3.4 SmartMedia

Read



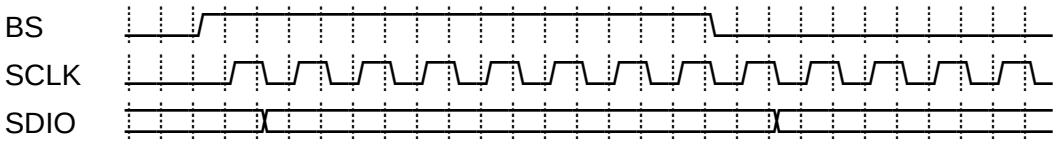
Write



Parameter	Description	Mode	Min	Typ	Max
Tcw	CLE active width	Normal		165	
		Slow		198	
Twc	Write data cycle time	Normal		100	
		Slow		166	
Tww	Write pulse width	Normal		66	
		Slow		100	
Tcd	CLE-to-command delay			33.3	
Tdw	Data width	Normal		67	
		Slow		100	
Tad	ALE-to-address delay			33.3	
Tai	Address data interval time			33.3	
Tdp	Data pre-output delay			33.3	
Tdd	Data delay time			33.3	
Tcr	Read data cycle time	Normal		133.3	
		Slow		166.6	
Trw	Read pulse width			100	
Tds	Data setup time			40	
Tdh	Data hold time			2	

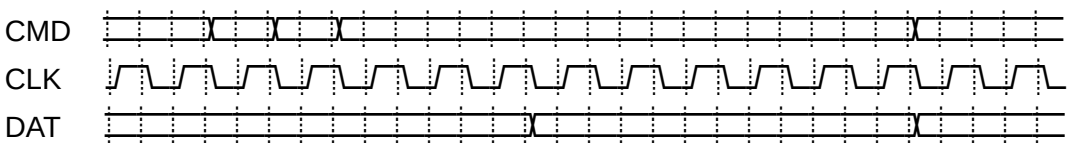
Unit: ns

5.3.5 MemoryStick



Parameter	Description	Mode	Typ	Unit	Remark
Fck	SCLK frequency	0	1.5M	Hz	
		1	6M		
		2	15M		
		3	24M		

5.3.6 Secure Digital / MultiMedia Card

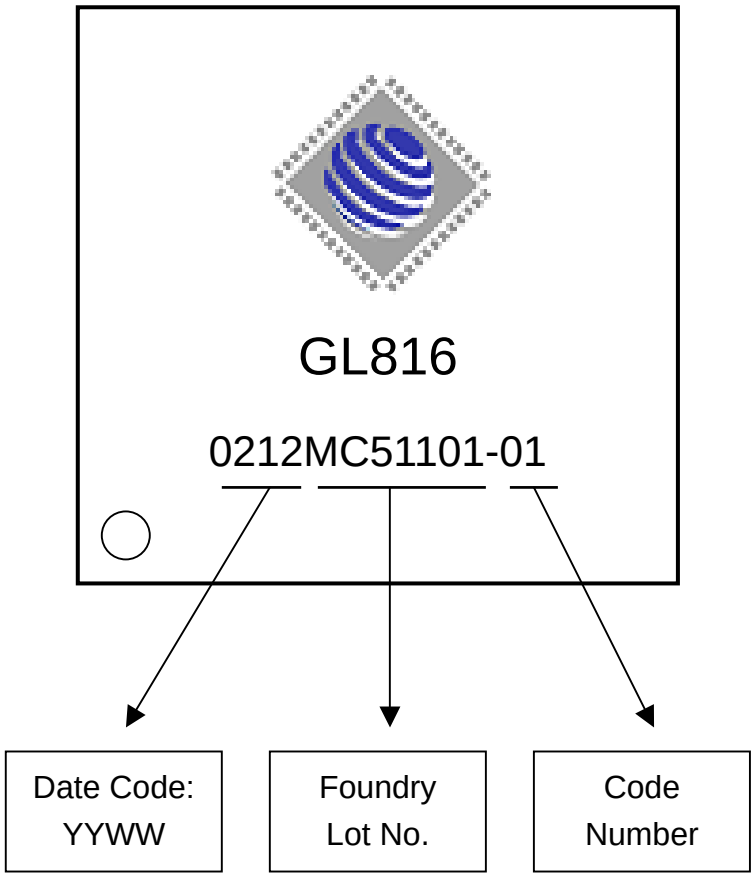


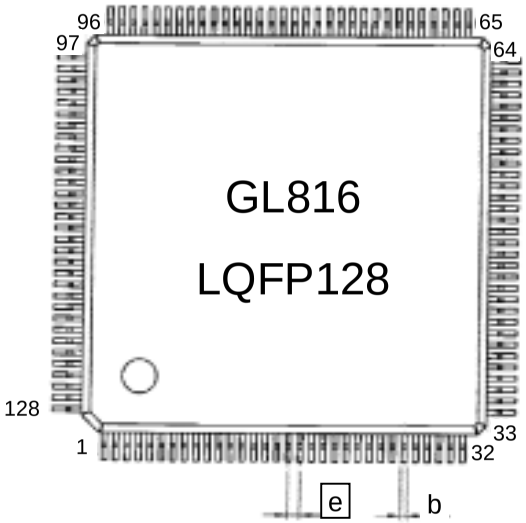
Parameter	Description	Mode	Typ	Unit	Remark
Fck	CLK frequency	0	375K	Hz	
		1	6M		
		2	15M		
		3	24M		

6. Package Information

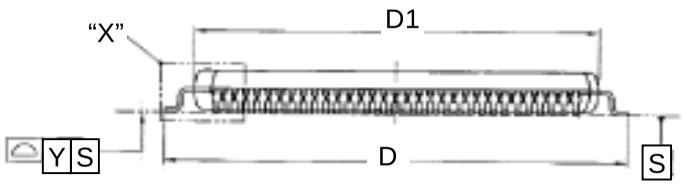
Type No.	Package	
GL816	Name	Description
	LQFP128	Plastic low profile quad flat package; 128 leads; Body 14 x14 x1.4 mm

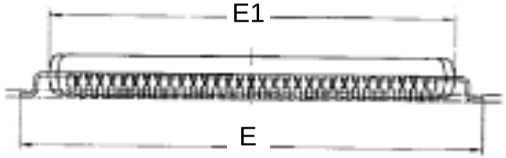
EX:

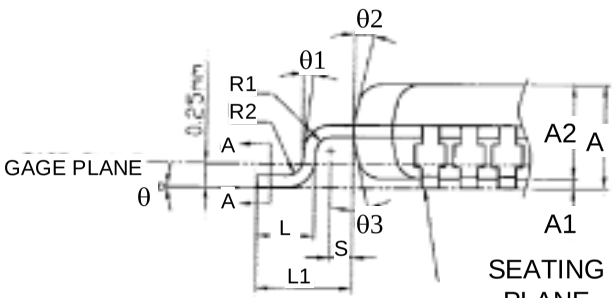




SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.60			63
A1	0.05		0.15	2		6
A2	1.35	1.40	1.45	53	55	57
b	0.13	0.18	0.23	5	7	9
b1	0.13	0.16	0.19	5	6.3	7.5
c	0.09		0.20	4		8
c1	0.09		0.16	4		6
D	16.00 BSC			630 BSC		
D1	14.00 BSC			551 BSC		
E	16.00 BSC			630 BSC		
E1	14.00 BSC			551 BSC		
e	0.40 BSC			16 BSC		
	0.45	0.60	0.75	18	24	30
L1	1.00 REF			39 REF		
R1	0.08			3		
R2	0.08		0.20	3		8
Y			0.075			3
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°			0°		
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
s	0.20			8		

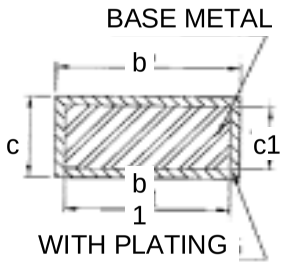






DETAIL "X"

(20/1)



SECTION A-A

Genesys Logic, Inc.
GL816
LQFP128 (14x14x1.4 mm)

7. Revision History

Version	Description	Date
1.0	First draft	2002/05/10
1.1	Change the package from QFP128 to LQFP128	2002/07/17
1.2	Add package information data	2002/09/20

