HARRIS Semiconductor

HS-2510RH

Radiation Hardened High Slew Rate Operational Amplifiers

August 1995

Features

- High Slew Rate 50V/μs (Min), 65V/μs (Typ)
- Wide Power Bandwidth 750kHz (Min)
- Low Offset Current 25nA (Min), 10nA (Typ)
- High Input Impedance 50MΩ (Min), 100MΩ (Typ)
- Wide Small Signal Bandwidth 12MHz (Typ)
- Fast Settling Time (0.1% of 10V Step) 250ns (Typ)
- Low Quiescent Supply Current 6mA (Max)
- Internally Compensated For Unity Gain Stability
- Total Gamma Dose 10K RAD (Si)

Applications

- Data Acquisition Systems
- RF Amplifiers
- Video Amplifiers
- Signal Generators
- Pulse Amplification

Description

The HS-2510RH is a radiation hardened high performance operational amplifier which set the standard for maximum slew rate and wide bandwidth operation in moderately powered, internally compensated, monolithic devices. In addition to excellent dynamic characteristics, this dielectrically isolated amplifier also offers low offset current and high input impedance.

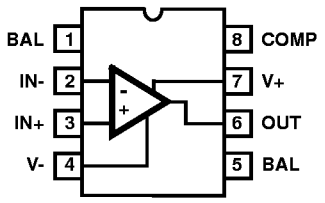
The ±50V/ms minimum slew rate and fast settling time of the HS-2510RH are ideally suited for high speed D/A, A/D, and pulse amplification designs. The HS-2510RH superior bandwidth and 750kHz minimum full power bandwidth are extremely useful in RF and video applications. To insure compliance with slew rate and transient response specifications, all devices are 100% tested for AC performance characteristics over full temperature limits. To improve signal conditioning accuracy, the HS-2510RH provides a maximum offset current of 25nA and a minimum input impedance of 50MΩ, both at +25°C, as well as offset voltage trim capability.

Ordering Information

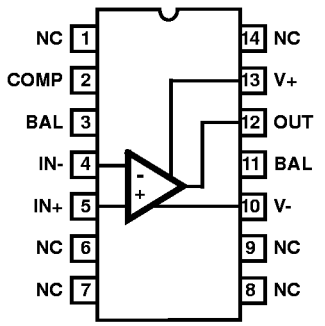
PART NUMBER	TEMPERATURE RANGE	PACKAGE TYPE
HS7-2510RH	-55°C to +125°C	8 Lead CerDIP
HS9-2510RH	-55°C to +125°C	14 Lead Ceramic Flatpack

Pinouts

8 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE (CERDIP) MIL-STD-1835, GDIP1-T8
TOP VIEW



14 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE (FLATPACK) MIL-STD-1835, CDFP3-F14
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

Spec Number 518809
File Number 3592.1

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 40V
Differential Input Voltage 15V
Voltage at Either Input Terminal . . . . . V+ to V-
Peak Output Current. 50mA
Junction Temperature (TJ) . . . . . +175°C
Storage Temperature Range . . . . . -65°C to +150°C
ESD Rating. . . . . <2000V
Lead Temperature (Soldering 10s) . . . . . +275°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
CerDIP Package	120°C/W	30°C/W
Ceramic Flatpack Package	125°C/W	35°C/W

Max Package Power Dissipation Limit at +125°C Ambient
CerDIP Package 0.42W
Ceramic Flatpack Package 0.40W
If Device Power Exceeds Package Dissipation Capability, Provide Heat Sinking or Derate Linearly at the Following Rate
CerDIP Package . . . . . 8.3mW/°C
Ceramic Flatpack Package . . . . . 8.0mW/°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended Operating Conditions

Operating Temperature Range . . . . . -55°C to +125°C
Operating Supply Voltage . . . . . ±15V

VINcm ≤ 1/2 (V+ - V-)
RL ≥ 2kΩ

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: VSUPPLY = ±15V, RSOURCE = 100Ω, RLOAD = 500kΩ, VOUT = 0V, Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Offset Voltage	VIO	VCM = 0V	+25°C	-8	8	mV
			+125°C, -55°C	-10	10	mV
Input Bias Current	+IB	VCM = 0V, +RS = 100kΩ -RS = 100Ω	+25°C	-200	200	nA
			+125°C, -55°C	-400	400	nA
	-IB	VCM = 0V, +RS = 100Ω -RS = 100kΩ	+25°C	-200	200	nA
			+125°C, -55°C	-400	400	nA
Input Offset Current	IIO	VCM = 0V, +RS = 100kΩ -RS = 100kΩ	+25°C	-25	25	nA
			+125°C, -55°C	-50	50	nA
Common Mode Range	+CMR	V+ = 5V V- = -25V	+25°C	+10	-	V
			+125°C, -55°C	+10	-	V
	-CMR	V+ = 25V V- = -5V	+25°C	-	-10	V
			+125°C, -55°C	-	-10	V
Large Signal Voltage Gain	+AVOL	VOUT = 0V and +10V RL = 2kΩ	+25°C	10	-	kV/V
			+125°C, -55°C	7.5	-	kV/V
	-AVOL	VOUT = 0V and -10V RL = 2kΩ	+25°C	10	-	kV/V
			+125°C, -55°C	7.5	-	kV/V
Common Mode Rejection Ratio	+CMRR	ΔVCM = +10V, +V = +5V -V = -25V, VOUT = -10V	+25°C	80	-	dB
			+125°C, -55°C	80	-	dB
	-CMRR	ΔVCM = -10V, +V = +25V -V = -5V, VOUT = +10V	+25°C	80	-	dB
			+125°C, -55°C	80	-	dB
Output Voltage Swing	+VOUT	RL = 2kΩ	+25°C	10	-	V
			+125°C, -55°C	10	-	V
	-VOUT	RL = 2kΩ	+25°C	-	-10	V
			+125°C, -55°C	-	-10	V

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: VSUPPLY = ±15V, RSOURCE = 100Ω, RLOAD = 500kΩ, VOUT = 0V, Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS		UNITS
				MIN	MAX	
Output Current	+IOUT	VOUT = -10V	+25°C	10	-	mA
			+125°C, -55°C	7.5	-	mA
	-IOUT	VOUT = +10V	+25°C	-	-10	mA
			+125°C, -55°C	-	-7.5	mA
Quiescent Power Supply Current	+ICC	IOUT = 0mA	+25°C	-	6	mA
			+125°C, -55°C	-	6.5	mA
	-ICC	IOUT = 0mA	+25°C	-6	-	mA
			+125°C, -55°C	-6.5	-	mA
Power Supply Rejection Ratio	+PSRR	ΔVSUP = 10V +V = +20V, -V = -15V +V = +10V, -V = -15V	+25°C	80	-	dB
			+125°C, -55°C	80	-	dB
	-PSSR	ΔVSUP = 10V +V = +15V, -V = -20V +V = +15V, -V = -10V	+25°C	80	-	dB
			+125°C, -55°C	80	-	dB
Offset Voltage Adjustment	+V10Adj	Note 1	+25°C	V10-1	-	mV
			+125°C, -55°C	V10-1	-	mV
	-V10Adj	Note 1	+25°C	V10+1	-	mV
			+125°C, -55°C	V10+1	-	mV

NOTE:

1. Offset adjustment range is (VIO (measured, ±1mV) minimum referred to output this test is for functionality only to assure adjustment through 0V.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: VSUPPLY = ±15V, RSOURCE = 1KΩ, RLOAD = 2kΩ, CLOAD = 50pF, AVCL = +1V/V, Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS		UNIT
				MIN	MAX	
Slew Rate	+SR	VOUT = -5V to +5V	+25°C	50	-	V/µs
			+125°C, -55°C	45	-	V/µs
	-SR	VOUT = +5V to -5V	+25°C	50	-	V/µs
			+125°C, -55°C	45	-	V/µs
Rise and Fall Time	TR	VOUT = 0 to +200mV 10% ≤TR ≤90%	+25°C	-	50	ns
			+125°C, -55°C	-	60	ns
	TF	VOUT = 0 to -200mV 10% ≤TR ≤90%	+25°C	-	50	ns
			+125°C, -55°C	-	60	ns
Overshoot	+OS	VOUT = 0 to +200mV	+25°C	-	40	%
			+125°C, -55°C	-	50	%
	-OS	VOUT = 0 to -200mV	+25°C	-	40	%
			+125°C, -55°C	-	50	%

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: VSUPPLY = ±15V, RLOAD = 2kΩ, CLOAD = 50pF, Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Differential Input Resistance	RIN	VCM = 0V	1	+25°C	50	-	MΩ
Full Power Bandwidth	FPBW	VPEAK = 10V	1, 2	+25°C	750	-	kHz
Minimum Closed Loop Stable Gain	CLSG		1	-55°C to +125°C	1	-	V/V
Quiescent Power Consumption	PC	VOUT = 0V, IOUT = 0mA	1, 3	-55°C to +125°C	-	195	mW

NOTES:

1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.
2. Full power bandwidth guarantee based on slew rate measurement using FPBW = Slew Rate/(2πVPEAK).
3. Quiescent power consumption based upon quiescent supply current last maximum. (No load on outputs.)

TABLE 4. POST 10K RAD(SI) ELECTRICAL CHARACTERISTICS

Device Tested at: VSUPPLY = ±15V, RSOURCE = 100Ω, RLOAD = 500kΩ, VOUT = 0V, Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS		UNITS
				MIN	MAX	
Input Offset Voltage	VIO	VCM = 0V	+25°C	-10	10	mV
Input Bias Current	+IB	VCM = 0V, +RS = 100kΩ -RS = 100Ω	+25°C	-600	600	nA
	-IB	VCM = 0V, +RS = 100Ω -RS = 100kΩ	+25°C	-600	600	nA
Input Offset Current	IIO	VCM = 0V, +RS = 100kΩ -RS = 100kΩ	+25°C	-50	50	nA
Common Mode Range	+CMR	V+ = +5V V- = -25V	+25°C	+10	-	V
	-CMR	V+ = +25V V- = -5V	+25°C	-	-10	V
Large Signal Voltage Gain	+AVOL	VOUT = 0V and +10V RL = 2kΩ	+25°C	5	-	kV/V
	-AVOL	VOUT = 0V and -10V RL = 2kΩ	+25°C	5	-	kV/V
Common Mode Rejection Ratio	+CMRR	ΔVCM = +10V, +V = +5V -V = -25V, VOUT = -10V	+25°C	80	-	dB
	-CMRR	ΔVCM = -10V, +V = +25V -V = -5V, VOUT = +10V	+25°C	80	-	dB
Output Voltage Swing	+VOUT	RL = 2kΩ	+25°C	10	-	V
	-VOUT	RL = 2kΩ	+25°C	-	-10	V
Output Current	+IOUT	VOUT = -10V	+25°C	7.5	-	mA
	-IOUT	VOUT = +10V	+25°C	-	-7.5	mA
Quiescent Power Supply Current	+ICC	VOUT = 0mA	+25°C	-	6.5	mA
	-ICC	VOUT = 0mA	+25°C	-6.5	-	mA

TABLE 4. POST 10K RAD(SI) ELECTRICAL CHARACTERISTICS (Continued)

Device Tested at: VSUPPLY = ±15V, RSOURCE = 100Ω, RLOAD = 500kΩ, VOUT = 0V, Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS		UNITS
				MIN	MAX	
Power Supply Rejection Ratio	+PSRR	ΔVSUP = 10V +V = +20V, -V = -15V +V = +10V, -V = -15V	+25°C	75	-	dB
	-PSRR	ΔVSUP = 10V +V = +15V, -V = -20V +V = +15V, -V = -10V	+25°C	75	-	dB
Offset Voltage Adjustment	+VIOAdj	Note 1	+25°C	VIO-1	-	mV
	-VIOAdj	Note 1	+25°C	VIO+1	-	mV
Slew Rate	+SR	VOUT = -5V to +5V	+25°C	45	-	V/µs
	-SR	VOUT = +5V to -5V (Note 2)	+25°C	45	-	V/µs
Rise and Fall Time	TR	VOUT = 0 to +200mV 10% ≤TR ≤90% (Note 2)	+25°C	-	60	ns
	TF	VOUT = 0 to -200mV 10% ≤TR ≤90% (Note 2)	+25°C	-	60	ns
Overshoot	+OS	VOUT = 0 to +200mV (Note 2)	+25°C	-	50	%
	-OS	VOUT = 0 to -200mV (Note 2)	+25°C	-	50	%

NOTES:

1. Offset adjustment range is (VIO (measured, ±1mV) minimum referred to output this test is for functionality only to assure adjustment through 0V.
2. RLOAD = 2kΩ, CLOAD = 50pF, RSOURCE = 1kΩ, AVCL = +1V/V.

TABLE 5. POST BURN-IN DELTA PARAMETERS (T_A = 25°C)

Device Tested at: VSUPPLY = ±15V, RSOURCE = 100Ω, RLOAD = 500kΩ, VOUT = 0V

PARAMETERS	DELTA LIMITS
VIO	±2.0mV
+IB, -IB	±50nA

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP	MIL-STD-883 METHOD	GROUP A SUBGROUPS	
		TESTED FOR -Q	RECORDED FOR -Q
Initial Test	100% 5004	1, 9	1 (Note 1)
Interim Test	100% 5004	1, 9, Δ	1, Δ (Note 1)
PDA	100% 5004	1, Δ	
Final Test	100% 5004	2, 3, 10, 11	
Group A (Note 2)	Sample 5005	1, 2, 3, 9, 10, 11	
Subgroup B5	Sample 5005	1, 2, 3, 9, 10, 11, Δ	1, 2, 3, Δ (Note 1)
Subgroup B6	Sample 5005	1, 9	
Group D	Sample 5005	1, 9	
Group E, Subgroup 2	Sample 5005	1, 9	

NOTE:

1. Table 5 parameters only.
2. Alternate Group A testing may be exercised in accordance with MIL-STD-883, Method 5005.

Harris Space Level Product Flow -Q

Wafer Lot Acceptance (All Lots) Method 5007 (Includes SEM) (Note 1)

GAMMA Radiation Verification (Each Wafer) Method 1019, 4 Samples/Wafer, 0 Rejects

100% Die Attach

100% Nondestructive Bond Pull, Method 2023

Sample - Wire Bond Pull Monitor, Method 2011

Sample - Die Shear Monitor, Method 2019 or 2027

100% Internal Visual Inspection, Method 2010, Condition A

CSI and/or GSI PreCap (Note 7)

100% Temperature Cycle, Method 1010, Condition C, 10 Cycles

100% Constant Acceleration, Method 2001, Condition per Method 5004

100% PIND, Method 2020, Condition A

100% External Visual

100% Serialization

100% Initial Electrical Test (T0)

100% Static Burn-In, Condition A or B, 240 Hours, +125^{o}C or Equivalent, Method 1015

100% Interim Electrical Test (T1)

100% Delta Calculation (T0-T1)

100% PDA, Method 5004 (Note 2)

100% Final Electrical Test

100% Fine/Gross Leak, Method 1014

100% Radiographic (X-Ray), Method 2012 (Note 3)

100% External Visual, Method 2009

Sample - Group A, Method 5005 (Note 4)

Sample - Group B, Method 5005 (Note 5)

Sample - Group D, Method 5005 (Notes 5, 6)

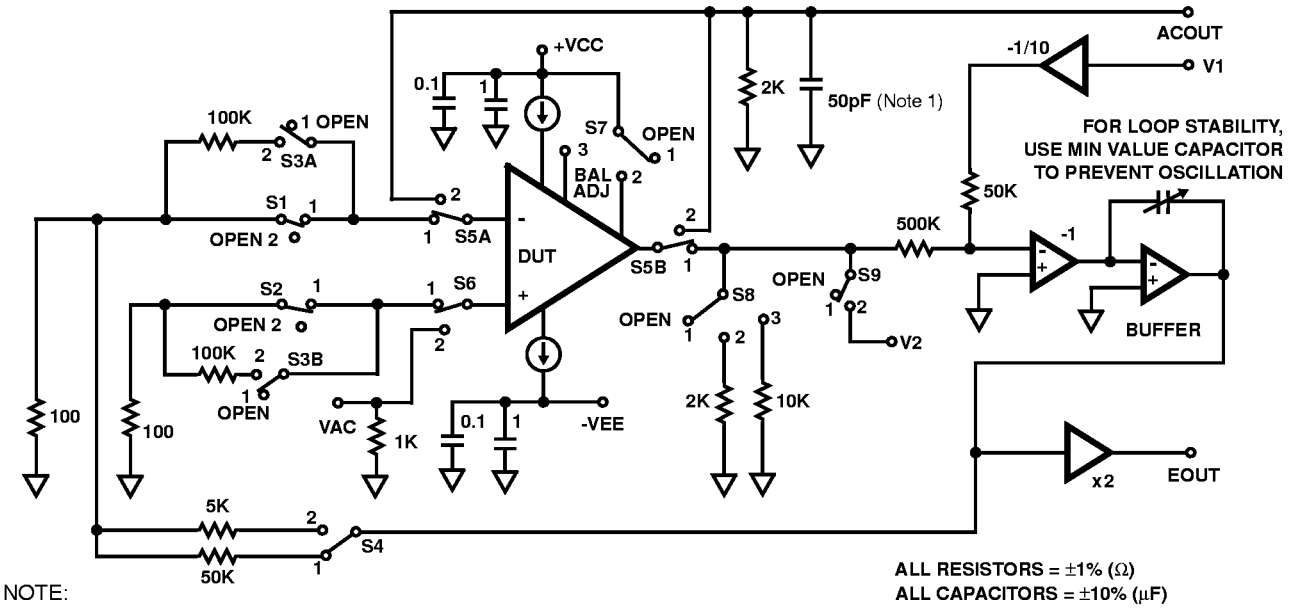
100% Data Package Generation (Note 8)

CSI and/or GSI Final (Note 7)

NOTES:

1. Modified SEM Inspection, not compliant to MIL-STD-883, Method 2018. This device does not meet the Class S minimum metal step coverage of 50%. The metal does meet the current density requirement of $<2\ E^5$ A/cm^2. Data provided upon request.
2. Failures from subgroup 1 and deltas are used for calculating PDA. The maximum allowable PDA = 5%.
3. Radiographic (X-Ray) inspection may be performed at any point after serialization as allowed by Method 5004.
4. Alternate Group A testing may be performed as allowed by MIL-STD-883, Method 5005.
5. Group B and D inspections are optional and will not be performed unless required by the P.O. When required, the P.O. should include separate line items for Group B test, Group B samples, Group D test and Group D samples.
6. Group D Generic Data, as defined by MIL-I-38535, is optional and will not be supplied unless required by the P.O. When required, the P.O. should include a separate line item for Group D generic data. Generic data is not guaranteed to be available and is therefore not available in all cases.
7. CSI and/or GSI inspections are optional and will not be performed unless required by the P.O. When required, the P.O. should include separate line items for CSI PreCap inspection, CSI Final Inspection, GSI PreCap inspection, and/or GSI Final Inspection.
8. Data Package Contents:
   Cover Sheet (Harris Name and/or Logo, P.O. Number, Customer Part Number, Lot Date Code, Harris Part Number, Lot Number, Quantity).
   Wafer Lot Acceptance Report (Method 5007). Includes reproductions of SEM photos with percent of step coverage.
   GAMMA Radiation Report. Contains Cover page, disposition, RAD Dose, Lot Number, Test Package used, Specification Numbers, Test equipment, etc. Radiation Read and Record data on file at Harris.
   X-Ray report and film. Includes penetrometer measurements.
   Screening, Electrical, and Group A attributes (Screening attributes begin after package seal).
   Lot Serial Number Sheet (Good units serial number and lot number).
   Variables Data (All Delta operations). Data is identified by serial number. Data header includes lot number and date of test. (See Table 6.)
   Group B and D attributes and/or Generic data is included when required by the P.O.
   The Certificate of Conformance is a part of the shipping invoice and is not part of the Data Book. The Certificate of Conformance is signed by an authorized Quality Representative.

Test Circuit (Applies to Tables 1, 2, 4, 5)



NOTE:

1. Includes stray capacitances.

FIGURE 1. SIMPLIFIED TEST CIRCUIT (Applies to Table 2)

Test Circuit and Waveforms

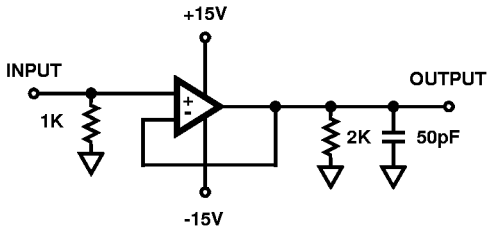
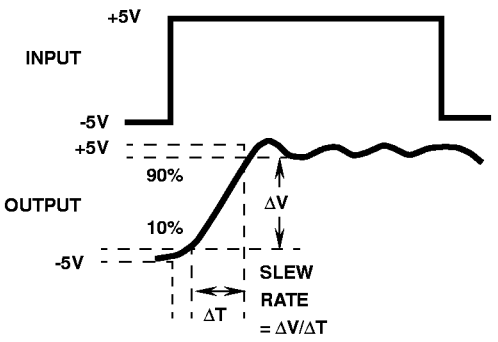
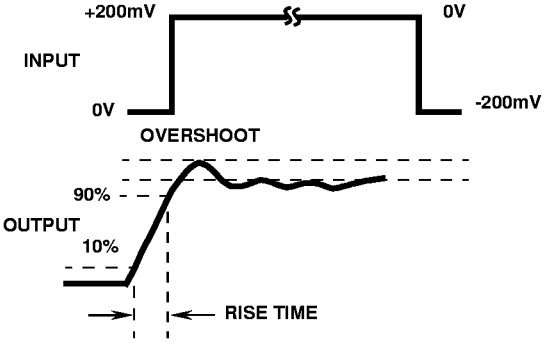


FIGURE 2. SIMPLIFIED TEST CIRCUIT (Applies to Table 2)



NOTE: Measured on both positive and negative transitions. Capacitance at Compensation pin should be minimized.

FIGURE 3. SLEW RATE WAVEFORM



NOTE: Measured on both positive and negative transitions. Capacitance at Compensation pin should be minimized.

FIGURE 4. TRANSIENT RESPONSE WAVEFORM

Typical Performance Curves Unless Otherwise Specified: T_A = +25°C, VSUPPLY = ±15V

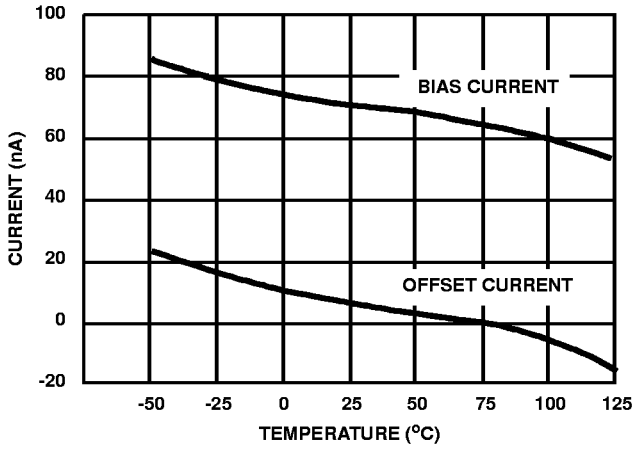


FIGURE 5. INPUT BIAS AND OFFSET CURRENT vs TEMPERATURE

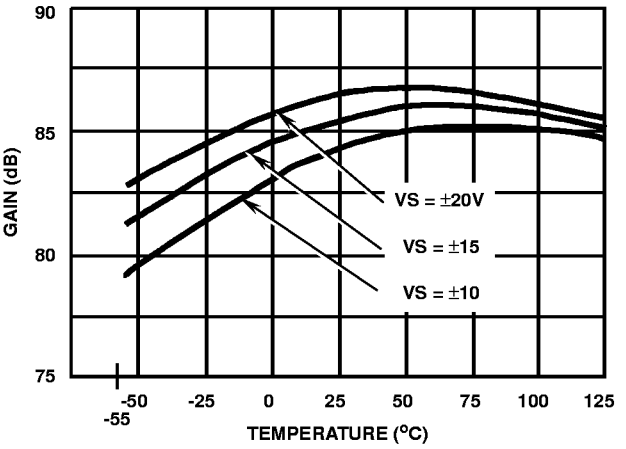


FIGURE 6. OPEN LOOP VOLTAGE GAIN vs TEMPERATURE

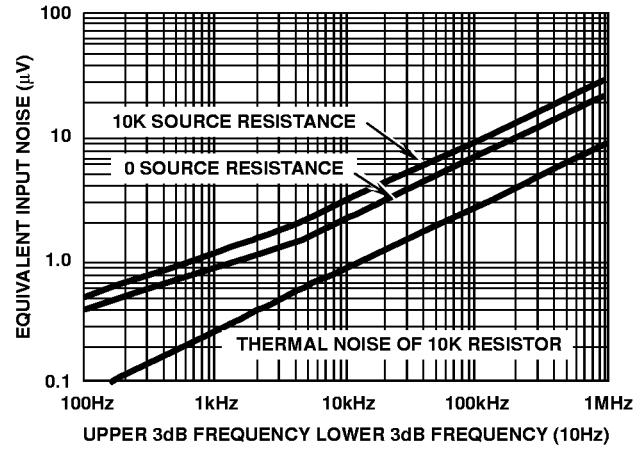


FIGURE 7. EQUIVALENT INPUT NOISE vs BANDWIDTH

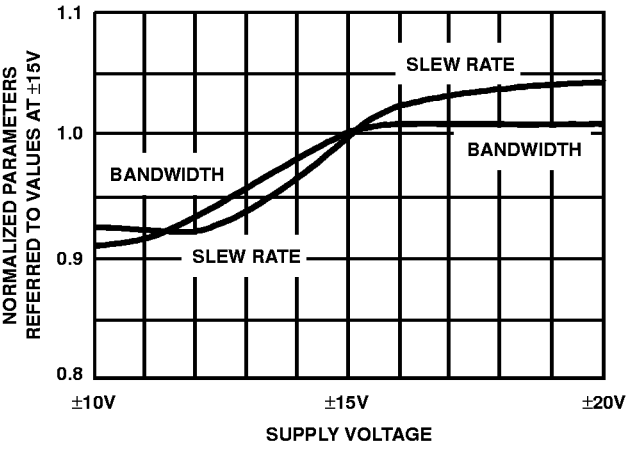


FIGURE 8. NORMALIZED AC PARAMETERS vs SUPPLY VOLTAGE AT +25°C

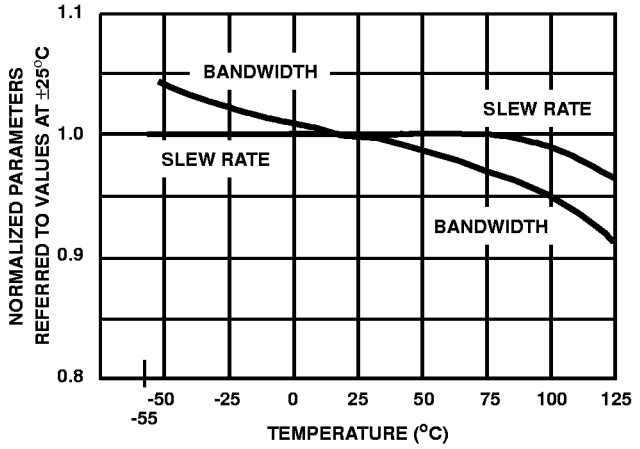


FIGURE 9. NORMALIZED AC PARAMETERS vs TEMPERATURE

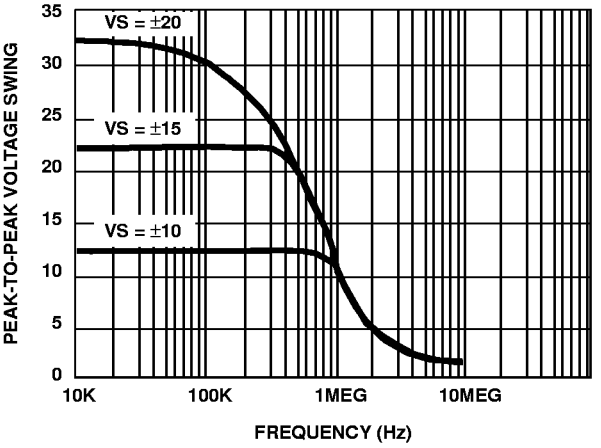
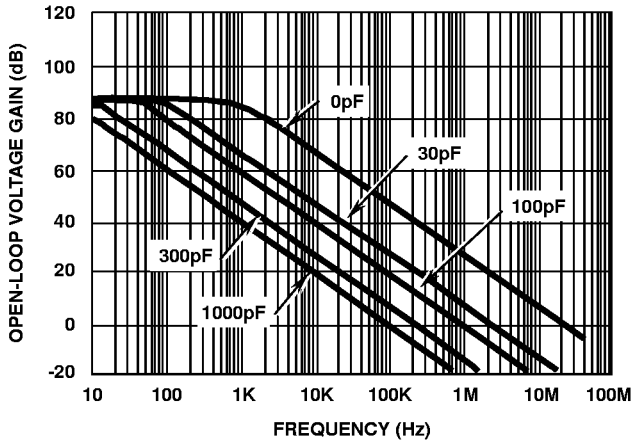


FIGURE 10. OUTPUT VOLTAGE SWING vs FREQUENCY AT +25°C

Typical Performance Curves Unless Otherwise Specified: T_A = +25°C, VSUPPLY = ±15V (Continued)



NOTE: External compensation components are not required for stability, but may be added to reduce bandwidth, if desired.

FIGURE 11. OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM COMPENSATION PIN TO GROUND

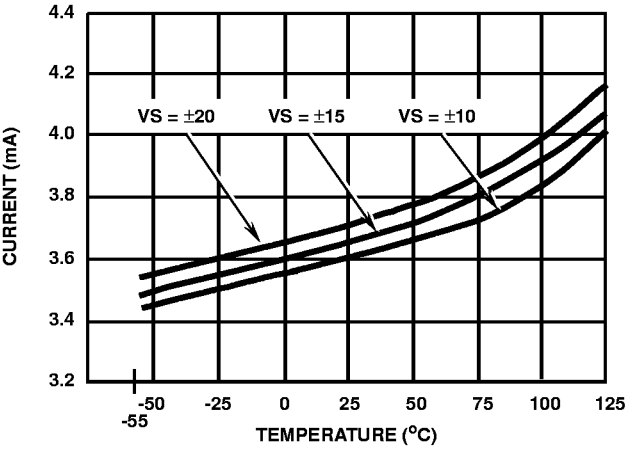


FIGURE 12. POWER SUPPLY CURRENT vs TEMPERATURE

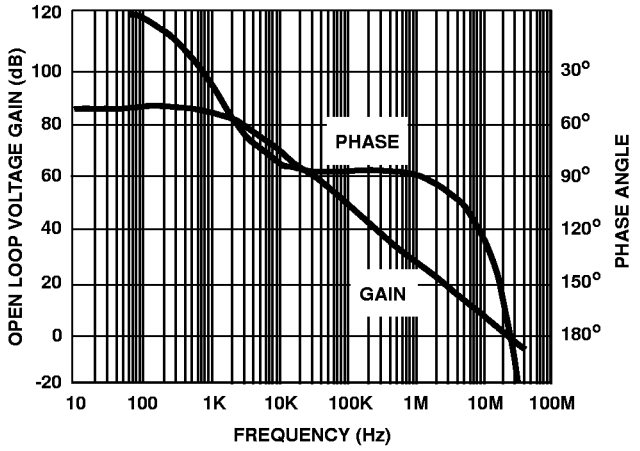
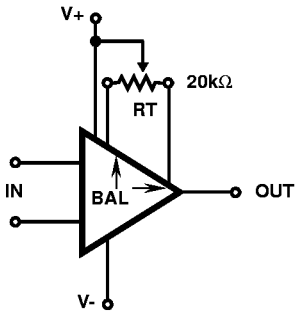


FIGURE 13. OPEN LOOP GAIN AND PHASE RESPONSE vs FREQUENCY



TESTED OFFSET ADJUSTMENT IS |VOS + 1mV|
MINIMUM REFERRED TO OUTPUT
TYPICAL RANGE IS ±8mV FOR RT = 20kΩ

FIGURE 14. SUGGESTED VOS ADJUSTMENT

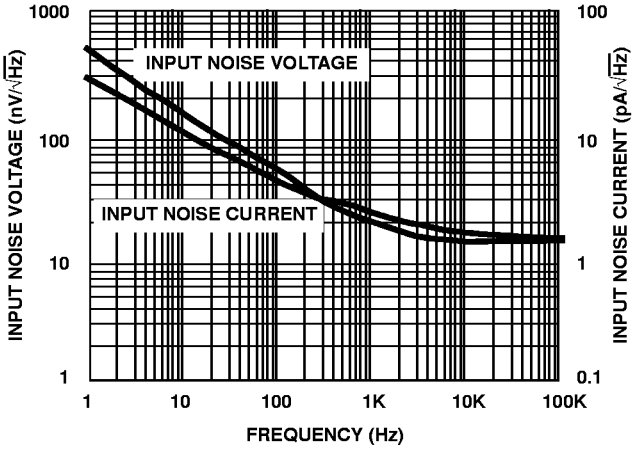
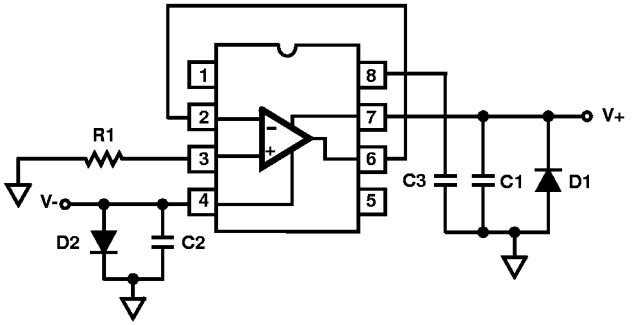


FIGURE 15. INPUT NOISE DENSITY vs FREQUENCY

Burn-In Circuits

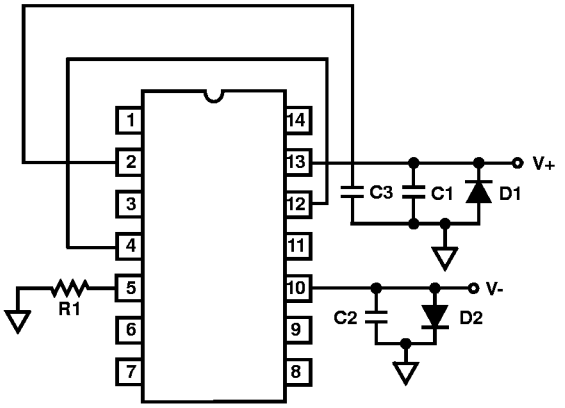
HS7-2510RH CerDIP



NOTES:

1. R1 = 1MΩ, ±5%, 1/4W (Min)
2. C1 = C2 = 0.01µF/Socket (Min) or 0.1µF/Row (Min)
3. C3 = 0.01µF/Socket (10%)
4. D1 = D2 = 1N4002 or Equivalent (Per Board)
5. |(V+) - (V-)| = 30V

HS9-2510RH CERAMIC FLATPACK

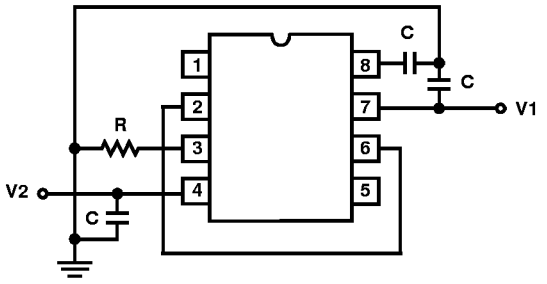


NOTES:

1. R1 = 1MΩ, ±5%, 1/4W (Min)
2. C1 = C2 = 0.01µF/Socket (Min) or 0.1µF/Row (Min)
3. C3 = 0.01µF/Socket (±10%)
4. D1 = D2 = 1N4002 or Equivalent (Per Board)
5. |(V+) - (V-)| = 31V ±1V

Irradiation Circuit

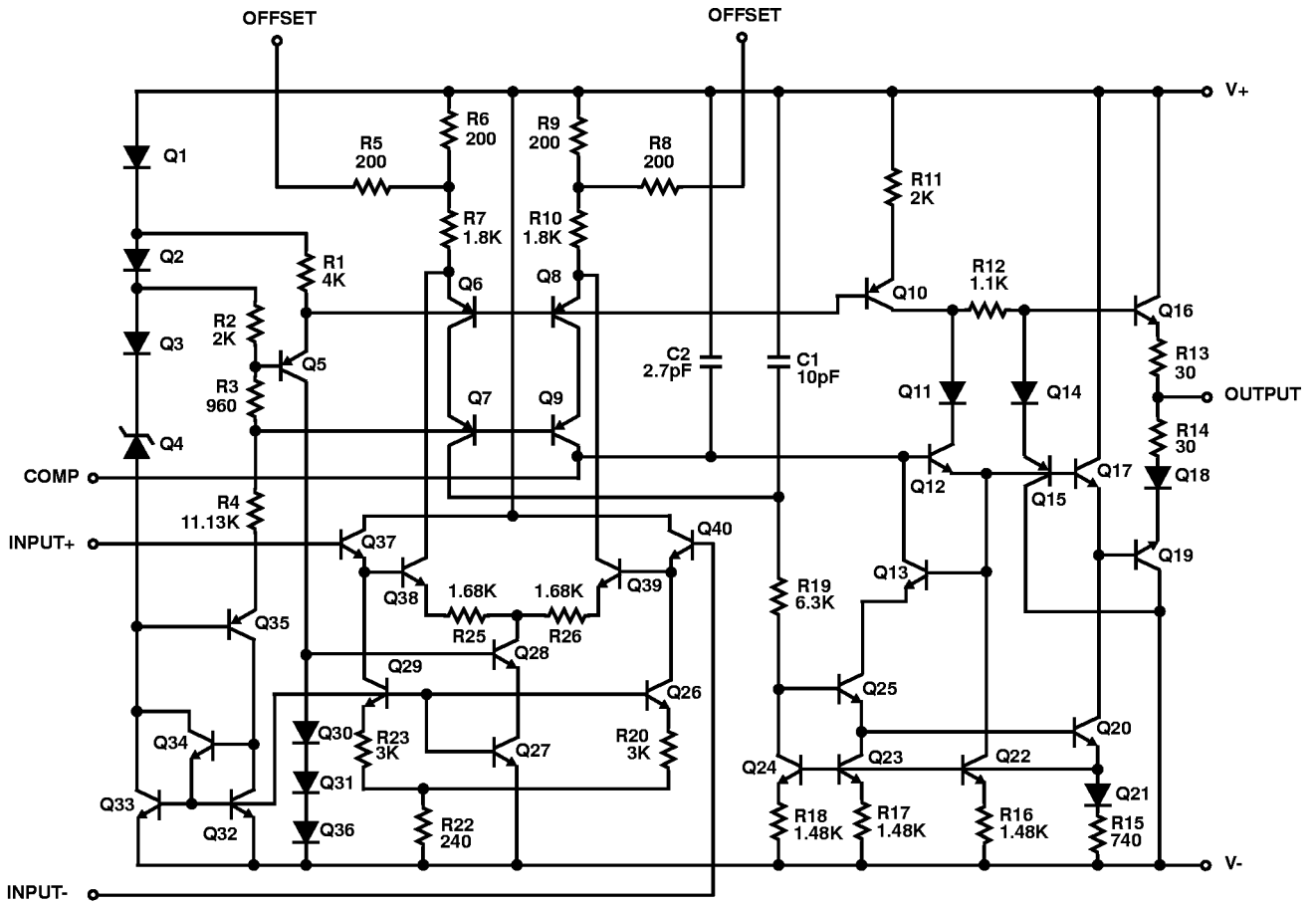
HS7-2510RH



NOTES:

1. V1 = +15V ±10%
2. V2 = -15V ±10%
3. R = 1MΩ ±5%
4. C = 0.1µF ±10%

Schematic Diagram



Metallization Topology

DIE DIMENSIONS:
65 mils x 57 mils x 19 mils
(1660µm x 1950µm x 483µm)

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ±2kÅ

GLASSIVATION:
Type: Nitride
Thickness: 7kÅ ±0.7kÅ

TRANSISTOR COUNT:
40

WORST CASE CURRENT DENSITY:
$<2 \times 10^5 A/cm^2$

SUBSTRATE POTENTIAL (Powered Up):
Unbiased

DIE ATTACH:
Temperature: CerDIP 460°C (Max)

Metallization Mask Layout

HS-2510RH